# Getting started with STM32H7Rx/7Sx MCUs hardware development

## Introduction

This application note is intended for system designers who develop applications based on the STM32H7Sxx and STM32H7Rxx MCUs.

This document provides an implementation overview of the following hardware features:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management.

STM32H7R3/7S3 and STM32H7R7/7S7 are product lines with different memory sizes, packages, and peripherals. In this document, they are referred to as STM32H7Rx/7Sx.

This document describes the minimum hardware resources required to develop an application using STM32H7Rx/7Sx MCUs.

**Table 1. Applicable products**

| Type | Product lines |
|---|---|
| Microcontrollers | STM32H7R3/7S3 and STM32H7R7/7S7 |

# 1 General information

This document applies to STM32H7Rx/7Sx Arm®-based MCUs.

STM32H7Rx/7Sx MCUs are highly integrated microcontrollers that are based on the Arm® Cortex®-M7 32-bit core.

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### Reference documents

[1] Datasheet *Arm® Cortex®-M7 32-bit 600 MHz MCU, 64 KB flash, 620 KB RAM, Ethernet, 2x USB, 2x FD-CAN, advanced graphics and security, 2x12-bit ADCs* (DS14359)

[2] Datasheet *Arm® Cortex®-M7 32-bit 600 MHz MCU, 64 KB flash, 620 KB RAM, Ethernet, 2x USB, 2x FD-CAN, advanced graphics, 2x12-bit ADCs* (DS14360)

[3] Application note *Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs* (AN2867)

[4] Application note *STM32 microcontroller system memory boot mode* (AN2606)

[5] Errata sheet *STM32H7Rxx/7Sxx device errata* (ES0596)

[6] Reference manual *STM32H7Rx/7Sx Arm®-based 32-bit MCUs* (RM0477)

# 2 Description

The following table provides an overview of the security and graphic peripherals available per product line.

**Table 2. Security and graphics peripheral availability per product line**

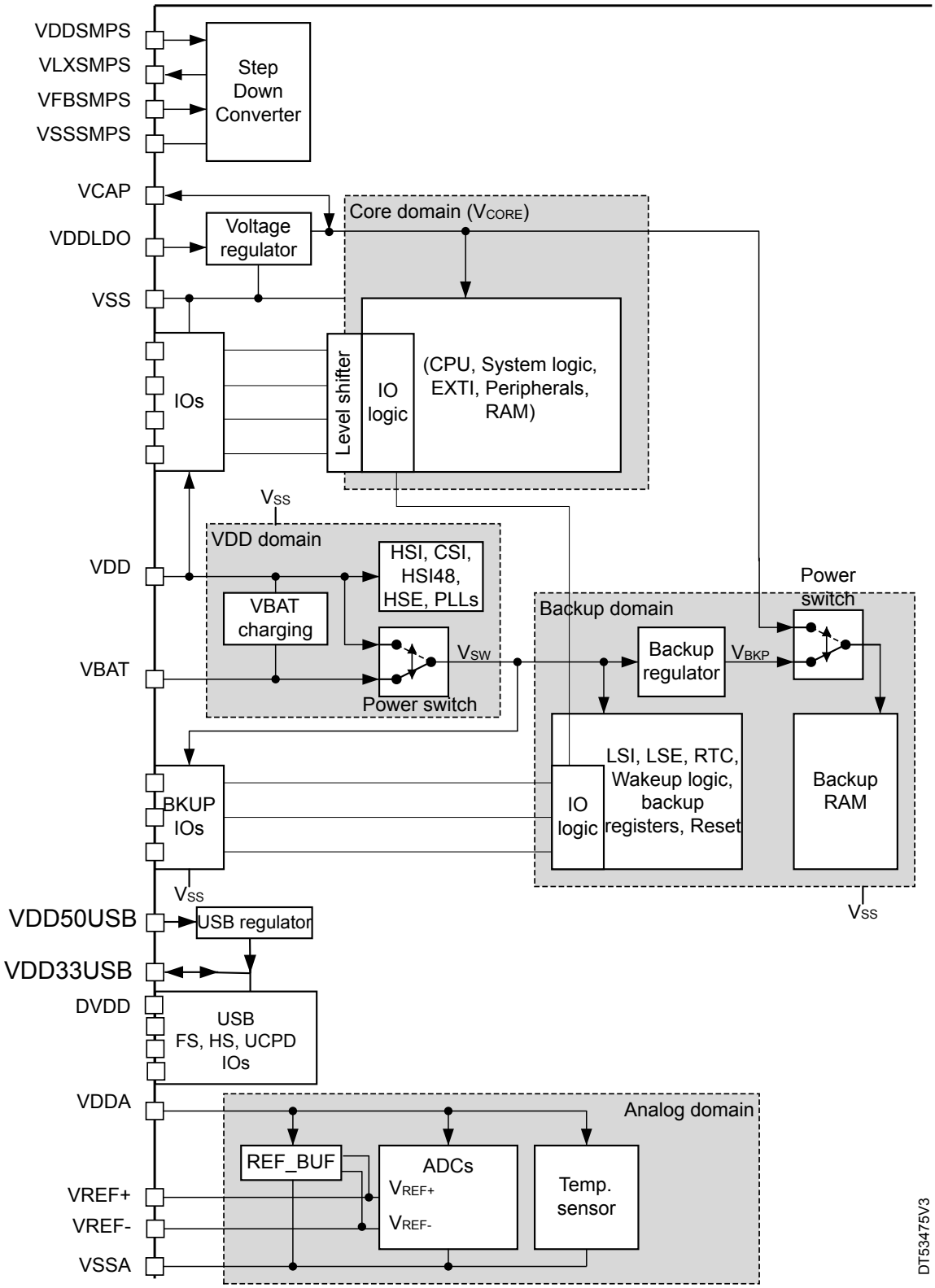
| Peripheral type | | STM32H7R3xx | STM32H7R7xx | STM32H7S3xx | STM32H7S7xx |
|---|---|---|---|---|---|
| Graphics | Neo-Chrom (GPU2D) | N | Y | N | Y |
| | Chrom-ART (DMA2D) | Y | | | |
| | Chrom-GRC (GFXMMU) | Y | | | |
| | Hardware codec (JPEG) | Y | | | |
| | LCD-TFT | N | Y | N | Y |
| | Parallel display (FMC8/16) | Y | | | |
| Security | Life cycle support (HDPL0/1/2) | Y | | | |
| | Root of trust (ST-iROT) | N | N | Y | Y |
| | Debug authentication | Y | | | |
| | Secure firmware install (SFI) | Y | | | |
| | Root secure service (RSS) | Y | | | |
| | HASH acceleration and PKA verification | Y | | | |
| | Crypto processor (CRYP, PKA, SAES) | N | N | Y | Y |
| | On the fly, encrypt/ decrypt (MCE) | N | N | Y | Y |
| | True random generator (TRNG) | Y | | | |

# 3 Power supply management

STM32H7Rx/7Sx MCUs require at least one single power supply to be fully operational. Additional power supplies or voltage references are required for some use cases.

The general design guidelines are explained in the following sections. In all the diagrams, the gray boxes represent power domains. The figure below illustrates the power supply layout:

**Figure 1. Power supply layout**




*Note: The following are not available on STM32H7R3R8V, STM32H7R3V8T, STM32H7R3Z8T, STM32H7S3R8V, STM32H7S3V8T, and STM32H7S3Z8T devices: VDDSMPS, VLXSMPS, VFBSMPS, and VSSSMPS.*

*When VDDLDO is not available on a pin/ball, it is internally connected to $V_{DD}$.*

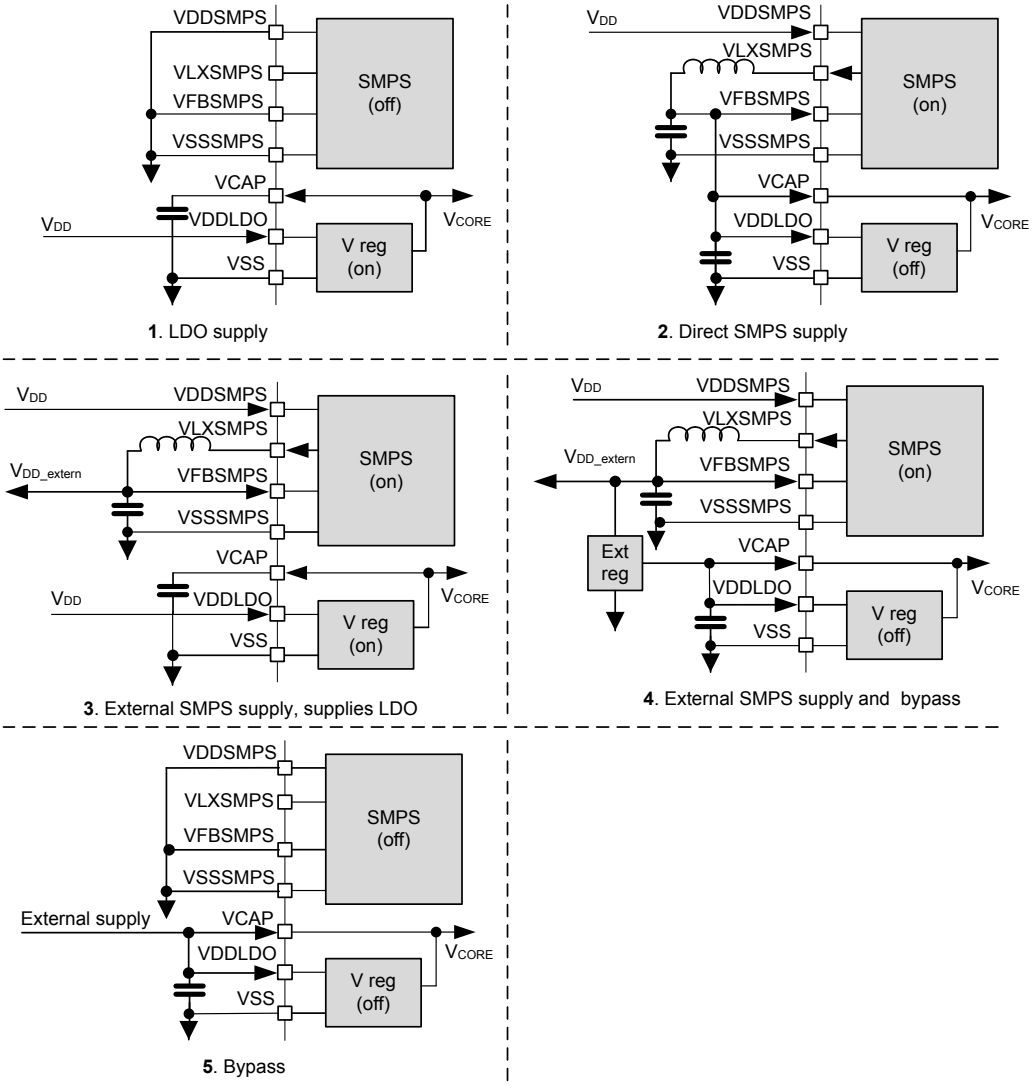
The table below lists the pin name, the signal type, and the description for PWR input and output signals that are connected to the package pins/balls.

**Table 3. PWR input and output signals connected to package pins/balls**

| Power supply | Signal type | Description |
|---|---|---|
| $V_{DD}$ | Supply input | Main I/O and $V_{DD}$ domain supply input. |
| $V_{SS}$ | Supply input | Main ground. |
| $V_{DDA}$ | Supply input | External analog power supply for analog peripherals. |
| $V_{SSA}$ | Supply input | Separated isolated ground for analog peripherals. |
| $V_{BAT}$ | Supply input/output | Backup battery supply:<br>• Optional external supply for backup domain when $V_{DD}$ is not present.<br>• It can also be used to charge the external battery. |
| $V_{DDSMPS}$ | Supply input | Supply for switch mode power supply (SMPS) step-down converter. |
| $V_{LXSMPS}$ | Supply output | SMPS step-down converter output. |
| $V_{FBSMPS}$ | Supply regulation input | SMPS feedback voltage sense. |
| $V_{SSSMPS}$ | Supply input | Ground for SMPS step-down converter. |
| $V_{DDLDO}$ | Supply input | Supply for the integrated low drop out regulator. |
| $V_{CAP}$ | Supply input/output | Figure 2. System supply configurations shows the different possible regulator supply configurations: using one, both or none.<br>Digital Core supply input / output pin. It is either provided by the embedded regulator or from an external source.<br>Refer to Figure 2. System supply configurations for the different possible configurations |
| $V_{DD50USB}$ | Supply input | USB regulator supply input |
| $V_{DD33USB}$ | Supply input/output | USB regulator supply output or external USB supply input |
| $V_{REF+}$ | Supply input/output | Reference voltage for ADCs.<br>It can be generated through the internal $V_{REFBUF}$ or provided by an external source. |
| $V_{REF-}$ | Supply input | Ground reference for ADCs. |
| $V_{DDXSPI1}$ | Supply input | Supply for XSPI I/O manager port 1 |
| $V_{DDXSPI2}$ | Supply input | Supply for XSPI I/O manager port 2 |
| DVDD | Supply input | Digital supply for the USB HS PHY |

The following figure illustrates the system supply configurations:

**Figure 2. System supply configurations**




## 3.1 External power supplies and components

The STM32H7Rx/7Sx uses an automatic voltage scaling (AVS) mechanism to ensure that the maximum frequency is reached with the minimum power consumption. This mechanism is automatically selected when using an internal power supply. The AVS setting is die dependent, and cannot be modified. All values given in this document are derived and guaranteed for an internal supply with LDO or SMPS only, and not when a bypass mechanism is used.

For further detail on the electrical characteristics, refer to the documents [1] and [2].

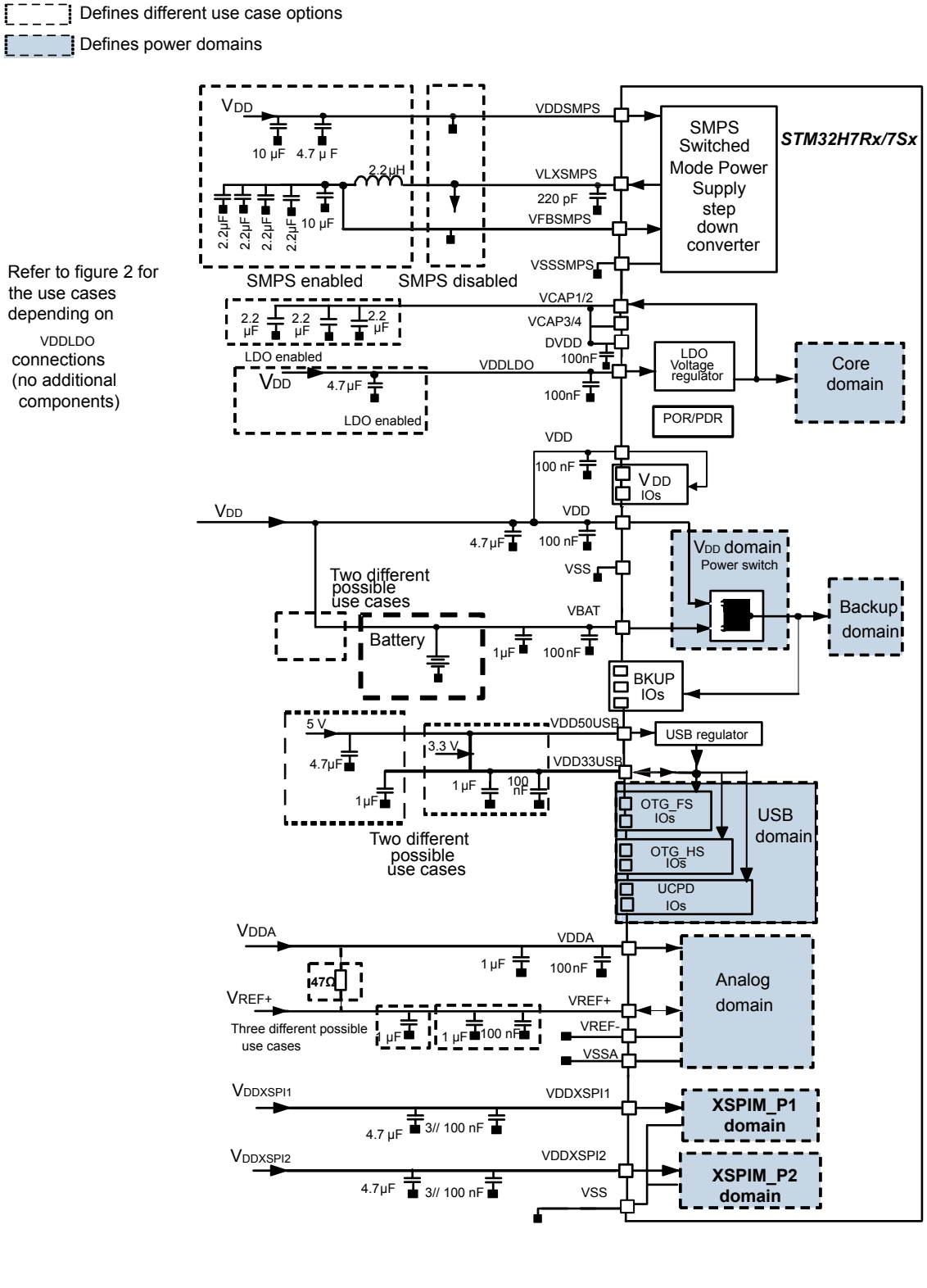
**Table 4. Power supply connection**

| Package pin/ ball | Voltage range | External components | Comments |
|---|---|---|---|
| VDD | 1.71 V to 3.6 V | 100 nF ceramic, for each VDD as close as possible to the pins. A 4.7 µF ceramic connected to one of the VDD pins. | - |
| VDDA | 1.62 V to 3.6 V | 1 µF ceramic and 100 nF as close as possible to the pin. | $V_{DDA}$ can be connected to $V_{DD}$ through a ferrite bead. |
| | 2.1 V to 3.6 V | | Restriction if $V_{REFBUF}$ is used. |
| | 0 V to 3.6 V | | ADC and $V_{REFBUF}$ are not used. |
| VBAT | 1.2 V to 3.6 V | 1 µF ceramic and 100 nF close to the VBAT pin. | It can be connected directly to an external battery or supply.<br>The external battery can be charged through the internal 5 kΩ or 1.5 kΩ resistor.<br>See document [6]. |
| VDDSMPS | 0 V | No capacitor required. | $V_{DDSMPS}$ is connected to $V_{SS}$ when the converter is not used. |
| | 1.71 to 3.6 V = $V_{DD}$ | Four different solutions are recommended:<br>• 10 µF (best cost trade-off), ESR 10 mΩ<br>• 2x 10 µF (best area/performance trade- off)<br>• 10 µF + 100 nF close to the pin (best cost/ performance trade-off)<br>• 10 µF + 4.7 µF (best performance) | For SMPS supplying $V_{CORE}$. |
| | 2.3 V to 3.6 V = $V_{DD}$ | | For SMPS, the output is regulated to 1.8 V.<br>The SMPS supplies an external regulator. |
| VLXSMPS | $V_{CORE}$ or 1.8 V | When the SMPS is used:<br>• 2.2 µH (DCR 110 mΩ, Isat 1.7 A, Itemp 1.4 A) as close as possible to VLXSMPS.<br>• LQFP/BGA packages: 220 pF ceramic capacitor on VLXSMPS.<br>• 10 µF + 2× 4.7 µF or 4× 2.2 µF (ESR 5 mΩ) close to the inductor on VFBSMPS connection side. | Depending on the use case, the SMPS provides the digital core supply or a supply provided to another external regulator.<br>See Figure 2. System supply configurations for connection details. |
| VFBSMPS | $V_{CORE}$ or 1.8 V | - | Refer to Figure 2. System supply configurations for details on the use case regarding this pin. |
| VDDLDO | 1.71 V to 3.6 V | When the LDO is used: 1x 4.7 µF capacitor close to one VDDLDOx pin, all VDDLDOx pins correctly connected.<br>Otherwise: no capacitor is required. Connect VDDLDOx to VCAP. | $V_{DDLDO} \leq V_{DD}$.<br>Up to four $V_{DDLDO}$ pins are available depending on the package specification. |
| VCAP | VOS low/high<br>SVOS low/high | LDO enabled:<br>3× 2.2 µF ESR < 100 mΩ must be connected to VCAPX | If a fourth VCAP pin is available (depending on the package), it must be connected to the other VCAP pins but no additional capacitor is required for the fourth one.<br>In bypass mode, the $V_{CORE}$ supply is externally provided through the VCAPX pins. |
| VDD50USB | 4.0 Vto 5.5 V | 4.7 µF ceramic | Connected to an external supply or USB $V_{BUS}$ for an internal USB regulator use case. |
| | 3 V to 3.6 V | | Connected to $V_{DD33USB}$ when the internal USB regulator is not used (for packages on which this pin is available). |

| Package pin/ ball | Voltage range | External components | Comments |
|---|---|---|---|
| VDD33USB | 3.0 V to 3.6 V | 1 µF ceramic and 100 nF ceramic (USB reg not used)<br>1 µF max ESR 600 mΩ (USB reg used) | The$V_{DD33USB}$ supply can be provided externally, or through the internal USB regulator.<br>When the regulator is enabled, its output is provided to $V_{DD33USB}$ through the internal connection. |
| | 0 V to 3.6 V | - | If USB is not used, it is recommended to use 0 V. |
| VREF+ | 1.62 V to ≤$V_{DDA}$ | 1 µF ceramic and<br>100 nF ceramic close to the pin<br>or connected to VDDA through a resistor (typically 47 Ω) | $V_{REF+}$is provided externally. |
| | 2 V to ≤$V_{DDA}$ | | External VREF+ with VDDA > 2 V and ADC used. |
| | $V_{REFBUF}$ reference voltage | 1 µF | $V_{REF+}$ is provided by the embedded $V_{REFBUF}$ regulator.<br>Do not activate the internal $V_{REFBUF}$ when $V_{REF+}$ is provided externally. |
| VREF- | $V_{SSA}$ | Tied to VSSA | Only available on some packages.<br>Internally tied to $V_{SSA}$ when this pin is not present. |
| VDDXSPI1 | Supported voltage range (1.62 V to 3.6 V). | 1 µF ceramic and 3× 100 nF ceramic | The $V_{DDXSPI1}$ supplies the XSPI I/O manager port 1. |
| VDDXSPI2 | Supported voltage range (1.62 V to 3.6 V). | 1 µF ceramic and 3× 100 nF ceramic | The $V_{DDXSPI2}$ supplies the XSPI I/O manager port 2. |

**Caution:** The I/O HSLV configuration bit must not be set if the I/O supply (VDD) is above 2.7 V. Setting it while the voltage is higher than 2.7 V can damage the device. For more details, refer to the *High-speed low-voltage mode (HSLV)* section in the document [6].

**Figure 3. Power supply component layout**




*Note:*

1. *$V_{DD\_HEXASPI}$ and $V_{DD\_OCTOSPI}$ supply voltage names are relative reference names to $V_{DDXSPI1}$ and $V_{DDXSPI2}$ supply in the STM32H7S78-DK board.*
2. *$V_{DD\_OCTO1}$ and $V_{DD\_OCTO2}$ supply voltage names are relative reference names to $V_{DDXSPI1}$ and $V_{DDXSPI2}$ supply in the NUCLEO-H7S3L8 board.*

## 3.2 Digital circuit core supply ($V_{core}$)

As shown in Figure 2. System supply configurations, the digital power can be supplied either by the internal linear voltage regulator, the embedded SMPS step-down converter, or directly by an external supply voltage (regulator bypass).

In system Run mode, this digital core voltage can be set dynamically to the required performance (voltage scaling VOS low/high).

In system Stop mode, the digital core voltage can be reduced to improve the power consumption (voltage scaling SVOS low/high).

For a detailed definition on the available power modes, read the power control (PWR) chapter in the document [6].

## 3.3 Independent analog supply and reference voltage

To improve analog peripheral performance, the analog peripherals feature an independent power supply that can be separately filtered and shielded from noise on the PCB:

- The analog supply voltage input is available on a separate VDDA pin.
- An isolated ground connection is provided on the VSSA pin.

To ensure better ADC accuracy, the reference voltage can be provided externally through the $V_{REF+}$ pin. This, however, is not available in all packages.

The VREF-pin is available on some packages to improve the ground noise immunity.

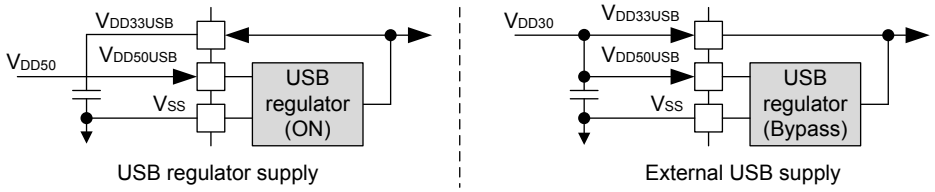
The VDDA minimum value ($V_{DDA\_MIN}$) depends on the analog peripheral and on whether a reference voltage is provided or not. For further details, refer to Table 4. Power supply connection .

## 3.4 Independent USB transceiver power supply

The USB transceivers are supplied from a dedicated $V_{DD33USB}$ supply that can be provided either by the integrated USB regulator, or by an external USB supply.

For more details on how to configure the USB transceiver, refer to the USB regulator section in the document [6].

**Figure 4. USB supply configuration**




There are different ways to supply the USB transceivers, depending on $V_{DD33USB}$ and $V_{DD50USB}$ availability (see Figure 4. USB supply configuration ):

When supplied through the VDD50USB pin, an internal regulator dedicated to the USB transceivers is used. In this case:

- Either the USB $V_{BUS}$ or an external power supply can be used to provide the required voltage.
- The internal regulator output supply is connected to the USB FS PHY/ USB HS PHY/ UCPD1 (only available on some of the packages) and is also available on the VDD33USB pin. In this configuration, the $V_{DD50USB}$ voltage can rise either before or after the $V_{DD}$ power supply (see Figure 5. VDD50USB power supply ).
- An external capacitor must be connected to $V_{DD33USB}$ (see Table 4. Power supply connection ).

When supplied through the VDD33USB pin, the internal USB regulator is disabled and an external supply is provided through the VDD33USB pin. In this case:

- The VDD33USB pin must receive a voltage ranging between 3.0 V to 3.6 V (see Figure 6. VDD33USB connected to $V_{DD}$ power supply ). If the VDD50USB pin is available and the internal USB regulator is not used, $V_{DD50USB}$ must be connected with the VDD33USB pin. As an example, when the device is powered at 1.8 V, an independent 3.3 V power supply can be applied to VDD33USB.
- When $V_{DD33USB}$ is connected to a separate power supply, it is independent from $V_{DD}$ and $V_{DDA}$. In this case, it must be the last supply to be turned on and the first supply to be switched off. The following conditions must be respected (see Figure 7. VDD33USB connected to external power supply ):
  1. During the power-on and power-down phases ($V_{DD}$ < $V_{DD\_MIN}$ value), $V_{DD33USB}$ must always be lower than $V_{DD}$
  2. $V_{DD33USB}$ rising and falling time specifications must be compliant. Refer to the tables *power-up/power-down operating conditions for regulator on*, and *power-up/power-down operating conditions for regulator off* in the documents [1] and [2].
- In operating mode, $V_{DD33USB}$ can be either lower or higher than $V_{DD}$.
- If a USB interface is used (USB OTG_HS/OTG_FS/UCPD), the associated GPIOs powered by $V_{DD33USB}$ operate between $V_{DD33USB\_MIN}$ and $V_{DD33USB\_MAX}$ (see Figure 7. VDD33USB connected to external power supply ).

**Figure 5. VDD50USB power supply**

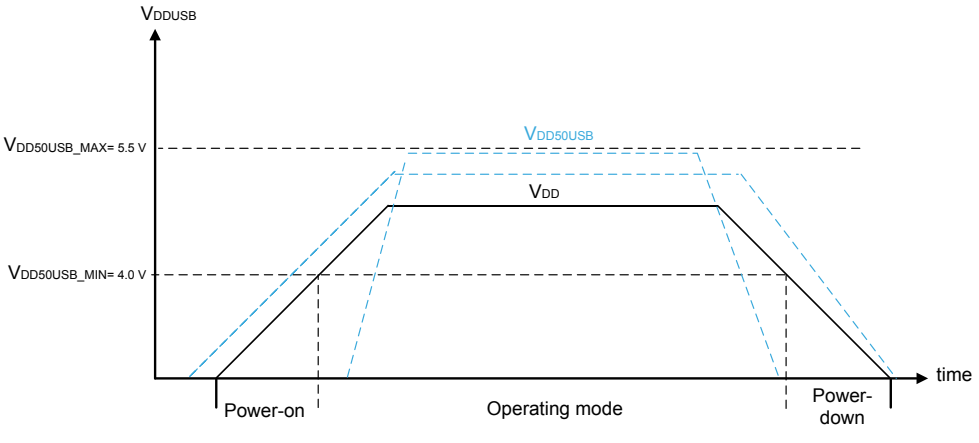



**Figure 6. VDD33USB connected to $V_{DD}$ power supply**

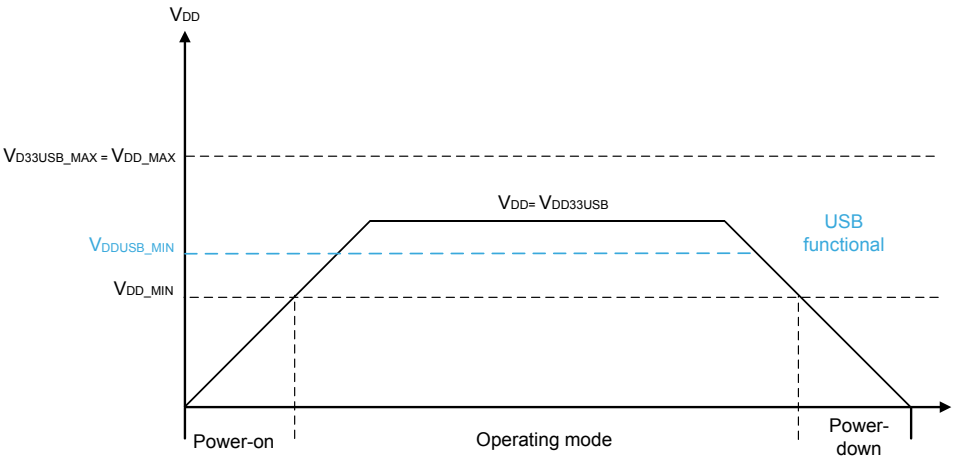
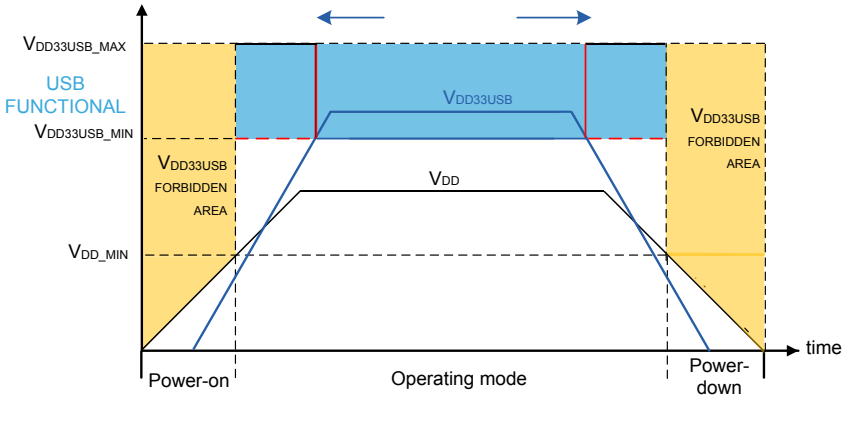


Figure 7. **VDD33USB connected to external power supply**




## 3.5 Battery backup domain

### Backup domain description

To retain the content of the RTC backup registers, backup SRAM, and supply the RTC when $V_{DD}$ is turned off, the VBAT pin can be connected to an optional 1.2 V to 3.6 V standby voltage supplied by a battery. Otherwise, VBAT must be connected to another source, such as $V_{DD}$.

When the backup domain is supplied by $V_{BAT}$ (an analog switch connected to $V_{BAT}$ since $V_{DD}$ is not present), the following functions are available:

- PC14 and PC15 can be used as LSE pins only.
- PC13 can be used as RTC_OUT1, RTC_TS, TAMP_IN1, TAMP_OUT2 through RTC pin PC13 configuration
- PB9/TAMP_IN2, PE1/TAMP_IN3 when configured by the RTC as tamper pins. See document [6].

During $t_{RSTTEMPO}$ (temporization at $V_{DD}$ startup) or after a power-down reset (PDR) is detected, the power switch between $V_{BAT}$ and $V_{DD}$ remains connected to $V_{BAT}$.

During the startup phase, if $V_{DD}$ is established in less than $t_{RSTTEMPO}$, and is greater than $V_{BAT}$ + 0.6 V, a current may be injected into $V_{BAT}$ through an internal diode connected between $V_{DD}$ and the power switch ($V_{BAT}$).

If the power supply/battery connected to the $V_{BAT}$ pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the $V_{BAT}$ pin. For the value of $t_{RSTTEMPO}$, refer to the documents [1] and [2].

### Battery charging

When $V_{DD}$ is present, the external battery connected to $V_{BAT}$ can be charged through an internal resistance. An internal 5 kΩ or 1.5 kΩ resistor can perform this operation. Software configures the resistor value.

Battery charging is automatically disabled in $V_{BAT}$ mode.

## 3.6 Low drop-out (LDO) voltage regulator

The low drop-out (LDO) voltage regulator is always enabled after power-on reset. If it is disabled, it remains disabled even after any reset source except for a power-on reset. For system supply configuration, if this regulator is not needed, the user software switches it off after system startup. On some packages, the LDO power supply is available on external VDDLDO pins. When it is not available on an external pin, $V_{DDLDO}$ is connected internally to $V_{DD}$.

For the configuration where the $V_{core}$ is supplied by the LDO, the default output level is set to VOS low. Refer to Figure 2. System supply configurations for further details.

The LDO can be set to one out of four different modes. One mode corresponds to the regulator switched off and the three other modes to the regulator switched on, in which case the mode depends on the application operating modes:

- Switched off:
  - The $V_{core}$ is supplied externally through the $V_{CAP}$ pin (bypass mode), or
  - The $V_{core}$ is supplied through the SMPS step-down converter (see Section 3.7: SMPS step-down converter).
- In Run mode:
  - The LDO regulator supplies the core and the backup domains.
  - The LDO regulator output voltage can be dynamically scaled by programming the voltage scaling (VOS low/high), depending on the required performance (see document [6]).
- In Stop mode: the voltage regulator supplies the $V_{CORE}$ domain to retain the content of registers and internal memories, and must be set in LP mode.
  In LP mode: the regulator mode is selected through the SVOS bit in the PWR control register 1 (PWR_CR1). Due to a lower voltage level for SVOS low scaling, the Stop mode consumption can be further reduced.
- In Standby mode: the voltage regulator is off and the $V_{CORE}$ domains are powered down. The content of the registers and memories is lost except for the Standby circuitry and the backup domain.

## 3.7 SMPS step-down converter

The SMPS step-down converter information applies only if the SMPS converter is available.

The embedded switch mode power supply (SMPS) step-down converter has a higher efficiency than the embedded LDO regulator.

By using the SMPS, the overall system power consumption is improved for all power modes at the extra cost of an additional external inductor.

Refer to the documents [1] and [2] to compare power efficiencies. The possible configurations are available in Figure 2. System supply configurations.

The SMPS step-down converter is always enabled after Power-on reset when its power supply is provided on the VDDSMPS pin. If it is disabled, it remains disabled even after any reset, except for Power-on reset.

The regulated output at startup is set to VOS low.

The three main SMPS configurations are:

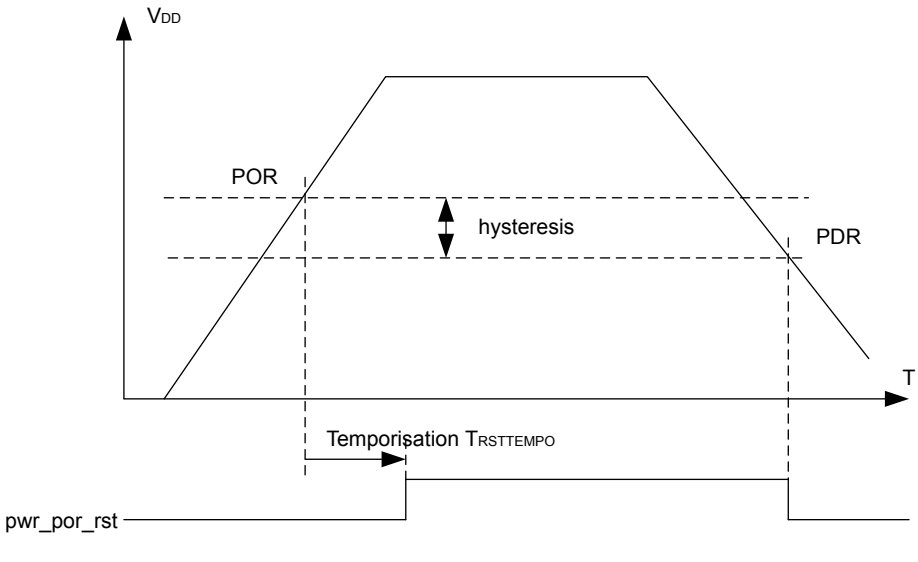
- The SMPS is used but the $V_{CORE}$ supply is provided by the internal LDO regulator. After startup, the software sets up the SMPS, providing a regulated output of 1.8 V.
- The SMPS is used but the $V_{CORE}$ supply is provided by an external regulator. After startup, the software sets the SMPS to provide a regulated output of 1.8 V. The external regulator must ensure the correct voltage scaling for the Run and Stop modes (VOSx and SVOSx).
- The SMPS is directly connected to the VCAP pin and provides the regulated supply to the $V_{CORE}$. In this configuration, the SMPS runs in one of the following modes:
  - Run mode: the converter can be dynamically scaled by programming the voltage scaling (VOS low and VOS high) to the required performance. For further information, refer to the document [6].
  - In Stop mode: the SMPS step-down converter supplies the $V_{CORE}$ domain to retain the content of registers and internal memories. The SMPS step-down converter must be set in LP mode through the SVOS in the PWR control register 1 (PWR_CR1). In LP mode, only SVOS low/high scalings are allowed. Due to a lower voltage level for such scaling, the Stop mode consumption can be further reduced.
  - In Standby mode: the converter is powered down. Both the register and SRAM content is lost except for the content related to the standby circuitry and the backup domain.

## 3.8 Reset and power supply supervisor

### 3.8.1 Power-on reset (POR)/power-down reset (PDR)

The devices have an integrated POR/PDR circuitry, which ensures correct operational startup from 1.71 V. The device remains in reset mode while $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit as illustrated in the figure below. For more details concerning the POR/PDR threshold, refer to the electrical characteristics in the documents [1] and [2].

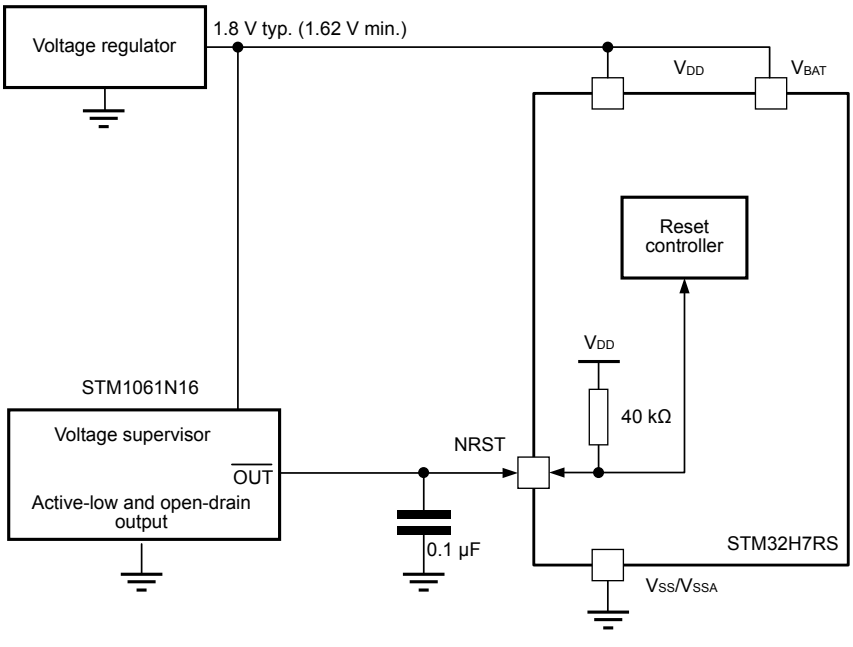
**Figure 8. Power on reset/power down reset waveform**




$t_{RSTTEMPO}$ is approximately 377 µs. $V_{POR/PDR}$ rising edge is 1.67 V (typical) and $V_{POR/PDR}$ falling edge is 1.62 V (typical). For the values, refer to the documents [1] and [2].

The device must be maintained in reset mode as long as $V_{DD}$ is below 1.62 V. The implemented circuit is illustrated in the figure below.

**Figure 9. Power supply supervisor interconnection with internal reset OFF**




The supply ranges, which never go below 1.71 V, are managed more effectively using the internal circuitry (no additional components are needed, thanks to the fully embedded reset controller).

When the embedded power supply supervisor is off, the following integrated features are no longer supported:

- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$ functionality is no longer available. VBAT pin must be connected to $V_{DD}$.

### 3.8.2 Brownout reset (BOR)

If enabled through the option bytes, the BOR keeps the system under reset until the $V_{DD}$ supply voltage reaches the selected $V_{BOR}$ threshold (also selected through option bytes. Refer to the document [6]).

Three BOR levels are possible (2.1 V, 2.4 V, 2.7 V). For further information on the electrical characteristics, refer to the documents [1] and [2].

### 3.8.3 Programmable voltage detector (PVD)

The PVD can be used to monitor the $V_{DD}$ power supply by comparing it to a threshold selected by the PLS[2:0] bits in the PWR power control register (PWR_CR1). For further information, refer to the document [6].

The PVD is enabled by setting the PVDE bit.

The selectable threshold is between (PVD level 1) 1.95 V and (PVD level 7) 2.85 V. See document [6].

A PVDO flag is available in the PWR control status register 1 (PWR_SR1) to indicate if $V_{DD}$ or PVD_IN voltage is higher or lower than the PVD threshold. This event is internally connected to the EXTI and can generate an interrupt, assuming it has been enabled through the EXTI registers. The PVDO output interrupt can be generated when $V_{DD}$ or PVD_IN voltage drops below the PVD threshold and/or when $V_{DD}$ or PVD_IN voltage rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example the service routine can perform emergency shutdown tasks.

### 3.8.4 Analog voltage detector (AVD)

The AVD can be used to monitor $V_{DDA}$ power supply by comparing it to a threshold selected through the ALS[1:0] bits of the PWR power control register (PWR_CR1). The threshold value can be configured to 1.7 V, 2.1 V, 2.5 V or 2.8 V (AVD level 1 to AVD level 4). For the values, refer to the documents [1] and [2].

The AVD is enabled by setting the AVDEN bit in PWR_CR1 register. An interrupt can be raised when $V_{DDA}$ goes above or below the configured threshold.

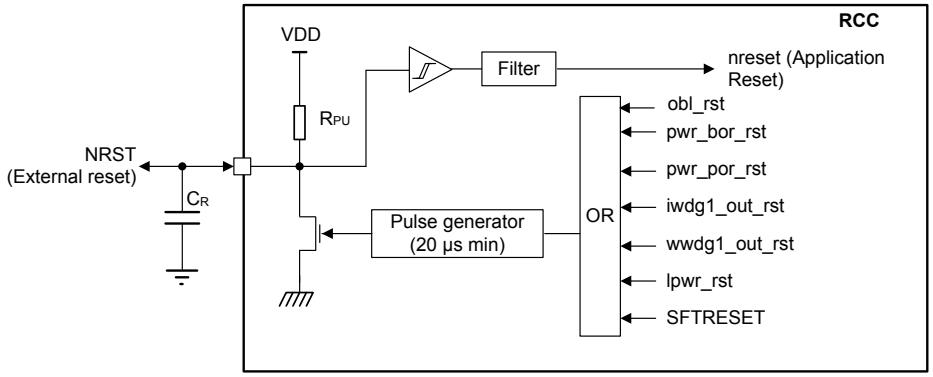
### 3.8.5 System reset

An application reset (nreset) resets most of the registers to their default values unless otherwise specified in the register description.

A system reset can be generated from one of the following sources:

- An assertion of the NRST pin (external reset).
- A reset from the power-on/off reset block (pwr_por_rst).
- A reset from the brownout reset block (pwr_bor_rst).
- A reset from the independent watchdogs (iwdg_out_rst).
- An exit from Standby (rcc_vcore_rst).
- A reset from the window watchdogs depending on WWDG configuration (wwdg_out_rst).
- A software reset from the Cortex®-M7 core. It is generated via the SYSRESETREQ signal issued by the Cortex®-M7 core. This signal is also named SFTRESET in this document.
- A reset from the low-power mode security reset, depending on option byte configuration (lpwr_rst).
- An option byte reload request from the flash interface (obl_rst)

Figure 10. **Reset circuit**




### 3.8.6 Bypass mode

When $V_{CORE}$ is supplied from an external source (Bypass mode), different operating modes can be used depending on the system operating modes (Run, Stop, or Standby):

- In Run mode: the external source supplies full power to the $V_{CORE}$ domain (core, memories, and digital peripherals). The external source output voltage is scalable through different voltage levels (VOS low and VOS high). The externally applied voltage level must be reflected in the VOS bit of the PWR_CSR4 register. The RAMs must only be accessed for write operations when the external applied voltage level matches VOS settings.
- In Stop mode: the external $V_{CORE}$ supply must be maintained at the VOS level or at least over 0.95 V to ensure proper internal wake-up.
- In Standby mode: the wake mechanism must be monitored externally. Refer to the documents [1] and [2] for the $V_{CORE}$ ramp time.

# 4 Clocks

The STM32H7Rx/7Sx microcontrollers support several possible clock sources:

- Two external oscillators (this requires external components):
  - High-speed external oscillator (HSE).
  - Low-speed external oscillator (LSE).
- Four internal oscillators:
  - High-speed internal oscillator (HSI).
  - High-speed internal 48 MHz oscillator (HSI48).
  - Low-power internal oscillator (CSI).
  - Low-speed internal oscillator (LSI).
- Three embedded PLLs can be used to generate the high frequency clocks for the system and the peripherals.

For both the HSE and LSE, the clock can also be provided from an external source using the OCS_IN and OSC32_IN pins (HSE bypass and LSE bypass modes).

Figure 11. Clock generation and clock tree shows the clock generation and clock tree architecture. For further details, refer to the documents [1] and [2].

The choice of clocks depends strongly on the application use case.

Refer to the STM32H7R3x8, STM32H7S3x8, STM32H7R7x8, and STM32H7S7x8 datasheets for the electrical characteristics such as range and accuracy.

Figure 11. **Clock generation and clock tree**

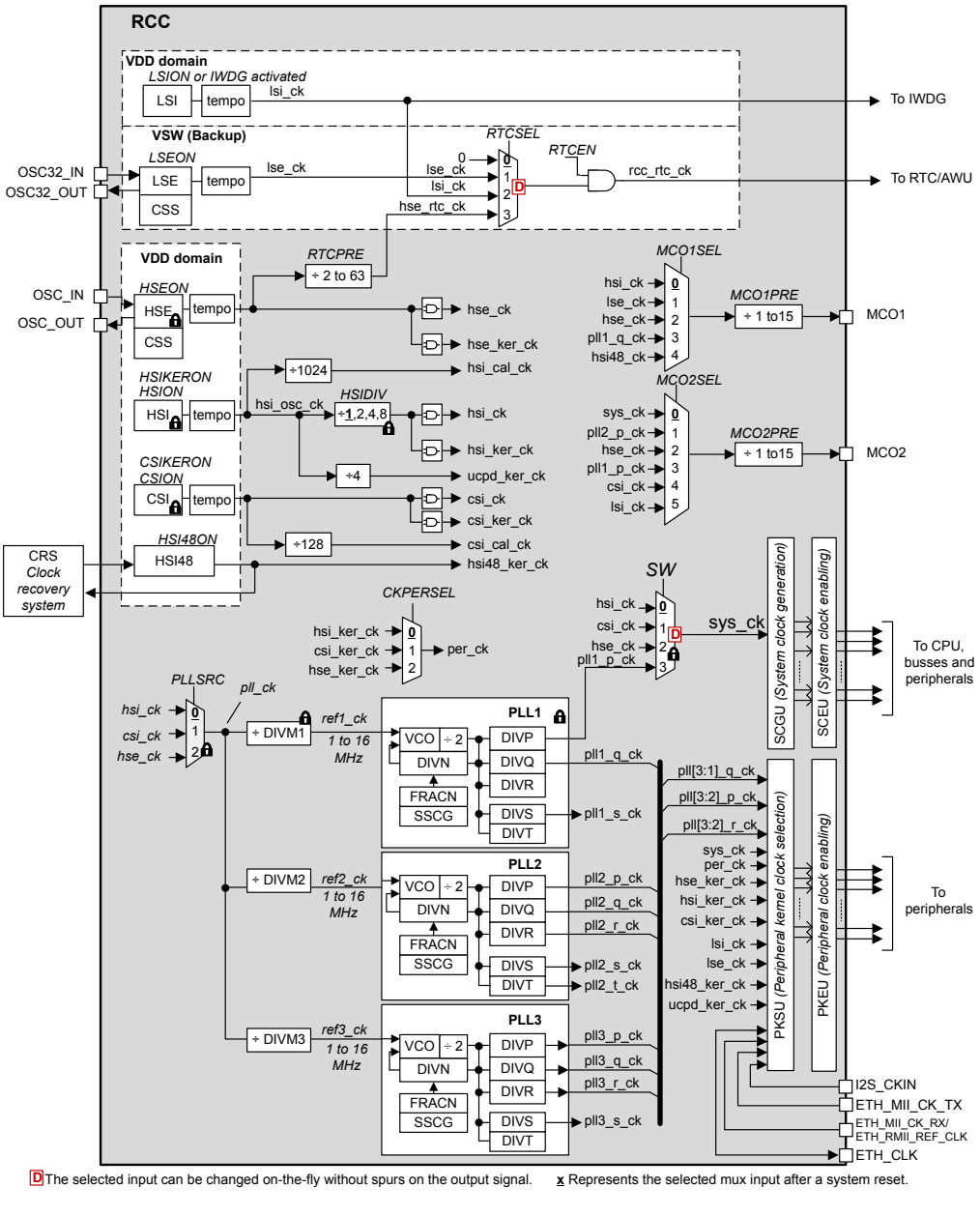



Table 5. **Clock connections**

| Pin | External component | Comment |
|---|---|---|
| OSC32_IN | Typical example:<br>Crystal: 32.768 kHz (6 pF, 50 KΩ)<br>Capacitor: 2x 1.5 pF<br>All components must be placed as close as possible to the pins | LSE oscillator input (see Figure 12. HSE/LSE clock source ).<br>LSE oscillator output<br>The external capacitor must be tuned because it is strongly dependent on the PCB design. |
| OSC32_OUT | Unconnected in bypass | Not used in bypass mode. |
| OSC_IN | External clock input | HSE oscillator<br>HSE bypass input 4 MHz ≤ f ≤ 50 MHz. |

| Pin | External component | Comment |
|---|---|---|
| OSC_OUT | Typical example:<br>Crystal: 24 MHz (6 pF, 80 Ω) Capacitor: 2× 33 pF<br>All components must be placed as close as possible to the pins<br>Unconnected in bypass | HSE oscillator input (see Figure 12. HSE/LSE clock source). |
| | | HSE oscillator input<br>The external capacitor must be tuned because it is strongly dependent on the PCB design. |
| | Unconnected in bypass | Not used in bypass mode. |
| I2S_CKIN | External clock input | When an external clock reference is needed, use the external kernel clock input for audio interface SAI, ADF, I2S/SPI. |
| ETH_MII_TX_CLK/ ETH_MII_RX_CLK/ ETH_RMII_REF_CLK | External clock input | Ethernet transmit and receive clock provided from an external Ethernet PHY |
| ETH_CLK | External clock output | |
| MCO1 | Internal clock output | Some internal clocks can be provided to MCO1 pin. An embedded divider allows frequency reduction.<br>See Figure 11. Clock generation and clock tree. |
| MCO2 | Internal clock output | Some internal clocks can be provided to MCO2 pin. An embedded divider allows frequency reduction.<br>See Figure 11. Clock generation and clock tree. |
| SYNC | External sync signal | Synchronization source for the HSI48 MHz embedded oscillator clock recovery system (CRS)<br>One of the three possible sync signals, see document [6]. |

**Figure 12. HSE/LSE clock source**

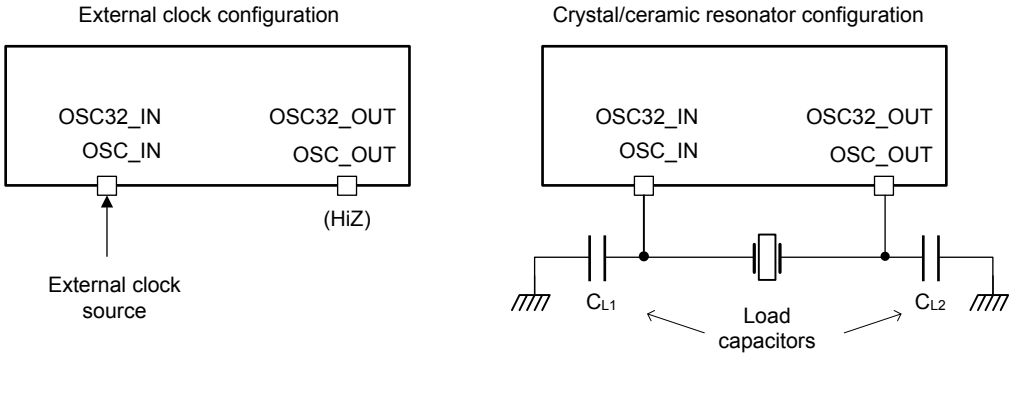


Table 6. **Clock source generation**

| Source | Frequency range | External component | Comments |
|---|---|---|---|
| HSE | 4 to 50 MHz | Yes | High-speed external clock<br>Used when a very accurate high-speed clock is needed. |
| LSE | 32.768 kHz<br>(max 1 MHz) | Yes | Low-speed external clock<br>Used when a very accurate low-speed clock is needed. For instance, for the real-time clock (RTC). |
| HSI | 8, 16, 32 or 64 MHz | No | High-speed internal clock<br>Default system clock after a reset. |
| HSI48 | 48 MHz | No | High-speed internal 48 MHz clock kernel clock for some peripherals.<br>High precision clock for USB with clock recovery system, which can use the USB SOF signal. |
| CSI | 4 MHz | No | Low-power internal oscillator faster startup time than HSI<br>It can be used for wake-up from Stop mode |
| LSI | 32 kHz | No | Low-speed internal clock, for independent watchdog (IWDG), RTC, and autowake-up unit (AWU).<br>This clock can run in Stop or Standby modes. |
| PLL | 2 to 16 MHz input | No | Wide-range mode |
| | 1 to 2 MHz input | | Low-range mode<br>Some specific frequencies are obtained with an integer ratio, which may be needed for some application (for example, audio). |
| | 150 to 420 MHz VCO output | | Integer or fractional ratios are supported for all PLLs. |
| | 400 to 1600 MHz VCO output | | |

To optimize power consumption, each clock source can be switched on or off independently when it is not used. For a detailed description of the clock tree, see document [6]. This document provides a complete view of clock usage by a peripheral is provided in the kernel clock distribution overview.

## 4.1 HSE and LSE bypass (external user clock)

In this mode, an external clock source must be provided to the OSC_IN/OSC32_IN pins.

For LSE bypass, the external source has to be "low swing".

The signal (square, sinus, or triangle) with ~50% duty cycle drives the OSC_IN/OSC32_IN pin.

## 4.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator has the advantage of producing a very accurate main clock.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins to minimize the output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For $C_{L1}$ and $C_{L2}$, use high-quality ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high frequency applications and selected to meet the requirements of the crystal or resonator. $C_{L1}$ and $C_{L2}$ are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of $C_{L1}$ and $C_{L2}$. The PCB and MCU pin capacitances must be included when sizing $C_{L1}$ and $C_{L2}$ (10 pF can be used as a rough estimate for the combined pin and board capacitance).

The HSERDY flag in the RCC clock control register (RCC_CR) indicates if the high-speed external oscillator is stable or not. At startup, the clock is not provided until the hardware provides this bit. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

If it is not used as a clock source, the HSE oscillator can be switched off using the HSEON bit in the RCC clock control register (RCC_CR).

## 4.3 LSE oscillator clock

The use of an external oscillator provides a low-power highly accurate clock source, which is required for real-time clock (RTC), clock/calendar, and other timing functions.

The LSE crystal oscillator has a configurable driving capability. This capability is chosen according to the external resonator component to ensure stable oscillation. It is based on the maximum critical crystal gm. See documents [1], [2] and [3] for further information.

The driving capability is set through the LSEDRV [1:0] in the RCC_BDCR register:

- 00: Low drive
- 10: Medium low drive
- 01: Medium high drive
- 11: High drive.

The LSERDY flag in the RCC backup domain control register (RCC_BDCR) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by the hardware.

An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIER).

The LSE oscillator is switched on and off by programming the LSEON bit in the RCC backup domain control register (RCC_BDCR).

## 4.4 Clock security system (CSS)

The device provides two clock security systems (CSS), one for HSE oscillator and one for LSE oscillator. Software can independently enable them.

When the clock security system on HSE is enabled, the clock detector is activated after the HSE oscillator startup delay, and disabled when this oscillator is stopped:

- The HSE oscillator can be used directly or indirectly as the system clock. When used indirectly, it means that it is used as a PLL input clock, and the PLL clock is the system clock. When failure is detected, the system clock switches to the HSI oscillator and the HSE oscillator is disabled.
- If a failure is detected on the HSE clock, this oscillator is automatically disabled, a clock failure event is sent to the break inputs of the advanced-control timers TIM1, TIM15, TIM16, and TIM17 and a nonmaskable interrupt is generated to inform the software of the failure (clock security system interrupt rcc_hsecss_it), allowing the MCU to perform the rescue operations needed. The rcc_hsecss_it is linked to the Arm® Cortex®-M7 NMI (nonmaskable interrupt) exception vector.
- If the HSE oscillator clock is used as the PLL clock source, the PLL is also disabled when the HSE fails.

The clock security system on LSE must be enabled only when the LSE is enabled and ready, and after the RTC clock has been selected through the RTCSRC[1:0] bits of RCC_BDCR register.

When an LSE failure is detected, the CSS on the LSE wakes the device up from all low-power modes except $V_{BAT}$.

If the failure occurred in $V_{BAT}$ mode, the software can check the failure detection bit when the device is powered on again. In all cases, the software can select the best behavior to adopt (including disabling the CSS on LSE, which is not automatic).

## 4.5 Clock recovery system (CRS)

The clock recovery system (CRS) is dedicated to the internal HSI48 RC oscillator. The CRS is an advanced digital controller acting on the internal fine-granularity trim resulting in a very precise 48 MHz clock.

The CRS is ideally suited to provide a precise clock for the USB OTG_FS peripheral in device mode.

The CRS requires a synchronization signal.

Three possible sources are selectable with programmable prescaler and polarity:

- SYNC external signal provided through pin;
- LSE oscillator output;
- USB SOF packet reception.

For more details, see document [6].

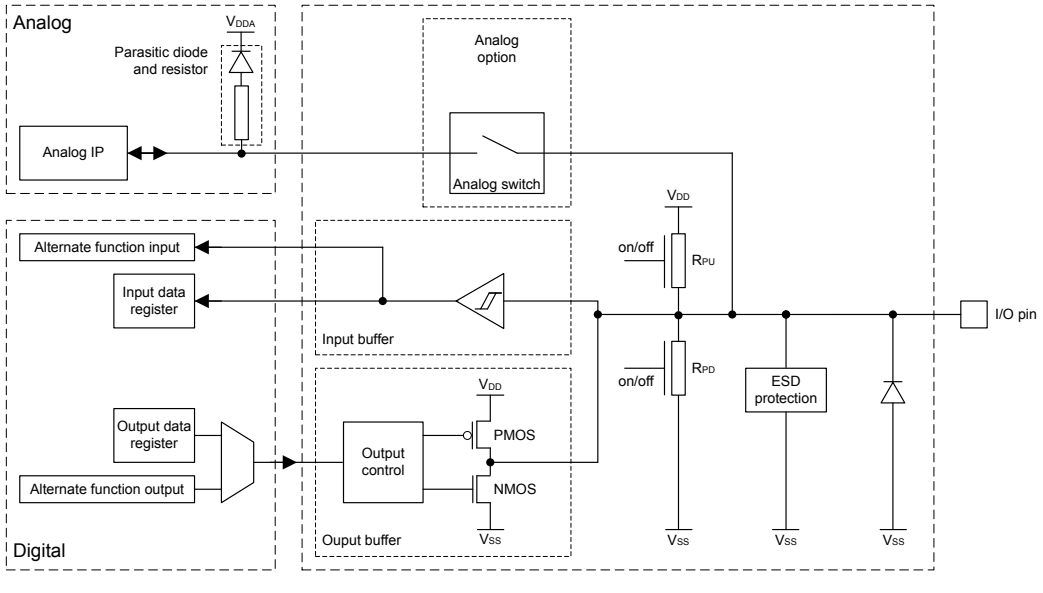
# 5 Alternate function mapping to pins

To effectively explore the alternate peripheral function pin mapping, refer to the STM32CubeMX tool available on www.st.com.

## 5.1 Analog inputs for ADC1, ADC2

The figure below shows the pad schematic. For further information, see document [6].

**Figure 13. GPIO STRUCTURE**




Each ADC has 19 inputs INP0 to INP18 and INN0 to INN18 (17 external channels). For further information on the ADC connectivity figure, see document [6].

STM32CubeMX and the table “pin/ball definition” in the documents [1] and [2] show the availability of the Pxy depending on the package.

STM32CubeMX and the table “Port A,B,C and Port F alternate function” in the documents [1] and [2] indicate the functions available on the Pxy pads by closing the switch between the two pads.

Closing the switch in the pad (GPIOx_MODER bit) connects an ADC input to the Pxy pad. For further details, see the figure *ADC connectivity* in the document [6], and the characteristic table in the documents [1] and [2].

During the rate estimation, an additional serial impedance due to this switch (300 Ω to 550 Ω) and additional parasitic capacitance (2.5 pF) may impact timing sensitive signals. For further information, refer to the sampling rate in the *ADC characteristic table* in the documents [1] and [2].

# 6 Boot configuration

## 6.1 Boot mode selection

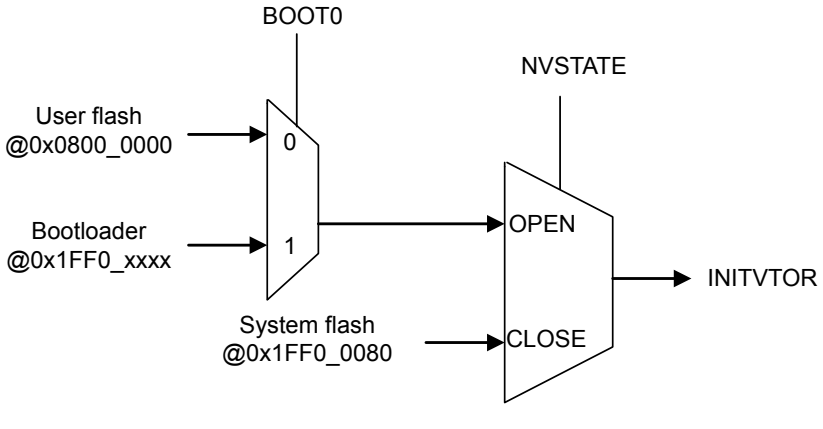
Two different boot areas can be selected through the BOOT0 pin, depending on the PRODUCT-STATE and NVSTATE, as shown in Table 7. Boot modes and in Figure 14. SBS boot control.

The BOOT0 state coming from the external pin is latched upon reset release. This pin is in input mode during the complete reset phase, and then switches automatically in analog mode after the reset is released.

**Table 7. Boot modes**

| Boot mode selection | | | BOOT AREA |
|---|---|---|---|
| PRODUCT-STATE | NVSTATE | BOOT0 | |
| Open | OPEN | 0 | Boot from the user flash memory at 0x0800 0000. |
| | | 1 | Boot from the bootloader. |
| Closed | CLOSE | - | Boot from the RSS in flash memory at 0x1FF0 0080. |

**Figure 14. SBS boot control**



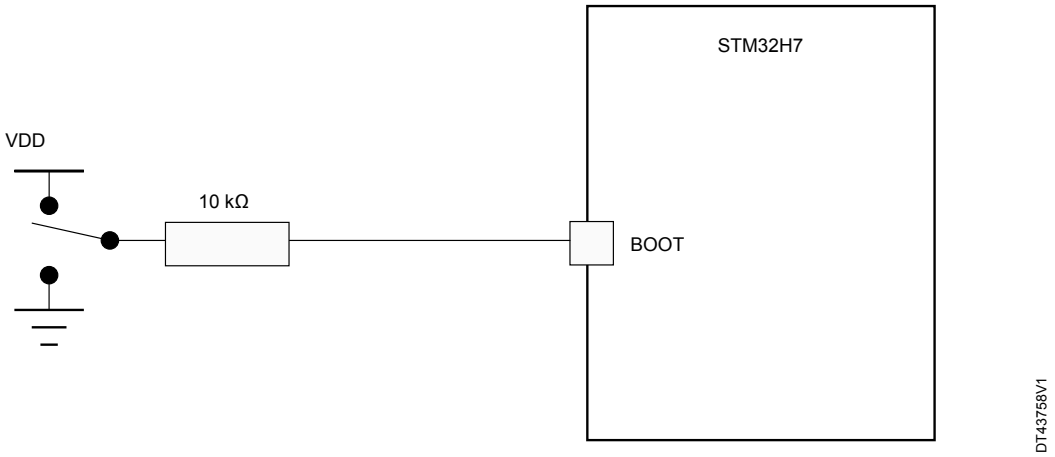

The NVSTATE value comes from the flash memory interface, following an automatic option-byte load sequence. For further information, see embedded flash memory (FLASH) in document [6].

Depending on the life cycle of the device, the debug is always allowed for open devices (NVSTATE = OPEN) and disabled for close devices (NVSTATE = CLOSE), but can be reopened during the boot after an authenticated debug sequence. For further information, see system configuration, boot, and security (SBS) in the document [6].

## 6.2 Boot pin connection

The figure below shows the external connection required to select the boot memory of STM32H7Rx/7Sx microcontrollers.

Figure 15. **Boot mode selection implementation example**




*Note: Resistor values are given only as a typical example.*

## 6.3 System bootloader mode

The embedded bootloader code is located in the system memory. It is programmed by STMicroelectronics during production. It is used to reprogram the flash memory using one of the following serial interfaces.

The table below shows the supported communication peripherals by the system bootloader.

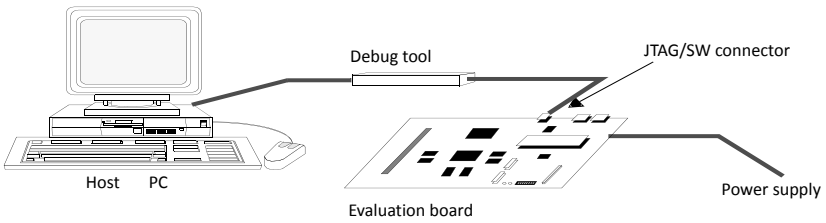
Table 8. **STM32H7Rx/7Sx MCU bootloader communication peripherals**

| Bootloader peripherals | Bootloader pins |
|---|---|
| DFU | USB OTG FS (PM12/PM11) in device mode |
| USART1 | PA10/PA9 |
| USART2 | PA3/PA2 |
| USART3 | PD9/PD8 |
| UART4 | PD0/PD1 |
| FDCAN2 | PB5/PB1 |
| I2C1 | PB8/PB7 |
| I2C2 | PB10/PB11 |
| I2C3 | PA8/PC9 |
| I3C1 | PB8/PB7 |
| SPI1 | PA4/PA5/PA6/PA7 |
| SPI2 | PB15/PB14/PB13/PB12 |
| SPI3 | PC12/PB4/PB3/PA15 |

# 7 Debug management

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG, or software connector and a cable connecting the host to the debug tool. The figure below illustrates the connection of the host to the evaluation board.

**Figure 16. Host to board connection**




DT41077V1

## 7.1 SWJ debug port (serial wire and JTAG)

The core of the STM32H7Rx/7Sx microcontrollers integrates the serial wire/JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port that combines a 5-pin JTAG-DP interface and a 2-pin SW-DP interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two SW-DP JTAG pins the are multiplexed with some of the JTAG-DP five JTAG pins.

For more details on the SWJ debug port, refer to the SWJ debug port section (serial wire and JTAG) in the document [6].

### 7.1.1 TPIU trace port

The TPIU trace port comprises four data outputs plus one clock output.

Software configures the number of data outputs. Unused signals can be reused as GPIOs.

If the trace port is not required, all the signals can be used as GPIOs. By default, the trace port is disabled.

The trace data and clock can operate at up to 133 MHz. As a result, care must be taken with the layout of these signals: the trace connector must be located as close as possible to the microcontroller, while still allowing enough space to attach the trace port analyzer probe.

The table below contains a summary of trace pins and GPIO assignment.

**Table 9. TPIU trace pins**

| Trace pin name | Type | Description | Pin assignments |
|---|---|---|---|
| TRACED0 | Output | Trace synchronous data out0 | PC1 or PE3 orPG13 |
| TRACED1 | Output | Trace synchronous data out1 | PC8 pr Ë4 or PG14 |
| TRACED2 | Output | Trace synchronous data out2 | PD2 or PE5 |
| TRACED3 | Output | Trace synchronous data out3 | PC12 or PE6 |
| TRACECLK | Output | Trace clock | PE2 |

### 7.1.2 External debug trigger

The bidirectional TRGIO signal can be configured as TRGIN or TRGOUT by software.

The table below contains a summary of trigger pins and GPIO assignment.

**Table 10. External debug trigger pins**

| Trigger pin name | Type | Description | Pin assignments |
|---|---|---|---|
| TRGIO | Input/output | Bidirectional external trigger | PC7 |

## 7.2 Pinout and debug port pins

STM32H7Rx/7Sx MCUs are available in various packages, with different number of pins.

As a result, some functionalities are related to the pin availability (TPIU parallel output interface), and differ between packages.

### 7.2.1 SWJ debug port pins

Five pins are used as outputs from the STM32H7Rx/7Sx MCUs for the SWJ-DP as alternate general-purpose I/O functions. These pins are available on all packages and detailed in the table below.

**Table 11. SWJ debug port pins**

| SWJ-DP pin name | JTAG DEBUG PORT | | SW debug port | | Pin assignments |
|---|---|---|---|---|---|
| | Type | Description | Type | Description | |
| JTMS/SWDIO | I | JTAG test mode selection | IO | Serial wire data input/output | PA13 |
| JTCK/SWCLK | I | JTAG test clock | I | Serial wire dock | PA14 |
| JTDI | I | JTAG test data input | - | - | PA15 |
| JTDO/TRACESW | O | JTAG test data | - | TRACESWO if asynchronous trace is enabled | PB3 |
| NJTRST | I | JTAG test nReset | - | - | PB4 |

### 7.2.2 Flexible SWJ-DP pin assignment

After RESET (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately available to the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32H7Rx/7Sx microcontrollers offer the possibility of disabling some or all of the SWJ-DP ports and so freeing the associated pins for general-purpose IO (GPIO) usage.

The table below shows the different possibilities to release some pins.

**Table 12. Flexible SWJ-DP assignments**

| Available debug ports | SWJ IO pin assigned | | | | |
|---|---|---|---|---|---|
| | PA13 JTMS | PA14/JTCK/ SWCLK | PA15/JTDI | PB3/JTDO | PB4/NJTRST |
| Full SWJ (JTAG-DP + SW-DP) - reset state | X | X | X | X | X |
| Full SWJ (JTAG-DP + SW-DP) but without NJTRST | X | X | X | X | - |

| Available debug ports | SWJ IO pin assigned | | | | |
|---|---|---|---|---|---|
| | PA13 JTMS | PA14/JTCK/ SWCLK | PA15/JTDI | PB3/JTDO | PB4/NJTRST |
| JTAG-DP disabled and SW-DP enabled | X | X | - | | - |
| JTAG-DP disabled and SW-DP disabled | Released | | | | |

For more details on how to disable SWJ-DP port pins, refer to the I/O pin alternate function multiplexer and mapping section in the document [6].

### 7.2.3 Internal pull-up and pull-down on JTAG pins

The devices embed internal pull-ups and pull-downs to guarantee a correct JTAG behavior. Consequently, the pins are not left floating during reset and they are configured as follows until the user software takes control:

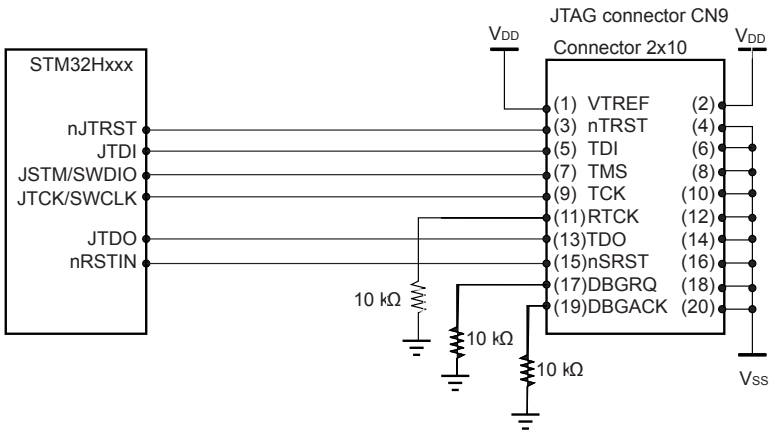
- NJTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- JTCK/SWCLK: internal pull-down
- JTDO: floating state (tristate)

If these I/Os are externally connected to a different voltage, a leakage current flows during and after reset, until they are reconfigured by software. Special care must be taken with the TCK/SWCLK pin, which is directly connected to some of the clock flip-flops, since it must not toggle before JTAG I/O is released by the user software.

### 7.2.4 SWJ debug port connection with standard JTAG connector

The figure below shows the connection between STM32H7Rx/7Sx MCUs and a standard JTAG connector.

**Figure 17. JTAG connector implementation**



# 8 Recommendations

### Printer circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to the ground ($V_{SS}$), and another one dedicated to the $V_{DD}$ supply.

This provides both good decoupling and good shielding effect. For many applications, cost reasons prohibit the use of this type of board.

In this case, the major requirement is to ensure a good structure for the ground and the power supply.

### Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution to reduce the cross-coupling on the PCB (noisy, high-current circuits, low-voltage circuits, and digital components).

### Ground and power supply ($V_{ss}$, $V_{DD}$)

Every block (such as noisy, low-level sensitive, and digital) must be grounded individually. All ground must return to a single point. Loops must be avoided or have a minimum area. The power supply must be implemented close to the ground line to minimize the supply loop area. This is because the supply loop acts as an antenna, and therefore becomes the EMI main transmitter and receiver. All component-free PCB areas must be filled with additional grounding to create adequate shielding (especially when using single-layer PCBs).

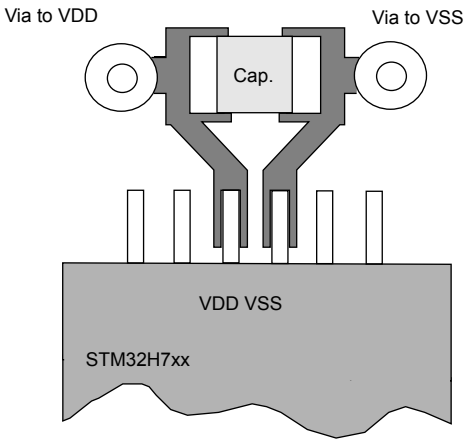
### Decoupling

All the power supplies and ground pins must be properly connected to the power supplies. These connections, including pads, tracks, and vias must have the lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with filtering ceramic capacitors (100 nF) and one single ceramic capacitor (min. 4.7 µF) connected in parallel. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but the exact values depend on the application needs.

The figure below shows the typical layout of such a $V_{DD}/V_{SS}$ pair.

**Figure 18. Typical layout for VDD/VSS pair**



### Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (the crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clock).
- Sensitive signals (such as high-Z).

### Unused I/Os and features

All the microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources. To increase the EMC performance, unused clocks, counters, or I/Os, must not be left free. For example, I/Os must be set to 0 or 1 (pull-up or pull-down to the unused I/O pins.) Unused features must be frozen or disabled.

# 9 Reference design description

The evaluation design kit and the NUCLEO-H7S3L8 board are relevant references that can be used as a basis for a specific application development.

For further details, refer to www.st.com.

# 10 Recommended PCB routing guidelines for STM32H7Rx/7Sx microcontrollers

## 10.1 PCB stack-up

To reduce the reflections on high-speed signals, the impedance between the source, sink, and transmission lines have to be matched. The impedance of a signal trace depends on its geometry and its position with respect to any reference plane.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing, which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which addresses all the impedance requirements.

The minimum configuration that can be used is four or six layers stack-up. An eight-layer board may be required for a very dense PCBs that have multiple SDRAM/SRAM/NOR/LCD components. The following stack-ups (See the two figures below) are intended as examples, which can be used as guide lines for a stack-up evaluation and selection.

These stack-up configurations place the GND plane next to the power plane to increase the capacitance and reduce the physical gap between GND and the power plane. So, high speed signals on the top layer have a solid GND reference plane, which helps reduce the EMC emissions. Therefore, moving up in the layers and having a GND reference for each PCB signal layer improves the radiated EMC performance.

**Figure 19. Layer PCB stack-up**

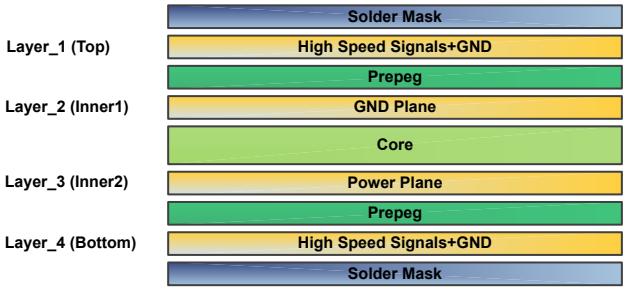
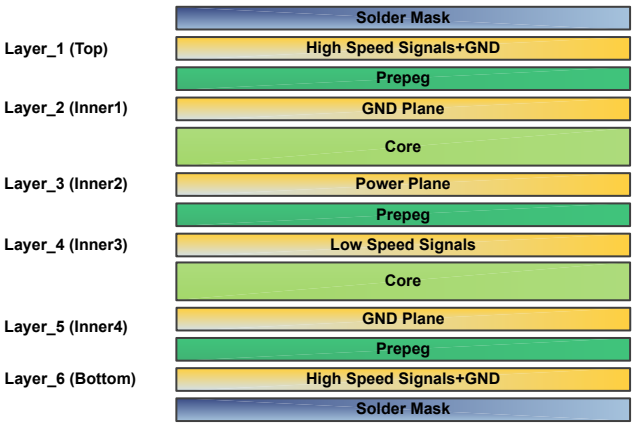



**Figure 20. Six layer PCB stack-up example**



## 10.2 Crystal oscillator

For further guidance on how to layout and route crystal oscillator circuits, check the document [3].

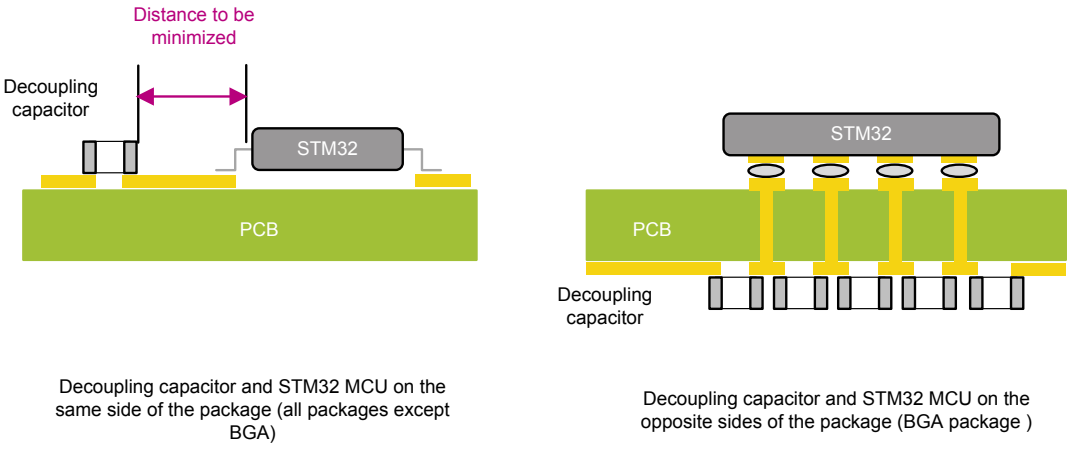
## 10.3 Power supply decoupling

An adequate power decoupling for STM32H7Rx/7Sx MCUs is necessary to prevent excessive power and ground bounce noise. Refer to Table 3. PWR input and output signals connected to package pins/balls.

The following recommendations must be followed:

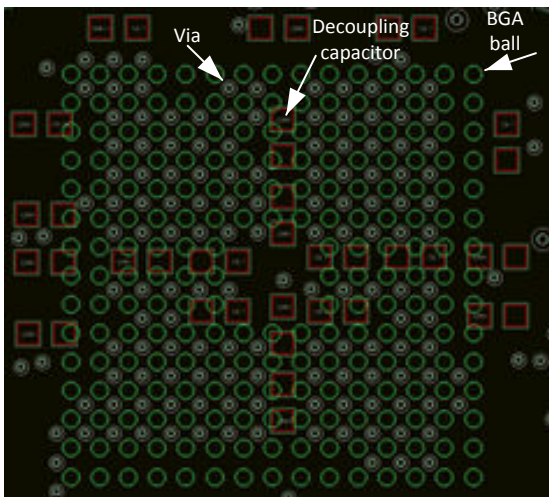
- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU. For BGA packages, it is recommended to place the decoupling capacitors on the opposing side of the PCB (see Figure 21. Decoupling capacitor placement depending on package type. Decoupling capacitor placement depending on package type).
- Add the recommended decoupling capacitors to as many $V_{DD}/V_{SS}$ pairs as possible.
- Connect the decoupling capacitor pad to the power and ground plane with a wide and short trace/via. This reduces the series inductance, maximizes the current flow, and minimizes the transient voltage drops from the power plane and in turn reduces the ground bounce occurrence.

**Figure 21. Decoupling capacitor placement depending on package type**




The figure below shows an example of decoupling capacitor placement underneath the STM32H7Rx/7Sx MCU, closer to the pins and with fewer vias.

**Figure 22. Example of decoupling capacitor placed underneath**



## 10.4 High speed signal layout

### 10.4.1 SDMMC bus interface

**Interface connectivity**

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the AHB peripheral bus and multimedia cards (MMCs), SD memory cards, and SDIO cards.

The SDMMC interface is a serial data bus interface that consists of a clock (CK), command signal (CMD), and eight data lines (D[0:7]).

**Interface signal layout guidelines**

- Reference the plane using GND or PWR (if PWR, add a 10 nf switching cap between PWR and GND).
- Trace impedance: 50 Ω ± 10%.
- All clock and data lines must have equal lengths to minimize any skew.
- The maximum skew between data and clock must be less than 250 ps @ 10 mm.
- The maximum trace length must be less than 120 mm. If the signal trace exceeds this trace-length/speed criteria, then a termination should be used.
- The trace capacitance must not exceed 20 pF at 3.3 V and 15 pF at 1.8 V.
- The maximum signal trace inductance must be less than 16 nH.
- Use the recommended pull-up resistance for CMD and data signals to prevent the bus from floating.
- The mismatch within data bus, data, and CK or CK and CMD must be below 10 mm.
- All data signals must have the same number of vias.

*Note: The total capacitance of the SD memory card bus is the sum of the bus controller capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line. The total bus capacitance is CL= CHost + CBus + N*CCard where the host is an MCU, the bus is all the signals, and the Card is an SD card.*

*The figures below show different typical use cases.*

**Figure 23. microSD™ card interconnection example**

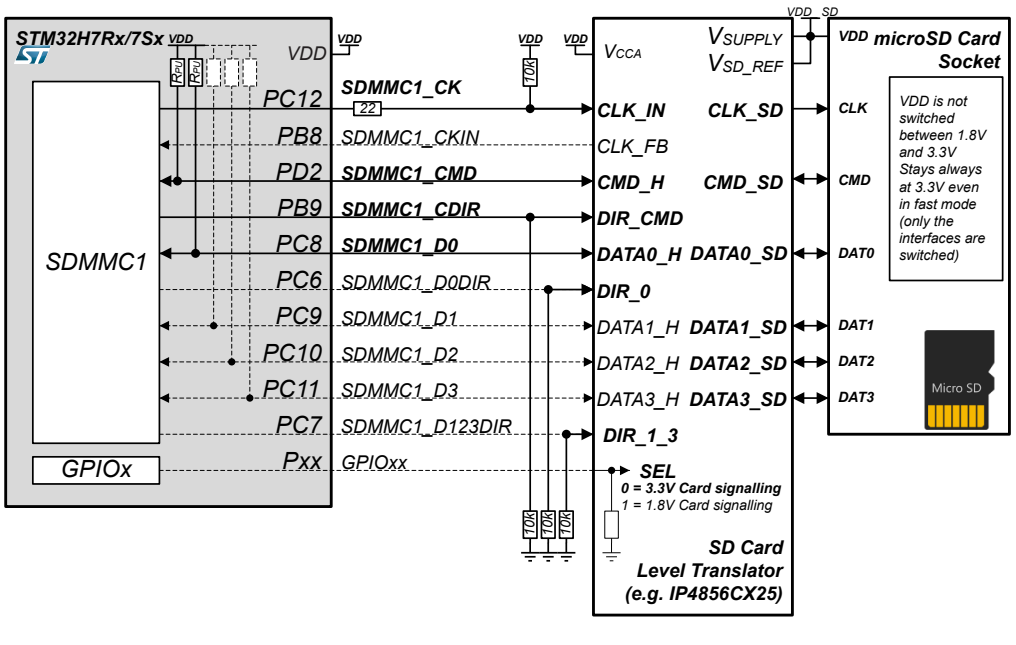
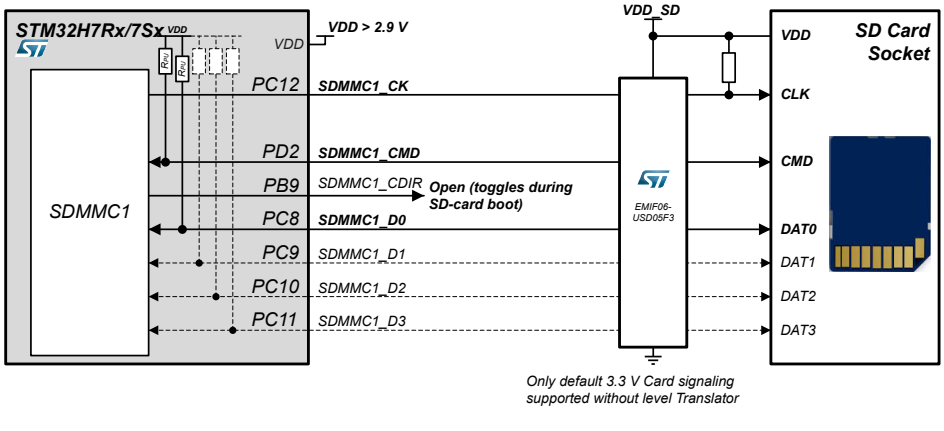



**Figure 24. SD card interconnection example**




## 10.4.2 Flexible memory controller (FMC) interface

### Interface connectivity

The flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND memory controller
- The synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main purposes of the FMC are:

- To translate AXI transactions into the appropriate external device protocol
- To meet the access time requirements of the external memory devices

All external memories share the addresses, data, and control signals with the controller. Each external device is accessed by means of a unique chip select. The FMC performs only one access at a time to an external device. The main features of the FMC are the following:

- Interface with static-memory mapped devices including:
  - Static random-access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by two.

**Interface signal layout guidelines**

- For reference the plane using GND or PWR (if PWR), add 10 nf stitching cap between PWR and GND.
- Trace impedance: 50 Ω ± 10%.
- The maximum trace length must not exceed 120 mm. If the signal trace exceeds this trace-length / speed criteria, then a termination must be used.
- To reduce the crosstalk, it is strongly recommended to place data tracks on the different layers to the address and control lanes. However, when the data and address / control tracks coexist on the same layer they must be separated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew.
- Serpentine traces (this is an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the clock traces to the data/address group traces length to within ±10 mm.
- Match the clock trace length to each signal trace in the address and command groups to within ±10 mm (with maximum of ≤ 20 mm).
- Trace capacitances:
  - At 3.3 V, keep the trace capacitance within 20 pF with overall capacitive loading (including data address, SDCLK, and control) to no more than 30 pF.
  - At 1.8 V, keep the trace capacitance within 15 pF with overall capacitive loading (including data, address, SDCLK, and control) to no more than 20 pF.

### 10.4.3 Extended-SPI interface (XSPI)

The XSPI interface provides communication with external high-speed volatile and nonvolatile memories. Thanks to its flexibility, it supports single-SPI, dual-SPI, quad-SPI, octo-SPI, and 16-bit protocol memories providing high performance, low pin count, and PCB design cost.

A dedicated external power supply for octo-SPI and hexa-SPI interfaces is available.

**XSPI I/O manager (XSPIM)**

The user can set a fully programmable premapping of the XSPI1 and XSPI2 ports signals with the XSPI I/O manager (XSPIM). It connects up to 16-bit external memory on the port 1, and up to 8-bit external memory on the port 2.

In direct mode, each XSPI directly drive the corresponding port (XSPI1 mapped to port 1, XSPI2 mapped to port 2). In Figure 25. XSPI direct mode example, a 16-bit SPI memory is connected to port 1 while an octo-SPI memory is connected to port2.

In swapped mode, the XSPI2 can be configured in 16-bit mode, and the XSPI1 can be configured in octal mode, to connect an external 16-bit memory on port 1, and to connect in a concurrent way an octal external memory connected to port 2 of the I/O manager.

In multiplexed mode, only one output port is used to access two memories. Each memory requests a dedicated chip select. The arbiter in the IO manager manages the access of XSPI1 and XSPI2 to the targeted memory. The external memories can be two separate chips or embedded in a single multichip package.

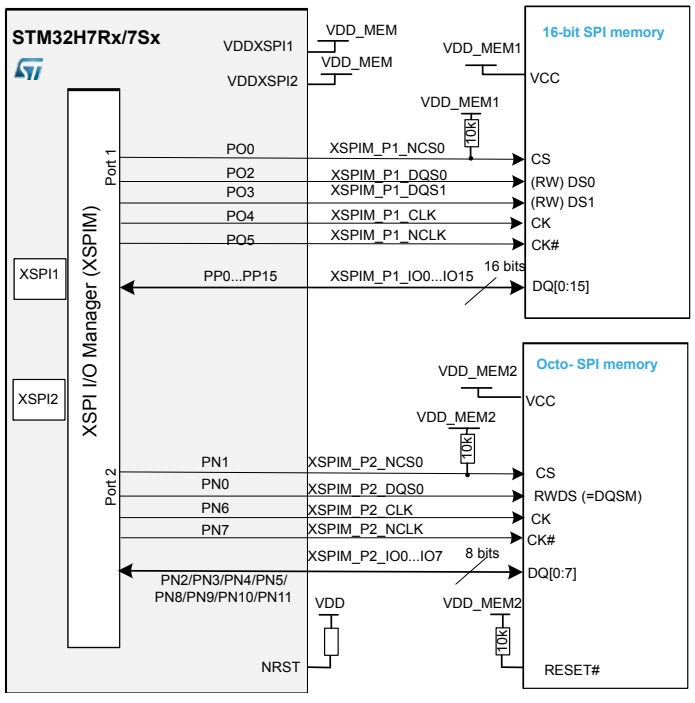
The multiplexed mode can be very useful for some packages where the port2 (or port1) is not mapped. In Figure 26. XSPI multiplexed interconnection example , the same bus of port 1 is shared between two external 16-bit SPI memories.

For additional descriptions of use cases, refer to the XSPI I/O manager (XSPIM) section in the document [6].

**Interface signal layout guidelines**

- Reference the plane using GND or PWR (if PWR, add 10 F stitching capacitor between PWR and GND).
- Trace impedance: 50 Ω for single-ended and 100 Ω for differential pairs (CLK/NCLK).
- The maximum trace length must be less than120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination must be used.
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew.
- Serpentine traces (this is an “S” shape pattern to increase trace length) can be used to match the lengths.
- Avoid using a serpentine routing for the clock signal and use via(s) as little as possible for the whole path. A via alters the impedance and adds a reflection to the signal.
- Avoid discontinuities on high speed traces. Such as vias and SMD components. If SMD components are needed, place these components symmetrically to ensure good signal quality

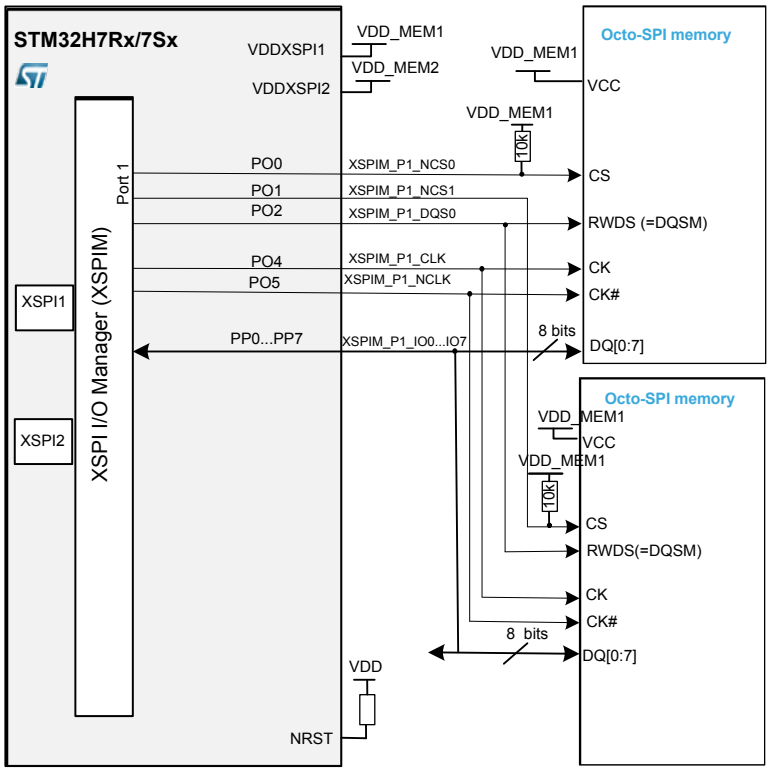
**Figure 25. XSPI direct mode example**




DT71836V2

*Note: Two octo-SPI memories accessed in XSPI dual octal mode can replace the 16-bit SPI memory.*

Figure 26. **XSPI multiplexed interconnection example**




*Note: $V_{DD}$, $V_{DD\_MEM1}$, $V_{DD\_MEM2}$ supply voltage names are completely independent.*

### 10.4.4 ADF interface

The audio digital filter (ADF) is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators, and specially the digital microphones. It is mainly targeted for the following applications: audio capture signals, metering. The ADF features one digital serial interface (SITF0) and one digital filter (DFLT0) with flexible digital processing options in order to offer up to 24-bit final resolution.

The ADF serial interface supports several standards allowing the connection of various ΣΔ modulator sensors: SPI interface, Manchester coded 1-wire interface, PDM interface. For further information, refer to the document [6].

### 10.4.5 Embedded trace macrocell (ETM)

**Interface connectivity**

The ETM enables the reconstruction of the program execution. The data is traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the four data bus lines D[0:3] and the clock signal CLK.

**Interface signals layout guidelines:**

- Reference the plane using GND or PWR (if PWR, add 10 F stitching capacitor between PWR and GNDTrace impedance: 50 Ω ± 10%.
- All the data traces must be as short as possible (≤25 mm).
- Trace the lines, which must run on the same layer with a solid ground plane underneath it without vias.
- Trace the clock, which must have only a point-to-point connection. Any stubs must be avoided.

It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they must be as short as possible. If long stubs are required, there must be a possibility to optionally disconnect them (for example, by jumpers).

### 10.4.6 USB interface

#### USB OTG high-speed controller (OTG_HS)

The USB high-speed host/device (up to 480 Mbit/s) supports both low-speed and full-speed, as well as high-speed modes. It integrates a physical interface (PHY) which can be used for either low-speed (1.5 Mbit/s), full-speed (12 Mbit/s) or high-speed operation (480 Mbit/s). It includes the SOF pulse on the PAD ALT function.

It includes power saving features such as system stop during USB suspend, switch-off of clock domains internal to the digital core, PHY, and DFIFO power management. It includes a dedicated RAM of 4 Kbytes with advanced FIFO control as configurable partitioning of RAM space into different FIFOs for flexible and efficient use of RAM. It supports charging port detection as described in the *Battery Charging specification* (Revision 1.2).

#### USB Type-C®/USB power delivery controller (UCPD)

It is compliant with USB Type-C® release.2.3 and USB Power Delivery release. 3.2 specifications. The controllers use specific I/Os supporting the USB Type-C® and the USB Power Delivery requirements, featuring the USB Type-C® pull-up ($R_p$, current source) and pull-down ($R_d$, resistors) and the USB Power Delivery message transmission and reception. The digital controller handles embed the USB Type-C® level detection with debounce, generating interrupts and FRS detection, generating an interrupt. The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

#### USB OTG full-speed controller (OTG_FS)

The USB OTG full-speed support both host-mode and device-mode. It is compliant with the universal serial bus specification (Rev 2.0). It includes an on-chip full-speed PHY. It includes full support (PHY) for the optional On-The-Go (OTG) protocol detailed in the On-The-Go supplement specification (Rev 2.0). It supports the A-B device identification (ID line). It supports OTG monitoring of VBUS levels with internal comparators and the SOF pulse on PAD ALT function.

It includes power saving features such as system stop during USB suspend, switch-off of clock domains internal to the digital core, PHY, and DFIFO power management. It includes a dedicated RAM of 1.25 Kbytes, with advanced FIFO control as configurable partitioning of RAM space into different FIFOs for a flexible and efficient use of the RAM. It supports charging port detection as described in *Battery Charging specification* revision 1.2.

*Note: For the OTG_HS and UCPD availability in a given package, refer to the documents [1] and [2].*

The internal USB PHYs can be supplied by a dedicated $V_{DD33USB}$ (3.3 V) or by $V_{DD50USB}$ (5 V).

- When supplied by $V_{DD50USB}$ (internal USB regulator used), $V_{DD33USB}$ reflects the output of the internal regulator and used internally to supply the PHYs(OTG_FS/HS) and UCPD (see Figure 27. USB interconnection example when an internal regulator is used).
- When supplied by $V_{DD33USB}$ (internal USB regulator not used), $V_{DD50USB}$ and $V_{DD33USB}$ must be connected to the same supply (see Figure 28. USB interconnection example when an internal regulator is not used).

**Figure 27. USB interconnection example when an internal regulator is used**

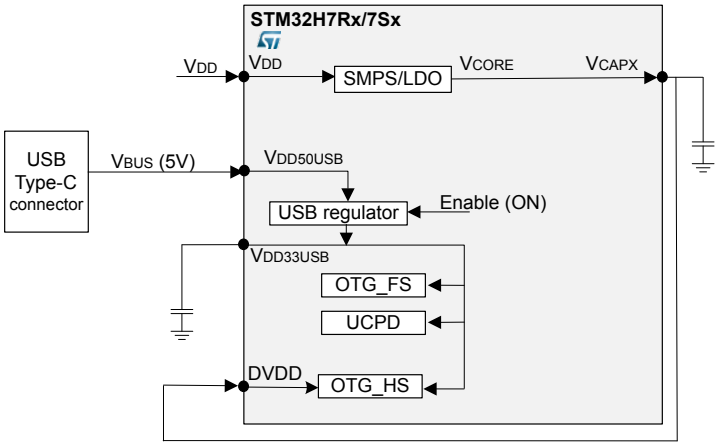
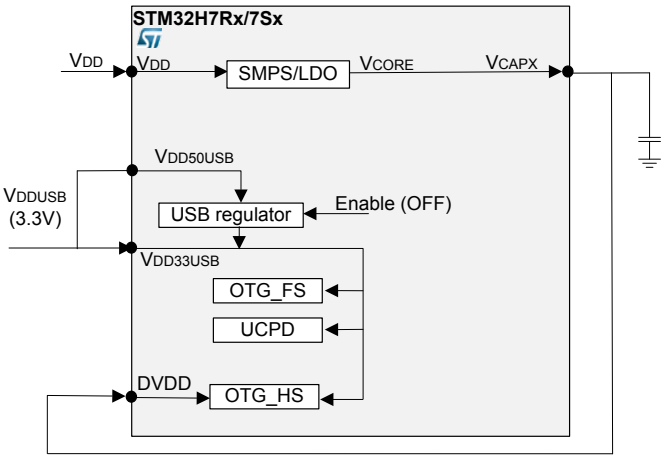


Figure 28. **USB interconnection example when an internal regulator is not used**



# 11 Use case examples

STM32CubeMX must be used to determine the most appropriate package for a given use case.

The table below gives some typical use-case examples.

The table defines the package, which supports a specific use case and identifies the peripherals that are available.

All the examples below are also supported on larger packages.

**Table 13. Use case examples**

| Package | Use case | Peripheral | Comment |
|---|---|---|---|
| TFBGA225 HEXA SMPS GFX | Graphic use case: Camera, display, microSD™, HEXA, and Octo-SPI memory support | LTDC24 | RGB display 8/8/8 |
| | | SDMMC | microSD™ (four-bit mode) |
| | | 1 OCTOSPI, 1 HEXASPI | External octo and 16-bit SPI memory |
| | | DCMIPP | 8-bit camera interface |
| | | OTG_FS/OTG_HS/UCPD | - |
| | | 2 SPI | Communication interface |
| | | 2 UART, 1 USART | Communication interface |
| | | 2 I2C | Communication interface |
| | | FDCAN | FD controller area network |
| | | Timer 4 channels | - |
| | | ADC 2 channels | Analog-to-digital converter |
| | | SAI | Communication interface |
| | | ETH-RMII | Ethernet |
| | | 1 tamper | - |
| | | 8 GPIO | Remaining GPIO available |
| LQFP176 GFX | Graphic use case: Display, microSD™, and Octo-SPI memory support | LTDC24 | RGB display 8/8/8 |
| | | SDMMC | microSD (four-bit mode) |
| | | 2 OCTOSPI | External Octo-SPI memory |
| | | OTG_FS | - |
| | | 2 SPI | Communication interface |
| | | 1 UART, 1USART | Communication interface |
| | | 2 I2C | Communication interface |
| | | FDCAN | FD controller area network |
| | | Timer 5 channels | - |
| | | ADC 4 channels | Analog-to-digital converter |
| | | SAI | Communication interface |
| | | 4 tampers | - |
| | | 8 GPIO | Remaining GPIO available |
| BGA144 GP | GP use case: microSD™, display, Ethernet, and Octo-SPI memory support | FMC | Memory interface used to drive a display (up to 16-bit parallel) |
| | | SDMMC | microSD (four-bit mode) |
| | | 1 OCTOSPI | External Octo-SPI memory |
| | | OTG_FS/OTG_HS/UCPD | - |
| | | 1 UART | Communication interface |
| | | 1 I2C | Communication interface |
| | | Timer 1 | Full |
| | | ADC 1 Channel | Analog-to-digital converter |
| | | ETH-RMII | Ethernet |
| | | 1 tamper | - |
| | | 6 GPIO | Remaining GPIO available |
| BGA144 GP | GP use case: Display, camera, motor control, and Octo-SPI memory support | FMC | Memory interface used to drive a display (up to 16-bit parallel) |
| | | DCMIPP | 8-Bit camera interface |
| | | 1 OCTOSPI | External Octo-SPI memory |
| | | OTG_FS/OTG_HS/UCPD | - |
| | | 1 UART | Communication interface |
| | | 1 I2C/I3C | Communication interface |
| | | Timer 1 | Full |
| | | ADC 7 channels | Analog-to-digital converter |
| | | 2 tamper | - |
| | | 5 GPIO | Remaining GPIO available |

# Revision history

Table 14. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 11-Mar-2024 | 1 | Initial release. |
| 13-Jun-2024 | 2 | Added Caution for Table 4. Power supply connection .<br>Modified typo in Table 2. Security and graphics peripheral availability per product line. |

# Contents

# List of figures

# List of tables