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Issues and Reliability of High-Density FeRAMs

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We discuss some technical issues on the realization of high-density ferroelectric random access memory (FeRAM). Due to reliability concerns of ferroelectric materials, such as fatigue, retention, and imprint, an extra sensing margin is required. In order to overcome these drawbacks, we have improved the ferroelectric capacitor process and design architecture. The fatigue and imprint degradations of the ferroelectric capacitor are significantly suppressed using the newly developed $(Bi_{1-x}La_x)_4Ti_3O_{12}$ (BLT) films. The design architecture was improved using the split word line (SWL) cell array and current gain cell (CGC) operation. Using the above BLT capacitors and design architectures, we have obtained a high sensing margin, a high cell efficiency, and a small cross-talk noise in high-density FeRAMs. [DOI: 10.1143/JJAP.42.2096]

KEYWORDS: ferroelectric, memory, BLT, reliability, design architecture

1. Introduction

Ferroelectric random access memory (FeRAM) is one of the strong candidates for application in mobile electronic devices, such as smart cards, cellular phones and PDA, due to low operation voltage, fast write speed, and high read/write endurance with nonvolatility.[1)] The commercially available dynamic random access memory (DRAM) and static random access memory (SRAM) are high-density devices with high speed, but they lose the recorded data in the event of power outage. The flash memory is nonvolatile but has a slow write speed and limited write endurance. On the other hand, FeRAM has ideal features of conventional memories. However, for the realization of high-density commercially available FeRAMs, some technical issues should be resolved. Ferroelectric materials have a perovskite structure with bistable polarization states. One of the states is used as logic "1" and the other state is used as logic "0". Under some conditions, the ferroelectric materials may degrade, which is the cause of unreliability of FeRAM. Due to the reliability concerns of ferroelectric materials, such as fatigue, retention, and imprint, it is not easy to obtain scaled down FeRAM cells.

Fatigue is the decrease of polarization charge after repeated writing and reading.[2)] Retention is the decrease of polarization after long-term storage.[3)] Imprint is the tendency of one polarization state to become more stable than the other state, which accompanies the loss of polarization.[4,5)] Among the important reliability issues on FeRAM, imprint is the crucial degradation factor. The imprint failure is caused by the shift in specific polarized direction in the hysteresis curve, which arises from the internal field generated during storage at an elevated temperature in ferroelectric capacitors with specific polarization. As a result of imprint, the remnant polarization decays as a function of storage time. On a device level of FeRAM, the bit line signals are determined by the magnitude of switching charge, non-switching charge, and bit line capacitance. Hence, the decay of polarization leads to the reduction of the bit line sensing signal margin. Consequently, it is impossible to distinguish "1" from "0".[6)]

The extra sensing margin considering the imprint degradation is an important factor that increases a cell size. For commercialization of FeRAM, the cell and chip size should be scaled down to the level of conventional memory. In order to overcome the drawbacks, we have to improve the ferroelectric capacitor module process and design architecture. In this paper, we report the enhanced reliabilities against the imprint degradation in newly developed $(Bi_{1-x}La_x)_4Ti_3O_{12}$ (BLT) films[7)] and the advanced design architectures such as split word line (SWL) cell array[8)] and current gain cell (CGC) operation scheme with a high device performance and cell efficiency.

2. Experimental Details

In order to investigate the imprint characteristics on a device level, the sensing margin of FeRAM cells was measured using the 0.35 μm complementary metal oxide semiconductor (CMOS) technology. SBT 2400 Å and BLT 900 Å thin films with Pt electrodes were used as storage capacitors. The ferroelectric capacitor area is 4 μm^2. The details of the measurement[6)] and ferroelectric capacitor process conditions were reported in our previous paper.[7)] The cell signal was determined by comparing cell data with externally supplied variable reference voltage from a memory tester (MS3480 from MOSAID Inc.). For retention and imprint tests, the following sequence was carried out. The devices were written with "1" in one-half of the cells and with "0" in the other one-half, and stored at 175°C for 504 h. After rewriting "1" and "0" for all cells and an interval of 5 s, the bit line voltage distributions were measured at 90°C.

The new design architectures were devised for a scaled down FeRAM chip and were applied to high-density FeRAMs. The design rule was 0.25 μm, and 1-poly/2-tungsten and 2-metal processes were applied. The memory cell size was 1.5 μm^2 and the capacitor size was 0.8 μm^2. The highly reliable BLT ferroelectric capacitors with Pt electrodes were integrated on IrO_2/Ir/TiN layers on top of a w-plug.

3. Results and Discussion

Figure 1 shows cell signal distributions and changes due to imprint degradation after storage at 175°C in SBT-based FeRAMs using the 0.35 μm CMOS technology. After storage at 175°C for 504 h, the single-peaked curves change

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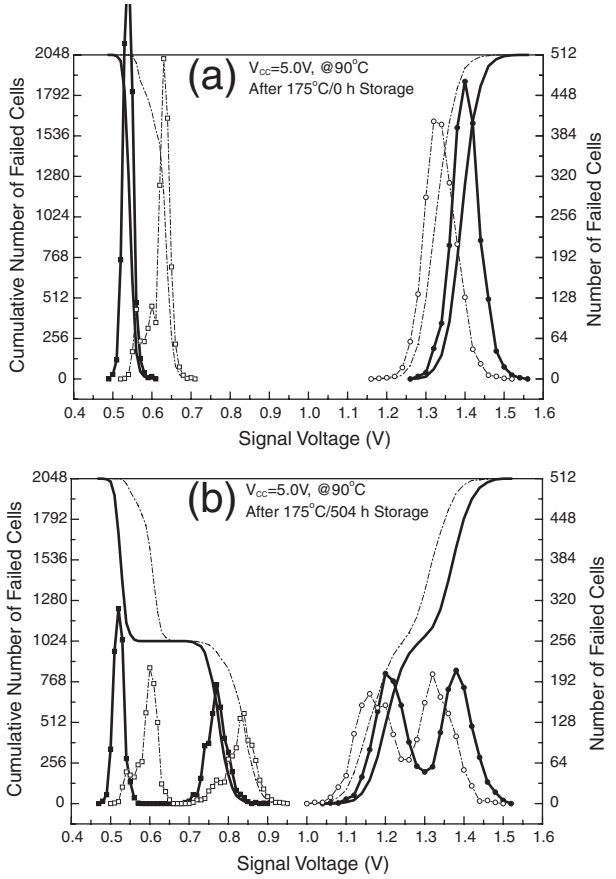

Fig. 1. Cell signal distributions at 90°C (a) before and (b) after storage at 175°C for 504 h in SBT-based FeRAMs using 0.35 μm CMOS technology. Solid and dot-line curves indicate data with the same and opposite data signals between neighboring bit lines, respectively.

to double-peaked curves. This change results from the fact that one-half of the memory cells were written with "0" and the other one-half were written with "1" before storage at 175°C. The memory cells written with "0" show a reduction of "1" signal, while those written with "1" show an increase in "0" signal. The degradation tendency of cell signals is consistent with that of polarization in ferroelectric capacitors. The significant decrease of the sensing signal margin indicates the severe imprint degradation in the SBT storage capacitors. Initially, there is a 450 mV signal margin, but after storage at 175°C for 504 h there remains only 60 mV signal margin. With the longer storage time at an elevated temperature, the larger decrease of the signal margin appears to be due to imprint. Finally, the remaining signal margin becomes smaller than the minimum sensitivity of the sense amplifier leading to a function failure in the FeRAM device. In order to compensate the significant reduction of signal margin due to imprint, the extra margin should be designed using a larger ferroelectric capacitor. Hence, the scaling of FeRAM device is mainly limited by the imprint degradation of ferroelectric capacitor.

In order to overcome the degradation of ferroelectric capacitor, we have to improve the ferroelectric capacitor module process. It has been recently reported that $Bi_4Ti_3O_{12}$ (BTO) thin films doped with La (BLT) are free from fatigue using Pt electrodes.[9] Because the BTO films have strong anisotropic polarization, it is important to control the crystalline direction. The polarization along *a*- or *b*-axis is much larger than that along *c*-axis. However BTO films have a very high tendency to undergo anisotropic crystallization along *c*-axis, so that it is hard to obtain *c*-axis-oriented films. In order to obtain large polarization, we have developed randomly oriented BLT thin films by rapid thermal treatments up to 600°C in oxygen atmosphere followed by a crystallization annealing at 650°C for 60 min. The fatigue and imprint degradation of a ferroelectric capacitor are significantly suppressed using the newly developed BLT films.

The imprint degradation of cell signal distributions after storage at 175°C in BLT-based FeRAMs using the 0.35 μm CMOS technology is shown in Fig. 2. Due to the larger polarization of BLT, the signal margin of BLT-based FeRAMs is larger than that of SBT-based FeRAMs. Furthermore, in comparison with SBT-based FeRAMs, the degradation of bit line signal margin in BLT-based FeRAMs is significantly suppressed. The initial signal margin of 810 mV decreases to 610 mV after storage at 175°C for 504 h. Using the newly developed BLT ferroelectric capacitors, the lifetime of FeRAMs can be greatly increased and the extra margin for imprint degradation is reduced. Hence, there is more possibility to obtain the scaled down cell for high-density FeRAMs.

In Figs. 1 and 2, the differences in the signal distribution between the solid and dot-line curves are also shown. The solid line curve indicates the same data signals between neighboring bit lines, while the dot-line curve indicates the opposite data signals. In the open-bit line cell array, the

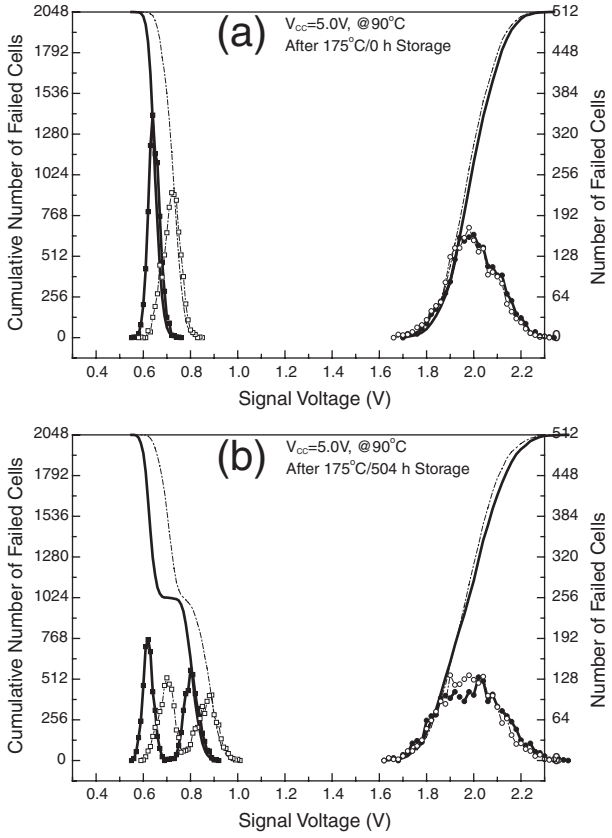

Fig. 2. Cell signal distributions at 90°C (a) before and (b) after storage at 175°C for 504 h in BLT-based FeRAMs using 0.35 μm CMOS technology. Solid and dot-line curves indicate data with the same and opposite data signals between neighboring bit lines, respectively.

opposite data signals between neighboring bit lines interfere with each other, which leads to the degradation of the signal margin. This bit line signal interference is called as the cross-talk noise. Since there is significant degradation of cell signals in FeRAM, the additional signal loss due to cross-talk noise should be overcome to obtain the scaled down chip size.

For the commercialization of FeRAMs, the chip size should be decreased in order to compete with other conventional memories. Therefore, not only the improvement of the ferroelectric capacitor module process, but also the development of advanced design architectures for scaled down FeRAMs is needed. The newly developed advanced design architectures such as the SWL cell array[8] and CGC operation scheme are shown in Figs. 3 and 4. A unit cell of a high-density FeRAM consists of one transistor and one capacitor (1T1C) similar to a DRAM cell. However, supplying a voltage to the plate line (PL) for switching the ferroelectric cell capacitor is additionally required. In the conventional FeRAM architecture, there is a PL parallel to the word line (WL). In the SWL architecture, a WL and its neighboring PL are merged to form a SWL cell array or a single merged line in cell array architecture.[8] In Fig. 3, the SWL array merges two conventional 1T1C cell arrays into one SWL array with an open-bit line. Using SWL, the larger size cell array block can be achieved and we can scale the chip size by 9%.

In conventional FeRAMs, cell operation is based on charge sharing similar to DRAM cell operation. In this scheme, in order to obtain the high cell efficiency of about 40%, a bit line has a large capacitance, which gives rise to a small sensing signal. The CGC operation is devised to have a high sensing margin with an optimized sub-bit line capacitance (<100 fF), a high cell efficiency, and a small cross-talk noise. Figure 3 shows the CGC architecture with a hierarchical bit line scheme, which is composed of a sub-bit line (SBL), a current gain transistor (CGT), and the main bit line (MBL). The SBL voltage is converted to a MBL-sensing voltage by CGT. As the SBL signal increases, more current passes through CGT. The MBL is initially precharged to operation voltage through MBL-sensing load (MSL) as shown in Fig. 4, and then the sensing voltage decreases as the current through CGT increases. Therefore, the larger signal (''1'') in SBL leads to the smaller signal in MBL and the smaller signal (''0'') in SBL leads to the larger signal in MBL. In the conventional cell operation architecture, the bit line capacitance is larger because both the capacitances of SBL (C_{SBL}) and MBL (C_{MBL}) contribute the charge sharing. In CGC operation, only a single optimized SBL capacitance contributes to the charge sharing. Consequently, a much larger cell signal can be generated in SBL.

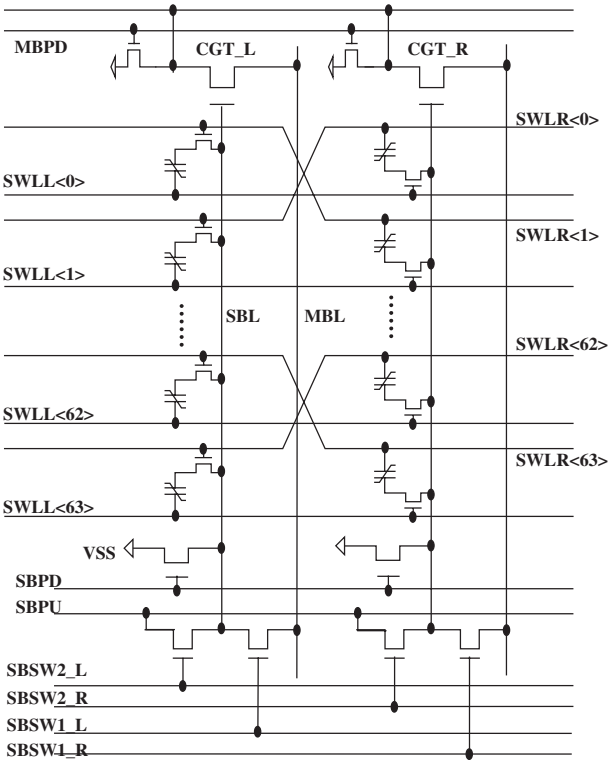

Fig. 3. CGC architecture with hierarchical bit lines and SWL cell arrays for high-density FeRAM.

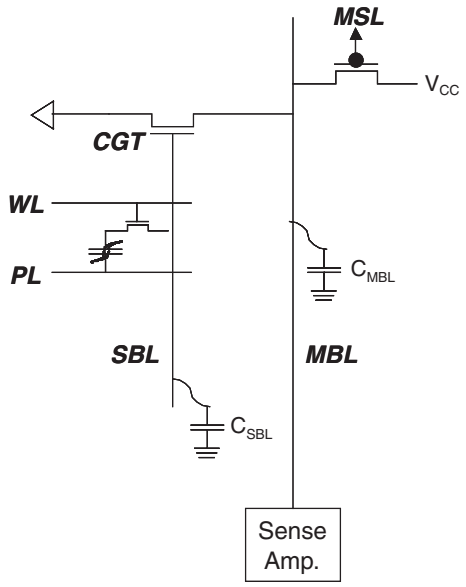

Fig. 4. Circuit diagram of FeRAM with CGC-sensing scheme.

In CGC architecture, the CGT converts the SBL voltage to MBL-sensing voltage based on the CGT gain. Figure 5

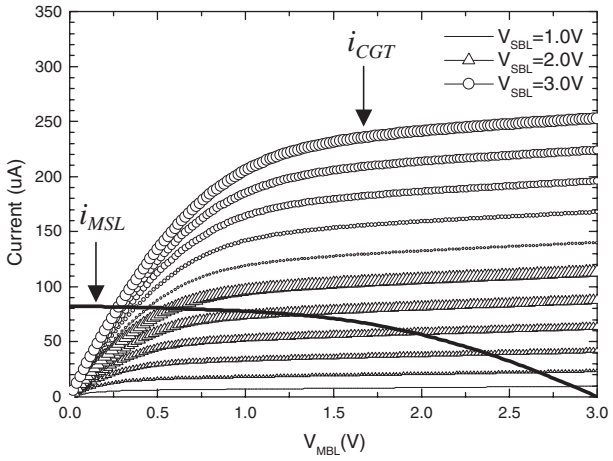

Fig. 5. Currents passing through MSL and CGT as a function of MBL voltage with SBL voltages from 1.0 to 3.0 V.

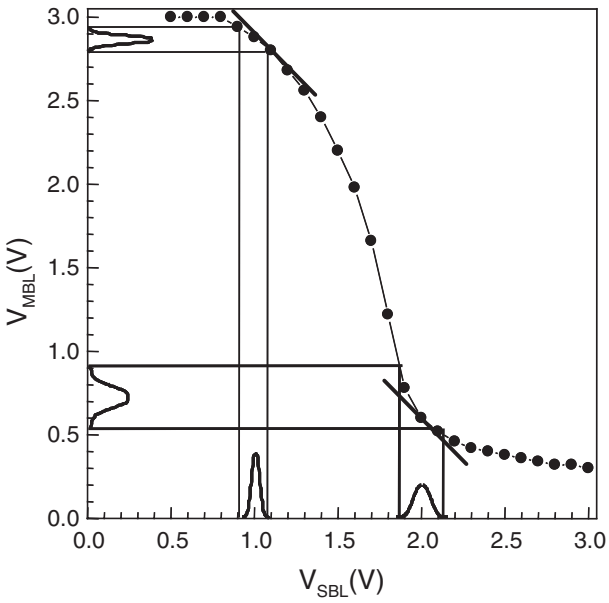

Fig. 6. Signal voltage at MBL (V_{MBL}) amplified by CGT as a function of SBL voltage (V_{SBL}).

shows the measured current-voltage characteristics of NMOS-CGT at various SBL voltages and PMOS-MSL transistors as a function of MBL voltage in our FeRAM devices using the 0.25 μm CMOS technology. At a higher SBL voltage, more current flows through CGT. The sensing voltage of MBL is determined at the points where the amounts of currents passing through CGT and MSL are equal. Consequently, the sensing voltage at MBL amplified by CGT is obtained as a function of SBL voltage as shown in Fig. 6. If the SBL signals are within the amplification window (between 1.0 and 2.0 V), the signal margin at SBL is amplified to a larger sensing margin at MBL. For example, if "0" in SBL is 1.1 V and "1" in SBL is 1.8 V, the signal margin in MBL is amplified to about 1.9 V. By adjusting the current level at CGT with varying the size of CGT, we can optimize the gain of MBL signal and the amplification signal window in SBL.

In the conventional FeRAM cell architecture, inter bit line cross-talk noise may degrade the sensing margin significantly as shown in Figs. 1 and 2. However, in the CGC architecture, SBL and MBL have a complement phase because the high signal in SBL leads to the low signal in MBL and vice versa. Therefore, the cross-talk noise in SBL is almost removed. Using the SWL and CGC design architectures, the chip size can be reduced to 63% and high device performance and cell efficiency can be obtained.

4. Conclusion

Due to the reliability concerns of ferroelectric materials, such as fatigue, retention, and imprint, it is difficult to obtain the scaled down FeRAM cells. In order to overcome these drawbacks, we have improved the ferroelectric capacitor process and design architecture. The fatigue and imprint degradations of ferroelectric capacitor are significantly suppressed by the newly developed BLT films. The key process is the randomly oriented crystallization using special bake treatment sequences to obtain a high polarization at crystallization temperatures less than 650°C. The design architecture is improved using the SWL cell array and CGC operation. In SWL, the larger size of cell array block can be achieved by merging a WL and its neighboring PL. The CGC operation has a high sensing margin with an optimized SBL capacitance, a high cell efficiency, and a small cross-talk noise. Using the above design architectures, the chip size is reduced to 63%.

1) J. F. Scott and C. A. Paz de Araujo: Science **246** (1989) 1400.
2) H. M. Duiker, P. D. Beale, J. F. Scott, C. A. Paz de Araujo, B. M. Melnick, J. D. Cuchiaro and L. D. McMillan: J. Appl. Phys. **68** (1990) 5783.
3) K. Nakao, Y. Judai, M. Azuma, Y. Shimada and T. Otsuki: Jpn. J. Appl. Phys. **37** (1998) 5203.
4) W. L. Warren, H. N. Al-Shareef. D. Dimos, B. A. Tuttle and G. E. Pike: Appl. Phys. Lett. **68** (1996) 1681.
5) M. Grossmann, O. Lohse, D. Bolten, U. Boettger, R. Waser, W. Hartner, M. Kastner and G. Schindler: Appl. Phys. Lett. **76** (2000) 363.
6) Y. M. Kang, S. S. Lee, K. H. Noh, B. Yang, C. H. Chung and N. S. Kang: Integr. Ferroelectr. **37** (2001) 115.
7) B. Yang, Y. M. Kang, S. S. Lee, K. H. Noh, N. K. Kim, S. J. Yeom, N. S. Kang and H. G. Yoon: Int. Electron Device Meet. Tech. Dig., 2001 p. 791.
8) H. B. Kang, D. M. Kim, K. Y. Oh, J. S. Roh, J. J. Kim, J. H. Ahn, H. G. Lee, D. C. Kim, W. Jo, H. M. Lee, S. M. Cho, H. J. Nam, J. W. Lee and C. S. Kim: IEEE Int. Solid States Circuits Conference Tech. Dig., 1999 p. 108.
9) B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, J. Lee and W. Jo: Nature **401** (1999) 682.