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FeRAM Retention Analysis Method Based on Memory Cell Read Signal Voltage Measurement

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Abstract - A novel retention analysis method for ferroelectric random access memory (FeRAM) has been developed, in which read signal voltages from memory cells are measured. It employs on-chip sample/hold circuits, an off-chip A/D converter, and memory LSI testing equipment. FeRAM chip reliability is estimated on the basis of FeRAM read signal voltages after retention periods of 1 day and longer. When used as a tool to estimate long-term data retention in FeRAM chips, and when used to analyze fluctuations in FeRAM cell characteristics, this method can be of significant help in improving the reliability of FeRAM chips.

INTRODUCTION

Ferroelectric random access memories (FeRAMs) require data retention guarantees of at least 10 years, making direct testing impractical. A method for accurately estimating long-term data retention is needed to take the place of such testing.

While much work has been done on estimating the retention characteristics in ferroelectric capacitors [1][2], little appears to have been done on estimating the retention in actual FeRAM chips. Reference [3] reports test results for FeRAM chip retention, but these results are only for failed bit counts after long retention. Estimating FeRAM chip retention lifetime based on ferroelectric physics is difficult.

We have developed a novel FeRAM retention analysis method in which read signal voltages can be directly measured at each of the cells of an FeRAM chip. These voltages can be used to calculate the cells' operational margins, which are related to the physical characteristics of the individual ferroelectric capacitors in the memory cells themselves. On the basis of measurements taken after a significant retention time (i.e., between one day and one month), 10-year data retention can be extrapolated with significant accuracy.

This paper describes this method for measuring read signal voltages and for estimating, based on those measurement results, the long-term retention characteristics of FeRAM chips.

TEST STRUCTURE AND MEASUREMENT METHOD

Figure 1 shows the measurement structure. The main FeRAM body includes memory cells, sense amplifiers (SA1 through SAn), an X-decoder (XDEC) and a Y-decoder (YDEC).

On-chip measurement circuits include sample/hold circuits (S/H1 through S/Hn), a sample/hold circuit selector (YDEC'), and an analog output buffer (BUF). Off-chip components include memory LSI testing equipment and an 8-bit A/D converter.

In normal read operation (see timing chart: Fig. 2), FeRAM cells on a selected word line (WLi) output read signal voltages (Vread) to corresponding bit lines (BLj).

0-7803-6511-9/01/$10.00©2001 IEEE 01CH37153

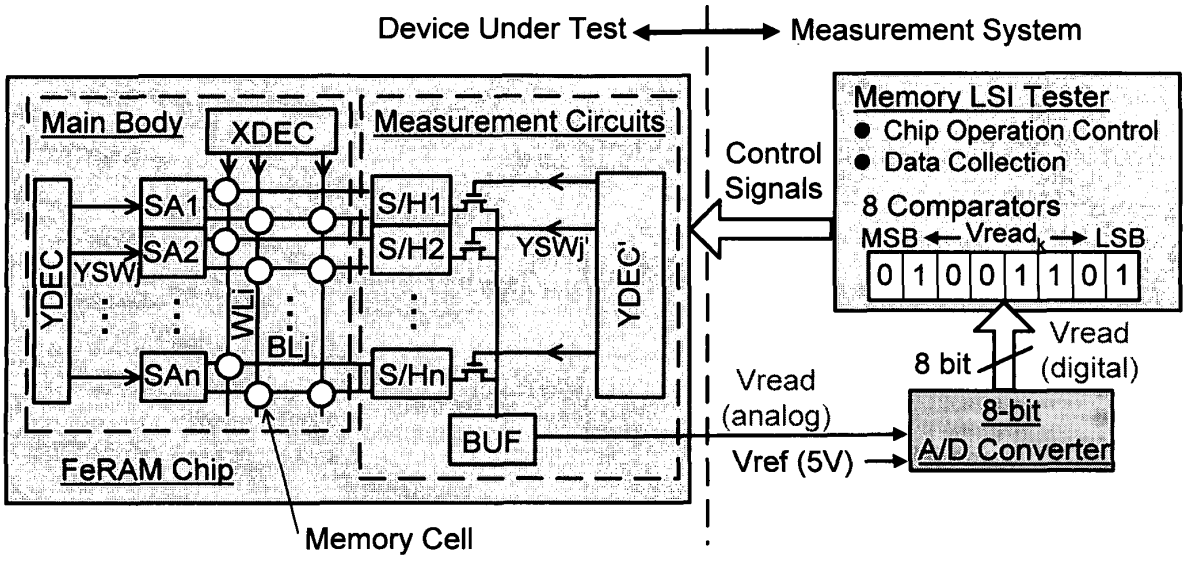


Figure 1. Measurement structure.

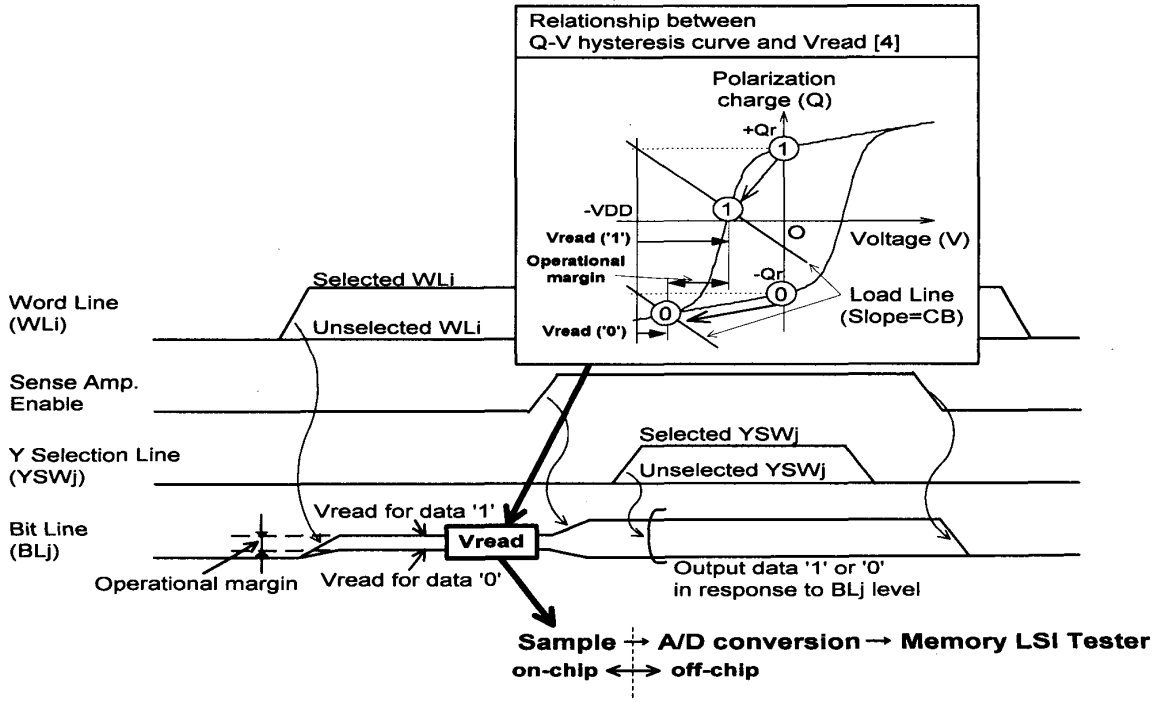


Figure 2. FeRAM read operation.

Sense amplifiers determine, on the basis of voltage level, whether to output a value of '1' or '0' for each piece of read data. The read data, selected by means of a Y selection line (YSWj), is then output from the FeRAM.

The difference in the read voltages from a cell (between '1' and '0') indicates the cell's operational margin. When the operational margin is 0V, the sense amplifier is no longer able to determine a value, and the memory cell does not operate. As generally known [4], Vread is correlated to the Q-V hysteresis characteristics of the cell capacitor, as shown in Fig. 2. Here, CB is the parasitic bit line capacitance, VDD is the voltage applied to the cell capacitor. Knowing Vread

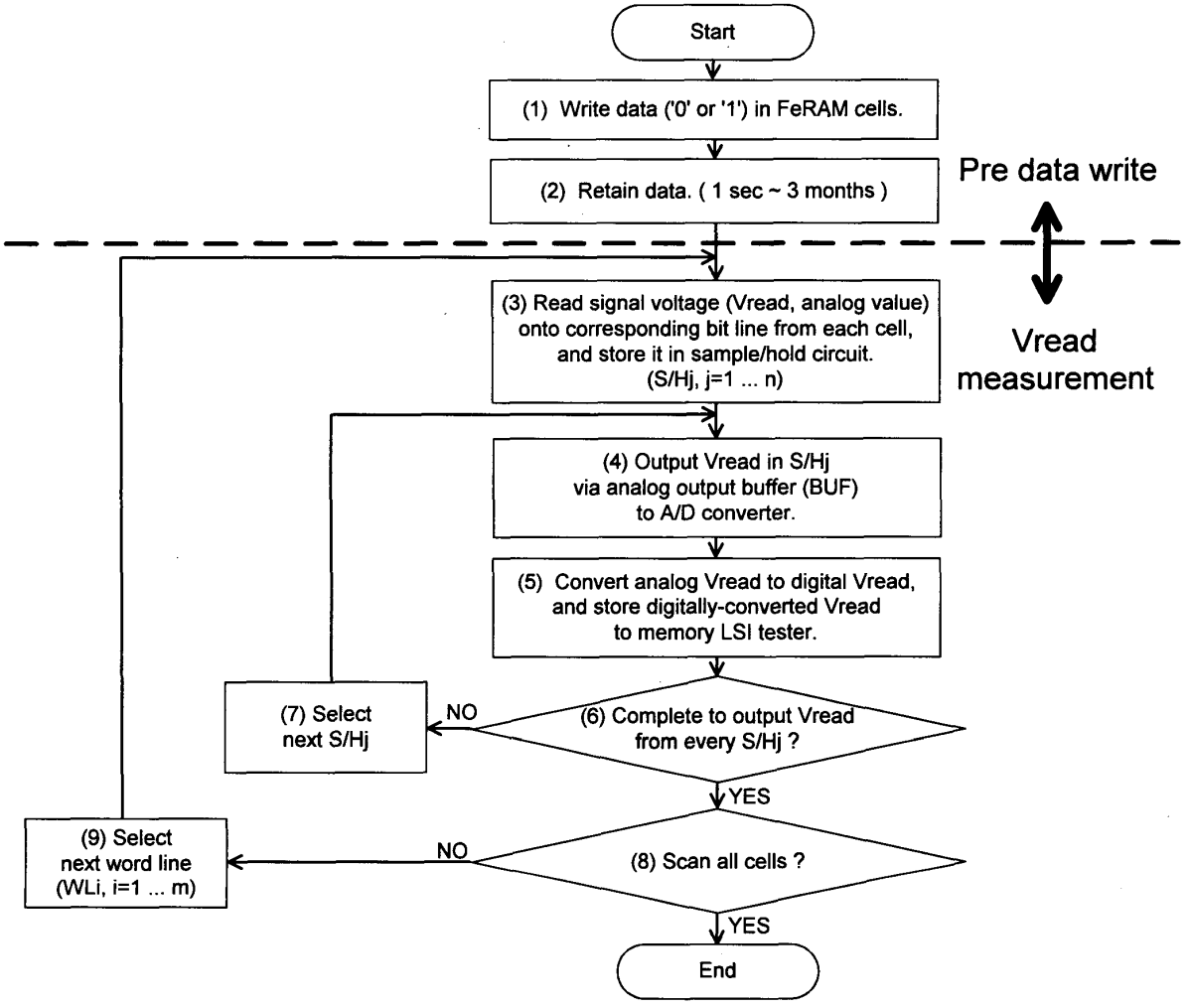


Figure 3. Flowchart of FeRAM read-signal voltage measurement after data retention.

allows us to estimate the "lifetime" of the cell in connection with the physical characteristics of the cell's ferroelectric capacitor. This is why measuring the read signal voltages is useful.

The detailed Vread measurement process is shown in Fig. 3. In this process, the on-chip measurement circuits are enabled, instead of the sense amplifiers and the Y-decoder (refer to Fig. 1). The Vread output from the FeRAM cell is analog, and converted to an 8-bit digital value by means of an off-chip A/D converter. Memory LSI testing equipment with 8 comparators receives the digitally converted Vread for each of the FeRAM cells, and holds these values in storage, along with the corresponding FeRAM cell addresses. The original value of Vread (analog) can easily be calculated using the following equation:

$$\text{Vread (analog)} = \text{Vref} \times \left(\sum_{k=0}^{7} \text{Vread}_k \text{ (digital)} \times 2^k \right) / 2^8 ,$$

where Vread_k represents the digitally-converted Vread (k=0 ~ 7) bit, and Vref is the reference level applied for the A/D converter. To illustrate, when Vread (digital)=01001101 and Vref=5.0 V, Vread (analog) is 1.50 V with a precision of ±0.02 V (1LSB).

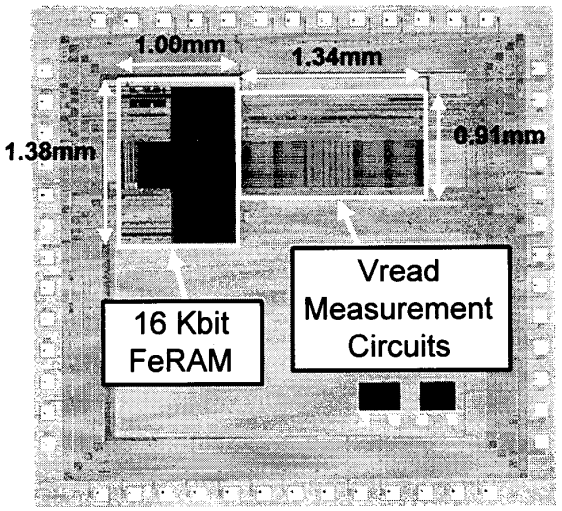
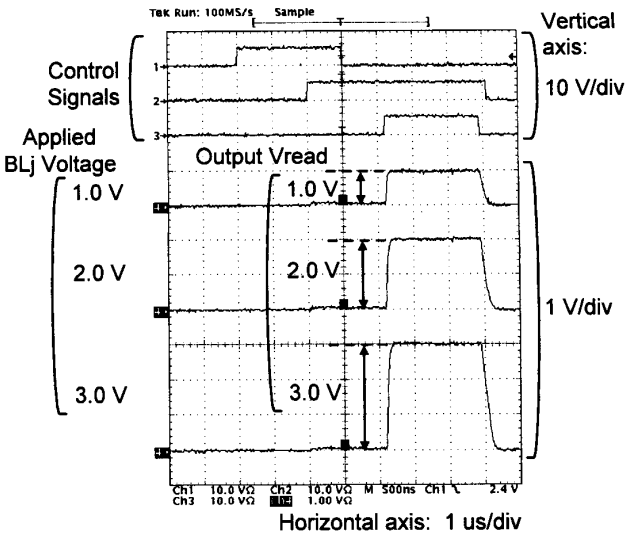
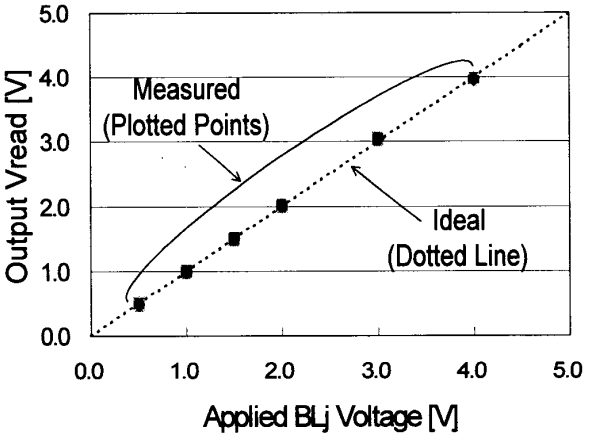


Figure 4. Microphotograph of test chip.



(a) Output waveforms.



(b) Output Vread vs. applied voltage for bit lines.

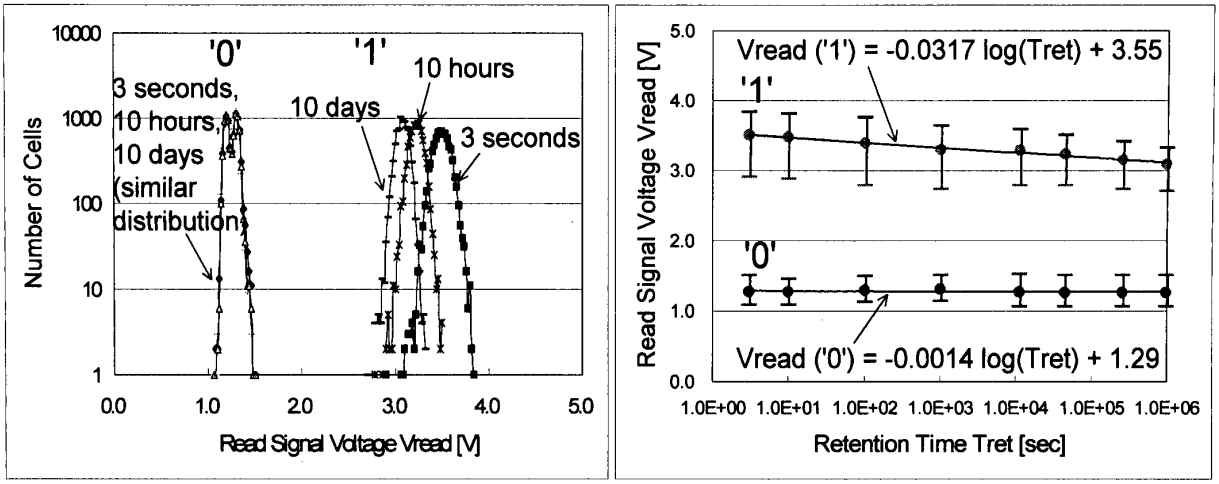
Figure 5. Experimental results: accuracy verification for measurement.

EXPERIMENTAL

We fabricated a 16-Kbit FeRAM test chip containing Vread measurement circuits (Fig. 4) using a 0.35-μm CMOS process. The FeRAM chip itself has 256 word lines and 64 bit line pairs, for which there are 64 corresponding sample/hold circuits in the measurement circuits.

We first tested this circuit to verify its measurement accuracy. Figure 5 (a) shows the waveforms for the Vread obtained from the analog output buffer in the test chip, after the known bit line voltage levels (1.0~3.0 V) were applied from the outside of the test chip. Figure 5 (b) shows the output signal voltage versus the bit line voltage for the 64 sample/hold circuits. The agreement between the measured and ideal values is nearly perfect.

Next, we measured the Vread in the memory cells to estimate the long-term retention of the test chip. Measurements were made between 3 seconds and 10 days after the data were written at 5.5 V and 25℃. Figure 6 (a) shows the distribution of the read signal voltages from the FeRAM cells. Figure 6 (b) is plotted using the same data as in Figure 6 (a), but the horizontal axis represents retention time, and the vertical axis represents read signal voltage. Distributions in read signal voltages of '1' and '0' are plotted with error bars, within which circles indicate the mean distribution values. As seen in Figure 6 (b), '0' data values showed almost no fluctuation over time, but those for '1' gradually decreased as retention time increased. Our experimental data showed that this decrease was proportional to the logarithm of retention time. When extrapolated, the indicated retention time is 6.1×10^{43} years. The accuracy of such estimation can be improved by



(a) Distribution.

(b) Read signal voltage vs. retention time.

Figure 6. Experimental results: read signal voltage after long data retention (max. 10 days ≅ 1 x 10^6 seconds) at 5.5 V and 25℃.

extending the retention time, and retention times of up to 3-months might be considered practical.

Estimation accuracy might be further improved by first using the measured voltage for each cell to calculate the activation energy of the cell's ferroelectric capacitor. An analysis of the relationship between the activation energies and the already measured, relatively short-term retention characteristics of the FeRAM chip could then help us refine the extrapolation-based estimate.

CONCLUSION

We developed a novel FeRAM-retention-analysis method expected to be of significant aid in designing FeRAM chips with improved reliability.

ACKNOWLEDGMENTS

The authors thank Dr. M. Fukuma and Dr. M. Yamashina for their encouragement and support. We also thank the members of the FeRAM-development team for their valuable comments.

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