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FeRAM technology for high density applications

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Abstract

Ferroelectric random access memories (FeRAMs) are new types of memories especially suitable for mobile applications due to their unique properties like nonvolatility, small DRAM-like cell size, fast read and write as well as low voltage/low power behavior. Although standard CMOS processes can be used for frontend and backend/metallization processes, FeRAM technology development has to overcome major challenges due to new materials used for capacitor formation. In this paper, advantages and disadvantages of different ferroelectric materials and major development issues for high density applications are discussed. Results of a 0.5 μm ferroelectric process using $SrBi_2Ta_2O_9$ as ferroelectric layer, Pt as electrode material as well as two-layer tungsten/aluminum metallization are given as an example. Integration and reliability issues are reviewed.

1. Introduction

In recent years ferroelectric random access memories (FeRAMs) have attracted considerable attention as a possible next generation nonvolatile memory technology [1]. This is due to the fact that FeRAMs promise to combine DRAM benefits like small cell size, low voltage and fast access time with a nonvolatile data storage (see Table 1). Up to now only low density products have appeared on the market. For high density applications some major technological issues remain to be solved. An overview of these problems is given in the following sections.

As ferroelectric material either PZT or $SrBi_2Ta_2O_9$ (SBT) is used in current applications. SBT offers the benefits of low fatigue and low voltage operation where PZT seems to be easier to integrate due to its lower processing temperature and higher polarization values.

Ferroelectric memories can be operated in a 2 transistor/2 capacitor (2T/2C) or in a 1 transistor/1 capacitor (1T/1C) mode. The 2T/2C mode offers the benefit of one reference capacitor for each cell and therefore an increased reliability margin. For high density applications, however, a 1T/1C approach is essential.

The simplest way to integrate a ferroelectric capacitor is to contact top and bottom electrode via metal lines resulting in a so called offset cell (Fig. 1b). A smaller bitcell can be obtained when the capacitor is arranged on top of the transistor resulting in the stacked cell structure shown in Fig. 1a. For high density applications the stacked cell is indispensable introducing additional process complexity.

2. Integration of a $SrBi_2Ta_2O_9$ capacitor into a half micron CMOS process

In this work a 0.5 μm, 3.3V CMOS process with two layers of metallization was used as a basis to integrate SBT capacitors. The base process uses LOCOS isolation, and retrograde twin wells in the frontend of line and an Al metallization with W contacts and vias as well as CMP planarization in the backend of line. The process described in the following refers to the fabrication of stacked cells. The used test chip allows the evaluation of stacked and offset cells.

After the transistors have been fabricated and the first interlayer dielectric (BPSG) is deposited and planarized, poly plugs are formed to connect the transistor to the capacitor in the stacked cells. Then the oxygen

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Table 1
Comparison of FeRAM with DRAM, flash and SRAM

	FeRAM[a]	DRAM	Flash	SRAM
Read cycles	10^{12} (10^{15})	10^{15}	10^{15}	10^{15}
Write cycles	10^{12} (10^{15})	10^{15}	10^{6}	10^{15}
Access time (ns)	100 (20)	40–70	40–70	6–70
Write time	100 ns (20 ns)	ns	μs	ns
Relative cell size	2×–5× (1×)	1×	1×	>4×
Data retention	10 years	None	10 years	None

[a] The numbers in parentheses refer to the prognosticated values for further generations.

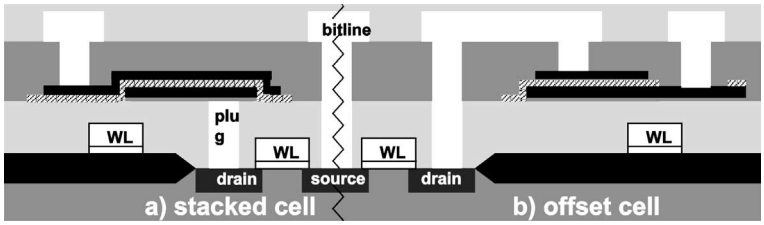

Fig. 1. Principle approaches to integrate a ferroelectric capacitor: (a) stacked cell (b) offset cell.

barrier is deposited and structured, followed by the deposition and structuring of the bottom electrode (Pt1). Subsequently SBT is deposited by chemical solution deposition (CSD) and subjected to a high temperature crystallization anneal. The SBT is then structured by a RIE process and subsequently the top electrode (Pt2) is deposited and also structured in a RIE process. In this way both offset and stacked cells can be characterized on the same chip. An isolation oxide is now deposited and planarized by CMP. After contact holes to Pt and diffusion/poly are etched the standard BEOL processing as used in the CMOS base process can continue. In Fig. 2a and b SEM cross-sections of a typical offset and a typical stacked cell are shown.

3. Oxygen barrier

In a stacked cell approach the capacitor is placed on top of the transistor. To achieve a ferroelectric film, a high temperature anneal in oxygen is necessary in order to transform the as deposited material to the ferroelectric phase. The contact formed between transistor and capacitor may not be degraded by this anneal. A barrier is necessary that withstands the high temperature anneal and keeps the oxygen away from the plug material. Ir based barriers can withstand temperatures in the 700°C range [2].

Stacked capacitors with good hysteresis contacted by poly as well as working stacked cells have been demonstrated with PZT [1] as well as with SBT [3]. Especially for very high density applications much work

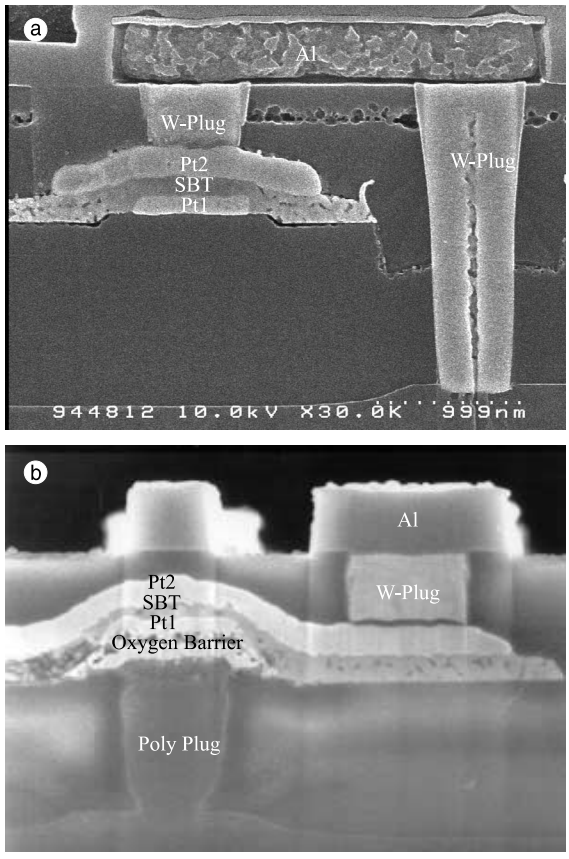

Fig. 2. (a) SEM cross-section of offset cell. (b) SEM cross-section of stacked cell.

remains to be done to reach a temperature stability which is sufficient for SBT with high $2P_r$ values.

4. Low temperature $SrBi_2Ta_2O_9$ processing

In this work SBT deposited by CSD was used. For high density applications the additional thermal budget must be as low as possible in order to keep the oxygen barrier as simple as possible and to influence the CMOS parameters as little as possible. In Fig. 3 the polarization values are given as a function of crystallization temperature for two different film thicknesses. For annealing temperatures below 650°C no ferroelectric behavior is observed [4]. As can be seen from Fig. 3 the crystallization temperature has to be well above 700°C to achieve high polarization values sufficient for a stable operation of very small capacitors.

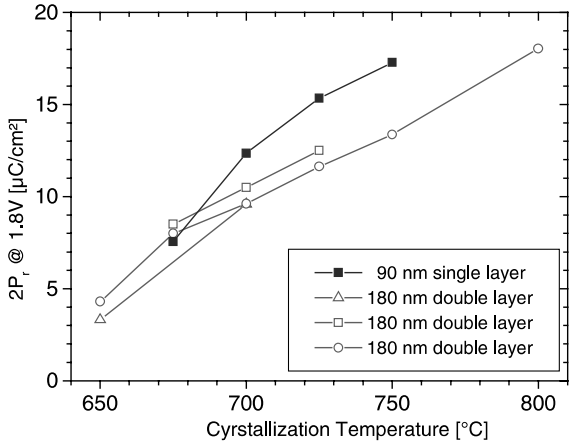

Fig. 3. Polarization values for different crystallization temperatures and SBT films with two different thicknesses.

Changing the SBT composition does not improve the polarization drastically [4]. Crystallization temperatures as low as 650°C could be achieved. But this is usually at the prize of a higher voltage or an increased annealing time.

For future high density applications three-dimensional structures will be necessary in order to establish the required switching charge. In that case a MOCVD technique will be required to achieve a sufficient step coverage. First very promising results with these films were obtained [5]. Some major manufacturing issues, however, still need to be solved.

5. Hydrogen barrier

One of the biggest challenges in the integration of either SBT or PZT into state of the art CMOS processes is the hydrogen sensitivity of these materials. Many different encapsulation layers like TiO_2 [1], Al_2O_3 [1], SiON [6] are proposed to reduce the hydrogen damage to the capacitor during BEOL processing in MLM. We have applied a novel SiN layer to our capacitor. Fig. 4 shows hysteresis loops after metal 1 and after metal 2 processing. After metal 2 some remaining damage is visible. This can also be caused by other effects like

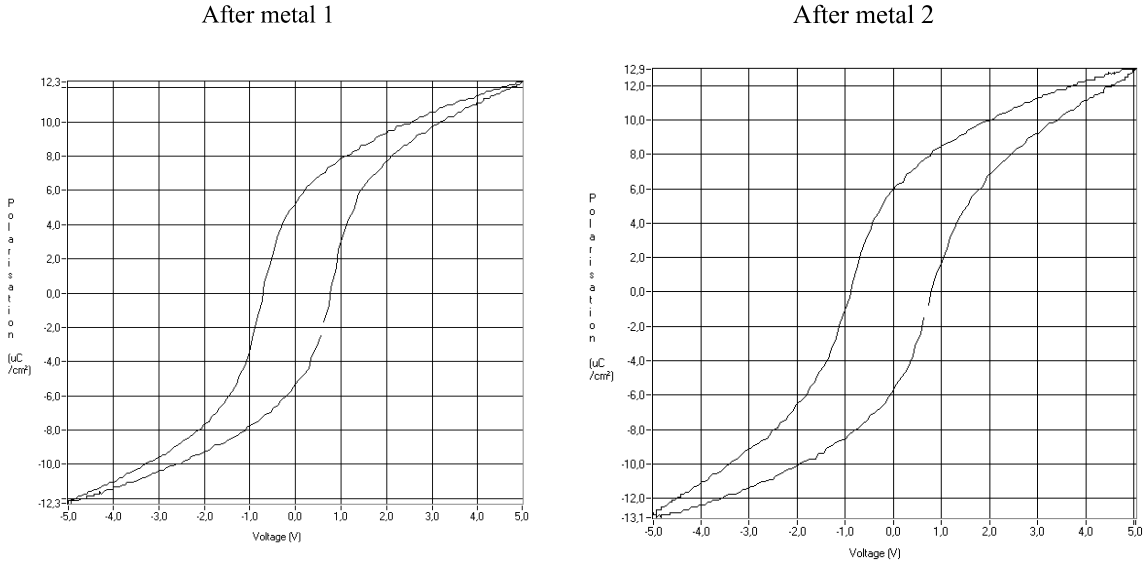

Fig. 4. Hysteresis loops for ferro capacitors with novel SiN EBL after metal 1 and after metal 2 processing. In both cases tungsten plugs for contact and via formation are used.

plasma damage. But a major improvement compared to unprotected capacitors is achieved [7].

6. Reliability

The reliability of a ferroelectric memory is characterized by three main effects:

1. retention,
2. imprint,
3. fatigue.

Retention is the loss of polarization with time. The retention loss at room temperature is generally very small for our capacitors. At 85°C the retention loss is usually in the 10% range and therefore, is not considered to be a major limitation. The stored information is additionally imprinted into the material, i.e., the hysteresis loop is shifted in the voltage direction. At temperatures of 85°C and below we observed extrapolated lifetimes of well above 10 years [8]. Finally fatigue describes the polarization loss with cycling. Fig. 5 shows a hysteresis curve for a capacitor integrated up to metal 1 after processing and after 10^{10} cycles. The loss of polarization is approximately 12%.

7. Summary

FeRAMs promise to be an ideal choice for next generation memory technology. To achieve high density memories, however, some major technological problems still have to be solved. The major challenges lie in the fields of oxygen barrier stability, low temperature processing and sensitivity of the ferroelectric films to BEOL processing. Reliability with respect to retention and imprint seems to be no issue for SBT and operating temperatures up to 85°C. Some improvement in either fatigue or initial polarization is necessary to reach 10^{15} cycles. For processes in the sub 0.2 μm range three-dimensional capacitors will be necessary this will lead to additional process complexity.

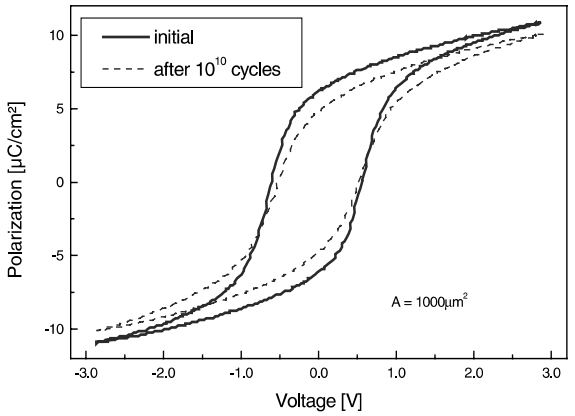

Fig. 5. Fatigue behavior of SBT capacitor directly after processing and after 10^{11} cycles.

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