# 6

# Ferroelectric Random Access Memory (FeRAM)

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***Abstract***

We examine the recent development of ferroelectric memory, along with ferroelectric random access memory (FRAM). Sophisticated non-volatile memories including resistive random access memory (ReRAM), phase-change random access memory (PRAM), and magnetoresistive random access memory (MRAM) have all been expanded, but FRAM is the first of these to be commercially available. Currently, a few Mb of extremely dependable FRAM is accessible. FRAM has been used in sophisticated smartcards, RFID tags, and other electronic devices because of its superior electric features, which include fast read/write speeds around 50 ns, low power consumption, and high switching durability around $10^{13}$. We also discuss recently created materials, manufacturing techniques, and circuit technologies that are anticipated to solve the scalability issue with FRAM.

***Keywords*:** FeRAM, ferroelectric, SRAM, polarization, PZT

## 6.1 Introduction

The polarization state of the ferroelectric material is used to store information in ferroelectric memory, which includes ferroelectric random access memory (FRAM or FeRAM). Ferroelectric materials have bistable polarization states that can be easily switched between even when there isn't an extrinsic electric field present. This field is typically applied at a rate of around 100 kV/cm. Such as FRAM offers superior electric characteristics

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to standard FLASH memory, such as fast read/write speeds around 50 ns, low power consumption, and high switching durability around $10^{13}$; it has been used in RFID tags, authentication systems, and sophisticated smartcards.

Pulvari proposed a ferroelectric material (barium titanate) based method of information storage in 1951 [1]. It is intriguing that he suggested operating this ferroelectric memory at a temperature that is not many degrees less than the Tc (Curie temperature) in order to attain minimum power consumption and fast write/read speeds. 4 years after this suggestion, in 1955, Ross put forth a semiconductor-based ferroelectric memory [2]. Numerous electronic companies throughout the world began challenging the advancement of FRAM in the late 1980s, with the intention of creating "a dream memory" that is non-volatile and has excellent read/write speeds. Some new businesses in the US started working on developing functional Si- based capacitor-type FRAMs in the late 1980s [3, 4]. In the late 1990s, a number of US and Japanese businesses produced FRAM in large quantities with memory densities ranging from 16 to 256 Kb [5, 6, 8]. FRAMs with capacities up to 8 Mb and several varieties of integrated FRAMs have recently entered the market. This paper seeks to provide an overview of FRAM's development over time.

### 6.1.1 Basic Characteristics of Ferroelectric Capacitors

To better understand the parts that follow, the basic characteristics of ferroelectric capacitors are briefly discussed in this section. The unprompted polarization of ferroelectric materials can be reversed by using outside electric field. A polarization-electric field (P-E) hysteresis curve is produced when a ferroelectric capacitor is exposed to such an electric field (Figure 6.1). The value of the electric field as a result of which the ferroelectric capacitor's macroscopic polarization vanishes is known as a coercive field (Ec). Remaining polarization without an electric field is referred to as residual polarization (Pr), where "±" denotes the polarization's direction. When reading data from a FRAM, the voltage produced by polarization-reversal current is measured.

Spontaneous polarization in a ferroelectric crystal results from the relative displacement of cations and anions. Both of these places in a unit cell are not charge-centered, therefore an electric dipole is created on its own. Figure 6.3 depicts schematically the connection between energy potential and ion displacement. By using an external electric field, the $Ti^{4+}$ or $Zr^{4+}$ ions may be shifted between the two stable locations, each of

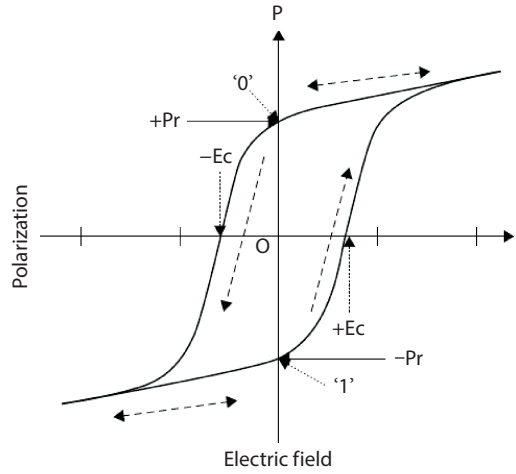


**Figure 6.1** Polarization-electric field hysteresis curve [7].

which they occupy. Figure 6.2 shows Schematic PZT crystal structure. A bistable condition combines into a single steady state when the temperature rises. The Curie temperature is referred to as this crucial temperature (Tc). PZT's crystal structure is tetragonal below Tc, here the lengths of all the a-axis, b-axis, and c-axis are approximately identical. However, beyond Tc, the structure changes to cubic (phase change). Specifically, Figure 6.3 illustrates the energy potential for the $2^{nd}$ order phase transition, here free energy varies continuously with temperature.

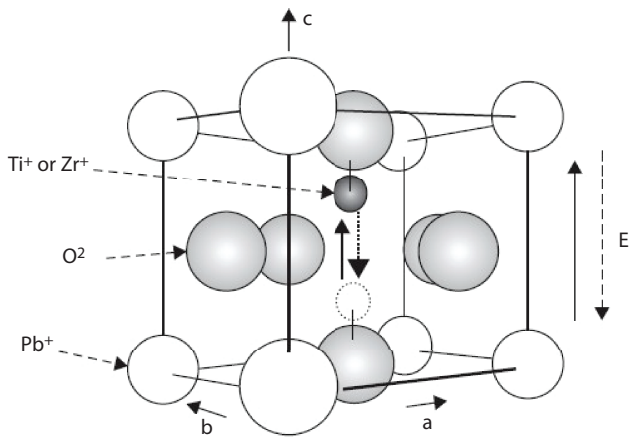


**Figure 6.2** Schematic PZT crystal structure [9].

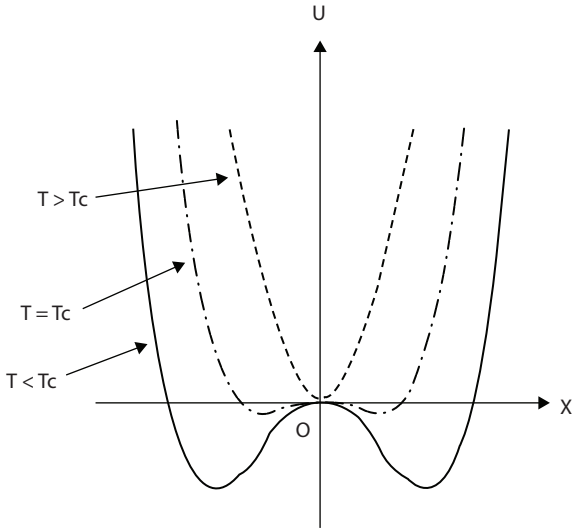


**Figure 6.3** The relationship between ion displacement (X) and energy potential (U) for a 2nd order phase transition [10].

There is a first-order phase transition as well, in which the free energy varies abruptly with temperature [9]. The dependency of temperature on polarization is expressed as

$$\left(\sqrt{1-T_c}\right)(0) = P(T) \to 1 \tag{6.1}$$

Where P (0) is polarization at zero Kelvin and T is temperature [59–63]. The ions are located on the same side of the double-well when seen microscopically, in a small area of hundreds of nm (Figure 6.3). It is often smaller than a ferroelectric polycrystalline grain and is referred to as a domain.

One of the things that worry FRAM developers the most is polarizing switching speed. Ishibashi has conducted theoretical research [10]. As seen in Figure 6.4, switching time is often made up of a nucleation time, domain growth time, and propagation time [9]. The nucleation time is the amount of time required to start the polarization reversal point; relatively small nucleation domains evaporate during this period. The switching time of a PZT capacitor is noticed to be between a few ns and some tens of ns in experimental studies [11, 12].

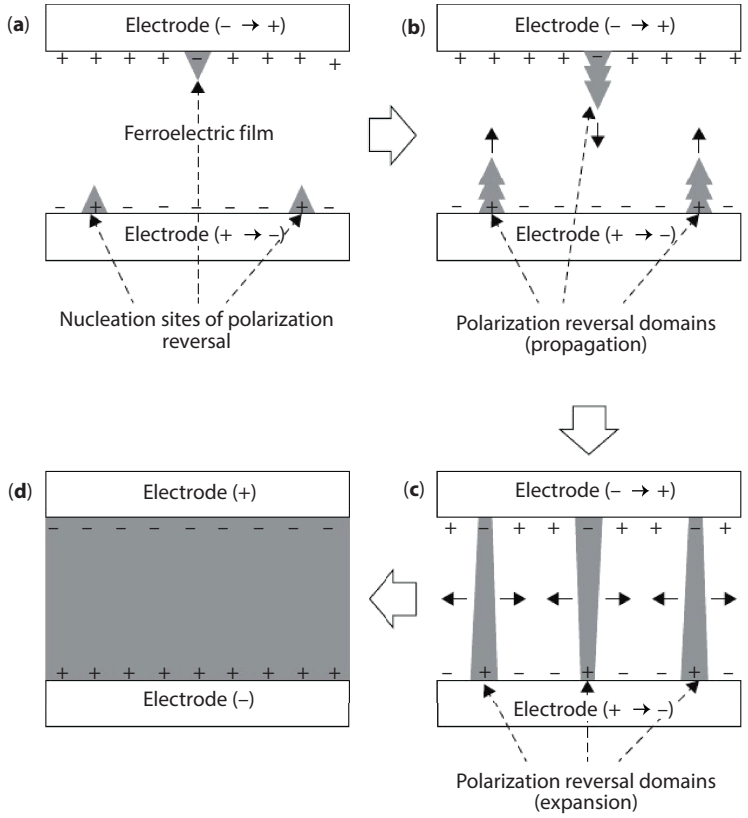


**Figure 6.4** Switching model of polarization [11].

### 6.1.2 FRAM Fabrication Process

Ferroelectric capacitor and traditional CMOS manufacturing techniques were used to create commercial Si-base FRAM. A ferroelectric capacitor fabrication procedure is typically implanted in the middle of a metallization procedure (back end of line: BEOL) and a transistor fabrication procedure (front end of line: FEOL). Because logic transistors may be used in FRAM memory cells "as is", the FRAM method is easier than the Flash memory technique, which requires a separate high voltage transistor manufacturing step. This is beneficial for making FRAM integrated logic devices in particular. For the same reason, noble metals like Ir, Pt, and $IrO_2$ are typically used as capacitor electrodes (and also these metals have high work functions). Perovskite-base electrodes that can withstand high temperatures have also been suggested [19].

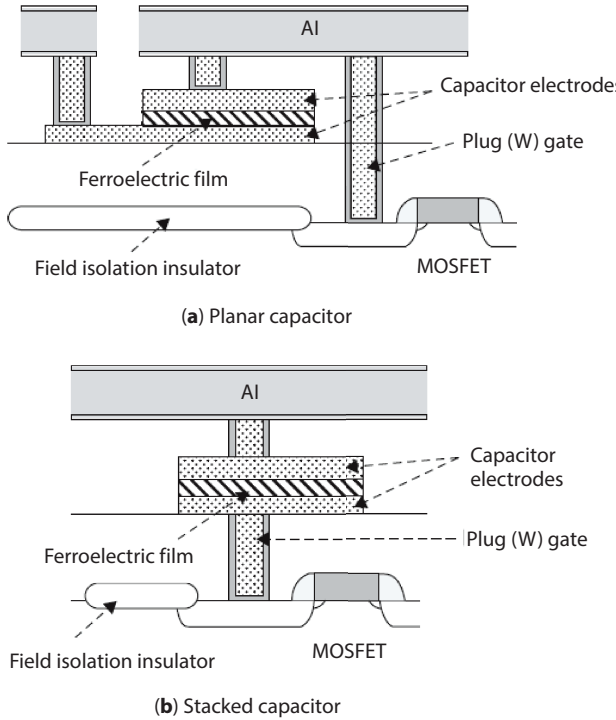


**Figure 6.5** Capacitor fabrication structure [26].

Ferroelectric capacitor structures come in two varieties as shown in Figure 6.5. After planarizing a dielectric layer over a MOSFET, a ferroelectric capacitor is positioned above field insulator layers [8, 14]. After the dielectric interlayer is deposited over the capacitor, electrical connections are created between the MOSFETs and the capacitor electrodes. Despite the unit memory cell area being greater, this procedure is easier than the stacked capacitor approach [20–23].

The electrode in the bottom of a ferroelectric capacitor is positioned straight onto the contact metal (W) linking a MOSFET when using stacked capacitors. An extremely fine electrode structure in the bottom and/or materials must be employed in the high temperature ferroelectric procedure to stop the contact metal from oxidizing. For a bottom electrode, oxygen barrier metals like TiN, Ir, IrO2, and/or their compounds are often utilized. Although the manufacturing technique and materials used are a

little more complex compared to a traditional planar CMOS approach, the stacked capacitor offers the benefit of a compact memory cell area.

Physical vapor deposition (PVD), which mostly uses MOCVD (metal organic chemical vapor deposition) [24, 25], sputter deposition [8], or CSV (chemical solution deposition), which primarily uses spin coating [5], were used to generate ferroelectric films. PVD is often used to deposit electrodes. Because of their cheap source costs and high throughput, PVD and CSD have lower deposition costs than MOCVD, but the MOCVD process offers the benefit of perfect source material controllability.

Due to the non-reactivity of noble metals, which are utilized for both the top and bottom electrodes of the ferroelectric capacitor, and the extremely low vapor pressure of ferroelectric byproducts, traditional RIE (reactive ion etching) cannot be used. Therefore, argon-mixed etching gases are used to physically enhance RIE.

## 6.2 Structure of Ferroelectric Memory Cells in Capacitor-Type FRAM Devices

### 6.2.1 A Capacitor-Type FRAM with a Memory Cell Resembling DRAM

A ferroelectric capacitor and a memory circuit resembling a DRAM circuit are included in this kind of FRAM [3, 4]. In comparison to FRAM, which uses the read/write operation voltage to apply a plate line, DRAM typically has a growth and cell structure with a voltage set at half of the provided voltage. There are two different types of memory circuits: The 1T1C, which consists of a single transistor, and the 2T2C, which consists of two transistors and two capacitors.

As a result of its two complementary memory units, 2T2C FRAM is extremely dependable despite having a larger memory area than 1T1C memory circuit, which is appropriate for high memory densities due to its tiny memory size.

Several electronics firms offered high density (≥1 Mb) FRAMs utilizing 1T1C stacked capacitors in the late 1990s and into the 2000s [15–18]. FRAMs of up to 8 Mb are currently available in the market. Figure 6.6 presents FRAM in the capacitor-type with a memory architecture similar to DRAM.

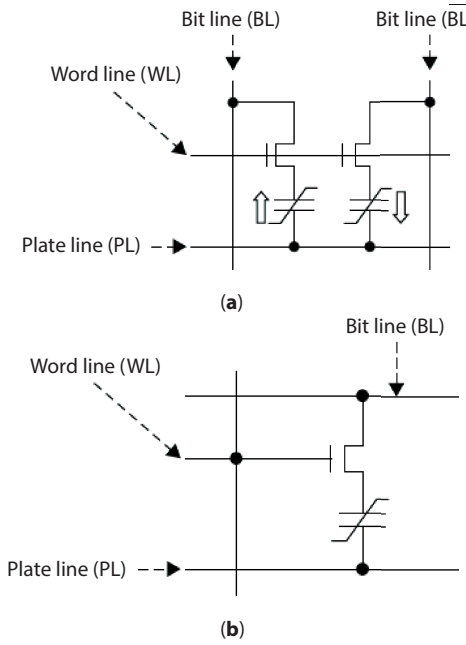


**Figure 6.6** FRAM in the capacitor-type with a memory architecture similar to DRAM: (a) a 2T2C; and (b) a 1T1C [27].

## 6.3 Write/Read Operations in the FRAM Using a Capacitor-Type Memory Cell that Resembles a DRAM

It provides a brief explanation of the fundamental write/read process of a FRAM using a capacitor- type memory cell that resembles DRAM (Figure 6.7). The bit line is initially assigned to "0" or "1" in a write operation. A voltage pulse is then supplied to the plate line once the selection transistor has been turned on. When the PL is at the maximal level (Figure 6.7(a)), data "0" is stored on the capacitor; when the PL is at the minimal level (Figure 6.7(b)), data "1" is stored. This process enables the capacitor to receive the entire supply voltage in both directions while sufficiently altering the polarization. The BL is first charged at 0 V and then set to floating during a read operation. The BL voltage rises as a result of charge flowing from the cell capacitor to the BL after the selection transistor is turned on and the PL is driven to the high level [39–40].

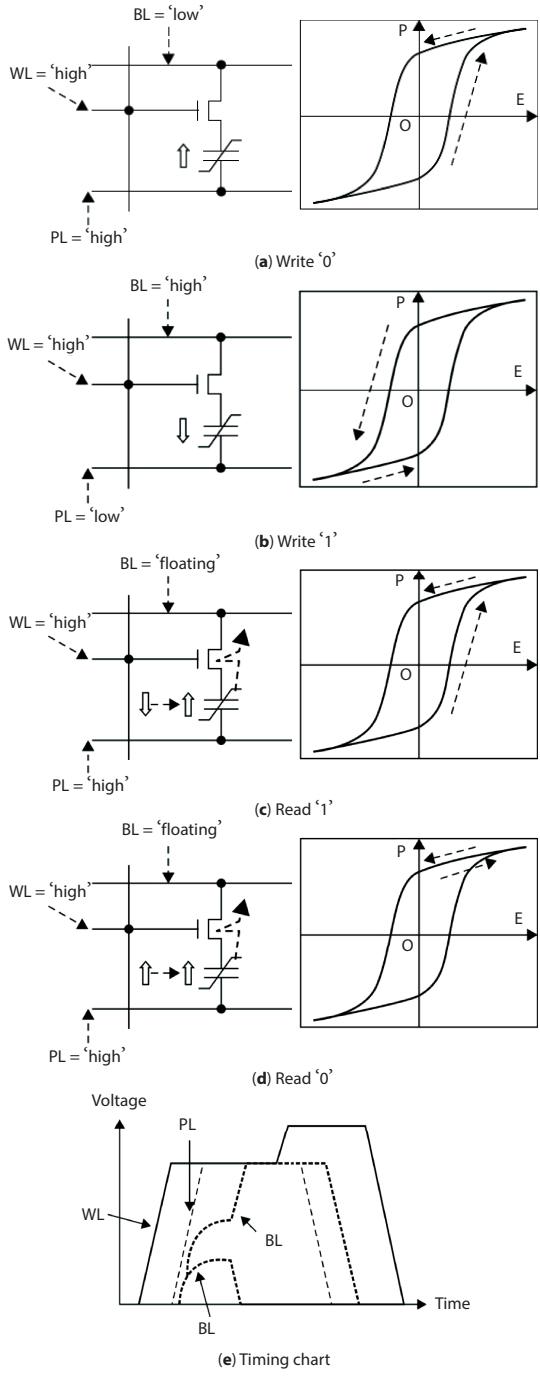


**Figure 6.7** Read/write operation of FRAM and timing chart [28].

When reading "1" polarization reversal charges flow to the BL (Figure 6.7(c)), but when reading "0" linear charges flow to the BL (Figure 6.7(d)). Because the polarization reversal charge is greater than the linear charge, the rise in the BL voltage from detecting "1" is often more than that from detecting "0". As it requires polarization reversal to read data, the read operation described above for FRAM is frequently referred to as "a destructive read" [60–63].

When using a 2T2C-type amplifier, FRAM compares the levels of the capacitors to determine whether it is "0" or "1" however when using a 1T1C-type amplifier, FRAM compares the bit line voltage to the reference voltage to identify the state. The ferroelectric capacitor's state determines the amount of polarization reversal charge, which might decrease if the capacitor is damaged by imprint, depolarization, fatigue, as described further. As a result, the 1T1C FRAM's sensing margin is highly dependent on the reference voltage.

Consequently, 1T1C FRAM is less durable than 2T2C FRAM. The term "High-Z", which refers to a high impedance, is used to describe this reading procedure. In this design, the externally provided voltage Vdd is applied to every cell capacitor as the floating bit line reduces the applied voltage by [Cb/(Cb+Cs)], where Cb and Cs are the BL's and the capacitor's respective capacitances. Kawashima *et al.* have presented the bit line ground sensing (BGS) method to increase the detecting percentage in the higher densities FRAMs [28].

Since the plate line is high in the p-MOS charge transfer's sensing method and the BL state is closer to ground, almost the whole external voltage may be applied to each cell capacitor, leading to a noticeably larger sensing margin.

The design of the FRAM depends on accurate polarization switching behavior prediction. However, because of the complicated hysteretic behavior, there are no suitable simulation models. The hysteresis loop is dependent on the rate of voltage variation because the applied voltage has a substantial impact on the polarization switching speed.

In generally presented models, the coercive voltage (the voltage that corresponds to the coercive field- is considered as a fixed value), while it really fluctuates depending on the conditions. A circuit simulation model that replicates the behavior of polarization switching under any voltage settings has been suggested [29–35]. A collection of capacitor elements with leftover polarization and a (fixed) coercive voltage make up the parallel element concept. By providing each component a voltage dependent switching period, the model accurately captures the nonlinear characteristics of the capacitor across a wide voltage range. This model depicts the ferroelectric capacitor's impaired states, which makes it a useful tool for creating FRAM circuits that are resistant to ferroelectric deterioration [64–68].

## 6.4 Other Capacitor-Type FRAM

Two ferroelectric capacitors and six transistors make up the "non-volatile SRAM" (6T2C) that Dimmer and Eaton proposed [30]. When an external power supply is present, it functions as normal SRAM (non-destructive read), but when it is not, it stores data on the ferroelectric capacitors. As a result, this kind of FRAM has the capacity to read and write data at high speeds that are nearly as fast as those of traditional SRAM. Using a non-volatile SRAM having just a 6T4C structure, Masui *et al.* enhanced the "recall operation" of 4T2C FRAM [31]. They suggested using their 6T4C non-volatile SRAM having a 4 nanoseconds data speed in a highly efficient dynamically programmed gate array. Non-volatile logic has been proposed to minimize power consumption by distributing storage components over the logic-circuit plane. Distributed system components' standby signals can be controlled with the help of ferroelectric-based non-volatile storage components [32].

A "chain FRAM" that consists of the parallel connection of one ferroelectric capacitor and one transistor was presented as a way to minimize the size of memory cells. A block-selecting transistor and several memory cells linked in series make up a memory cell block. According to sources, a chain FRAM design may attain a unit cell coverage of $4F^2$ [33].

## 6.5 FRAM of FET Type

A ferroelectric insulating film is placed to the FET's gate in a single transistor type FRAM (Figure 6.8). Since the polarization pattern of the ferroelectric film affects the transistor threshold voltage data is recorded in the gate ferromagnetic film and taken out as transistors drain current. It is fortunate because this kind of FRAM supports non-destructive read operations and is totally scalable with transistor design. A thin layer of triglycine sulphate was placed among a liquid crystal transistor and a gold base electrode to form a "solid state variable resistor," as Moll and Tarui termed it in 1963 [35].

Wu developed a FET-type FRAM using Bi4Ti3O12 in 1974 using a metal-ferroelectric-Si surface gate arrangement. Metallic Electric-semiconductor refers to this gate structure [13]. When fabricating transistors, ferroelectric material and silicon undergo a chemical reaction that alters the transistor's properties in MFS structure [38–41].

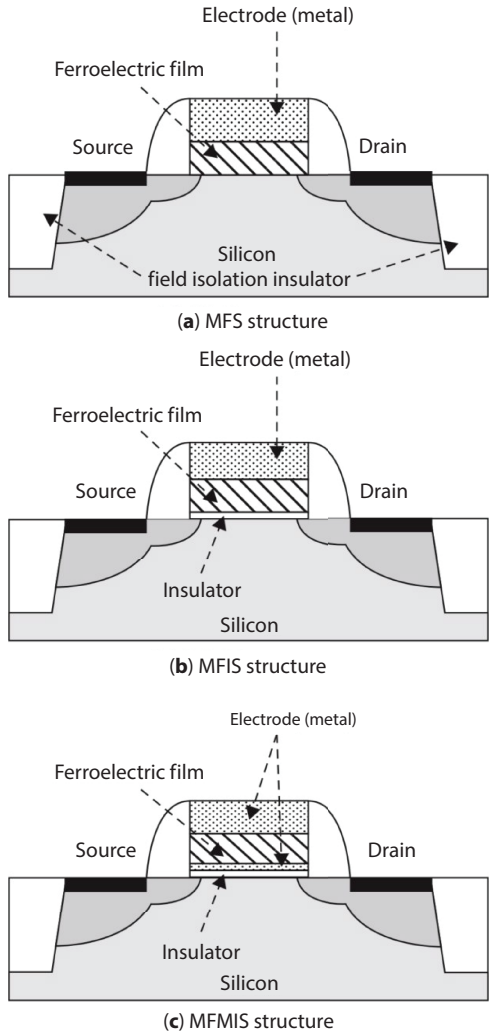


**Figure 6.8** FRAM of FET-type [34].

MFMIS substrates and MFIS substrates were suggested as solutions to this deterioration [36–38]. Though several testing have been carried out, these FRAMs have a limited capacity for data retention. The use of an MFIS gate structure, according to Takahashi *et al.*'s (2005) research, resulted in a significant improvement in data store retention lasting up to 30 days [42]. In order to adapt FET-type FRAM to NAND FLASH circuits,

Sakai proposed the usage of MFIS-type ferromagnetic in 2008. This might result in a reduction in the wipe away voltage compared to conventional Flash memory [43].

## 6.6 Memory Utilizing a Ferroelectric Tunnel Junction

Memory utilizing a Ferroelectric tunnel junction is a sandwich of two metals with a several nanometer thick ferroelectric coating. The value of current all over a semiconducting sheet is severely impacted by the propagation direction. Non-destructive reading is anticipated to be possible with this memory. Esaki *et al.* first suggested tunnel connections using a ferroelectric barrier in 1971 [44]. After the FTJ ($Pt/PbZr_{0.52}Ti_{0.48}O_3$ or $BaTiO_3/SrRuO_3$) was reported to operate at room temperature in 2002, in numerous reported tests, a high ON/OFF rate and low power usage were sought after [42]. Regarding this type of memory, the consistent and efficient control of nanometer-thick ferroelectric materials continues to be challenged [45, 46].

### 6.6.1 Previous Ferroelectric Memory Designs

Initial ferroelectric memory designs comprised not just the 2T2C cell mentioned, that is the type of dominant ferroelectric memory in use nowadays, but also prior less reliable cells like the cross-point matrix array, that experienced losing of data due to the half select impact. This also comprised multiple kinds of shadow RAMs that took on with the market's existing battery backup SRAM devices. Ferroelectric Shadow RAMs also became available in logic circuits as macros [69–73].

## 6.7 Cross Point Matrix Array

Previous research on ferroelectric memory employed a basic cross point matrix array structure, as seen in Figure 6.9 [47].

The half-select effect harmed these basic arrays. The voltage was applied to all of the cells across the chosen column and chosen row, although only chosen cell observed the voltage supplied to each of rows and columns. As a result of losing information caused by half select signals given to not chosen cells, the amount of read and write cycles was dramatically decreased compared to what might be predicted for just one cell of a ferroelectric array.

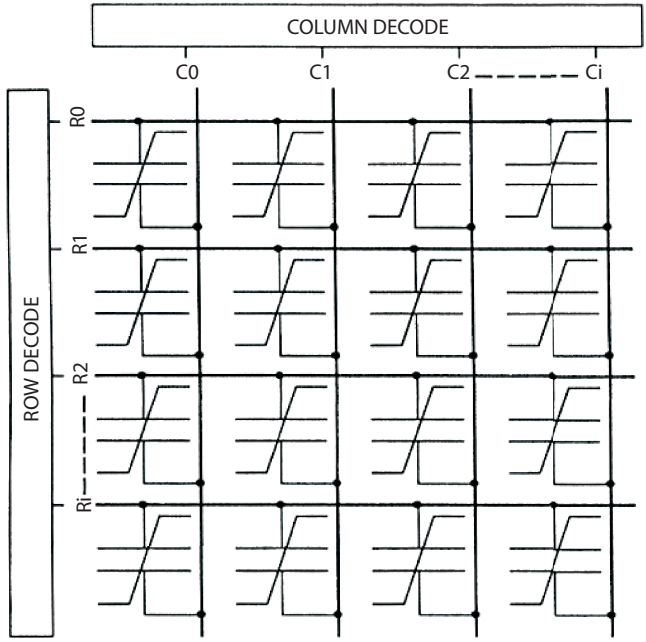


**Figure 6.9** Basic cross point matrix array [47].

Previous ferroelectric memories were additionally affected with extreme endurance, impacts at 2windividual unit range, that were eventually mitigated by advancements in ferroelectric substance characteristics.

## 6.8 Ferroelectric Shadow RAMs

Ramtron demonstrated a shadow RAM that connected a transistor to a ferroelectric capacitor in series to separate it from the bit line [47]. This separation helps to keep disrupt pulses away from the not chosen ferroelectric capacitors. As illustrated in Figure 6.10 [47], the capacitors which were linked to the SRAM cell's storage node.

They presented the notion of a cycled a shared plate link for a ferroelectric memory cell with two capacitors in the same research. Because this is a shadow RAM, the ferroelectric standby capacitors are configured only on power up and power down, bypassing the fatigue constraints associated with SRAM cells [74–80].

By powering down the circuit, the transistors which are in series are switched on along with the shared plate kept at "0," causing the ferroelectric

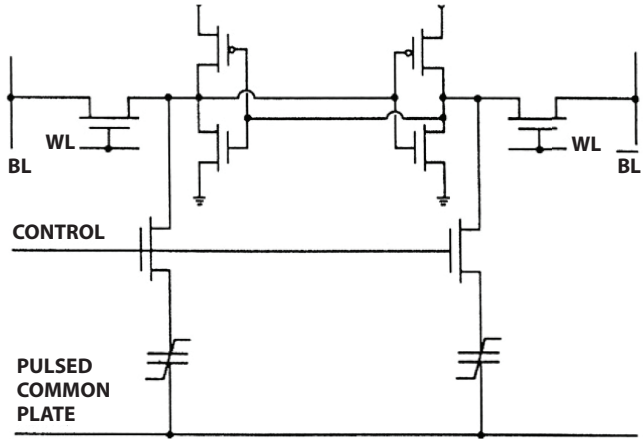


**Figure 6.10** Shadow RAM using a cycled shared plate link and a separating transistor connected in series to a ferroelectric capacitor [47].

capacitor at the highest node to be configured high. The shared plate is subsequently driven to Vdd, causing the ferroelectric capacitor at the lowest node to be configured low while the second capacitor remains unaffected. The data of SRAM latch is now encoded into both of the capacitors. When both capacitors are powered up, the shared plate is pulsating from 0 to Vdd, with the bit lines equalized to ground. This switches one ferroelectric capacitor while not another, resulting in a bit line imbalance that can be detected and encoded into the Static RAM [48].

Whereas one of the main benefits of the shadow RAM idea is the fact that ferroelectric fatigue disadvantages are prevented because the capacitors are configured only on power up and power down, among its disadvantages the area cost of the ten devices employed in the cell (8 transistors and 2 capacitors).

To conserve space on some of such transistors, NEC proposed a shadow RAM macro in 2000 that deleted the series transistors from the ferroelectric capacitors [49, 50].

As a result, every ferroelectric capacitor is directly coupled to an Static RAM cell storage node. The plate connections were tuned to Vdd/2 to ensure only a slight voltage imbalance through the capacitors, also the ferroelectric capacitors' coercive voltage was set to larger than Vdd/2. The goal was to prevent polarization changes also thereby fatigue. Another feature of this cell was its quick operation and lack of demand for enhancing circuits [81–83].

## 6.9 2T2C Ferroelectric RAM Architecture

Krysalis, an early pioneer in this field, demonstrated the 2T2C FRAM design in practically its present configuration for the first time in 1988 [51]. Figure 6.11 [51] depicts an illustrated block diagram of this component.

A dual ended sensory method and a self referencing differentiated signal are used in the portion. The two accessing transistors are controlled by the shared word-line. Two capacitor plates are controlled by the same driving line. In fundamental functionality, this 2T2C capacitor is practically unaltered today.

Figure 6.12 depicts a design of the standard 2T2C data route as it is used nowadays.

The sensing amplifier is adjusted to the required condition before writing. After activating the word line, the plate line is made high. The capacitor of the sense amplifier's grounded side is polarized to the Q(0) state. When the drive line is grounded, the capacitor of the sense amplifier's high side is polarized to the Q(1) state.

For reading the cell, the bit lines have been precharged to ground and floated, the sensing amplifier is turned off, and the plate line is connected to a voltage high. Whenever the word line is triggered, just a single capacitor switches polarization, resulting in a differential charge flowing on the bit

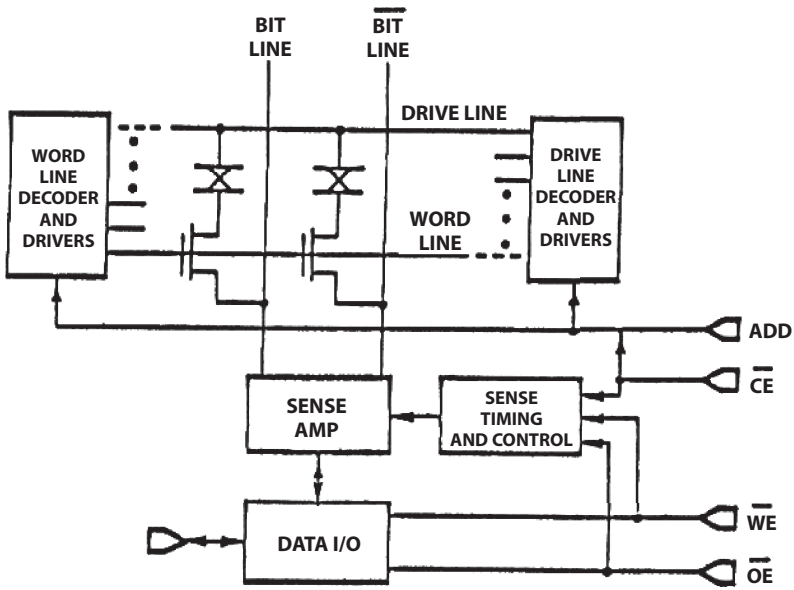


**Figure 6.11** Previous 2T2C Ferroelectric RAM Architecture [51].

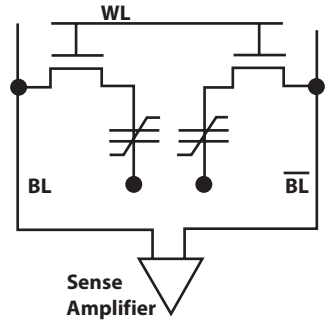


**Figure 6.12** Circuit illustration of 2T2C Ferroelectric RAM cell architecture [52].

line and bit line bar. When the sensing amplifier is turned on, the higher bit line voltage is generated by the switched capacitor, while the other side is driven low. If the plate line becomes low, the switched capacitor is reset and the initial information will return to the cell. This restoration is performed as part of the writing procedure and is not visible to the user [84–88].

Krysalis demonstrated a more detailed architectural picture of the data path of the 2T2C ferroelectric memory in 1989 [53]. This 16K-bit component was constructed in n-well CMOS which has a chip enable access period of 200 ns. As illustrated in Figure 6.13, it had a capacitor plate line that ran parallel to the bit lines and linked all bits in a single column. The operation is substantially the same as in the previous section.

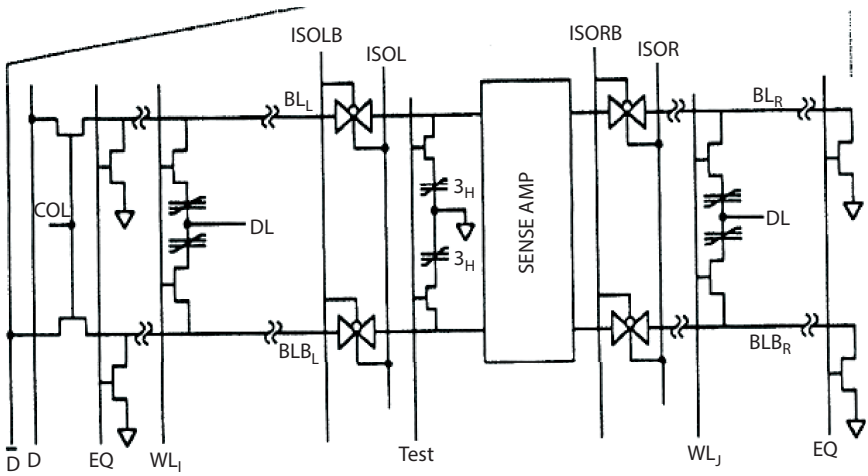


**Figure 6.13** A 16K-bit ferroelectric RAM data path circuit diagram [53].

In the dual ended sensing technique, the two 1T1C cell components which were employed as a 2T2C cell to provide a differential signal between the bit line bar and the bit line which is self-referencing. Since the capacitor plate line was shared by the whole column, neglected column bits received the plate signal at the time of read and write operations. It had no effect on the capacitors within the "0" state, but it did affect the capacitors within the "1" state's residual polarization. This component included a voltage sensor circuit that detected when the 5V Vdd dipped below 3.6V.

NEC provided another instance of a FeRAM device of 2T2C in 1998. They demonstrated a synchronized FeRAM macro designed for use in the microcontroller to substitute the EEPROM previously utilized in this application. Figure 6.14 [54] depicts the corresponding synchronous timing diagrams associated with this macro.

These time graphs show how the timings of write and read operations of FeRAM are comparable since both include switching the ferroelectric capacitor to determine its polarization direction [54].

The benefits of this synchronized FRAM were its rapid write and read speeds, as well as the power savings from not having to incorporate the high voltage on chip voltage generators necessary on the EEPROM for write and erase onto the microcontroller chip [89–94].

Because the time for read and write operations is identical, a FeRAM macro that functions entirely synchronous with the on chip CPU core was developed. In this circuit, operation is therefore similar to that of an SRAM. An FeRAM macro of this type might be employed to substitute each the

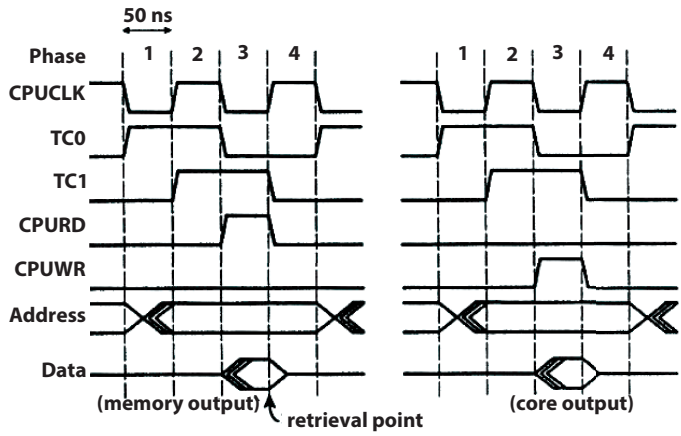


**Figure 6.14** Timing diagrams of read and write operations in a synchronous FeRAM [54].

EEPROM and the Static RAM built inside this microcontroller. As such, it is the predecessor of today's embedded FeRAM-based microcontrollers.

### 6.9.1 Evaluation of FRAM Devices' Reliability

Depolarization, imprint, and fatigue are the three main types of electrical deterioration processes of ferroelectric capacitors. These degradations are seen as a deviation from P-E hysteresis (Figure 6.15). As Pr drops from the starting value (Figure 6.15(a)), depolarization is shown. As hysteresis moves away from its starting point, imprint is seen (Figure 6.15(b)). After storing the "1" state, P-E hysteresis, for instance, switches to the + direction. In Figure 6.15(c), fatigue is shown as the hysteresis decreases from its initial value. The main reason for these degradations has been the subject of several studies. It is thought that certain kinds of deterioration are induced by charged defects, such as oxygen vacancies or their associated flaws [9, 55, 56].

An appropriate testing method is essential for assessing the aforementioned deterioration of ferroelectric capacitors in highly dependable mass manufacturing of FRAM. With the use of a retention test in Figure 6.16(a), which comprises writing, saving, and reading stored data, the ferroelectric capacitor's ability to preserve the original recorded data is evaluated. If the ferroelectric capacitor is destroyed by depolarization, the data accessing procedure in this experiment could not be successful.

An imprint test, illustrated in Figure 6.16(b), examines whether a ferroelectric capacitor can overwrite the data stored as the opposite data by recording and storing 1 and then overwriting the recorded 1 as 0.

The steps in this test are to write data, save it first, edit the opposing data, and then get the modified data. In this test, it's possible that the reading procedure with the altered data will fail if the ferroelectric capacitor's hysteresis shifts Figure 6.16(b), since doing the reverse is now more challenging due to a rise in Ec. An examination of the ferroelectric capacitor's read/write performance is done after several 0–1 switches using a switching/fatigue retention test Figure 6.16(c). Commonly produced FRAMs have switching capabilities more than $10^{13}$, or $10^{7}$ times that of Flash memory.

### 6.9.2 Comparative Analysis of FeRAM to Other Memory Technologies

Ramtron's FeRAM now falls into two separate groups: serial FeRAM and parallel FeRAM. Serial FeRAM is separated into two series: I2C 2-line

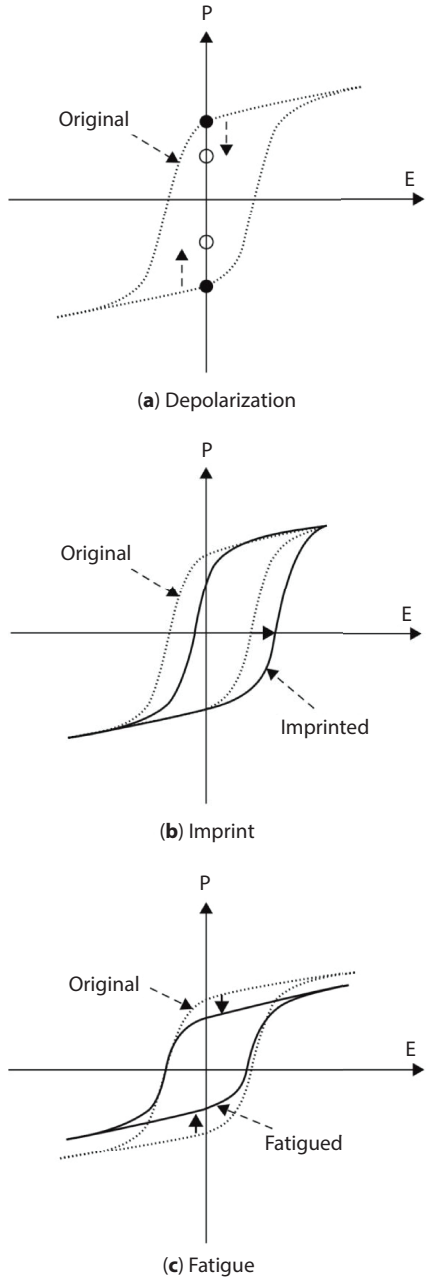


**Figure 6.15** Deterioration of the ferroelectric capacitance [55].

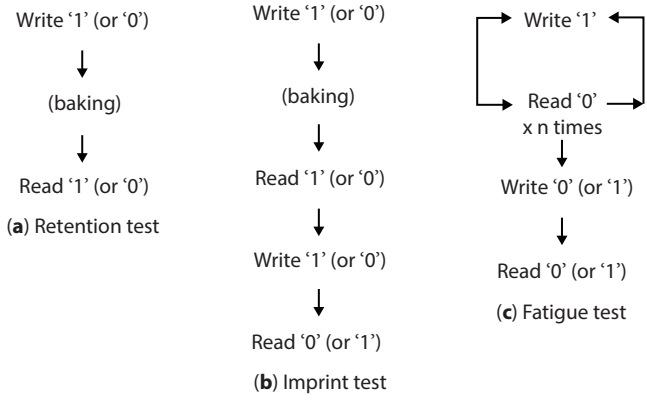


**Figure 6.16** Testing procedures of FRAM [56].

FM24 series and SPI 3-line FM25 series. Serial FeRAM pins and timing are interchangeable with the standard 24xx and 25xx EEPROM pins and timing.

FeRAM devices offer the benefits of RAM and ROM, as well as high read and write speeds; they may also be utilized as non-volatile memory. Because of the limitations of ferroelectric particles, the number of accesses is restricted, after which FeRAM becomes volatile. The maximum access duration specified is 10 billion, although this does not indicate that FeRAM will be terminated if it exceeds this limit. FeRAM isn't non-volatile in this sense, but it may still be utilized as regular RAM [116–117].

## 6.10 FeRAM vs. EEPROM

As an alternative to EEPROM, FeRAM can be employed. FeRAM access speed is considerably quicker than EEPROM performance. When employing FeRAM, it has to be verified that there is no damage once 10 billion accesses are down to FeRAM in the system [95–98].

## 6.11 FeRAM vs. Static RAM

Static RAM outperforms FeRAM in terms of speed, cost, and accessibility; yet, FeRAM has certain benefits in terms of overall design.

Non-volatile FeRAM may store starting programs as well as configuration data. If all of the memory in the application have a maximum access time of 70ns, one piece of FeRAM can be employed to finish the system, simplifying the system layout.

## 6.12 FeRAM vs. Dynamic RAM

Dynamic RAM is appropriate for situations in where density and cost are more essential than the speed of access. Dynamic RAM, for example, is the greatest option for graphics display memory. The amount of pixels to be saved is high, and the recovery time is not critical. Use volatile Dynamic RAM memory if you don't need to store previous data at the following boot. When compared to FeRAM, the use and price of Dynamic RAM are appropriate. To summarize, Dynamic RAM can't be completely replaced with FeRAM.

## 6.13 FeRAM vs. Flash Memory

Flash memory is currently the most often utilized program memory since it is more accessible and less expensive to use. The program memory has to be non-volatile and rewriteable, although the utilization of FRAM is constrained by time to access [57].

### 6.13.1 Uses of FRAM Devices

Commercialized FRAMs may be classified into two groups based on their use for memory: standalone FRAM and embedded FRAM. The latter are geared for specialized customers, whilst the former only test memory and are designed for general users [99–103].

Storage capacities for commonly available standalone FRAM varies from a several Kb to several Mb. FRAMs are frequently used to replace traditional EEPROMs in order to save energy and enhance read/write performance. For instance, electric power meters employ stand-alone FRAMs for their memory since they need to rewrite data several times per second. Due to a lack of rewriting capacity ($10^5$), EEPROM cannot be used for this application. FRAMs are frequently used in place of battery-backed SRAMs, which has several advantages because it is not only more affordable but also better for the environment than battery-backed memory. FRAMs are also

required for data monitoring, which is used to store technical information, in automation and automobiles because of their increased read/write and rewrite functionality [104–108].

FRAM-embedded LSIs come in a variety of forms, including sophisticated smart cards, RFID tags, and authentication LSIs. Greater communication distances between card/tag and reader/writer are possible in wireless applications due to decreased FRAM power consumption [109–115]. FRAM is also appropriate for smart card or RFID tag authentication since its fast read/write speeds allow for the adoption of powerful encryption methods. Compared to DRAM, EEPROM, and Flash memories, Gamma radiation is thought to be far less likely to damage FRAM. This is so that data is not stored in FRAM as electrostatic force, which gamma radiation has a significant negative influence on [58]. As a result, FRAM may be used for RFID tags linked to gamma-sterilized medical equipment [115–118].

## 6.14 Conclusion and Upcoming Trends

Although scaling is still one of its largest challenges, FRAM is the first high-end non-volatile memory to be commercially available, ahead of MRAM, PRAM, and ReRAM. As of 2021, depending on the manufacturer and application, ferroelectric RAM (FeRAM) technology is being employed at a variety of technology nodes ranging from 130 to 40 nm.

For example, Cypress Semiconductor manufactures FeRAM products using the 130 nm technology node, whereas Rohm Semiconductor manufactures FeRAM products using the 180 nm technology node. Moreover, Toshiba Memory and Fujitsu Semiconductor have been working on FeRAM products using the 40 nanometer technology node. Nonetheless, 40 nm FeRAM technology, in general, has significant advantages over previous nodes, including increased density, reduced power consumption, and quicker access times. Toshiba Memory's 40 nanometer FeRAM technology has the following specifications: 4 MB capacity (megabits), 1.8 V is the operating voltage, access time is 30 nanoseconds, $10^{12}$ cycles of read/write endurance, temperature range of operation is -40°C to +85°C. This progress is somewhat gloomy. FRAM has the ability to encounter its technical challenges and surpass these technologies, though, due to the recent major advances in ferroelectric developments taking place of FET-type FRAM components, as outlined above, and with just a moderate advancement in comparison to other enhanced semiconductor materials.

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