Inst	opcode	funct3	funct7	memWrite	rfWrite	aluSrcA	aluSrcB	pcSrc	rfWriteData	ALU Operation	aluOp	memOp	pcWrite	bInst	ebreak	ecall	mret	csrImmInst	csrInstType	csrWrite
LUI	0110111	xxx	x	0	1	x	1	0	0111	lui	1000	00	0	0	0	0	0	0	xx	0
AUIPC	0010111	xxx	x	0	1	0	1	0	0111	add	0000	00	0	0	0	0	0	0	xx	0
JAL	1101111	xxx	x	0	1	0	1	1	0000	add	0000	00	1	0	0	0	0	0	xx	0
JALR	1100111	000	x	0	1	1	1	1	0000	add	0000	00	1	0	0	0	0	0	xx	0
BEQ	1100011	000	x	0	0	1	0	0	xxxx	sub	0001	00	0	1	0	0	0	0	xx	0
BNE	1100011	001	x	0	0	1	0	0	xxxx	sub	0001	00	0	1	0	0	0	0	xx	0
BLT	1100011	100	x	0	0	1	0	0	xxxx	sub	0001	00	0	1	0	0	0	0	xx	0
BGE	1100011	101	x	0	0	1	0	0	xxxx	sub	0001	00	0	1	0	0	0	0	xx	0
BLTU	1100011	110	x	0	0	1	0	0	xxxx	sub	0001	00	0	1	0	0	0	0	xx	0
BGEU	1100011	111	x	0	0	1	0	0	xxxx	sub	0001	00	0	1	0	0	0	0	xx	0
LB	0000011	000	x	0	1	1	1	0	0100	add	0000	00	0	0	0	0	0	0	xx	0
LH	0000011	001	x	0	1	1	1	0	0010	add	0000	00	0	0	0	0	0	0	xx	0
LW	0000011	010	x	0	1	1	1	0	0001	add	0000	00	0	0	0	0	0	0	xx	0
LBU	0000011	100	x	0	1	1	1	0	0101	add	0000	00	0	0	0	0	0	0	xx	0
LHU	0000011	101	x	0	1	1	1	0	0011	add	0000	00	0	0	0	0	0	0	xx	0
SB	0100011	000	x	1	0	1	1	0	xxxx	add	0000	10	0	0	0	0	0	0	xx	0
SH	0100011	001	x	1	0	1	1	0	xxxx	add	0000	01	0	0	0	0	0	0	xx	0
SW	0100011	010	x	1	0	1	1	0	xxxx	add	0000	11	0	0	0	0	0	0	xx	0
ADDI	0010011	000	x	0	1	1	1	0	0111	add	0000	00	0	0	0	0	0	0	xx	0
SLTI	0010011	010	x	0	1	1	1	0	0110	sub	0001	00	0	0	0	0	0	0	xx	0
SLTIU	0010011	011	x	0	1	1	1	0	1000	sub	0001	00	0	0	0	0	0	0	xx	0
XORI	0010011	100	x	0	1	1	1	0	0111	xor	0100	00	0	0	0	0	0	0	xx	0
ORI	0010011	110	x	0	1	1	1	0	0111	or	0011	00	0	0	0	0	0	0	xx	0
ANDI	0010011	111	x	0	1	1	1	0	0111	and	0010	00	0	0	0	0	0	0	xx	0
SLLI	0010011	001	0	0	1	1	1	0	0111	shift left	0101	00	0	0	0	0	0	0	xx	0
SRLI	0010011	101	0	0	1	1	1	0	0111	shift right l	0110	00	0	0	0	0	0	0	xx	0
SRAI	0010011	101	1	0	1	1	1	0	0111	shift right a	0111	00	0	0	0	0	0	0	xx	0
ADD	0110011	000	0	0	1	1	0	0	0111	add	0000	00	0	0	0	0	0	0	xx	0
SUB	0110011	000	1	0	1	1	0	0	0111	sub	0001	00	0	0	0	0	0	0	xx	0
SLL	0110011	001	0	0	1	1	0	0	0111	shift left	0101	00	0	0	0	0	0	0	xx	0
SLT	0110011	010	0	0	1	1	0	0	0110	sub	0001	00	0	0	0	0	0	0	xx	0
SLTU	0110011	011	0	0	1	1	0	0	1000	sub	0001	00	0	0	0	0	0	0	xx	0
XOR	0110011	100	0	0	1	1	0	0	0111	xor	0100	00	0	0	0	0	0	0	xx	0
SRL	0110011	101	0	0	1	1	0	0	0111	shift right l	0110	00	0	0	0	0	0	0	xx	0
SRA	0110011	101	1	0	1	1	0	0	0111	shift right a	0111	00	0	0	0	0	0	0	xx	0
OR	0110011	110	0	0	1	1	0	0	0111	or	0011	00	0	0	0	0	0	0	xx	0
AND	0110011	111	0	0	1	1	0	0	0111	and	0010	00	0	0	0	0	0	0	xx	0
Ebreak	1110011	000	0	0	0	0	0	0	0000	add	0000	00	0	0	if f12 == 12'h001	if f12 == 12'h000	if f12 == 12'h302	0	xx	0
Ecall	1110011	000	0	0	0	0	0	0	0000	add	0000	00	0	0	if f12 == 12'h001	if f12 == 12'h000	if f12 == 12'h302	0	xx	0
CSRRWI	1110011	101	x	0	0	0	0	0	1001	add	0000	00	0	0	0	0	0	1	00	1
CSRRSI	1110011	110	x	0	0	0	0	0	1001	add	0000	00	0	0	0	0	0	1	01	1
CSRRCI	1110011	111	x	0	0	0	0	0	1001	add	0000	00	0	0	0	0	0	1	10	1
CSRRW	1110011	001	x	0	0	0	0	0	1001	add	0000	00	0	0	0	0	0	0	00	1
CSRRS	1110011	010	x	0	0	0	0	0	1001	add	0000	00	0	0	0	0	0	0	01	1
CSRRC	1110011	011	x	0	0	0	0	0	1001	add	0000	00	0	0	0	0	0	0	10	1

operation	code
add	0000
sub	0001
and	0010
or	0011
xor	0100
shift left	0101
shift right logical	0110
shift right arithmetic	0111
shift right arithmetic immediate	1001
lui	1000