



Verilog HDL Basics

Project: 2

SPI Slave with Single Port RAM

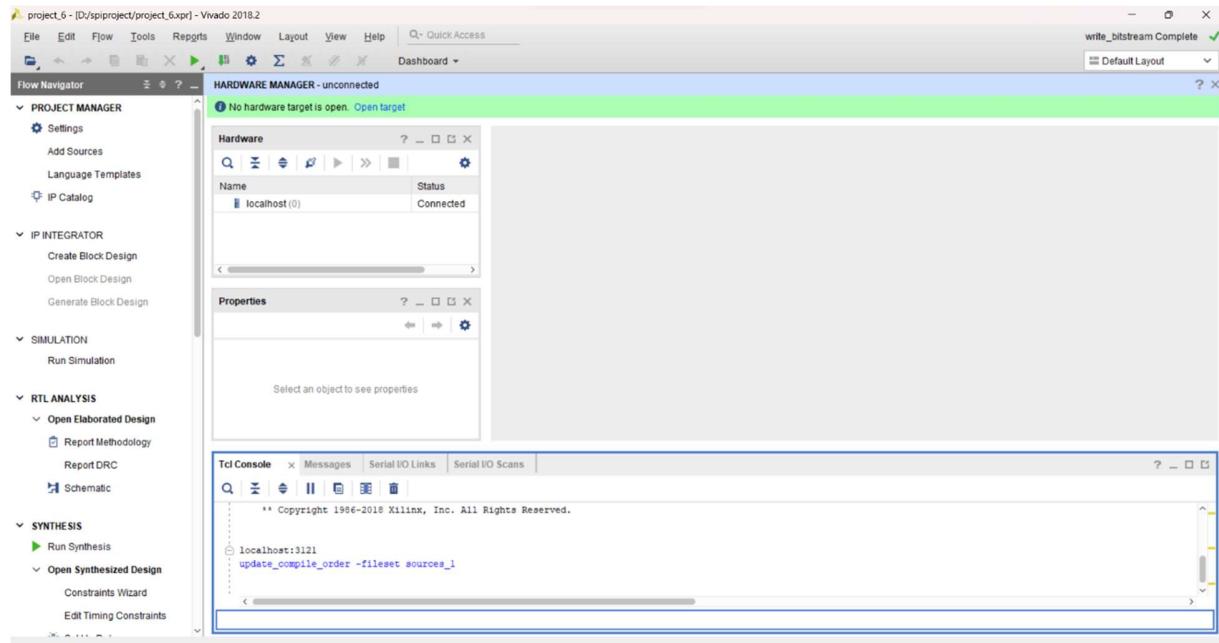
Submitted by
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Muhammed Aladdin Muhammed
Habib Hossam Eltabakh

To
Eng. Kareem Waseem

1) TCL File

```
create_project project_6 D:/spiproject -part xc7a35ticpg236-1L -force
add_files spi_slave.v ram.v wrapper.v spi_constraints.xdc
synth_design -rtl -top wrapper > elab.log
write_schematic elaborated_schematic.pdf -format pdf -force
launch_runs synth_1 > synth.log
wait_on_run synth_1
open_run synth_1
write_schematic synthesized_schematic.pdf -format pdf -force
write_verilog -force spi_netlist.v
launch_runs impl_1 -to_step write_bitstream
wait_on_run impl_1
open_run impl_1
open_hw
connect_hw_server
```

After running TCL file:



2) Constrains file:

```
## Clock signal
set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

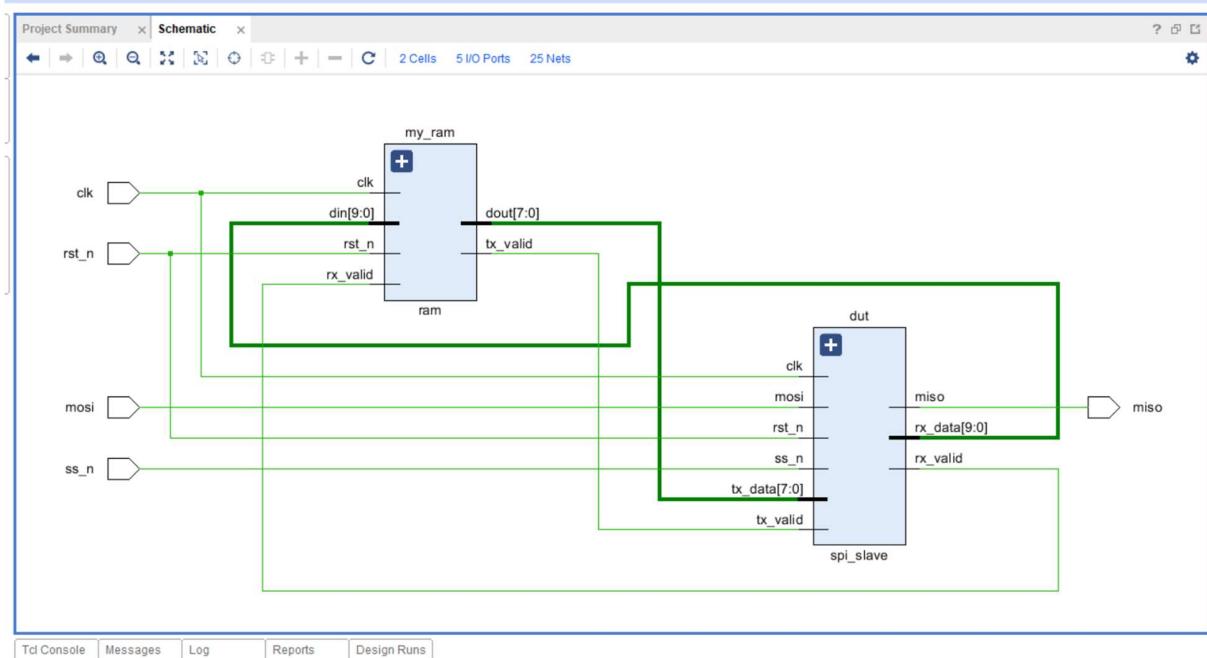
## Switches
set_property -dict { PACKAGE_PIN V17    IOSTANDARD LVCMOS33 } [get_ports {rst_n}]
set_property -dict { PACKAGE_PIN V16    IOSTANDARD LVCMOS33 } [get_ports {ss_n}]
set_property -dict { PACKAGE_PIN W16    IOSTANDARD LVCMOS33 } [get_ports {mosi}]

## LEDs
set_property -dict { PACKAGE_PIN U16    IOSTANDARD LVCMOS33 } [get_ports {miso}]

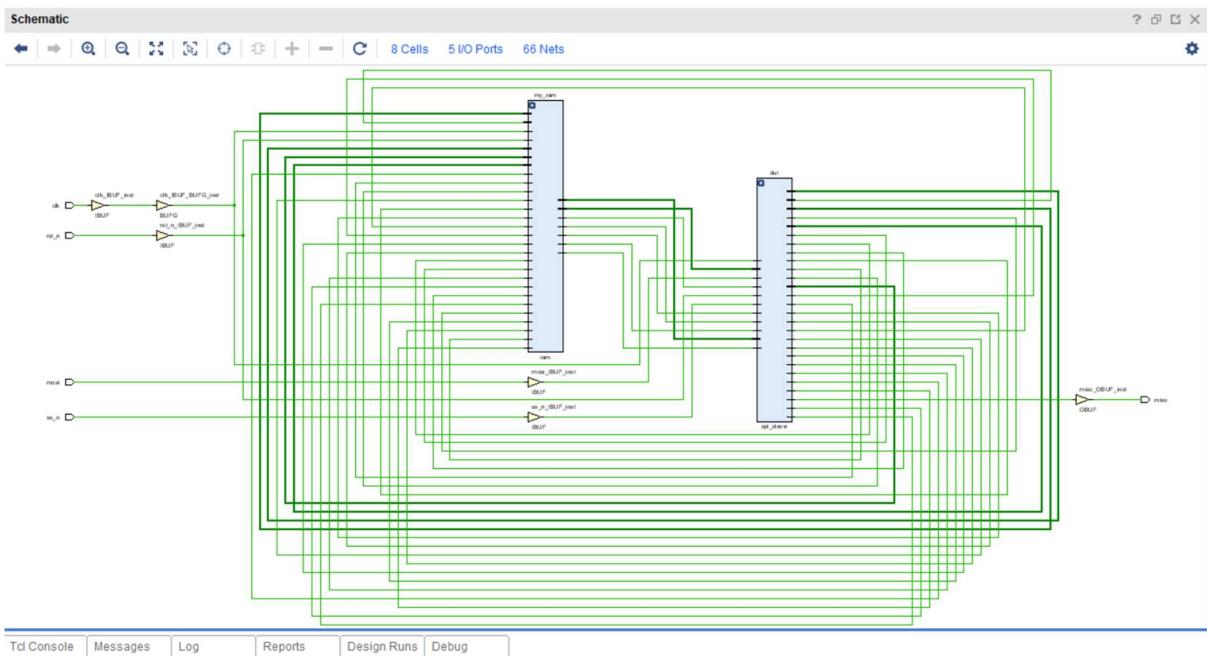
## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

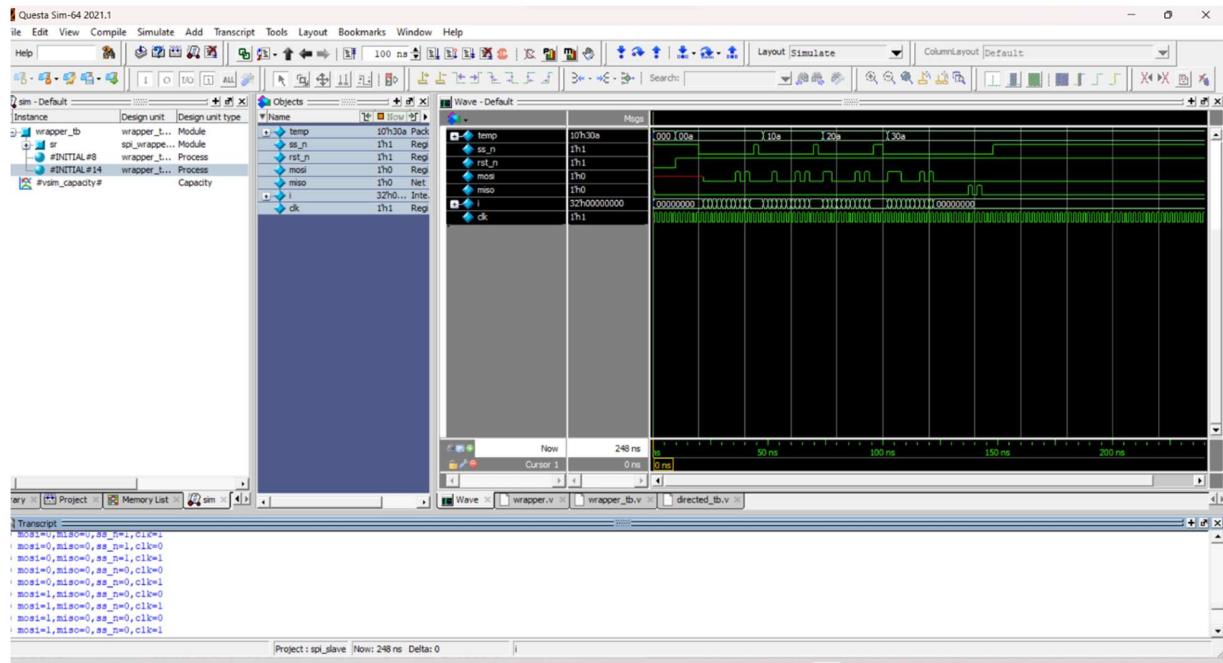
3) Spi wrapper after elaboration:



4) Spi wrapper after synthesis:

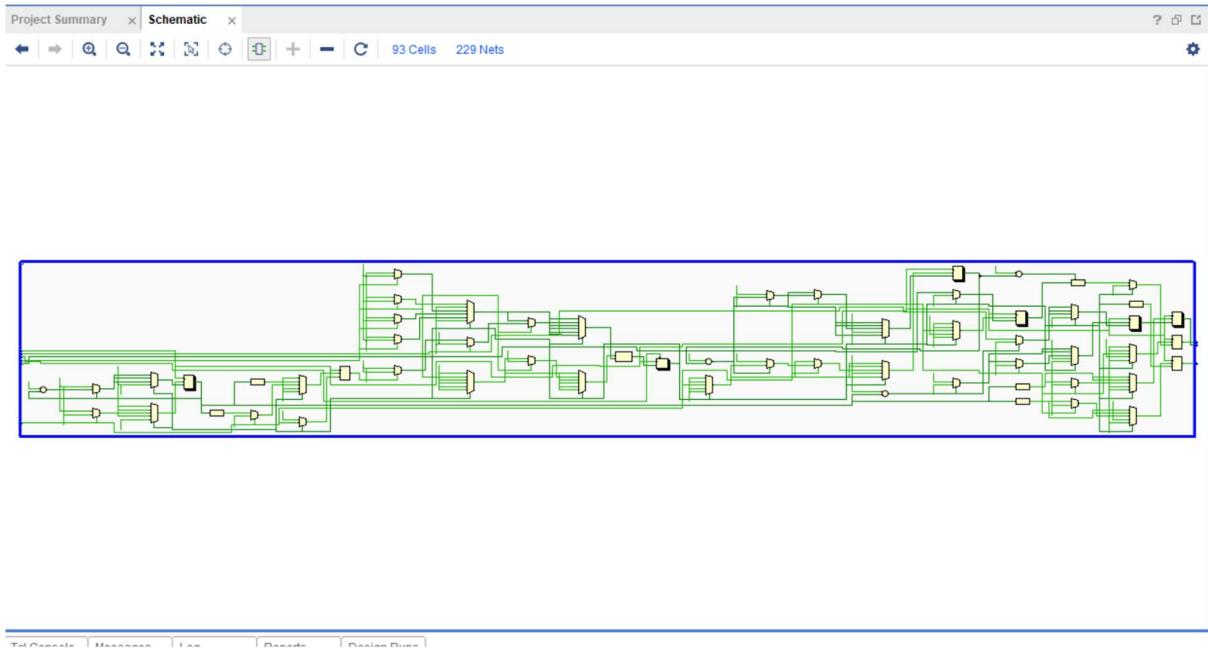


5) Questasim snippets:

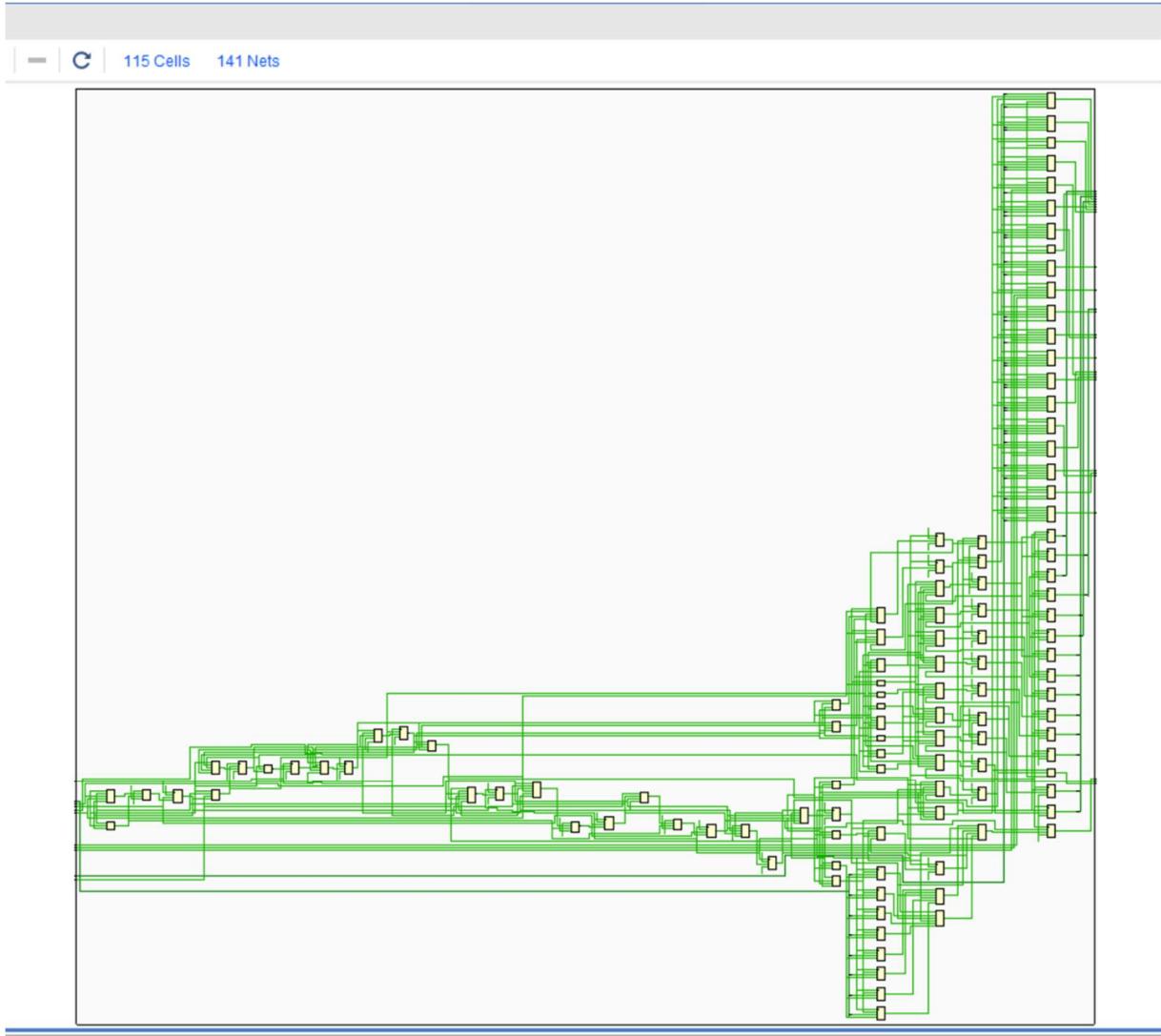


(1)Synthesis for gray coding:

Schematic after elaboration



Schematic after synthesis



Synthesis report

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
READ_DATA	011	100
READ_ADD	010	011
WRITE	111	010

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi_slave'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [D:/spi project/spi_slave.v:36]

Timing report

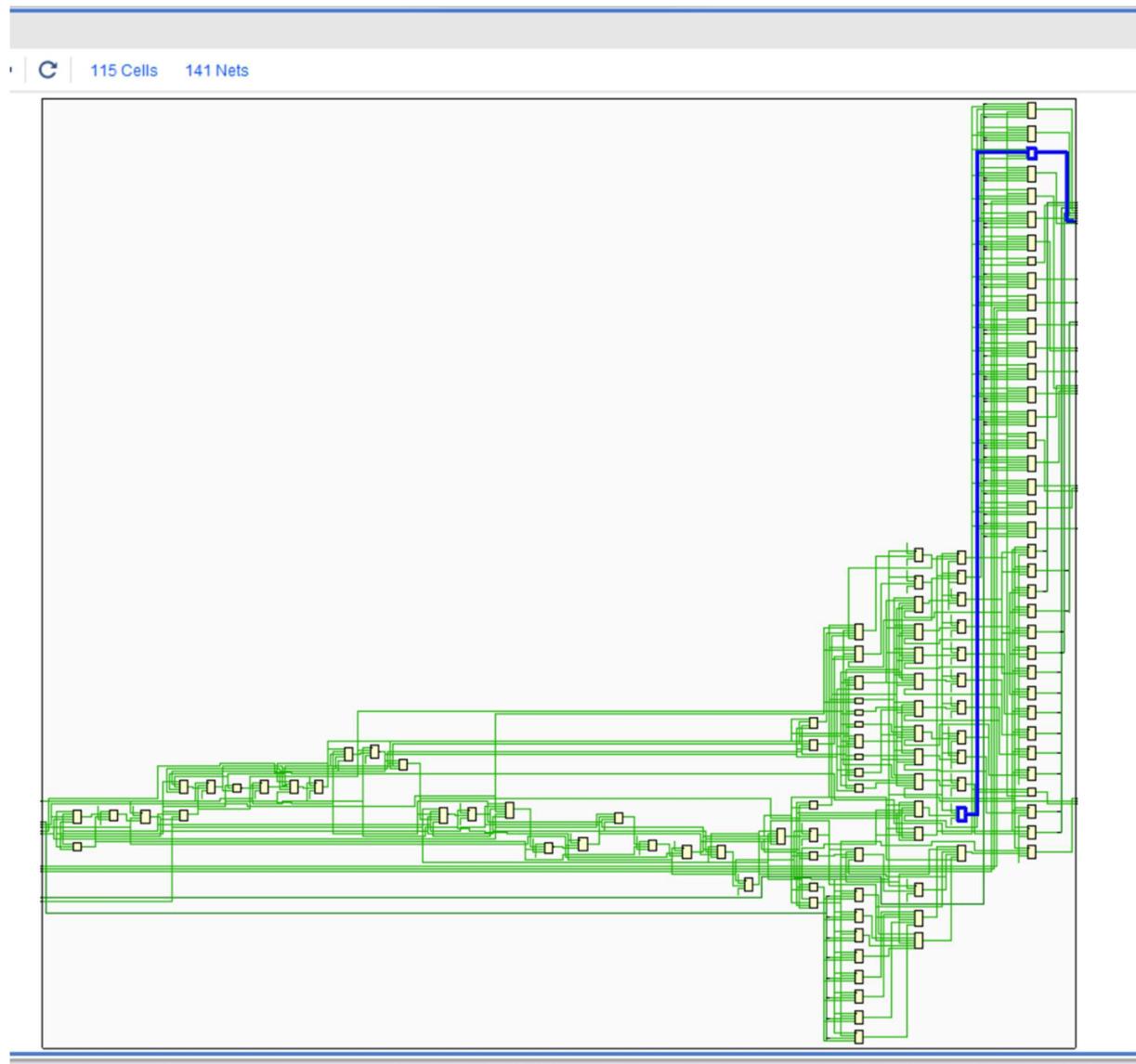
Design Timing Summary

Setup	Hold	Pulse Width			
Worst Negative Slack (WNS):	6.235 ns	Worst Hold Slack (WHS):	0.146 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4219	Total Number of Endpoints:	4219	Total Number of Endpoints:	2117

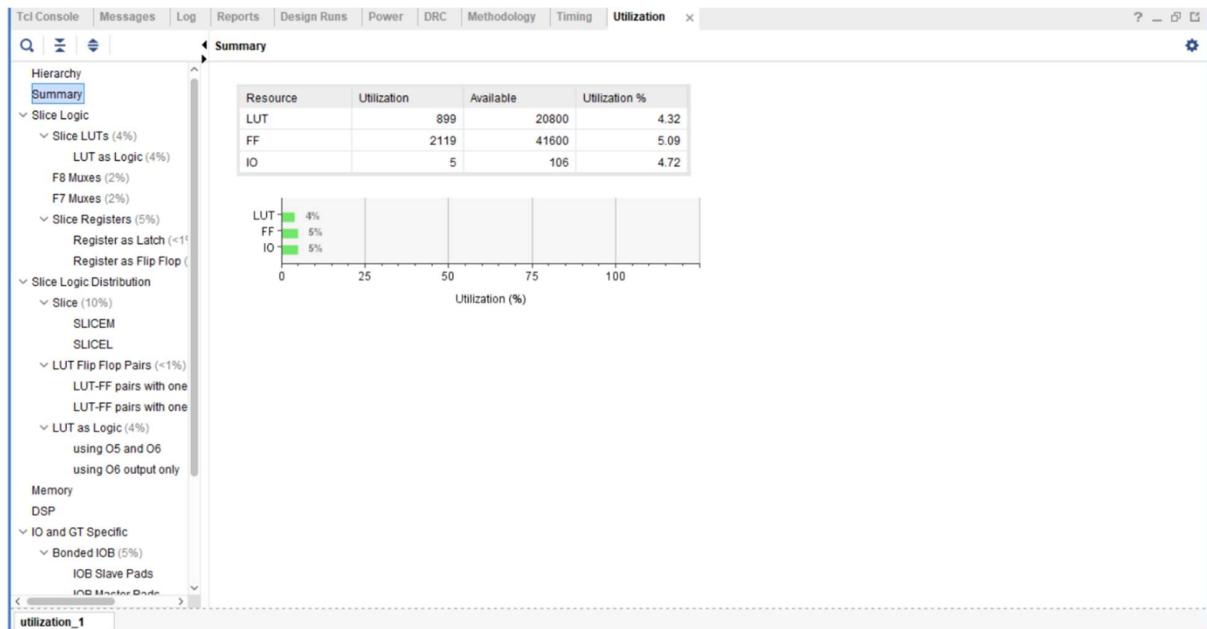
All user specified timing constraints are met.

Summary - timing_2

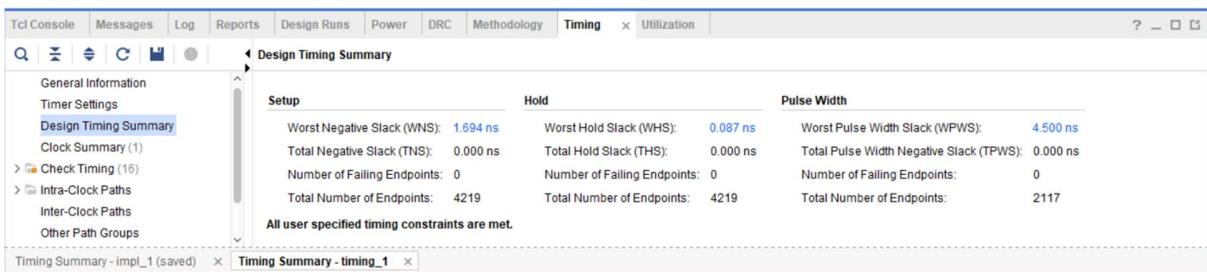
Critical path



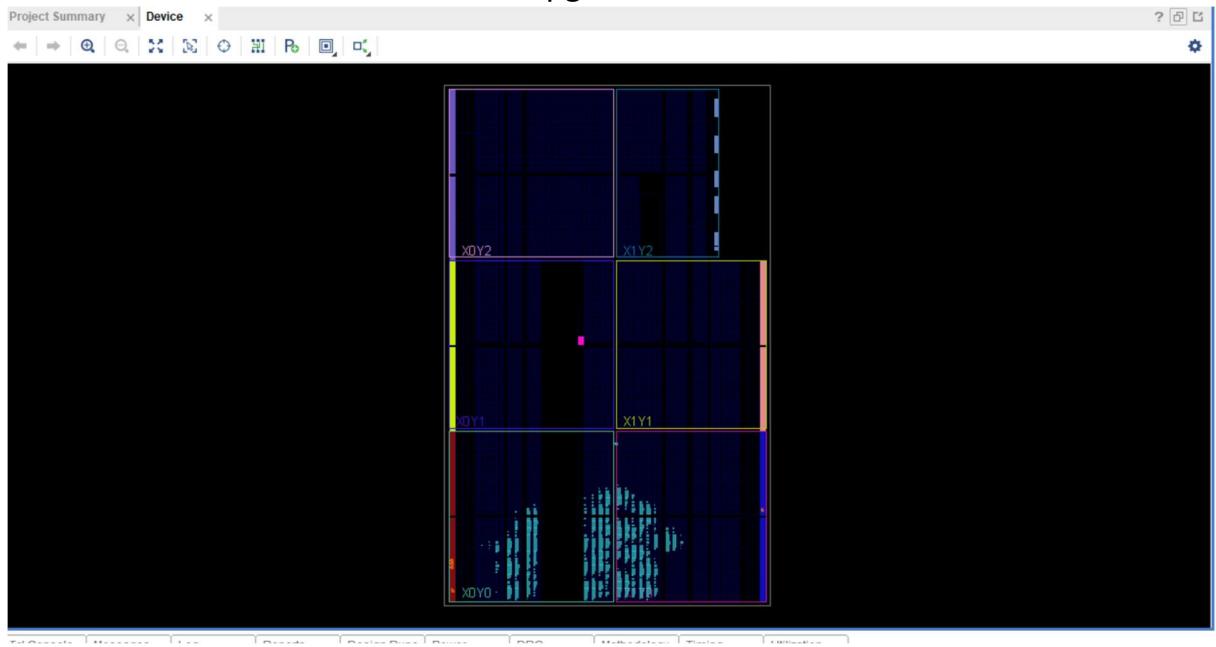
Utilization report



Timing report implementation

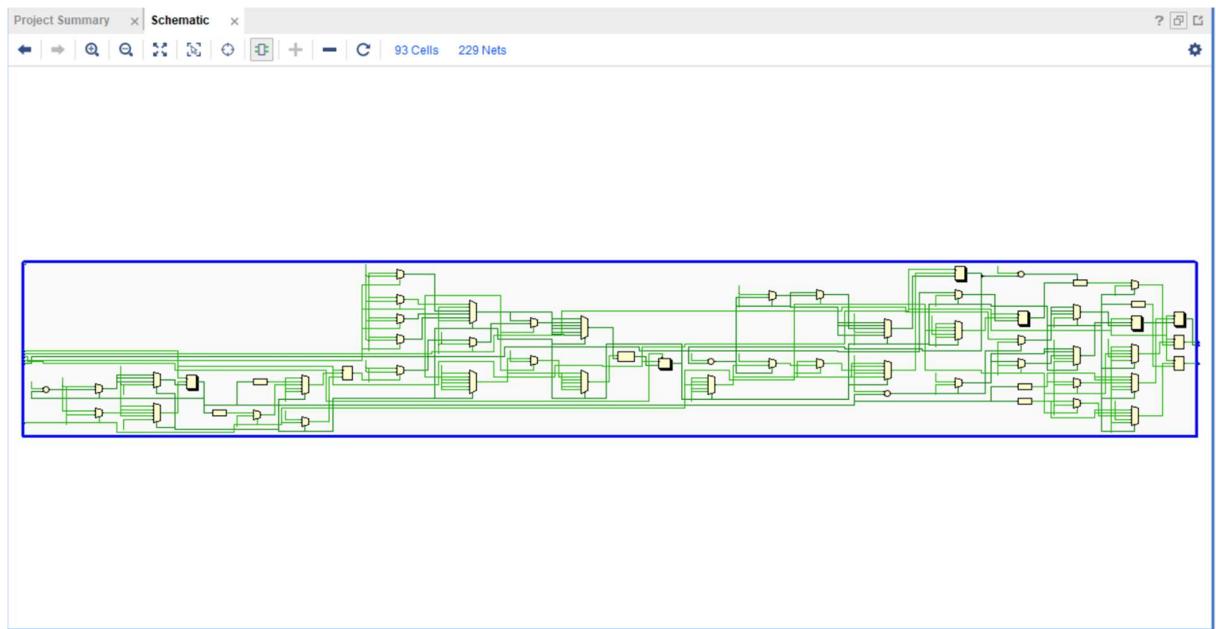


Fpga device

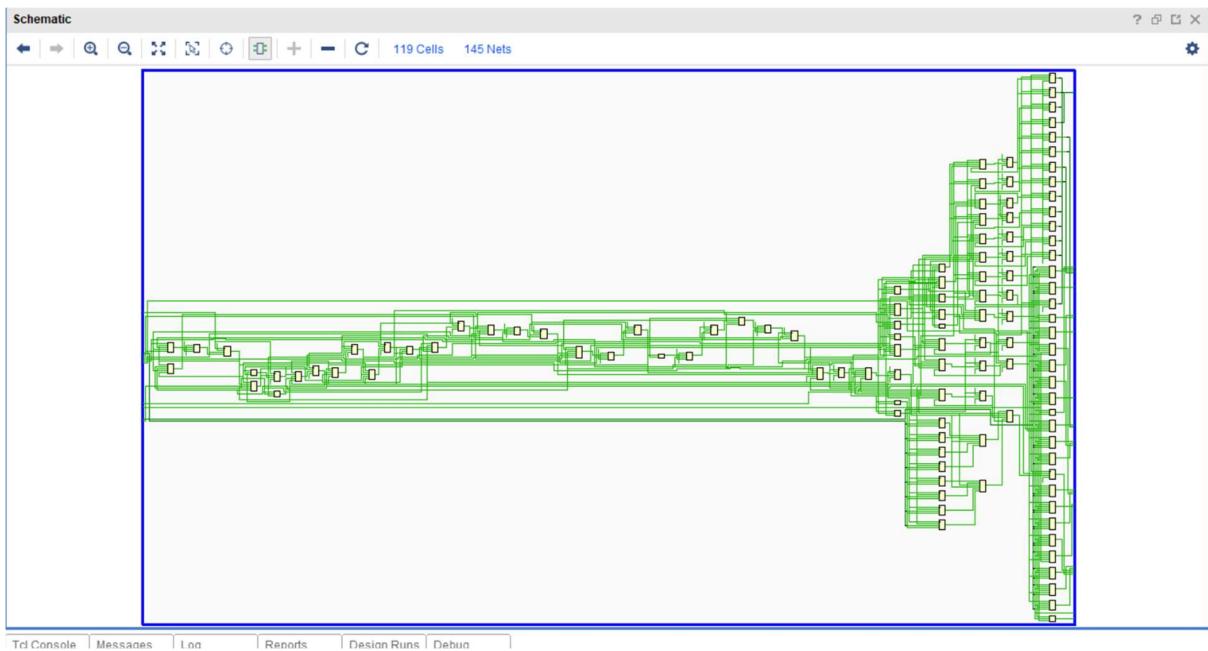


(2) Synthesis using one-hot:

Schematic after elaboration



Schematic after synthesis



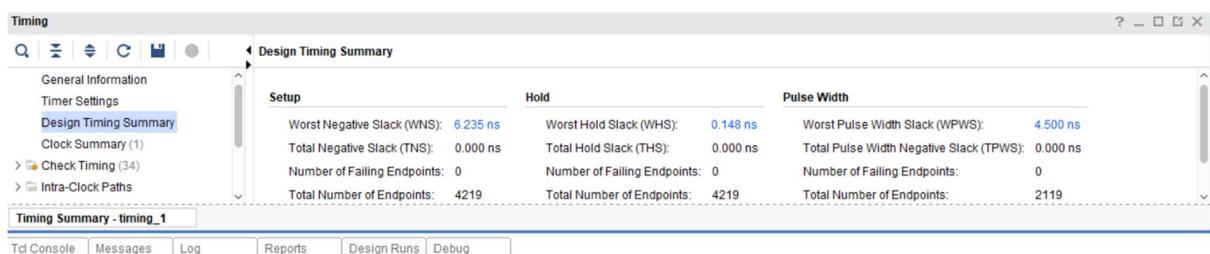
Synthesis report

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

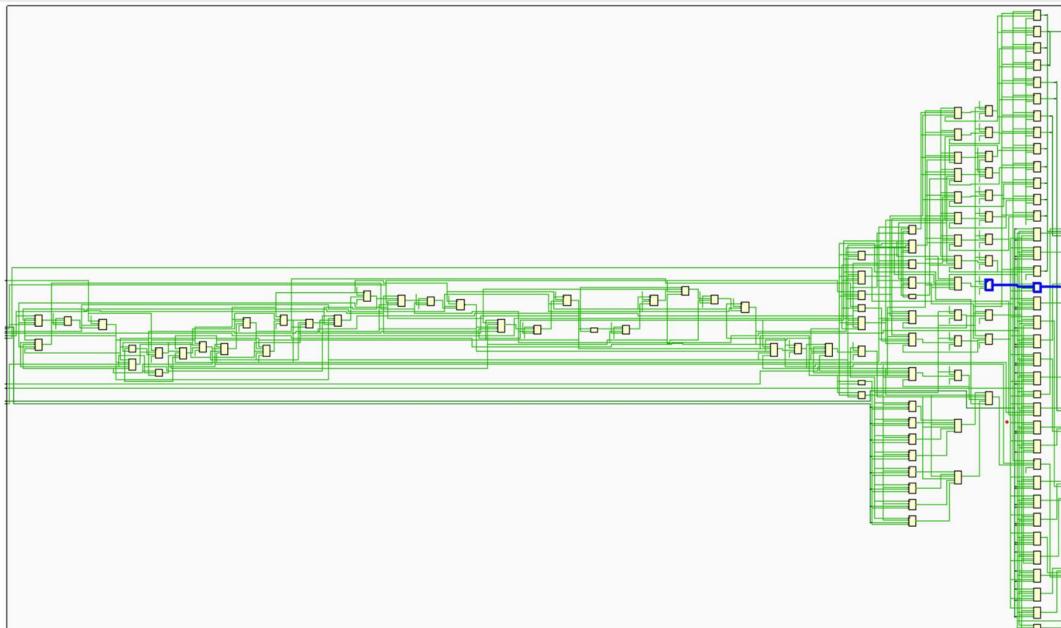
State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
READ_DATA	00100	100
READ_ADD	01000	011
WRITE	10000	010

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [D:/spi project/spi_slave.v:36]

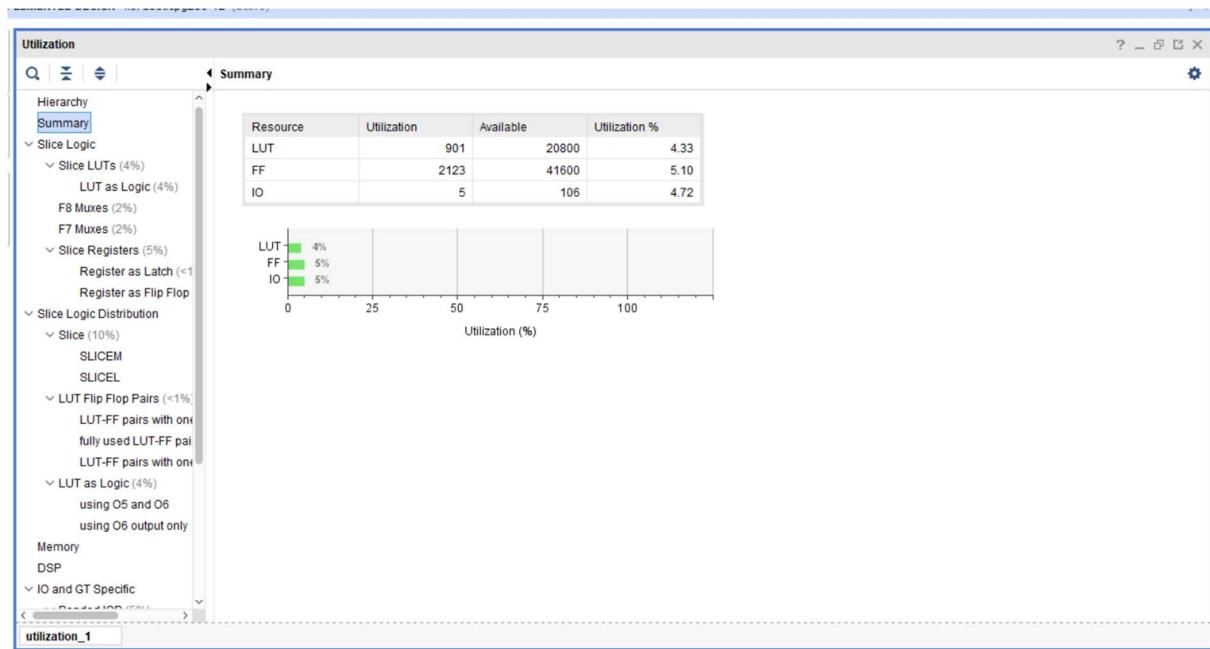
Timing report



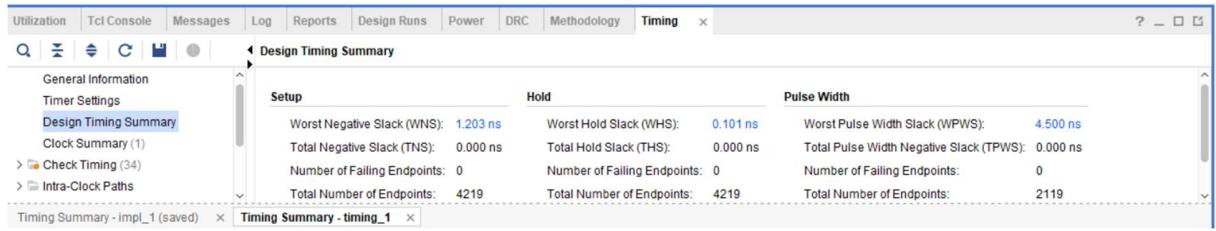
Critical path



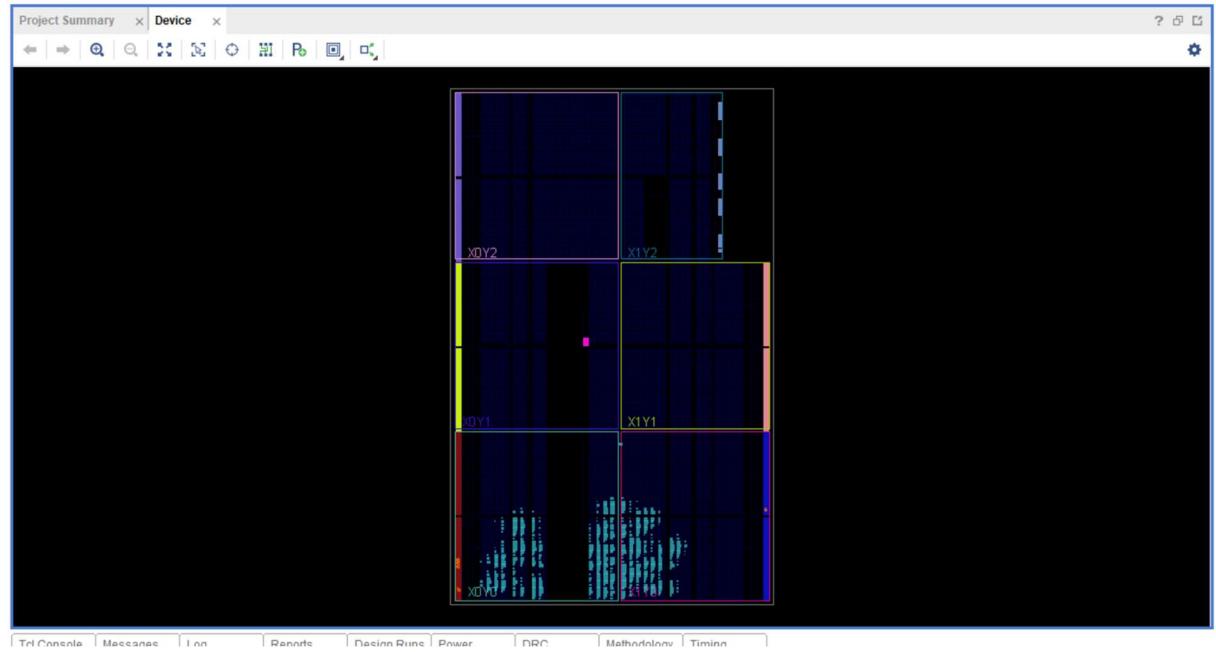
Utilization report



Timing report implementation

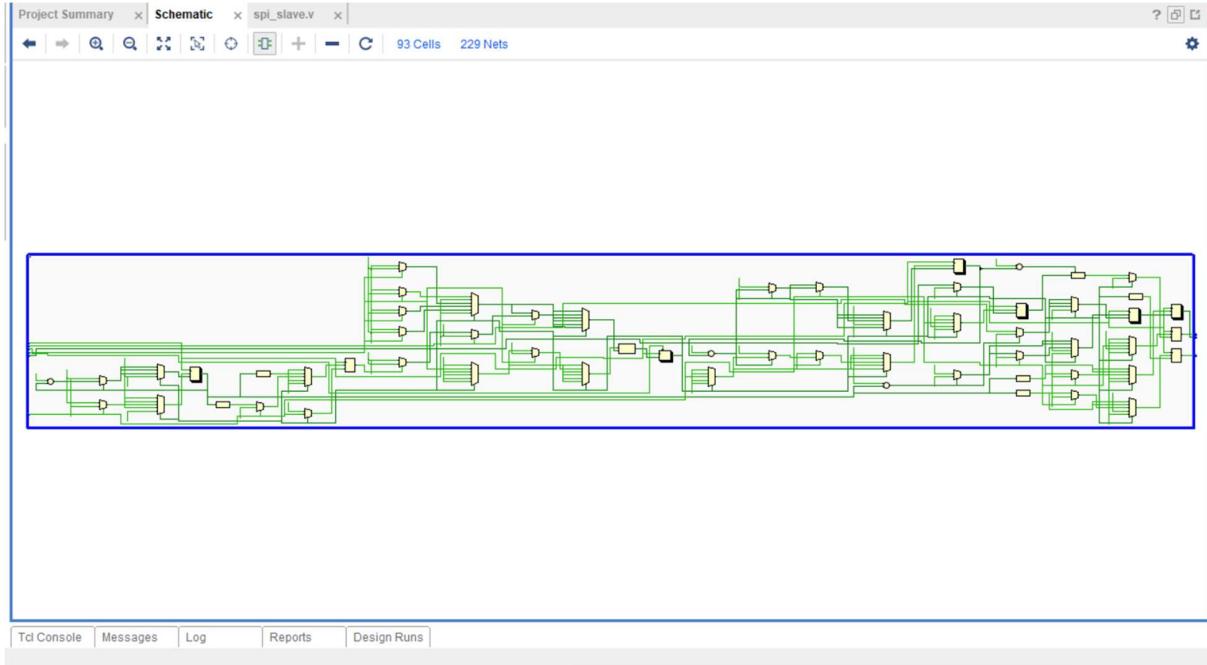


Fpga device

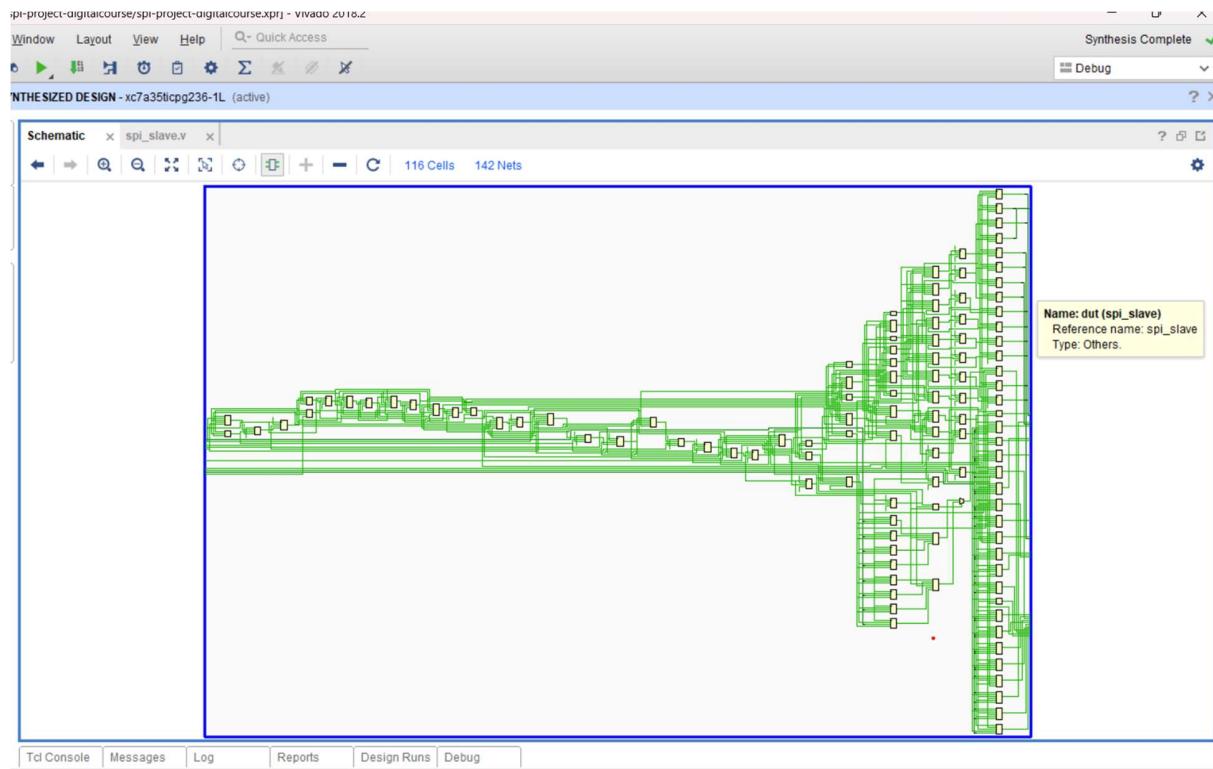


(3)Synthesis using sequential:

Schematic after elaboration



Schematic after synthesis



Synthesis report

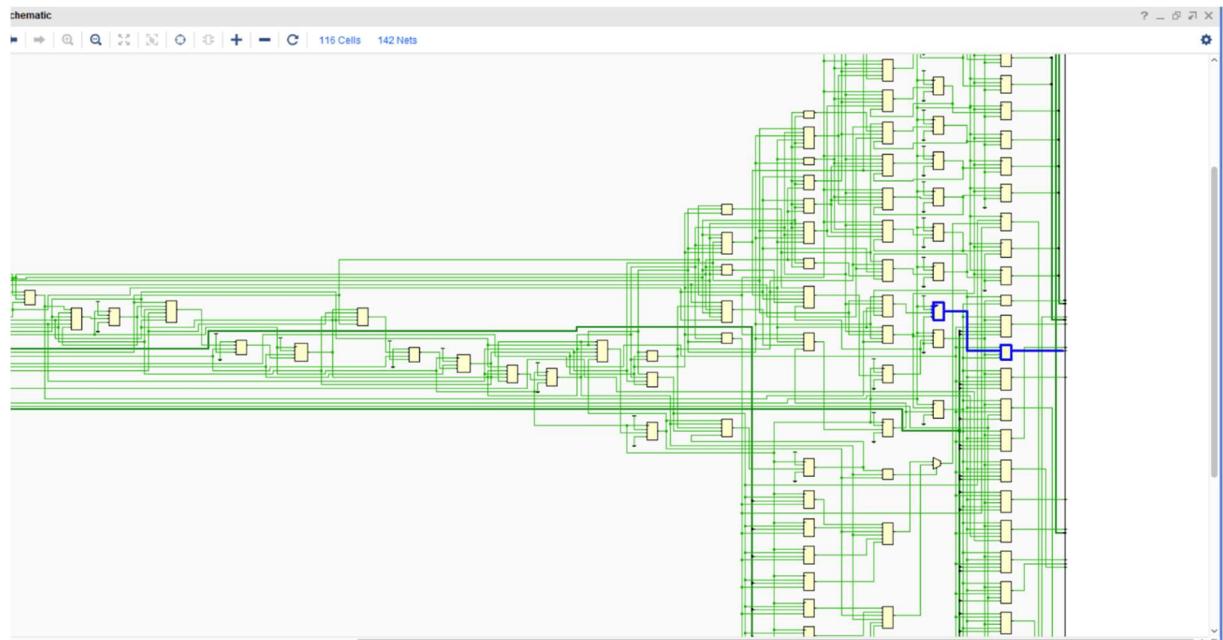
State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
READ_DATA	010	100
READ_ADD	011	011
WRITE	100	010

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'spi_slave'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [D:/spi project/spi_slave.v:36]

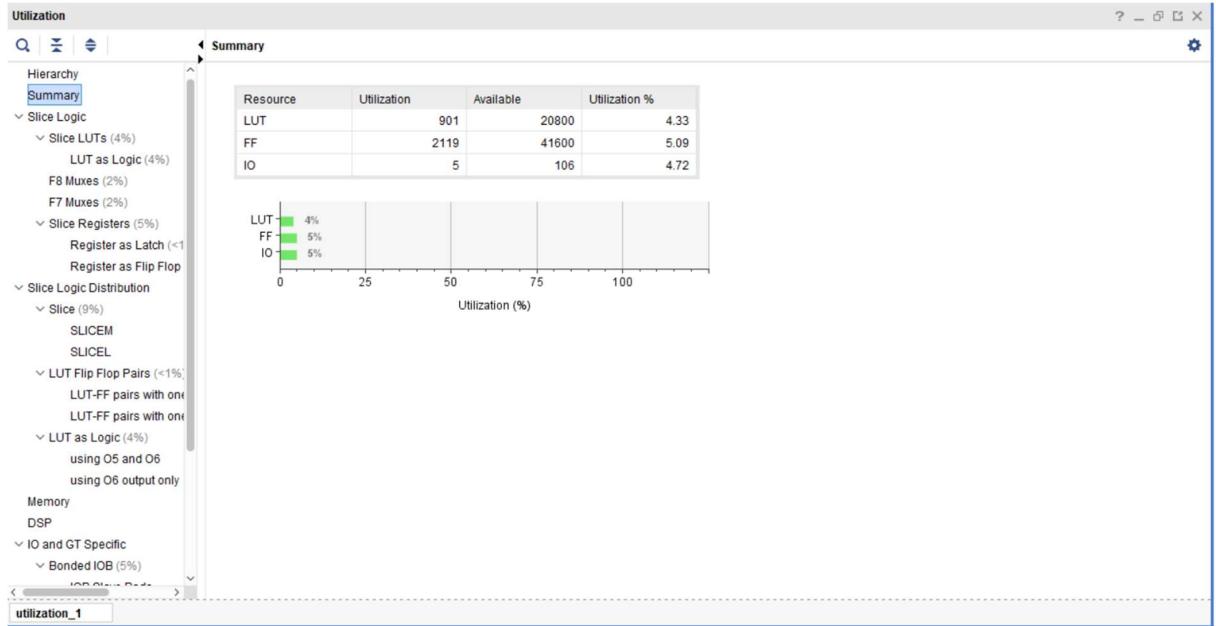
Timing report



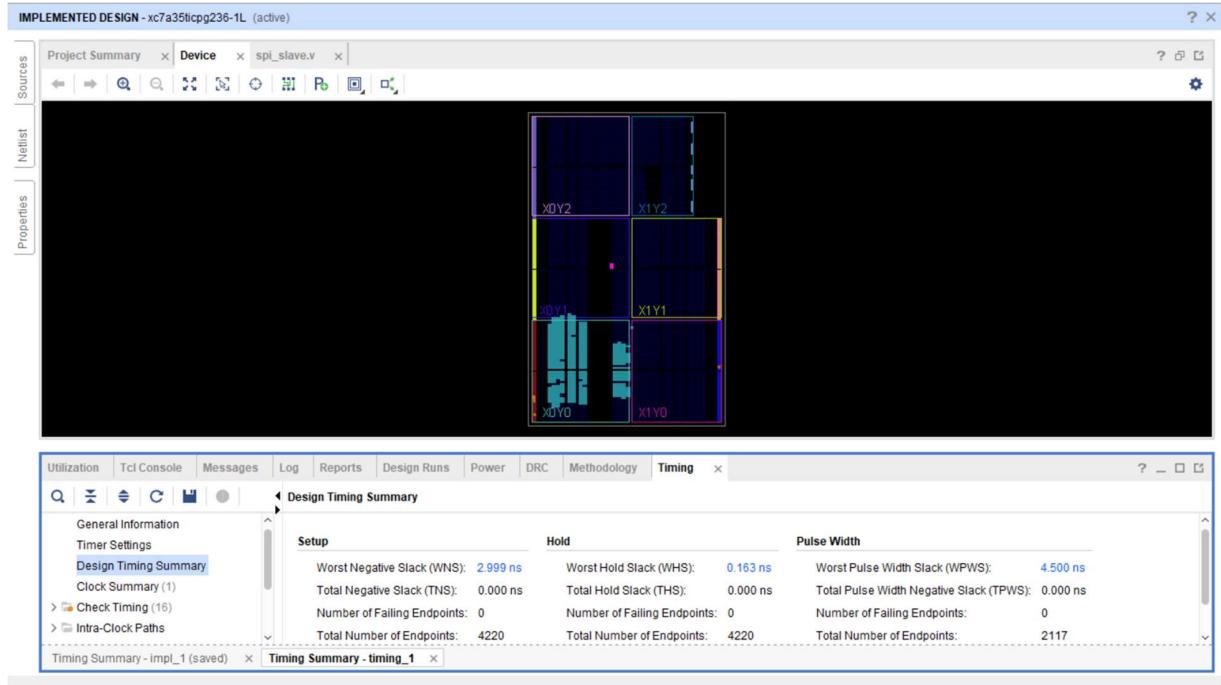
Critical path



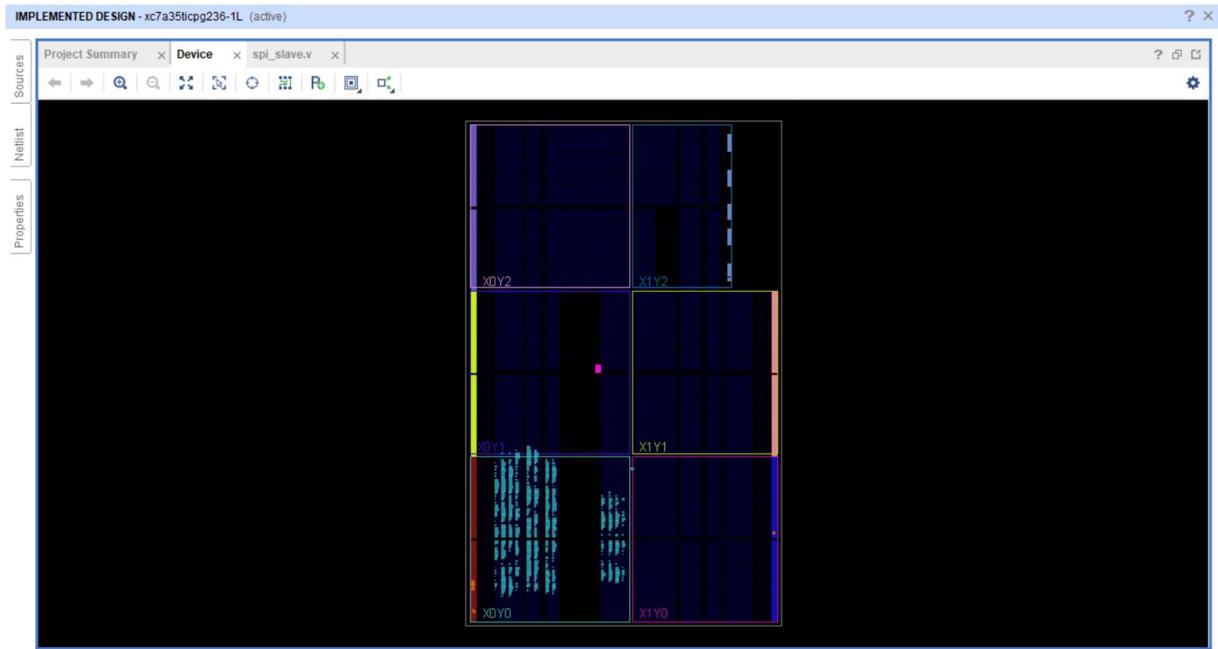
Utilization report



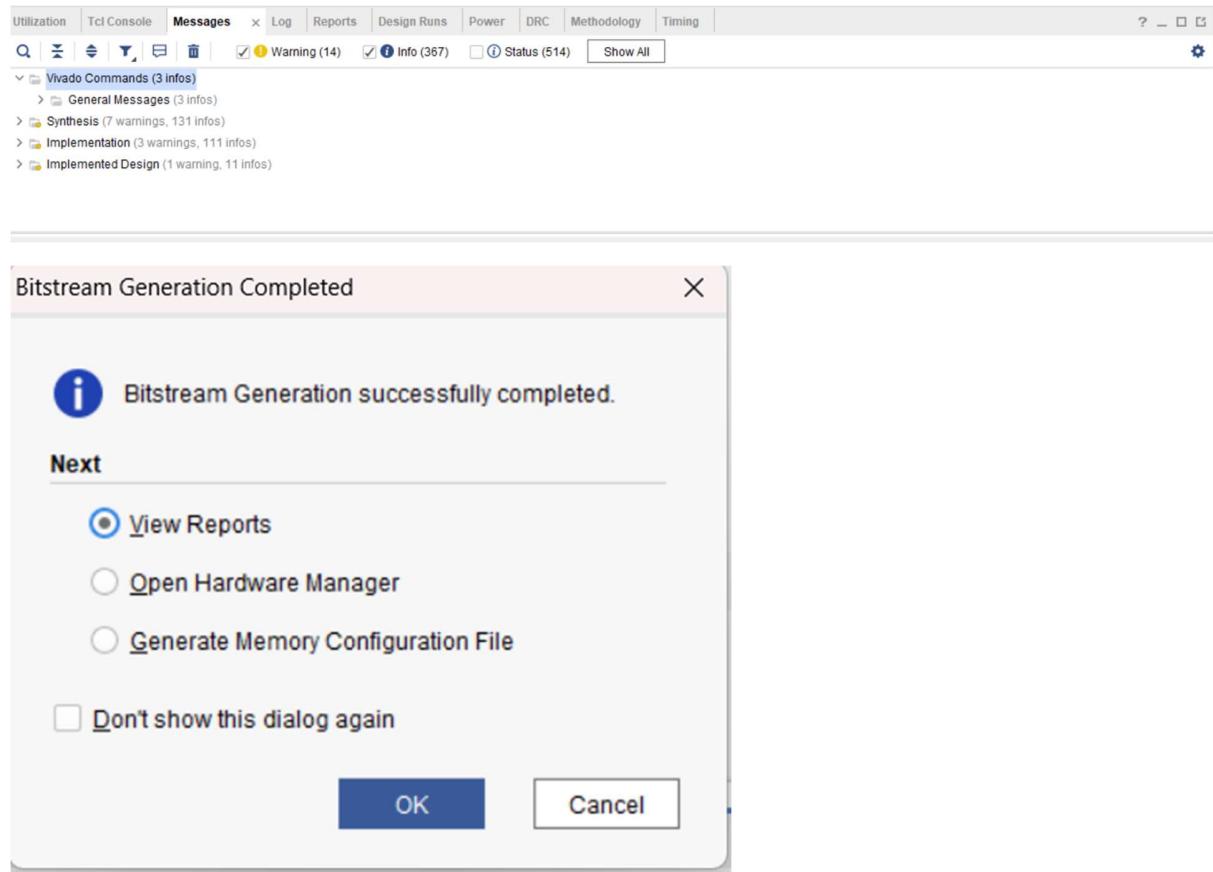
Timing report implementation



Fpga device



(4) Messages tab and successful bitstream



We found that the sequential coding has the highest setup slack

Schematic after debug:

