1. Description

1.1. Project

Project Name	Spokane_Application
Board Name	custom
Generated with:	STM32CubeMX 6.8.1
Date	01/15/2024

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4R5/S5
MCU name	STM32L4R5VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration
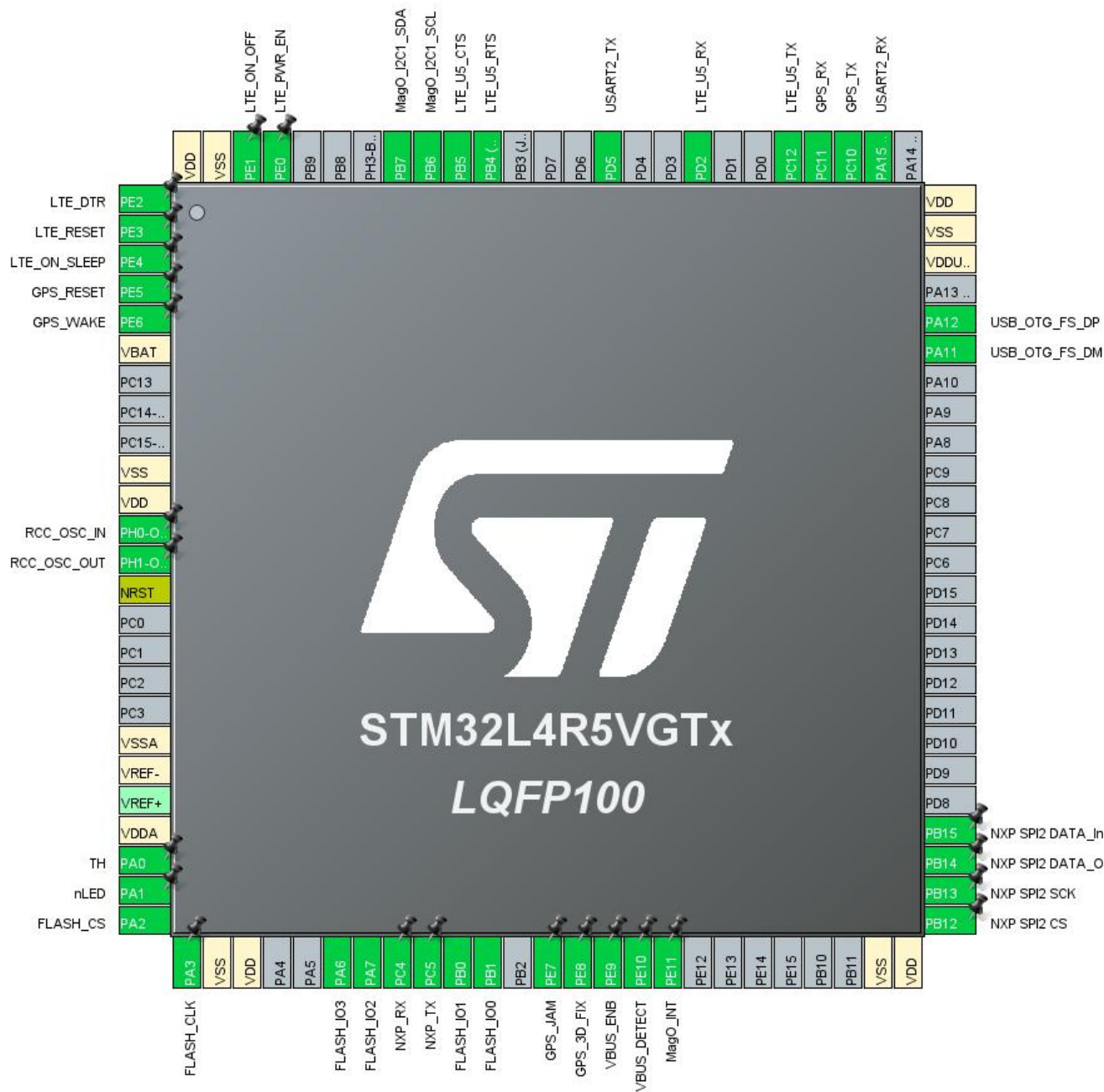
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	LTE_DTR
2	PE3 *	I/O	GPIO_Output	LTE_RESET
3	PE4 *	I/O	GPIO_Input	LTE_ON_SLEEP
4	PE5 *	I/O	GPIO_Output	GPS_RESET
5	PE6 *	I/O	GPIO_Output	GPS_WAKE
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0 *	I/O	GPIO_Output	TH
24	PA1 *	I/O	GPIO_Output	nLED
25	PA2	I/O	OCTOSPIM_P1_NCS	FLASH_CS
26	PA3	I/O	OCTOSPIM_P1_CLK	FLASH_CLK
27	VSS	Power		
28	VDD	Power		
31	PA6	I/O	OCTOSPIM_P1_IO3	FLASH_IO3
32	PA7	I/O	OCTOSPIM_P1_IO2	FLASH_IO2
33	PC4	I/O	USART3_TX	NXP_RX
34	PC5	I/O	USART3_RX	NXP_TX
35	PB0	I/O	OCTOSPIM_P1_IO1	FLASH_IO1
36	PB1	I/O	OCTOSPIM_P1_IO0	FLASH_IO0
38	PE7 *	I/O	GPIO_Input	GPS_JAM
39	PE8 *	I/O	GPIO_Input	GPS_3D_FIX
40	PE9 *	I/O	GPIO_Output	VBUS_ENB
41	PE10 *	I/O	GPIO_Input	VBUS_DETECT
42	PE11 *	I/O	GPIO_Input	MagO_INT
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	SPI2_NSS	NXP SPI2 CS
52	PB13	I/O	SPI2_SCK	NXP SPI2 SCK
53	PB14	I/O	SPI2_MISO	NXP SPI2 DATA_O

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
54	PB15	I/O	SPI2_MOSI	NXP SPI2 DATA_In
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
77	PA15 (JTDI)	I/O	USART2_RX	
78	PC10	I/O	UART4_TX	GPS_TX
79	PC11	I/O	UART4_RX	GPS_RX
80	PC12	I/O	UART5_TX	LTE_U5_TX
83	PD2	I/O	UART5_RX	LTE_U5_RX
86	PD5	I/O	USART2_TX	
90	PB4 (NJTRST)	I/O	UART5_RTS	LTE_U5_RTS
91	PB5	I/O	UART5_CTS	LTE_U5_CTS
92	PB6	I/O	I2C1_SCL	MagO_I2C1_SCL
93	PB7	I/O	I2C1_SDA	MagO_I2C1_SDA
97	PE0 *	I/O	GPIO_Output	LTE_PWR_EN
98	PE1 *	I/O	GPIO_Output	LTE_ON_OFF
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration
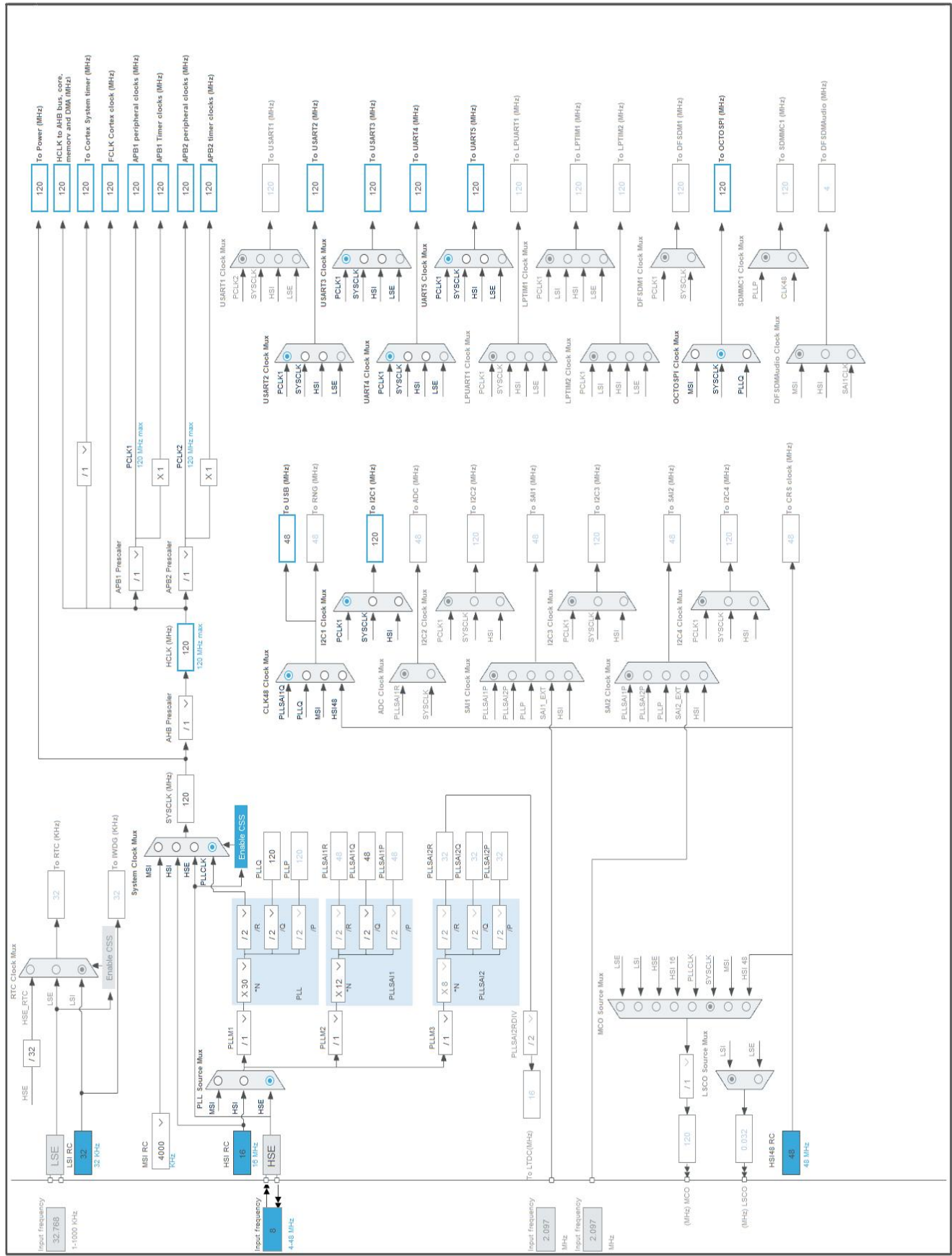
5. Software Project

5.1. Project Settings

Name	Value
Project Name	Spokane_Application
Project Folder	C:\Users\victoria\STM32CubeIDE\workspace_1.12.1\Spokane_Application
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x2000
Minimum Stack Size	0x2000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART3_UART_Init	USART3
5	MX_SPI2_Init	SPI2
6	MX_USB_OTG_FS_HCD_Init	USB_OTG_FS
7	MX_I2C1_Init	I2C1
8	MX_OCTOSPI1_Init	OCTOSPI1
9	MX_UART4_Init	UART4
10	MX_UART5_Init	UART5
11	MX_USART2_UART_Init	USART2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4R5/S5
MCU	STM32L4R5VGTx
Datasheet	DS12023_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH-SingleBank	n/a
CPU Frequency	120 MHz	0 Hz
Clock Configuration	HSE BYP PLL ART	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals	GPIOA GPIOB GPIOC GPIOE GPIOH I2C1 OCTOSPI1 SPI2 SYS-VREFBUF/COMP1:COMP_High_Speed-Square_VREFBUF_OFF UART4 USART1 USART3 USB_OTG_FS	
Additional Cons.	0 mA	0 mA
Average Current	30.17 mA	2.55 µA
Duration	0.1 ms	0.9 ms
DMIPS	150.0	0.0
Ta Max	101.2	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days, 10 hours	Average DMIPS	150.0 DMIPS

6.6. Chart

Consumption Profile by Step
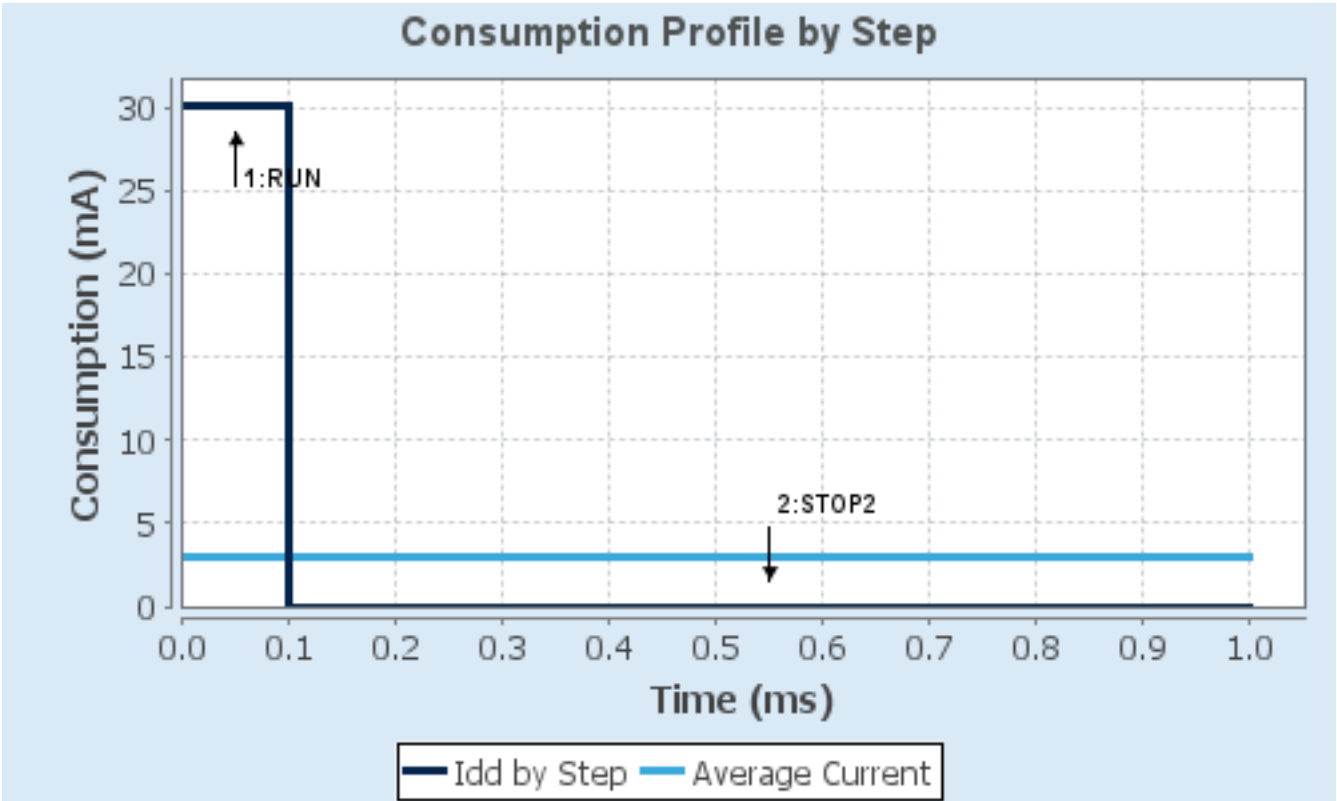
7. Peripherals and Middlewares Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.2. OCTOSPI1

Mode: Quad SPI

mode: Clock

Chip Select: Port1 NCS

Data [3:0]: Port1 IO[3:0]

7.2.1. Parameter Settings:

Generic:

Fifo Threshold	1
Dual Mode	Disable
Memory Type	Micron
Device Size	**27 ***
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Clock Prescaler	1
Sample Shifting	No Sample Shifting

Delay Hold Quarter Cycle	Disable
Chip Select Boundary	0
Delay Block	Disable

7.3. RCC
High Speed Clock (HSE): Crystal/Ceramic Resonator
7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 boost |

7.4. SPI2
Mode: Full-Duplex Master
Hardware NSS Signal: Hardware NSS Input Signal
7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**60.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Input Hardware

7.5. SYS
Timebase Source: SysTick

7.6. UART4
Mode: Asynchronous
7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.7. UART5

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.8. USART2

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.9. USART3
Mode: Asynchronous
7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First   Disable

7.10. USB_OTG_FS
Mode: Host_Only
7.10.1. Parameter Settings:

Signal start of frame   Disabled
Speed   Full Speed 12MBit/s

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**Very High** *	MagO_I2C1_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**Very High** *	MagO_I2C1_SDA
OCTOSPI1	PA2	OCTOSPIM_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FLASH_CS
	PA3	OCTOSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FLASH_CLK
	PA6	OCTOSPIM_P1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FLASH_IO3
	PA7	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FLASH_IO2
	PB0	OCTOSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FLASH_IO1
	PB1	OCTOSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FLASH_IO0
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	NXP SPI2 CS
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	NXP SPI2 SCK
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	NXP SPI2 DATA_O
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	NXP SPI2 DATA_In
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	GPS_TX
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	GPS_RX
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	LTE_U5_TX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	LTE_U5_RX
	PB4 (NJTRST)	UART5_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	LTE_U5_RTS
	PB5	UART5_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	LTE_U5_CTS
USART2	PA15 (JTDI)	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USART3	PC4	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	NXP_RX
	PC5	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	NXP_TX
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
GPIO	PE2	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	LTE_DTR
	PE3	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	LTE_RESET
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LTE_ON_SLEEP
	PE5	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	GPS_RESET
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPS_WAKE
	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TH
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	nLED
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPS_JAM
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPS_3D_FIX
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VBUS_ENB
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	VBUS_DETECT
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MagO_INT
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LTE_PWR_EN
	PE1	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	LTE_ON_OFF

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_RX	DMA1_Channel5	Peripheral To Memory	**Very High ***
SPI2_TX	DMA1_Channel6	Memory To Peripheral	**Very High ***
UART5_RX	DMA1_Channel1	Peripheral To Memory	Low
UART5_TX	DMA1_Channel2	Memory To Peripheral	Low
USART3_RX	DMA1_Channel3	Peripheral To Memory	Low
USART3_TX	DMA1_Channel4	Memory To Peripheral	Low

SPI2_RX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_TX: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_RX: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable

Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
UART4 global interrupt	true	0	0
UART5 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USB OTG FS global interrupt	unused		
OCTOSPI1 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
DMA1 channel6 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
USART2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
UART4 global interrupt	false	true	true
UART5 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32l4plus_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32l4plus_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32l4plus-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32l4plus_pres.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32ulp.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32l4plus.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/psa-certificate_stm32l4.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-

and-mpus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an3236-increase-the-number-of-touchkeys-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an3960-esd-considerations-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4299-improve-conducted-noise-robustness-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4310-sampling-capacitor-selection-guide-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4312-design-with-surface-sensors-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4316-tuning-a-touch-sensing-application-on-mcus-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4555-getting-started-with-stm32l4-series-and-stm32l4-series-hardware-development-stmicroelectronics.pdf

Application Notes   https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf

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