Iverilog教學

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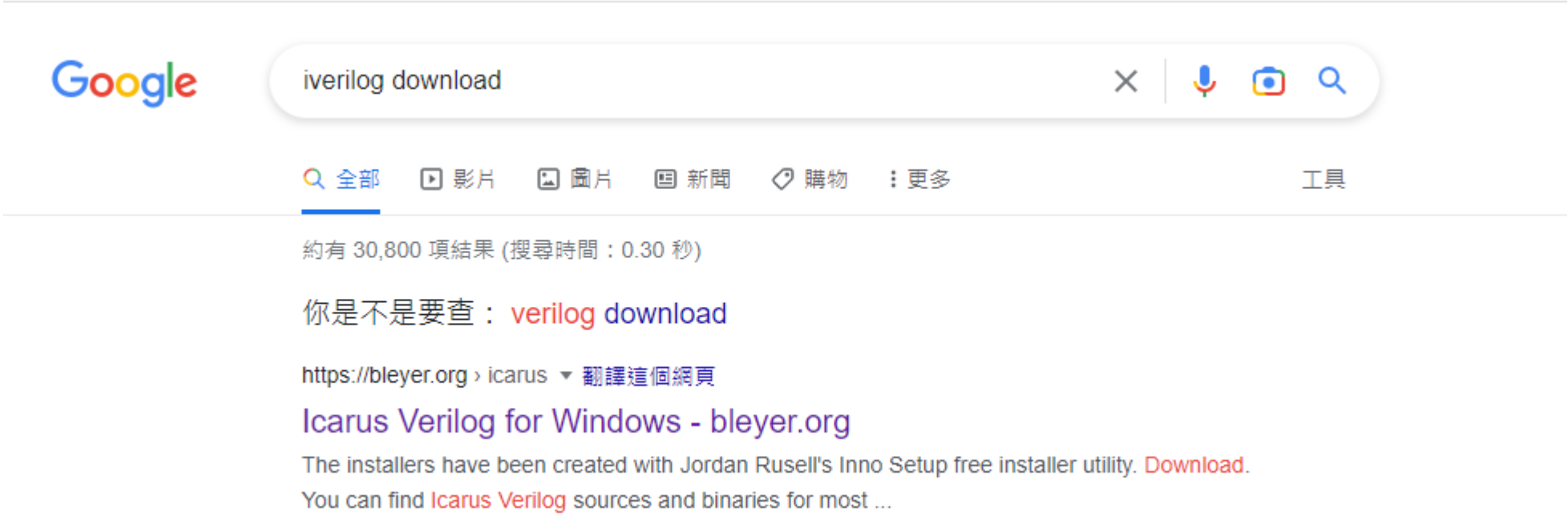


進入 Icarus Verilog for Windows 下載第一個連結

Icarus Verilog for Windows

Icarus Verilog is a free compiler implementation for the IEEE-1364 Verilog hardware description language. Icarus is maintained by Stephen Williams and it

In this page you will find easy to install Icarus Verilog packages compiled with the MinGW toolchain for the Windows environment. GTKWave for Win32 is al

Download

You can find Icarus Verilog sources and binaries for most platforms at the Icarus site FTP. The sources available here have been compressed with 7-zip.

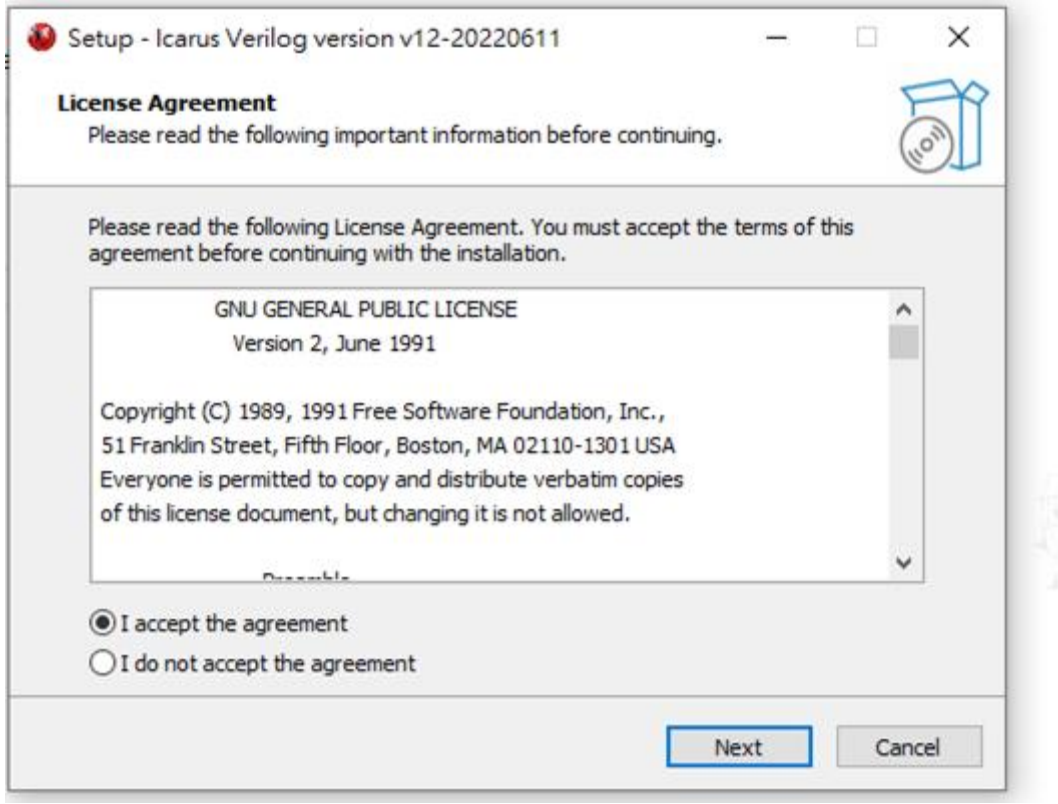
- iverilog-v12-20220611-x64_setup [18.2MB]
- iverilog-v11-20210204-x64_setup.exe [44.1MB]
- iverilog-v11-20201123-x64_setup.exe [18.1MB]
- iverilog-10.1.1-x64_setup.exe [9.77MB]
- iverilog-10.0-x86_setup.exe [11.1MB]
- iverilog-20130827_setup.exe (development snapshot) [11.2MB]
- iverilog-0.9.7_setup.exe (latest stable release) [10.5MB]
- iverilog-0.9.6_setup.exe [10.4MB]
- iverilog-0.8.6_setup.exe (latest release 0.8 series) [1.29MB] iverilog-0.8.6.7z [800kB]
- iverilog-0.7-20040706_setup.exe [1.09MB] iverilog-0.7-20040706.7z [588kB]

Resources

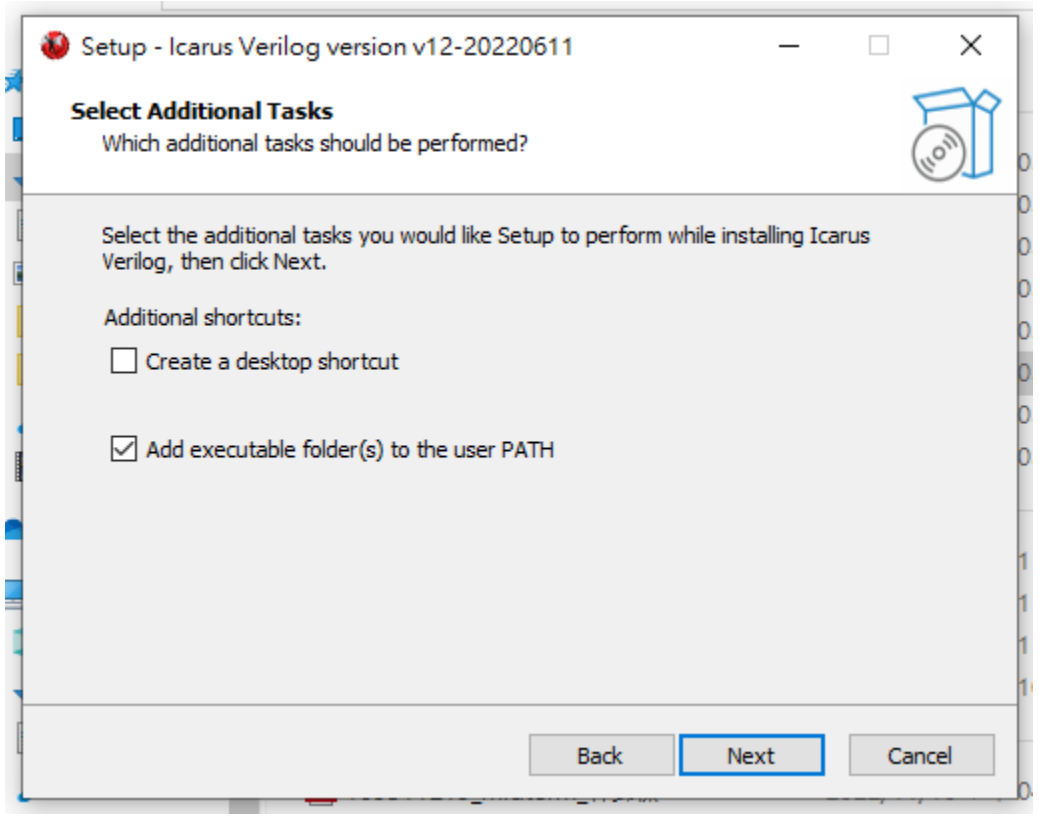
Here are some pointers to interesting Verilog related resources.

- Verilog Resources
- GTKWave Electronic Waveform Viewer
- GTKWave for Windows
- IVI, a graphical frontend for Icarus
- Eclipse Verilog Editor
- Verilog syntax highlighting for UltraEdit.

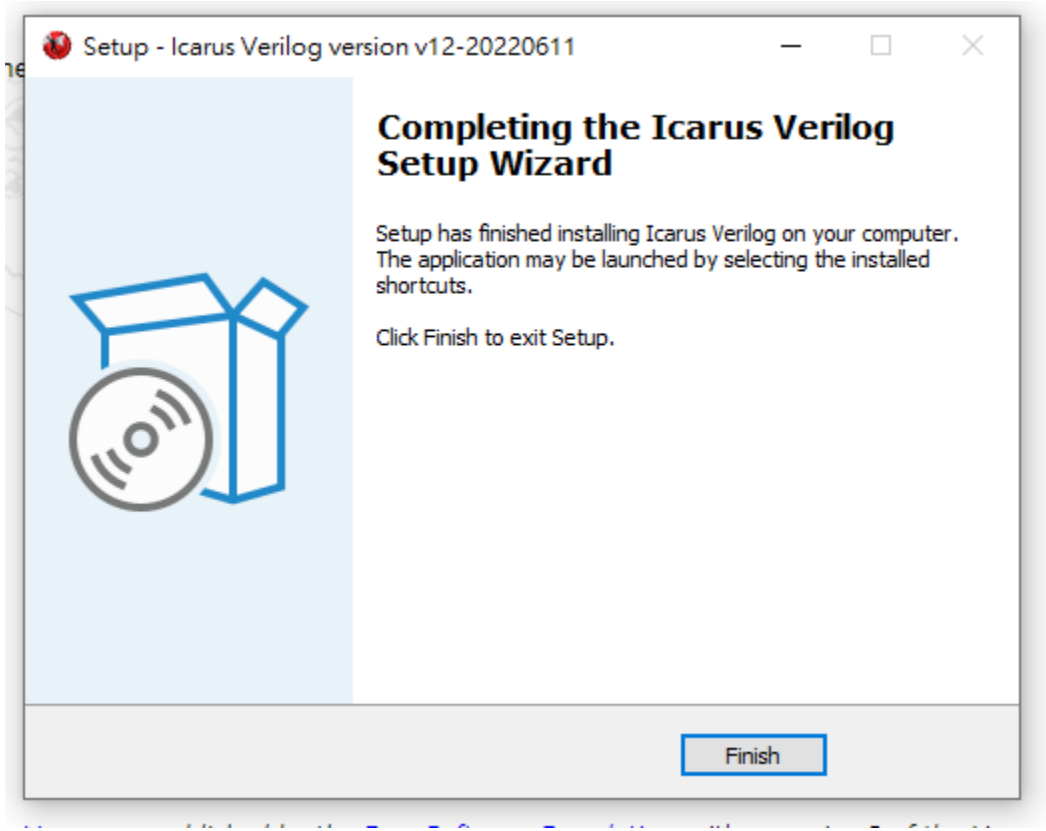
安裝 Icarus Verilog



注意! 安裝過程需勾選 add user PATH



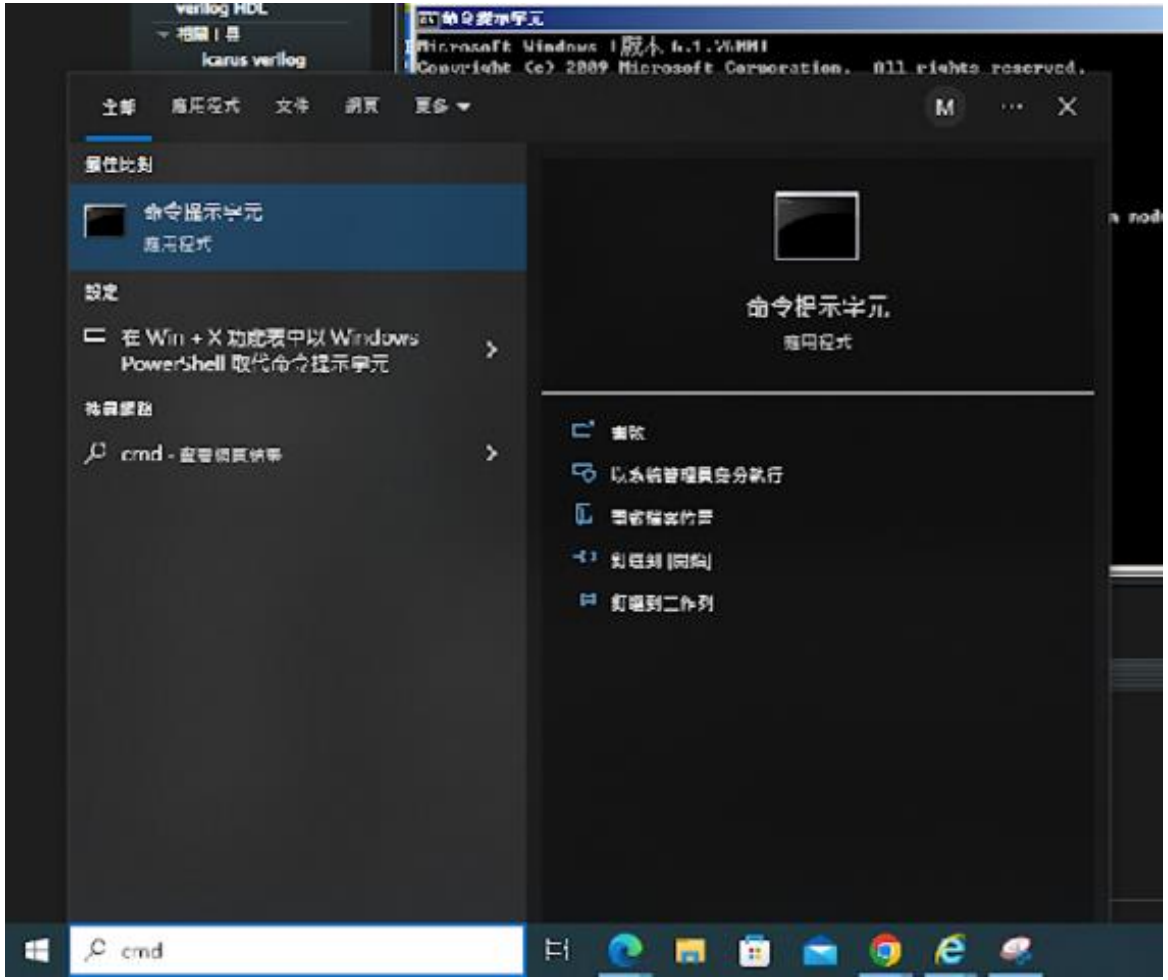
安裝結束


Setup - Icarus Verilog version v12-20220611
Completing the Icarus Verilog Setup Wizard
Setup has finished installing Icarus Verilog on your computer. The application may be launched by selecting the installed shortcuts.
Click Finish to exit Setup.
Finish

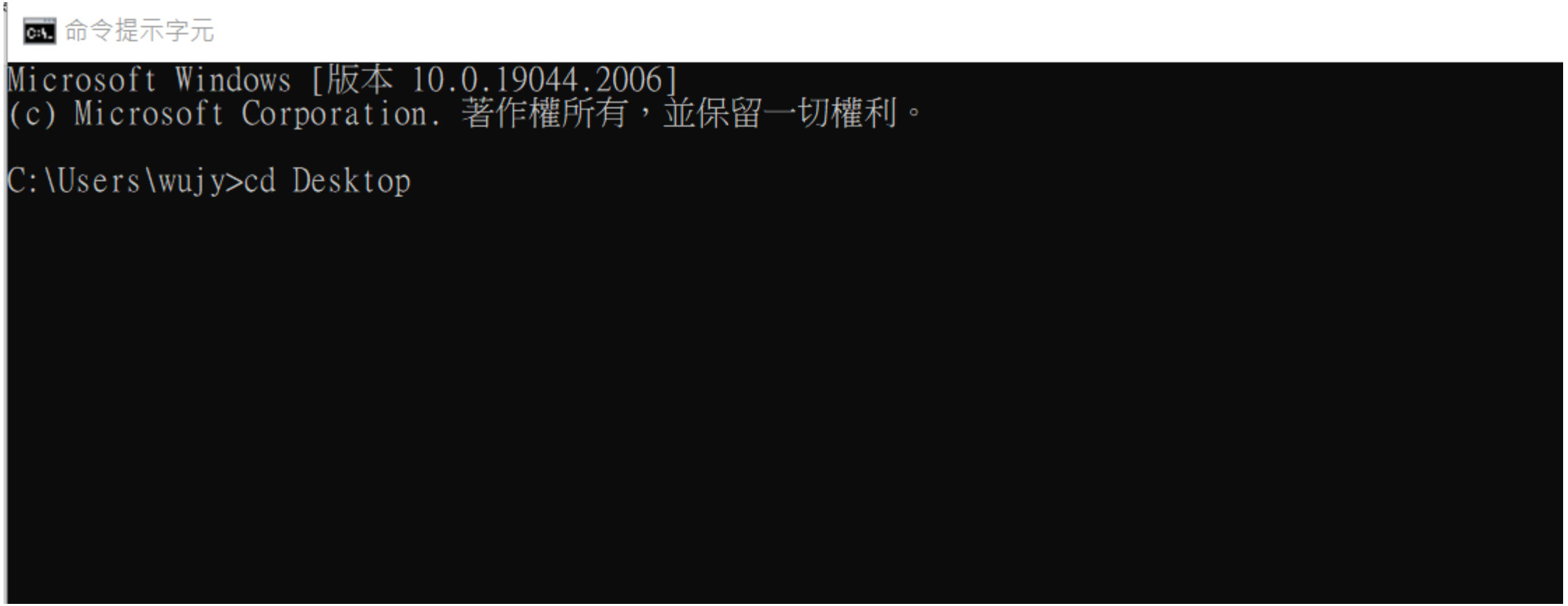
把測試資料夾放在桌面(資料夾內容如下)

名稱	修改日期	類型	大小
instruction	2022/11/24 上午 02:33	文字文件	3 KB
mem	2022/11/10 下午 11:59	文字文件	23 KB
MEM	2022/11/10 下午 11:59	V 檔案	25 KB
PATTERN	2022/11/27 下午 11:01	V 檔案	12 KB
PATTERN_p	2022/11/27 下午 11:01	V 檔案	13 KB
SP	2022/11/25 上午 09:59	V 檔案	2 KB
SP_pipeline	2022/11/25 上午 09:59	V 檔案	2 KB
TESTBED	2022/11/27 下午 10:56	V 檔案	2 KB
TESTBED_p	2022/11/27 下午 10:55	V 檔案	2 KB

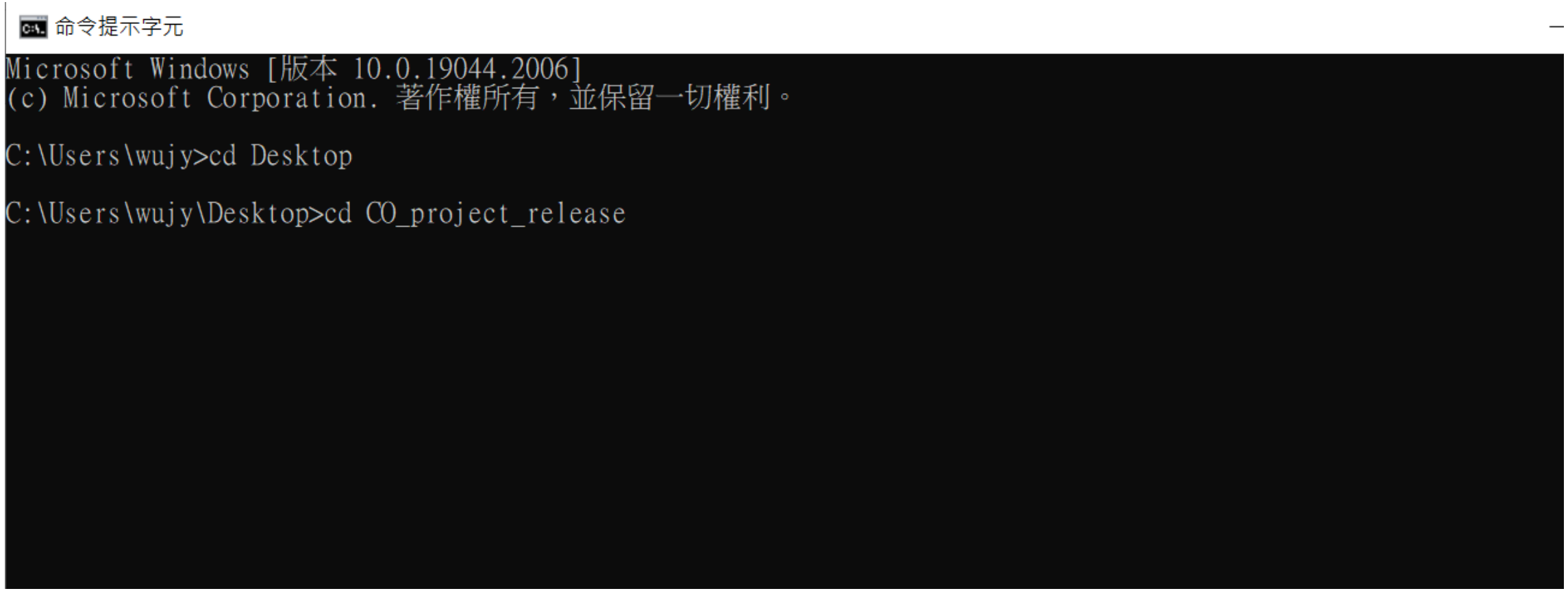
在 Windows 搜尋 cmd 打開命令提示字元



輸入 cd Desktop (進入桌面)



輸入 cd CO_project_release(測試資料夾檔名)



將TESTBED.v包成執行檔test
iverilog -o test TESTBED.v

- 非pipeline版本輸入iverilog -o test TESTBED.v
- pipeline版本輸入iverilog -o test TESTBED_p.v

輸入 vvp test (執行指令)

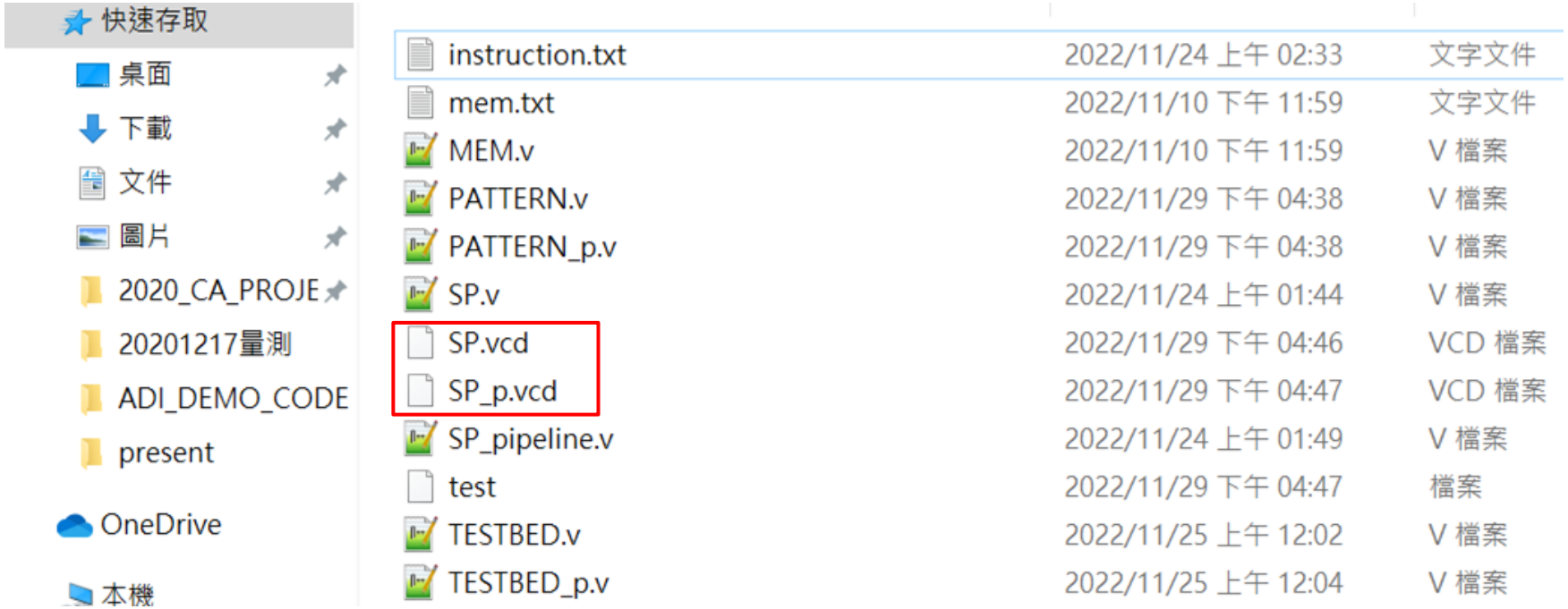
執行結果如下 (有龍貓表示通過pattern)

命令提示字元

```
VCD warning: array word TESTBED.My_SP.r[31] will conflict with an escaped identifier.


        ----------------------------
        --                        --       |__||
        --  Congratulations !!    --      / O.O  |
        --                        --    /_____   |
        --   [0;32mSimulation PASS!! [m     --   /^ ^ ^ \  |
        --                        --  |^ ^ ^ ^ |w|
        ----------------------------   \m___m__|_|


./PATTERN.v:416: $finish called at 1957500 (10ps)

C:\Users\wujy\Desktop\CO_project_release>
```

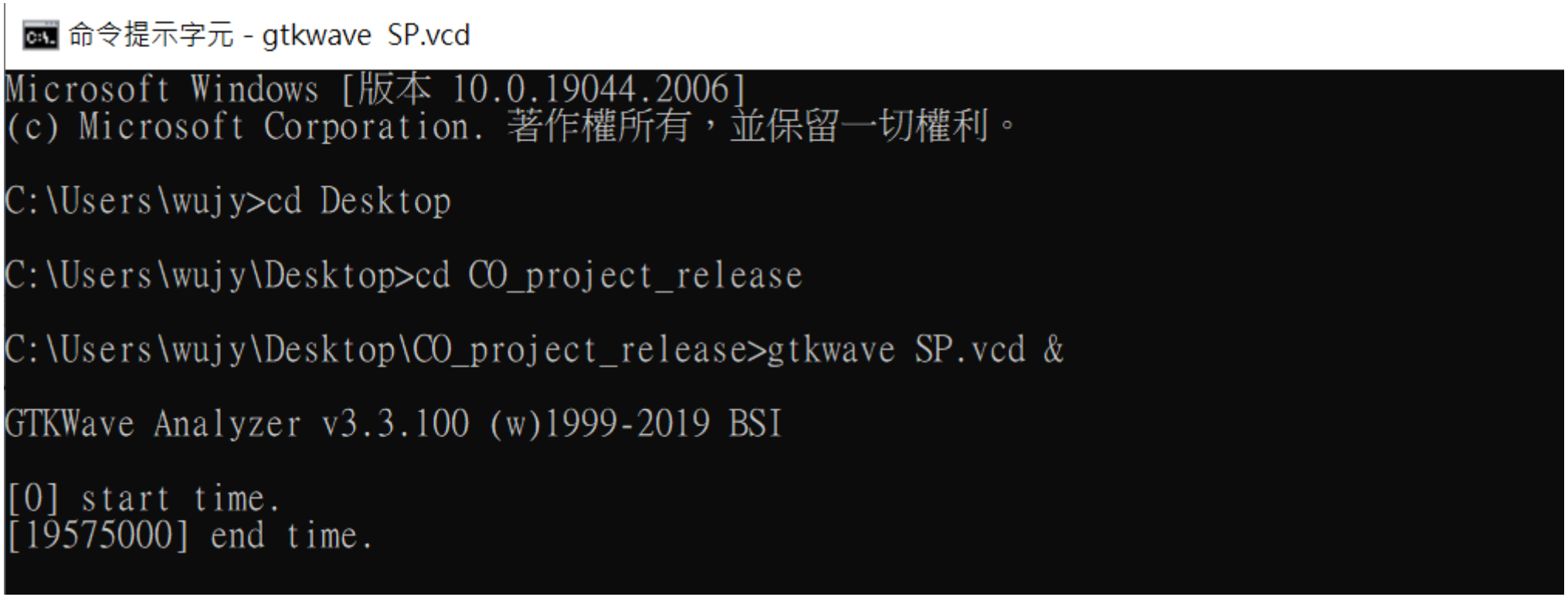
若有錯誤則需要波型輔助debug

- 執行指令完可以觀察測試檔案內有波型檔
- 非pipeline為SP.vcd
- pipeline為SP_p.vcd

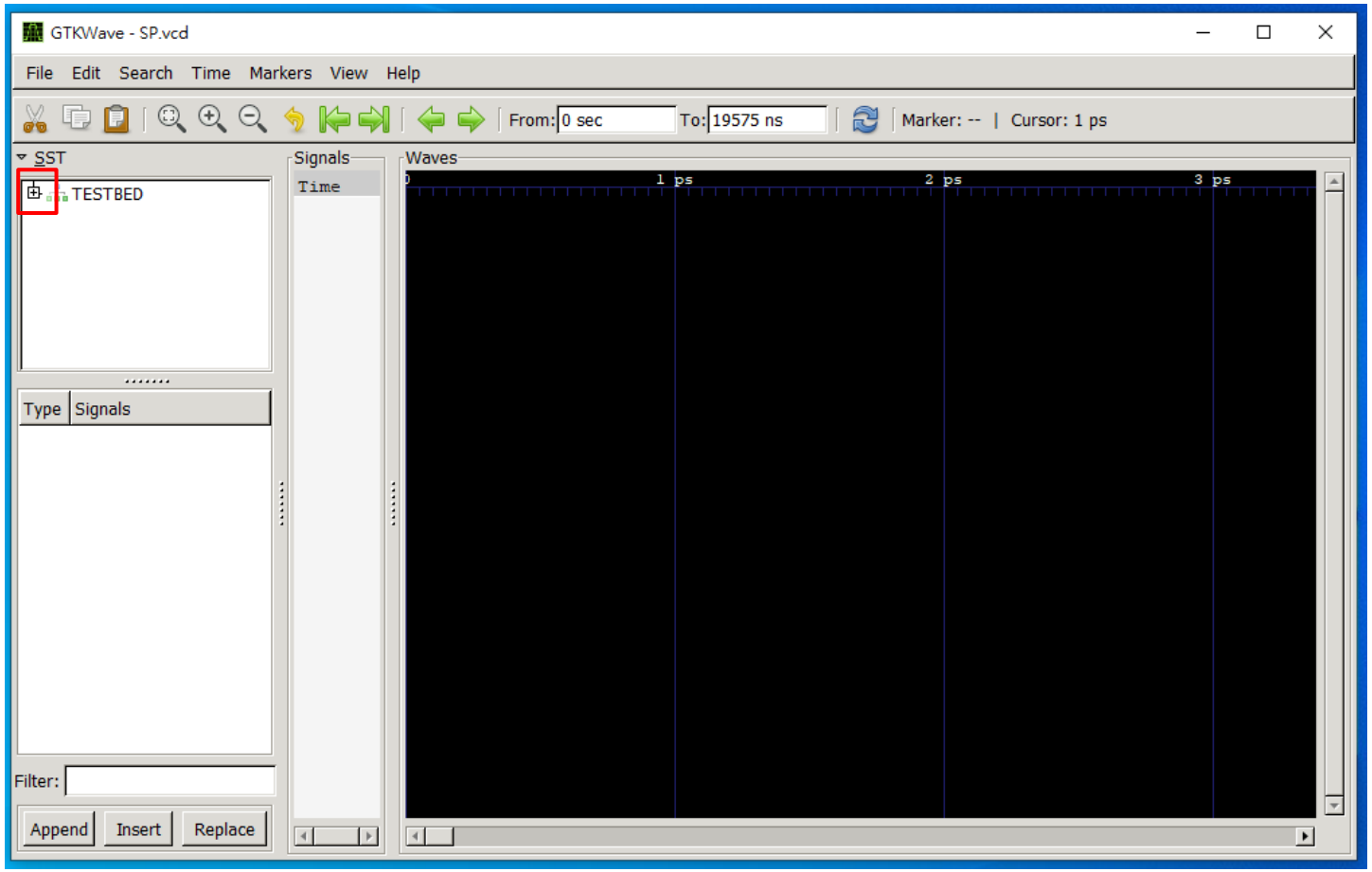


開啟另一個命令提示字元輸入指令打開波型

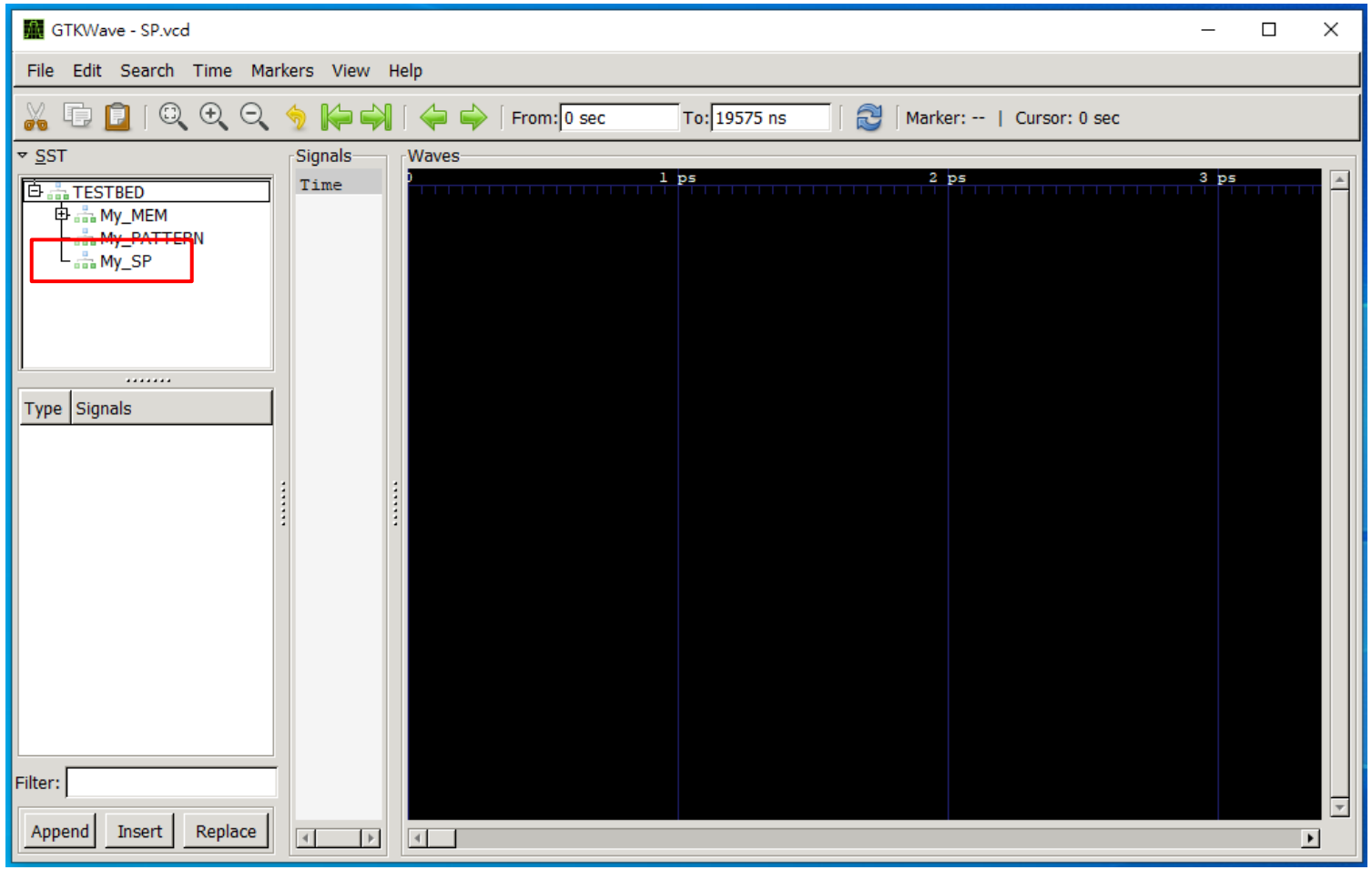
- 非pipeline輸入gtkwave SP.vcd &
- pipeline輸入gtkwave SP_p.vcd &



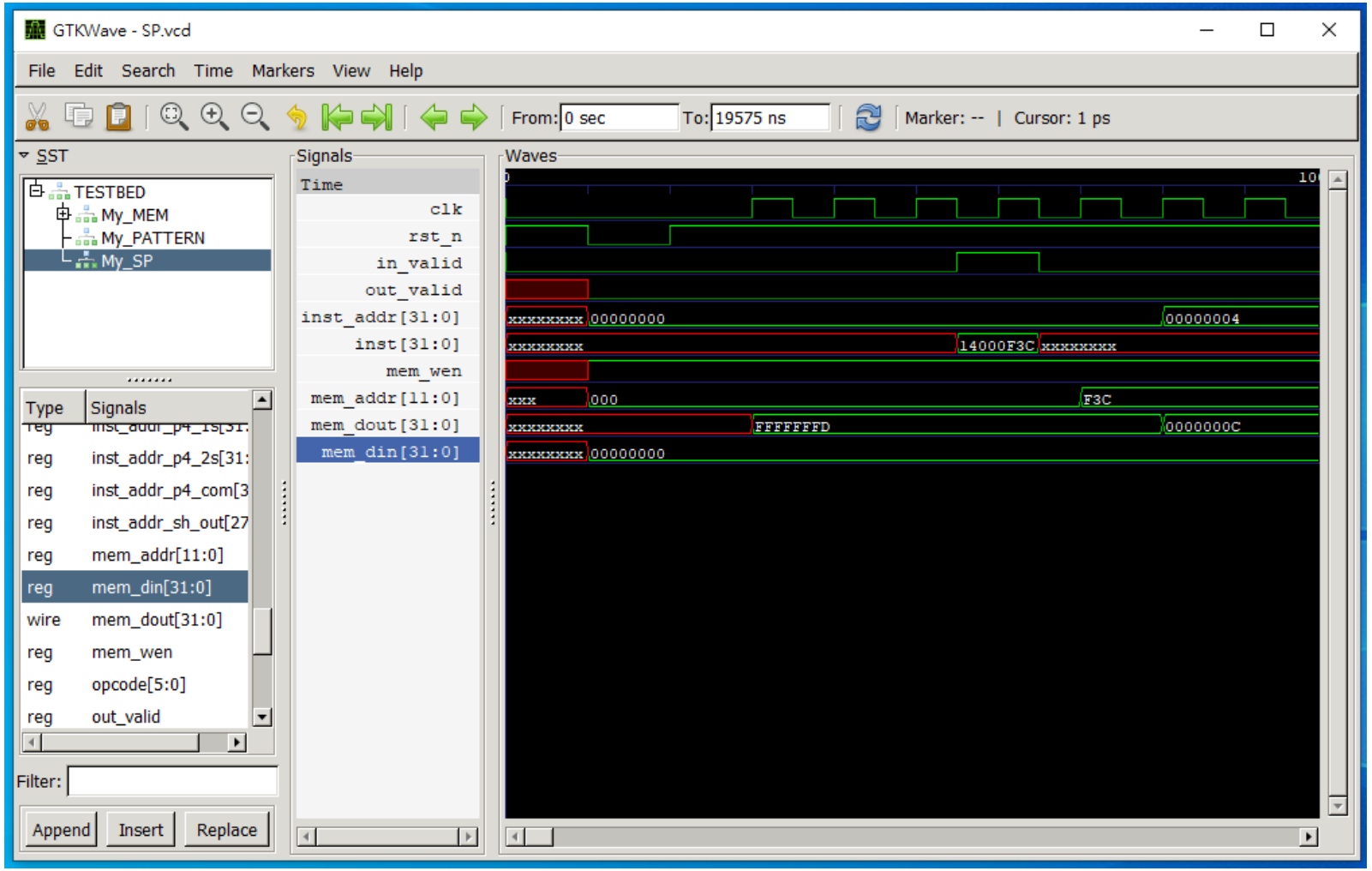
點開TESTBED左側+號



會出現TESTBED底下的module (design 檔為My_SP)



雙擊My_SP後，下方會出現訊號 (雙擊訊號即可叫出訊號)



對訊號點右鍵，在data format可選擇進制表示方式