8.3 Feature Description

8.3.1 Spectral Matching to Human Eye

OPT4001 spectral response closely matches that of the human eye. If the ambient light sensor measurement is used to help create a good human experience, or create optical conditions that are good for humans, then the sensor must measure the same spectrum of light that a human sees.

OPT4001 also has excellent infrared light (IR) rejection. This IR rejection is especially important because many real-world lighting sources have significant infrared content that humans do not see. If the sensor measures infrared light that the human eye does not see, then a true human experience is not accurately represented.

If the application demands hiding OPT4001 underneath dark window (such that the end-product user cannot see the sensor) the infrared rejection of the OPT4001 becomes significantly more important because many dark windows attenuate visible light but transmit infrared light. This attenuation of visible light and lack of attenuation of IR light amplifies the ratio of the infrared light to visible light that illuminates the sensor. Results can still be well matched to the human eye under this condition because of the high infrared rejection of the OPT4001.

8.3.2 Automatic Full-Scale Range Setting

The OPT4001 has an automatic full-scale range setting feature that eliminates the need to predict and set the best range for the device. In this mode, the device automatically selects the best full-scale range for varying lighting condition each measurement. The device has a high degree of result matching between the full-scale range settings. This matching eliminates the problem of varying results or the need for range-specific, user-calibrated gain factors when different full-scale ranges are chosen.

8.3.3 Output Register CRC and Counter

OPT4001 device features additional bits as part of the output register which helps in improving the reliability of light measurements for the application.

8.3.3.1 Output Sample Counter

The OPT4001 device features a register COUNTER as part of the output registers which increments for every successful measurement. This register can be read as part of the output registers which helps the application to keep track of measurements. The 4 bit counter starts at 0 on power-up and counts up to 15 after which the counter resets back to 0 and continues to count up, which is particularly helpful in situations like the following:

- Host or the controller needs consecutive measurements. Utilizing the COUNTER register allows the controller to compare samples and makes sure that the samples are in expected order without missing intermediate counter values.
- As a safety feature where when light level are not changing, the controller can make sure that the measurements from OPT4001 are not stuck by comparing values of register COUNTER between measurements. If the COUNTER values continue to change over samples, the device is updating the output register with the most recent measurement of light levels.

8.3.3.2 Output CRC

CRC register consists of Cyclic Redundancy Checker bits part of the output registers calculated within the OPT4001 device and updated on every measurement. This feature helps in detecting communication related bit errors during the output readout from the device. The calculation method for the CRC bits is shown in Figure 8-14, which can be independently verified in the controller or host firmware/software to validate if communication between the controller and the device was successful without bit errors during transmission.

8.3.4 Output Register FIFO

Output registers always contain the most recent light measurement. Along with output registers there are 3 more shadow registers which have the data from the previous 3 measurements. For every new measurement, the data on the 3 shadow registers are updated to contain the most recent measurements discarding the oldest measurement similar to a FIFO scheme. These shadow registers along with output registers act like a FIFO with a depth of 4. The INT pin (only on SOT-5X3 variant) can be configured as shown in the figure below to generate an interrupt every measurement or can be configured to generate an interrupt every 4 measurements using

the register INT_CFG. This way the controller reading data from OPT4001 device can minimize the number of interrupts by a factor of 4 and still get access to all the four measurements between the interrupts. By using the Burst Read Mode the output and FIFO registers can be read out with minimal I^2C clocks.

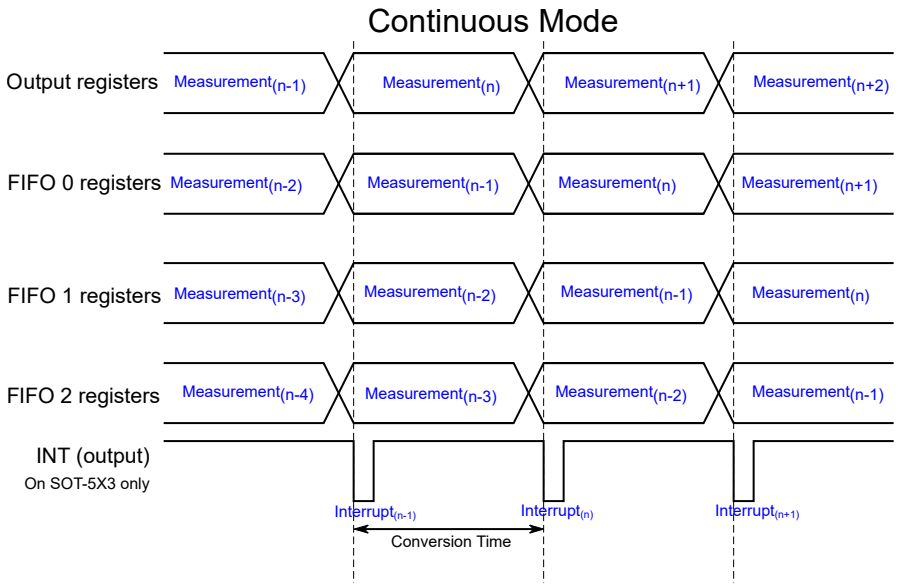

Figure 8-2. FIFO registers data movement

8.3.5 Threshold Detection

OPT4001 features a threshold detection logic which can be programmed to indicate and update register flags if measured light levels cross thresholds set by the user. There are independent low and high threshold target registers with independent flag registers to indicate the status of measured light level. Measured light level reaching below low threshold and above the high threshold are called faults. Users can program a fault count register, which counts consecutive number of faults before the flag registers are set. This is particularly useful in cases where the controller can read the flag register alone to get indication of measured light level not really needing to do the lux calculations. Details on the register and setting up the threshold is available in Section 8.3.5 and calculations for setting this up is available in *Threshold Detection Calculations*.

8.4 Device Functional Modes

8.4.1 Modes of Operation

The OPT4001 device has the following modes of operation:

- **Power-down mode:** This is power-down or standby mode where the device enters a low power state. There is no active light sensing or conversion in this mode. Device still responds to I^2C transactions which can be utilized to bring the device out of this mode. Register OPERATING_MODE is set to 0.
- **Continuous mode:** In this mode OPT4001 measures and updates the output registers continuously determined by the conversion time and generates hardware interrupt on pin INT (Only on SOT-5X3 package variant) for every successful conversion. TI recommends to configure the INT pin in output mode using the INT_DIR register. The device active circuits are continuously kept active to minimize the interval between measurements. Register OPERATING_MODE is set to 3.
- **One shot mode of operation:** There are several ways in which OPT4001 can be used in one shot mode of operation with one common theme where OPT4001 stays in standby mode and a conversion is triggered either by a register write to configuration register or hardware interrupt on the INT pin.

  There are two types of one shot modes.
  - **Force auto-range one shot mode:** Every one shot trigger forces a full reset on auto-ranging control logic and a fresh auto-range detection is initiated ignoring the previous measurements. This is particularly

useful in situations where lighting conditions are expected to change a lot and one shot trigger frequency is not very often. There is small penalty on conversion time due for the auto-ranging logic to recover from reset state. The full reset cycle on the auto-ranging control logic takes around 500 µs which needs to be accounted for between measurements when this mode is used. Register OPERATING_MODE is set to 1.

– **Regular auto-range one shot mode:** Auto-range selection logic utilizes the information from the previous measurements to decide the range for the current trigger. This mode is recommended only when the device needs time synchronized measurements with frequent triggers from the controller. In other words, this mode can be used as an alternative to continuous mode the key difference being that the interval between measurements is determined by the one shot triggers. Register OPERATING_MODE is set to 2.

One Shot can be triggered by the following

– **Hardware trigger (Only on SOT-5X3 variant):**INT pin can be configured to be an input to trigger a measurement setting INT_DIR register to 0. Since INT pin is used as input, there is no hardware interrupt to indicate completion of measurement. The controller needs to keep time from the trigger mechanism and read out output registers.
– **Register trigger:** An I^2C write to the OPERATING_MODE register triggers a measurement (value of 1 or 2). The register value is reset after next successful measurement. INT pin can be configured to indicate measurement completion to read out output registers setting the INT_DIR register to 1.

TI highly recommends to set the interval between subsequent triggers to account for all the aspects involved in the trigger mechanism like the I^2C transaction time, device wake-up time, auto-range time (if used) and device conversion time. If a conversion trigger is received before the completion of current measurement, the device simply ignores the new request until the previous conversion is completed.

Since the device enters standby after each one shot trigger, measurement interval in the one shot trigger mechanism needs to account for additional time T_{ss} as specified in the specification table for the circuits to recover from standby state. However setting the quick wake up register QWAKE eliminates the need for this additional T_{ss} at the cost of not powering down the active circuit with device not entering the standby mode between triggers.

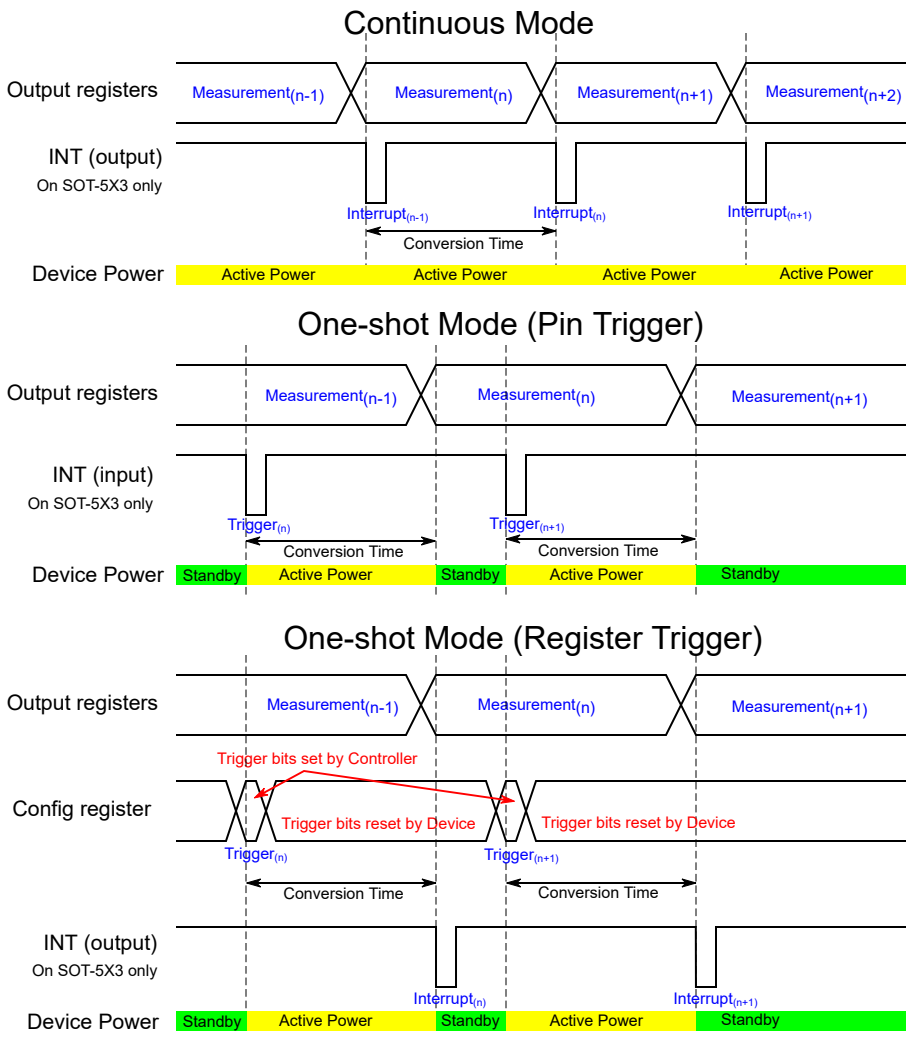

Figure 8-3. Timing Diagrams for different Operating modes

8.4.2 Interrupt Modes of Operation

The device has an interrupt reporting system that allows the processor connected to the I^2C bus to go to sleep, or otherwise ignore the device results, until a user-defined event occurs that requires possible action. Alternatively, this same mechanism can also be used with any system that can take advantage of a single digital signal that indicates whether the light is above or below levels of interest.

The INT pin has an open-drain output, which requires the use of a pull-up resistor. This open-drain output allows multiple devices with open-drain INT pins to be connected to the same line, thus creating a logical *NOR* or *AND* function between the devices. The polarity of the INT pin can be controlled by the INT_POL.

There are two major types of interrupt reporting mechanism modes: latched window comparison mode and transparent hysteresis comparison mode. The configuration register LATCH controls which of these two modes is used. Table 8-1 and Figure 8-4 summarize the function of these two modes. Additionally, the INT pin can either be used to indicate a fault in one of these modes (INT_CFG=0) or to indicate a conversion completion (INT_CFG >0). This is shown in Table 8-2.

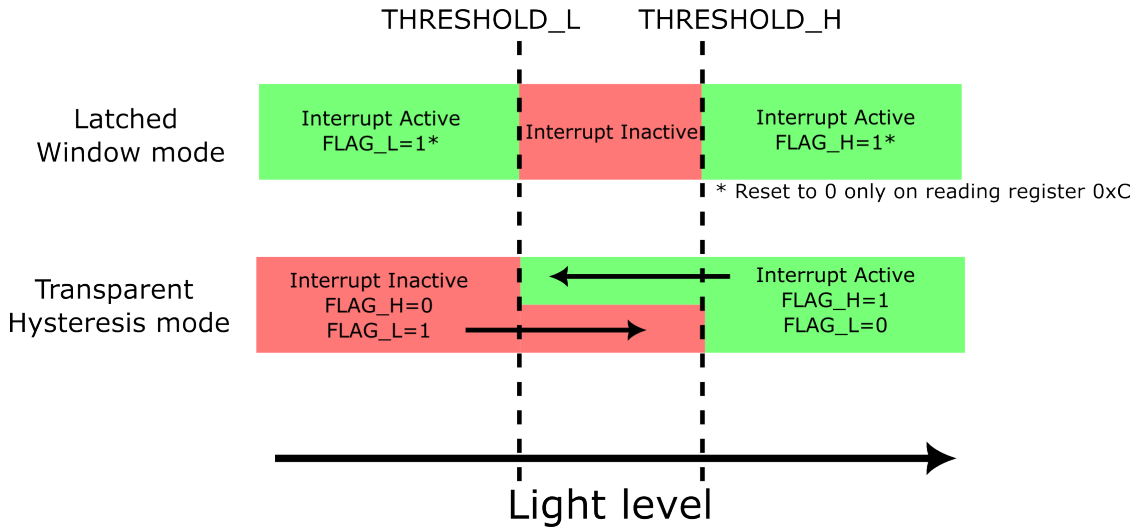

Figure 8-4. Interrupt Pin Status (for INT_CFG=0 setting) and Register Flag Behavior

Table 8-1. Interrupt Pin Status (for INT_CFG=0 setting) and Register Flag Behavior

LATCH Setting	INT Pin State (when INT_CFG=0)	FLAG_H Value	FLAG_L Value	Latching Behavior
0: Transparent hysteresis mode	INT pin indicates if measurement is above (INT active) or below (INT inactive) the threshold. If measurement is between the high and low threshold values then the previous INT value is maintained. This prevents the INT pin from repeated toggling when the measurement values are close to the threshold.	0: If measurement is below the low limit 1: If measurement is above the high limit If measurement is between high and low limits previous value is maintained	0: If measurement is above the high limit 1: If measurement is below the low limit If measurement is between high and low limits previous value is maintained	Not latching: Values are updated after each conversion
1: Latched window mode	INT pin becomes active if the measurement is outside the window (above high threshold or below the low threshold). The INT pin does not reset and return to the inactive state until register 0xC is read.	1: If measurement is above the high limit	1: If measurement is below the low limit	Latching: INT pin, FLAG_H and FLAG_L values do not reset until the register 0x0C is read.

The THRESHOLD_H, THRESHOLD_L, LATCH and FAULT_COUNT registers control the interrupt behavior. The LATCH field setting allows a choice between the latched window mode and transparent hysteresis mode as shown in the table. Interrupt reporting can be observed on INT pin (for SOT-5X3 variant only), the FLAG_H, and the FLAG_L registers.

Results from comparing the current sensor measurements with THRESHOLD_H and THRESHOLD_L registers are referred to as *fault events*. The calculations to set these registers can be found in Threshold Detection Calculations. The FAULT_COUNT register dictates the number of continuous *fault events* required to trigger an interrupt event and subsequently change the state of the interrupt reporting mechanisms. For example, with a FAULT_COUNT value of 2 corresponding to 4 fault counts, the INT pin (for SOT-5X3 variant only), FLAG_H and FLAG_L states shown in the table are not realized unless 4 consecutive measurements are taken that satisfy the fault condition.

INT pin function (for SOT-5X3 variant only) listed in Table 8-1is valid only when INT_CFG=0. The INT pin function can be changed to indicate an end of conversion or FIFO full state as shown in Table 8-2. The FLAG_H

and FLAG_L registers continue to behave as listed in Table 8-1 even while INT_CFG>0. The polarity of the INT pin is controlled by the INT_POL register.

Table 8-2. INT_CFG Setting and Resulting INT Pin Behavior

INT_CFG Setting	INT Pin Function
0	As per Table 8-1
1	INT pin asserted with 1us pulse width after every conversion
3	INT pin asserted with 1us pulse width every 4 conversions to indicate the FIFO is full

8.4.3 Light Range Selection

The OPT4001 has an automatic full-scale-range setting mode that eliminates the need for a user to predict and set the best range for the device. This mode is entered when register RANGE is set to 0xC. The device determines the appropriate full-scale range to take the measurement based on a combination of current lighting conditions and the previous measurement.

If a measurement is towards the low side of full-scale, then the full-scale range is decreased by one or two settings for the next measurement. If a measurement is towards the upper side of full-scale, the full-scale range is increased by one setting for the next measurement.

If the measurement exceeds the full-scale range, resulting from a fast increasing optical transient event, then the current measurement is aborted. This invalid measurement is not reported. If the scale is not at the maximum, then the device increases the scale by one step and a new measurement is retaken with that scale. Therefore, during a fast increasing optical transient in this mode, a measurement can possibly take longer to complete and report than indicated by the configuration register CONVERSION_TIME.

TI highly recommends to use this feature, since the device selects the best range setting based on lighting condition. However, there is an option to manually set the range. Setting the range manually turns off the automatic full-scale selection logic and the device operates for a particular range setting.

Table 8-3. Range Selection Table

RANGE register setting	Typical Full-scale Light level for PicoStar™ variant	Typical Full-scale Light level for SOT-5X3 variant
0	328 lux	459 lux
1	655 lux	918 lux
2	1311 lux	1835 lux
3	2621 lux	3670 lux
4	5243 lux	7340 lux
5	10486 lux	14680 lux
6	20972 lux	29360 lux
7	41943 lux	58720 lux
8	83886 lux	117441 lux
12	Determined by automatic full-scale range logic	

8.4.4 Selecting Conversion Time

The OPT4001 device offers several conversion times to select from. Conversion Time is defined as how much time for one measurement to complete and update the results in output register from the time measurement is initiated. Measurement initiation is determined by the mode of operation as specified in Modes of Operation.

Table 8-4. Conversion Time Selection

CONVERSION_TIME register	Typical Conversion Time
0	0.6 ms
1	1 ms
2	1.8 ms
3	3.4 ms
4	6.5 ms
5	12.7 ms
6	25 ms
7	50 ms
8	100 ms
9	200 ms
10	400 ms
11	800 ms

8.4.5 Light Measurement in Lux

The OPT4001 device measures light and updates output registers with proportional ADC codes. Output of the device is represented by two parts (i) 4 bits of EXPONENT and (ii) 20 bits of MANTISSA. This arrangement of binary logarithmic full-scale range with linear representation with in a range helps in covering a large dynamic range of measurements. MANTISSA represents the linear ADC codes proportional to the measured light within a given full-scale range and the EXPONENT represents the current-full scale range selected. The selected range can be automatically determined by the auto-range selection logic or manually selected as per Table 8-3.

Lux level can be determined using the following equations:

$$MANTISSA=(RESULT\_MSB<<8) + RESULT\_LSB \quad (1)$$

or

$$MANTISSA=(RESULT\_MSB \times 2^8) + RESULT\_LSB \quad (2)$$

where RESULT_MSB, RESULT_LSB and EXPONENT are parts of the output register

RESULT_MSB register carries the most significant 12 bits of the MANTISSA and RESULT_LSB register carries the least significant 8 bits of the MANTISSA. MANTISSA is then computed using the above equations to get the 20 bit number. EXPONENT is directly read from the register which is 4 bits.

Once the EXPONENT and MANTISSA portions are calculated the linearized ADC_CODES is calculated using the following equation:

ADC_CODES = (MANTISSA<<E) (3)

or

ADC_CODES = (MANTISSA x 2^E) (4)

With maximum value for register E being 8 ADC_CODES is effectively a 28 bit number. The semi-logarithmic numbers have been converted to a linear ADC_CODES representation, which is simple to convert to lux given by the following formula

lux = ADC_CODES x 312.5E-6 for the PicoStar™ variant (5)

lux = ADC_CODES x 437.5E-6 for the SOT-5X3 variant (6)

The MANTISSA and ADC_CODES are large numbers with 20 and 28 bits required to represent them. While developing firmware or software for these calculations, allocating appropriate data types to prevent data overflow is important. Some explicit typecasting to a larger data type such as 32 bit representation before left shift operation (<<) operations is recommended.

Threshold Detection Calculations

Threshold result registers THRESHOLD_H_RESULT and THRESHOLD_L_RESULT are 12 bit, while threshold exponent registers THRESHOLD_H_EXPONENT and THRESHOLD_L_EXPONENT are 4 bits. Since threshold is compared at linear ADC_CODES, the threshold registers are padded with zeros internally as shown to compare with the ADC_CODES

ADC_CODES_TH = THRESHOLD_H_RESULT << (8 + THRESHOLD_H_EXPONENT) (7)

or

ADC_CODES_TH = THRESHOLD_H_RESULT x 2^(8 + THRESHOLD_H_EXPONENT) (8)

and

ADC_CODES_TL = THRESHOLD_L_RESULT << (8 + THRESHOLD_L_EXPONENT) (9)

or

ADC_CODES_TL=THRESHOLD_L_RESULT x 2^(8 + THRESHOLD_L_EXPONENT) (10)

Threshold are then compared as shown to detect *fault events.*

If ADC_CODES < ADC_CODES_TL a *fault low* is detected (11)

and

If ADC_CODES > ADC_CODES_TH a *fault high* is detected (12)

Based on the FAULT_COUNT register setting, with consecutive *fault high* or *fault low* events, respective FLAG_H and FLAG_L registers are set, more details of which can be found in Section 8.4.2. Understanding the relation between THRESHOLD_H_EXPONENT, THRESHOLD_H_RESULT, THRESHOLD_L_EXPONENT, THRESHOLD_L_RESULT and the output registers is important to be able to set appropriate threshold based on application needs.

8.4.6 Light Resolution

The OPT4001 device's effective resolution is dependent on both the conversion time setting and the full-scale light range. Although the LSB resolution of the linear ADC_CODES doesn't change, the effective or useful resolution of the device is dependent on the conversion time setting and the full-scale range as per the table below. In conversion times where the effective resolution is lower, the LSBs are padded with 0.

Table 8-5. Resolution Table for the Picostar™ Variant

CONVERSION_TIME register	Conversion Time	MANTESSA effective bits	EXPONENT	0	1	2	3	4	5	6	7	8
			Full-scale lux	328	655	1310	2621	5243	10486	20972	41943	83886
				Effective Resolution in lux								
0	600us	9		640 m	1.28	2.56	5.12	10.24	20.48	40.96	81.92	163.84
1	1 ms	10		320 m	640 m	1.28	2.56	5.12	10.24	20.48	40.96	81.92
2	1.8 ms	11		160 m	320 m	640 m	1.28	2.56	5.12	10.24	20.48	40.98
3	3.4 ms	12		80 m	160 m	320 m	640 m	1.28	2.56	5.12	10.24	20.48
4	6.5 ms	13		40 m	80 m	160 m	320 m	640 m	1.28	2.56	5.12	10.24
5	12.7 ms	14		20 m	40 m	80 m	160 m	320 m	640 m	1.28	2.56	5.12
6	25 ms	15		10 m	20 m	40 m	80 m	160 m	320 m	640 m	1.28	2.56
7	50 ms	16		5 m	10 m	20 m	40 m	80 m	160 m	320 m	640 m	1.28
8	100 ms	17		2.5 m	5 m	10 m	20 m	40 m	80 m	160 m	320 m	640 m
9	200 ms	18		1.25 m	2.5 m	5 m	10 m	20 m	40 m	80 m	160 m	320 m
10	400 ms	19		0.625 m	1.25 m	2.5 m	5 m	10 m	20 m	40 m	80 m	160 m
11	800 ms	20		0.3125 m	0.625 m	1.25 m	2.5 m	5 m	10 m	20 m	40 m	80 m

Table 8-6. Resolution Table for the SOT-5X3 variant

CONVERSION_TIME register	Conversion Time	MANTESSA effective bits	EXPONENT	0	1	2	3	4	5	6	7	8
			Full-scale lux	459	918	1835	3670	7340	14680	29360	58720	117441
				Effective Resolution in lux								
0	600 us	9		896 m	1.792	3.584	7.168	14.336	28.672	47.344	114.688	229.376
1	1 ms	10		448 m	896 m	1.792	3.584	7.168	14.336	28.672	47.344	114.688
2	1.8 ms	11		224 m	448 m	896 m	1.792	3.584	7.168	14.336	28.672	47.344
3	3.4 ms	12		112 m	224 m	448 m	896 m	1.792	3.584	7.168	14.336	28.672
4	6.5 ms	13		56 m	112 m	224 m	448 m	896 m	1.792	3.584	7.168	14.336
5	12.7 ms	14		28 m	56 m	112 m	224 m	448 m	896 m	1.792	3.584	7.168
6	25 ms	15		14 m	28 m	56 m	112 m	224 m	448 m	896 m	1.792	3.584
7	50 ms	16		7 m	14 m	28 m	56 m	112 m	224 m	448 m	896 m	1.792
8	100 ms	17		3.5 m	7 m	14 m	28 m	56 m	112 m	224 m	448 m	896 m
9	200 ms	18		1.75 m	3.5m	7 m	14 m	28 m	56 m	112 m	224 m	448 m
10	400 ms	19		0.875 m	1.75m	3.5 m	7 m	14 m	28 m	56 m	112 m	224 m
11	800 ms	20		0.4375 m	0.875 m	1.75 m	3.5 m	7 m	14 m	28 m	56 m	112 m

8.5 Programming

The OP4001 supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). Fast and standard modes are described as the default protocol, referred to as *F/S*. High-speed mode is described in the *High-Speed I2C Mode* section.

8.5.1 I²C Bus Overview

The OPT4001 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another. The I²C interface is used throughout this document as the primary example with the SMBus protocol specified only when a difference between the two protocols is discussed.

The device is connected to the bus with two pins: an SCL clock input pin and an SDA open-drain bidirectional data pin. The bus must have a controller device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions. To address a specific device, the controller initiates a start condition by pulling the data signal line (SDA) from a high logic level to a low logic level while SCL is high. All targets on the bus shift in the target address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit by pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition. When all data are transferred, the controller generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The device includes a 28-ms timeout on the I²C interface to prevent locking up the bus. If the SCL line is held low for this duration of time, the bus state machine is reset.

8.5.1.1 Serial Bus Address

To communicate with the OPT4001, the controller must first initiate an I²C start command. Then, the controller must address target devices via a target address byte. The target address byte consists of a seven bit address and a direction bit that indicates whether the action is to be a read or write operation.

For the SOT 5X3 variant, four I²C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. Table below summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

ADDR PIN CONNECTION	DEVICE I²C ADDRESS
GND	1000100
VDD	1000101
SDA	1000110
SCL	1000101

In case of the PicoStar™ variant there is no target address selection capability and the device address is hard coded to 1000101b (0x45).

8.5.1.2 Serial Interface

The OPT4001 operates as a target device on both the I²C bus and SMBus. Connections to the bus are made via the SCL clock input line and the SDA open-drain I/O line. The device supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). All data bytes are transmitted most-significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. See the *Section 9.2.1* for further details of the I²C bus noise immunity.

8.5.2 Writing and Reading

Accessing a specific register on the OPT4001 is accomplished by writing the appropriate register address during the I²C transaction sequence. Refer to Section 8.6 for a complete list of registers and their corresponding

register addresses. The value for the register address (as shown in Figure 8-5) is the first byte transferred after the target address byte with the R/W bit low.

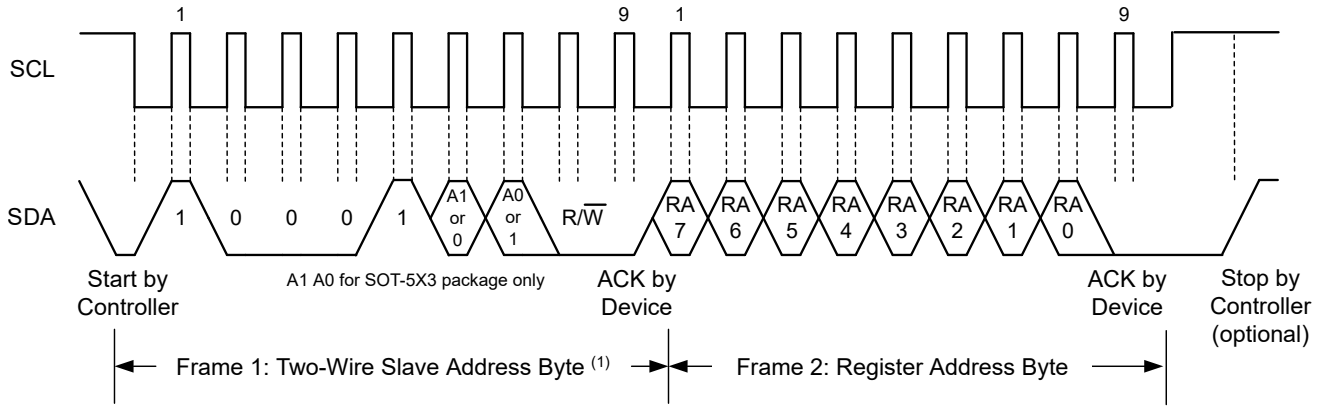

Figure 8-5. Setting the I²C Register Address

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register that data are to be written to. The next two bytes are written to the register addressed by the register address. The device acknowledges receipt of each data byte. The controller can terminate the data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register address by a write operation determines which register is read during a read operation. To change the register address for a read operation, a new partial I²C write transaction must be initiated. This partial write is accomplished by issuing a target address byte with the R/W bit low, followed by the register address byte and a stop command. The controller then generates a start condition and sends the target address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the terget and is the most significant byte of the register indicated by the register address. This byte is followed by an acknowledge from the controller; then the target transmits the least significant byte. The controller acknowledges receipt of the data byte. The controller can terminate the data transfer by generating a not-acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register address bytes is not necessary; the device retains the register address until that number is changed by the next write operation.