Proposal & Plan:
IC Packaging

James Lin

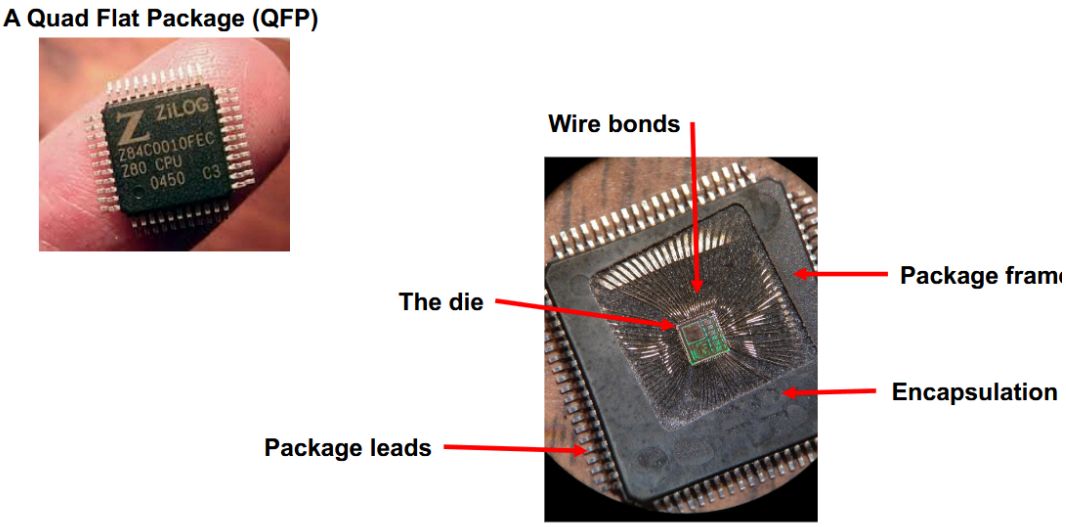
Background

Hacker Fab currently utilizes the probing station available at CMU for electrical characterization of its ICs, but these machines have proven difficult to both access and operate. Consequently, the team is developing a DIY probing station at a much lower price in hopes of bringing this capability in house. However, as our ICs eventually get more complex and start to increase in IO counts, characterization with a probing station will also require more time and effort.

Typical semiconductor packaging process goes through the following steps:

- Wafer-level probing for known good die (KGD)
- Wafer back grinding
- Wafer dicing
- Die pick & sort
- Die attach to package
- Wire bonding or flip chip bonding
- Package encapsulation
- Packaged die test
- Final assembly onto printed circuit board (PCB)

(Hacker Fab: Packaging, Robert M. Radway, 2024)



(also from Radway's presentation)

Since Hacker Fab is not geared towards high throughput and focuses on ease of manufacturing and accessibility, this process flow will likely be shortened to the following:

- Wafer-level probing for known good die (KGD) - optional
  - Depends on availability of probe station
- Wafer dicing
  - Can be easily done in house
- Die attach to package
  - Required to hold IC mechanically in package
- Wire bonding
  - We will be using wire bonders in the MEMs lab at CMU
- Package encapsulation
  - Required to protect IC from the environment
- Packaged die test + Final assembly onto PCB
  - Ultimate goal of the project to test IC on a PCB

As part of the metrology team, I will be working on a process to package our ICs so that it can eventually interface with an Analog Discovery 3 via a PCB, thus not only allowing us to characterize ICs with large IO counts quickly, but also allowing us to better test the entire IC's performance in the future. This capability will allow the team to further vertically expand in the IC manufacturing process.

IC Packaging Process

Technical requirements

- Lead Frame and IC Pads:
  - Both the lead frame and IC pads must be compatible with the wire bonding process and materials available in the MEMs lab
  - Lead frame and its leads should be mechanically strong enough for normal handling and installation, as well as compatible with soldering
  - IC pads needs to be compatible with Hacker Fab manufacturing and design capabilities
- Wire bonding:
  - Wires used should be compatible for bonding with substrate material
- Parasitic resistance:
  - All conducting materials should not introduce high parasitic resistance in order to preserve granularity of characterization data
- Encapsulation:
  - Be mechanically strong enough to withstand handling and high temperatures from both IC power dissipation and soldering
  - Electrically insulate the IC the environment without unplanned conduction paths
- Coefficient of Thermal Expansion (CTE):
  - All materials should have closely matched CTEs to the IC substrate to prevent mechanical failure from thermal stresses
- Package selection:
  - Spacing and dimension of leads should closely match existing packages to successfully mount on standard PCB boards or bread boards
- Minimize cost where possible

The process and design of the IC package will be developed from the ground up, which would require extensive research on industry practices and literature.

Major deliverables

- CAD of encapsulation and lead frame
- Full manufacturing process flow
    - Tools, materials, parameters
- Test and validate wire bonding recipes done in the MEMs lab
- Prototype with single transistor IC
- Prototype with multi-transistor ICs
- Stress testing package for thermal and moisture resistance
- Integration with process and metrology test plans

Things to consider

- Planned IC dimensions for current capabilities
    - Confirmed 1 cm x 1 cm
    - This may necessitate a costume package inspired by industry
- Lead frame manufacturing method
    - Very few sources are easily available for purchase
    - Possibility for in house etching, but stepper field size is not large enough for entire lead frame
    - Cannot do with TechSpark laser cutter bc reflective metal
        - Online sources says fiber laser or oxygen-high powered laser are preferred but don't know if available on campus
    - PCB mill is likely since people have used it to do lead frames before
        - Waiting on Joel to check
- Encapsulation manufacturing
    - May need very specialized epoxy due to CTE concerns
    - Might explore possibility of 3D printing, but has resolution and thermal concerns
    - Resin printing is an option
        - Joel can set up his printer in office
        - Ideate might also let us do it
- Adhesives:
    - Might also be specialized and hard to source depending on requirement
- Logistics with team:
    - Need to lock down specific materials and dimensions on IC side early on to begin testing process for wire bonding and address other design requirements
    - Week 4-6 EDA will be planning and finalizing test plan
        - Talk to Gongwei
    - Need to figure out who is making multi-transistor IC and what circuit/IO it will have
- Wire bonding:
    - Want to test with pad material and stack that matches final chip
        - Pad peel-off is current biggest concern
    - Can probably start rudimentary tests soon by just making a grid on silicon with thermal evaporated Al

Timeline

Deadline	Deliverable
1/28/25	Get familiarized with wire bonder in MEMS Lab
1/31/24	Pick package to reference for design
2/7/25	Finalize pad dimensions with EDA team
2/8/25	Wire bonding test with Al on Si
2/13/25	Lead frame and encapsulation design
2/16/25	Presentation 1
2/19/25	Lead frame and encapsulation manufactured
2/20/25	Work with EDA to finalize test plan
2/23/25	1 transistor chip manufactured
2/28/25	1 transistor package assembled
3/7/25	Testing with 1 transistor package
3/9/25	Lead frame and encapsulation design
3/14/25	Lead frame and encapsulation manufactured
3/26/25	Presentation 2
TBD	Multi-transistor IC manufactured
TBD	Multi-transistor IC assembled
TBD	Multi-transistor IC tested
4/25/25	Documentation
4/27/25	Final Presentation