Fabrication and Testing of Enhancement Load NMOS Inverter Based on HackFab’s Standard Process Flow

1. Introduction

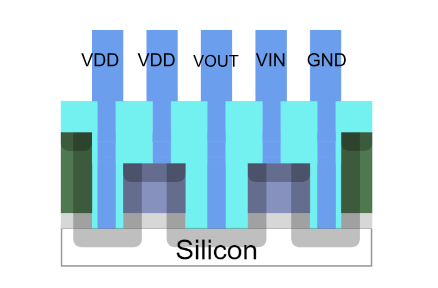
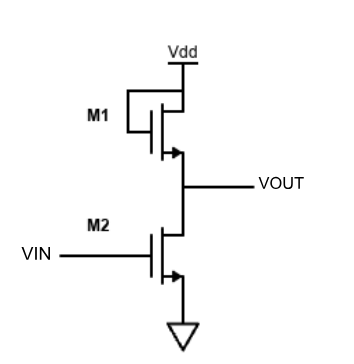
NOT gate or inverter outputs the opposite of its input as shown in Table 1 is a basic but crucial part of the digital logic circuit. An NMOS logic inverter normally consists of two parts, a resistive load connected between the supply voltage (VDD) and the output as the “pull up” part and a switching transistor as the “pull down” part. To save device area and fabrication cost, instead of using resistors for the load, an active load such as an enhancement load transistor is used in the design as shown in Figure 1 (left). Enhancement load means a transistor’s gate and the drain are both connected to the supply voltage and make the transistor always in the saturation region. However, this causes there will be a constant current going through the transistors even if it is not performing which makes NMOS logic technology have higher power consumption and eventually be replaced by CMOS technology.

|  |  |
| --- | --- |
| Input | Output |
| 0 | 1 |
| 1 | 0 |

Table 1. Inverter Truthtable

1. Theory

As shown in Figure 1 (left), the enhancement load transistor is M1 and the functioning switching transistor is M2. For M1 since the drain and the gate are both connected to the supply voltage, always holds, making it stay “ON” at the saturation region. When the input of the M2 transistor is low, . The transistor is at the cut-off region and its effective resistance is very high. Therefore, when the input is low, the output of the inverter is high. As input voltage increases, M1’s increase. When , the transistor is also turned “ON”, the voltage between the drain and source drops. Therefore, when input is high the output of the inverter is low.



**M2**

**M1**

Figure 1. (a) The Schematic of the Enhancement Load NMOS Inverter (left)

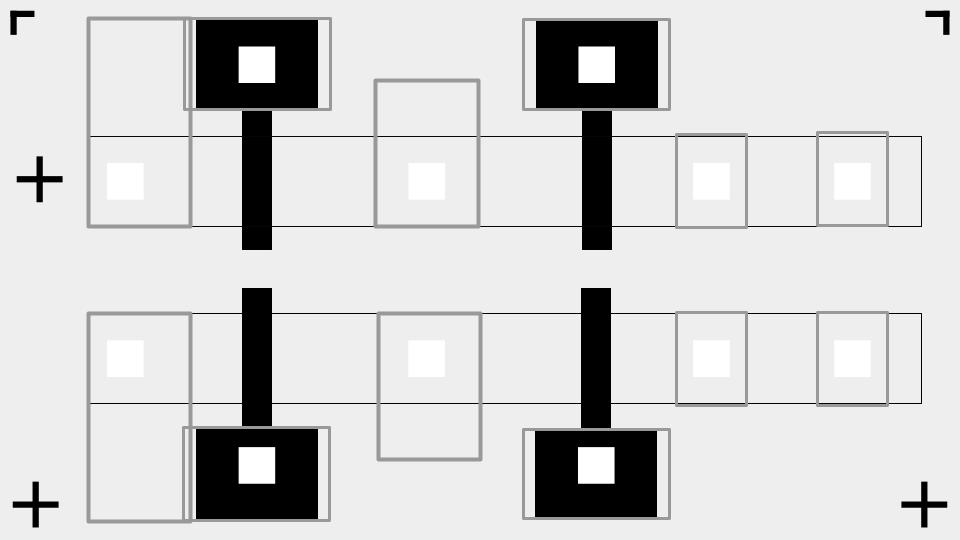
(b) Cross-section view of Enhancement Load NMOS Inverter (right)

1. Fabrication

3.1 Mask Design

In terms of design, since the source terminal of M1 and the drain terminal of M2 are connected, to make the device more compact, we can design the layout of the inverter to make these two transistors share the source and drain region. The cross-section view of the enhancement load NMOS inverter is shown in Figure 1 (right).

The mask used to fabricate the inverter contains 2 devices as shown in Figure 2. The load transistor M1 is on the left and the switching transistor M2 is on the right. The gate and drain of M1 are connected by a L-shaped aluminum contact. The extra contact pad was added on the right of the ground contact pads to test if the doped active area is working properly. As for the feature size of the patterns, 0.1 inches marked on the Google Slide is scaled to 10 um for the actual pattern.



**GND**

**Vout**

**VDD**

**Vin**

Figure 2. Top View of All Inverter Masks Overlapped

Based on the standard HackerFab process, we need to pattern the device four times: gate, active area, via, and contact pad. The mask for each patterning process and the actual inspection images during the fabrication process are shown below.

3.1.1 Gate Mask

This mask defines the gate regions of the transistors and leaves space for the contact pads for the gate. This mask is also commonly used for later patterning steps in the fabrication process to align the pattern.

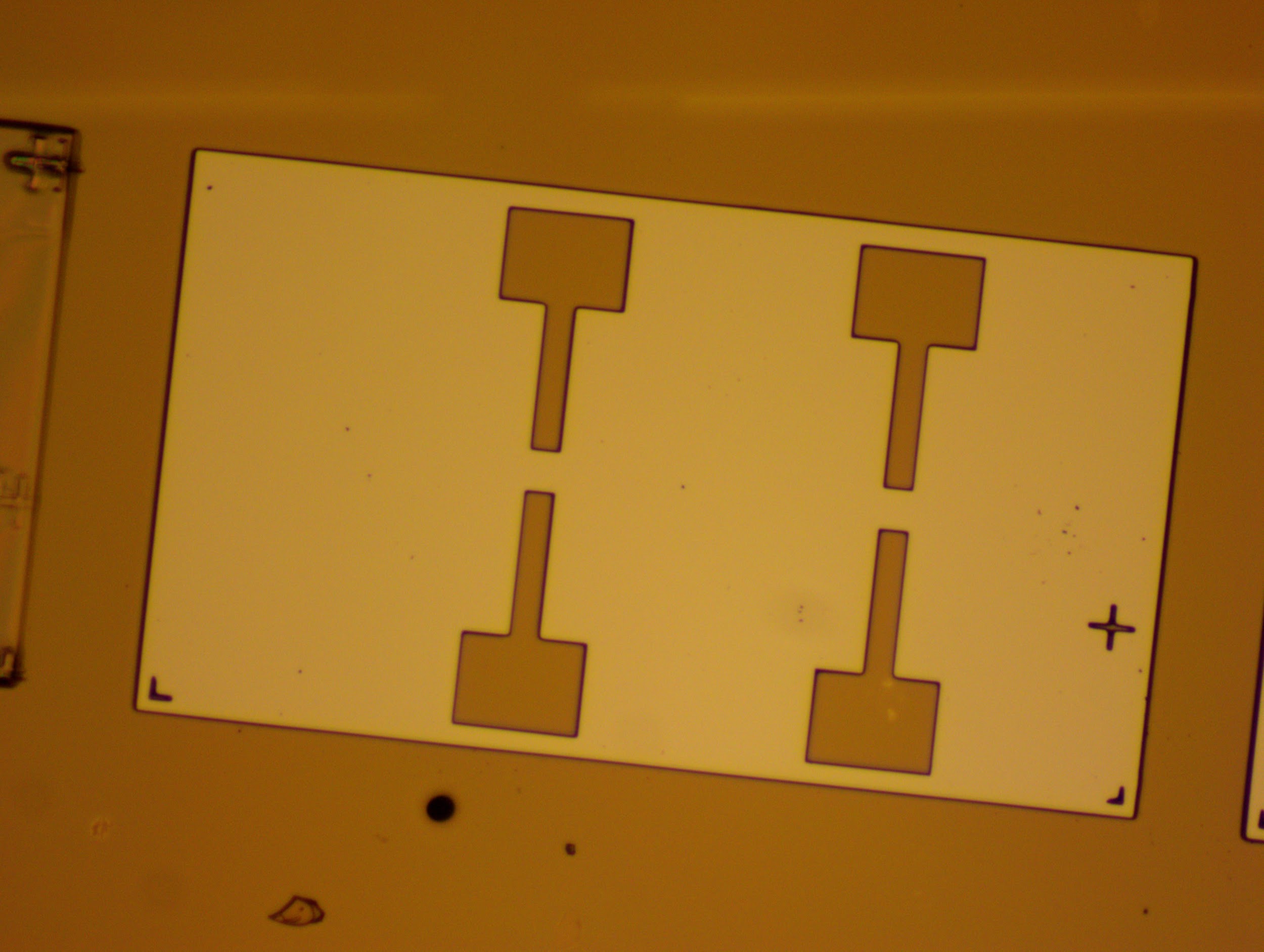
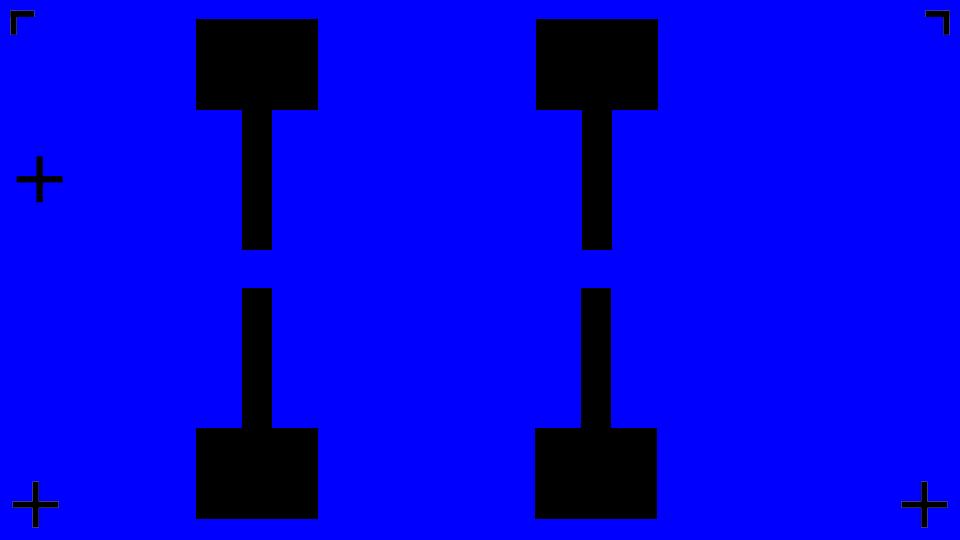


Figure 3. (a) Gate Mask of the NMOS Inverter (left)

(b) Inspection Image After Gate Patterning (right)

3.1.2 Active Area Mask

This mask defines the active area of the transistors which will be doped to form the drain and source region of the transistors.

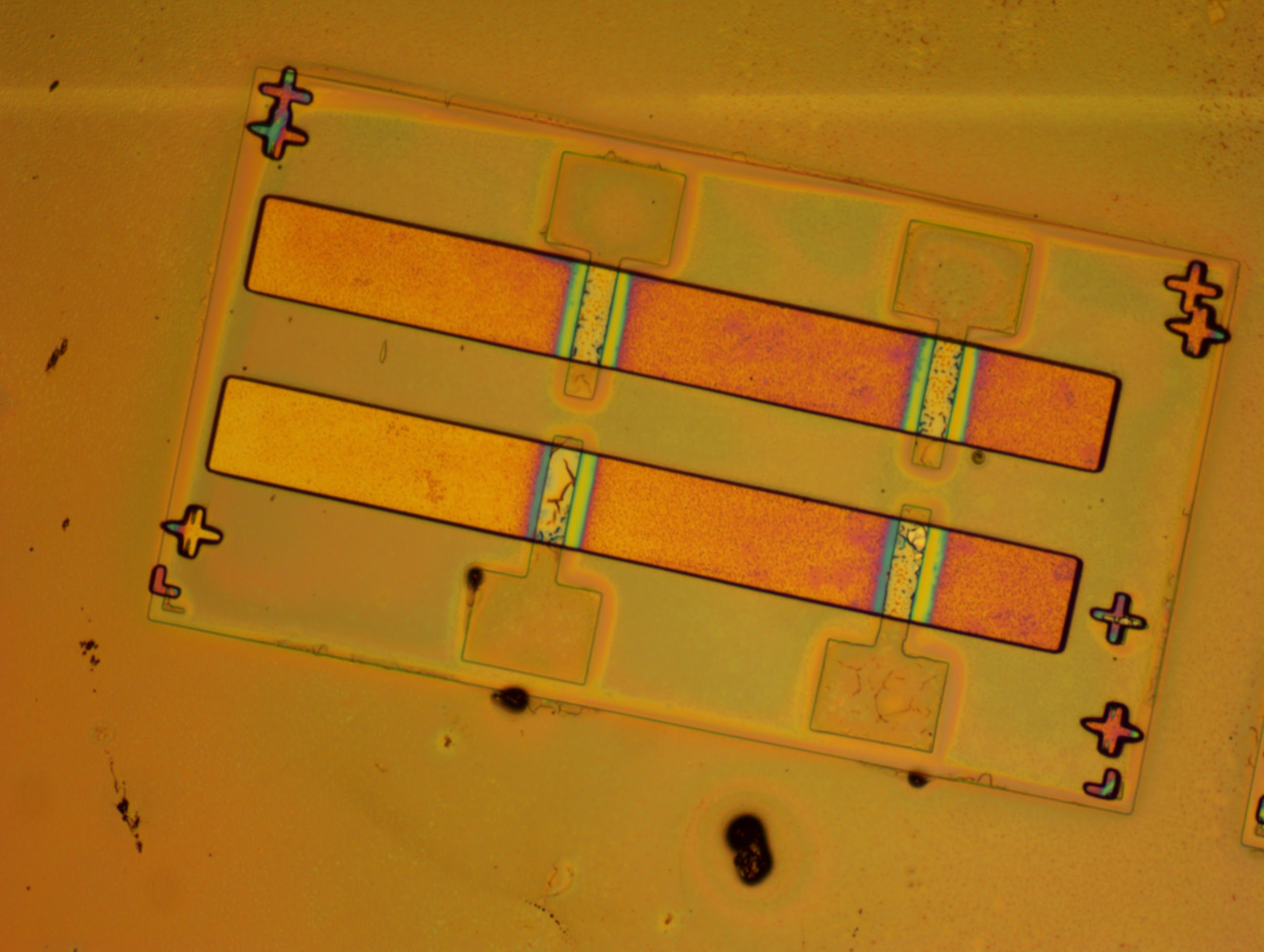


Figure 4. (a) Active Area Mask of the NMOS Inverter (left)

(b) Inspection Image After Active Area Patterning (right)

3.1.3 Via Mask

This mask creates contact holes on the spin-on-glass layer above the active area and the gate area so that the exposed area can be connected to the aluminum contact pads for interconnecting or testing.

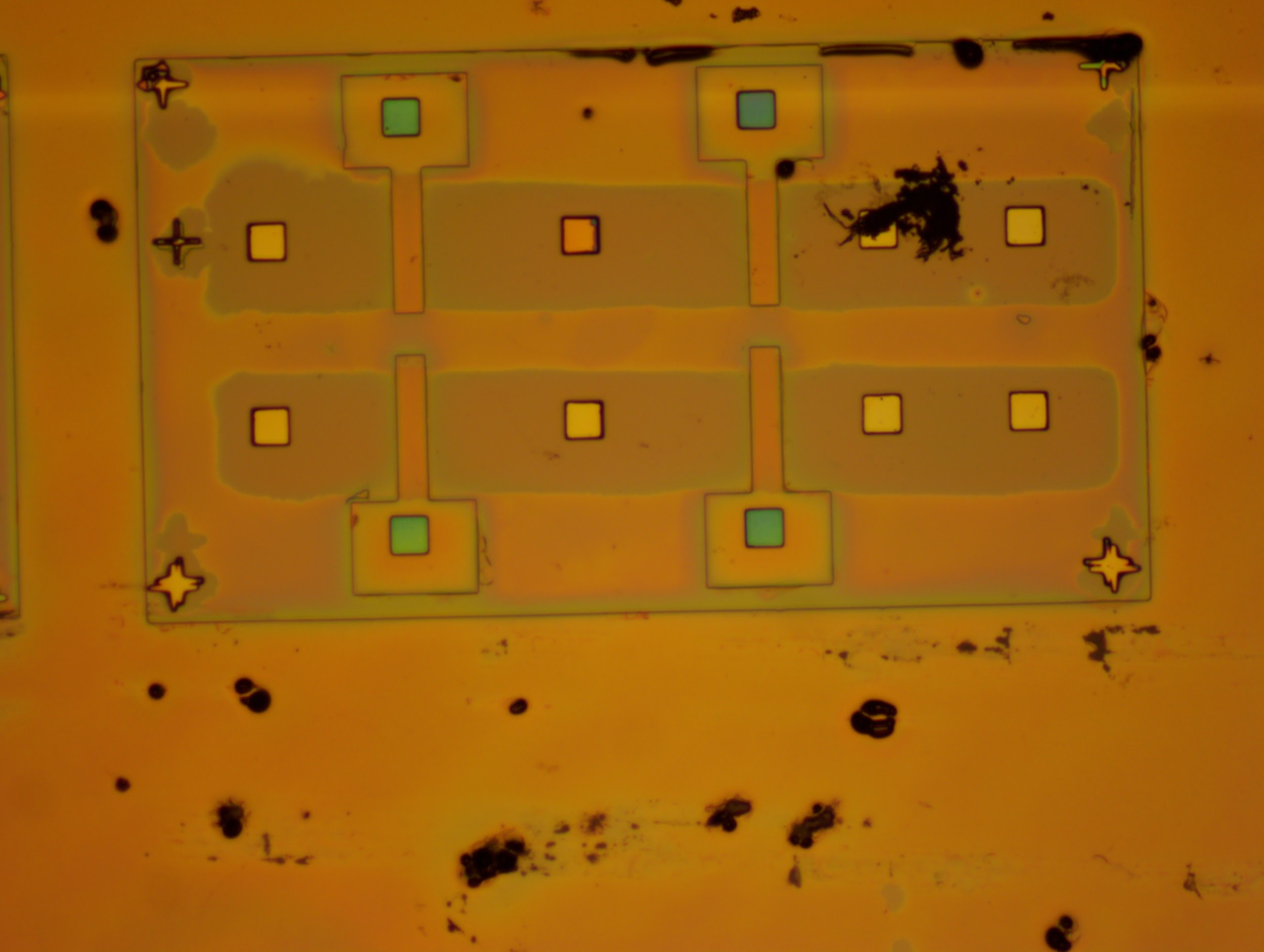
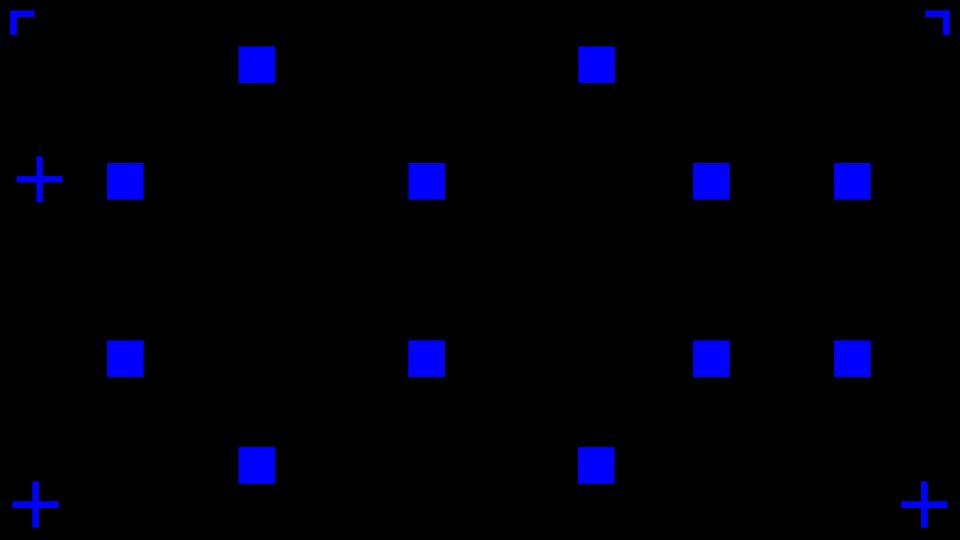


Figure 5. (a) Via Mask of the NMOS Inverter (left)

(b) Inspection Image After Via Patterning (right)

3.1.4 Contact Pad Mask

This mask defines the area of the aluminum contact pads and interconnect wire of the transistors. Note that the edge of the contact pad area shouldn’t be too close to the edge of the mask to prevent short circuits.

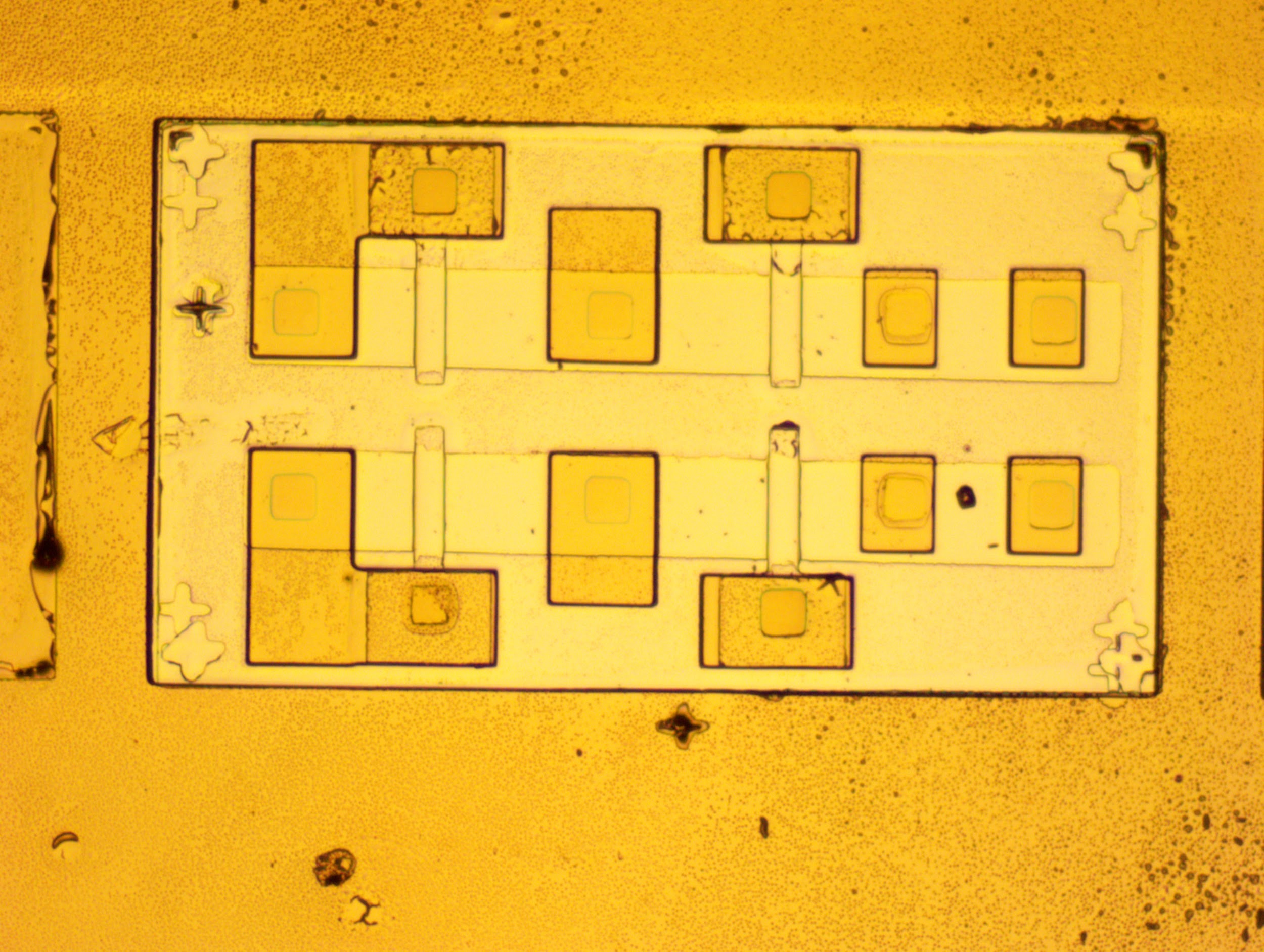
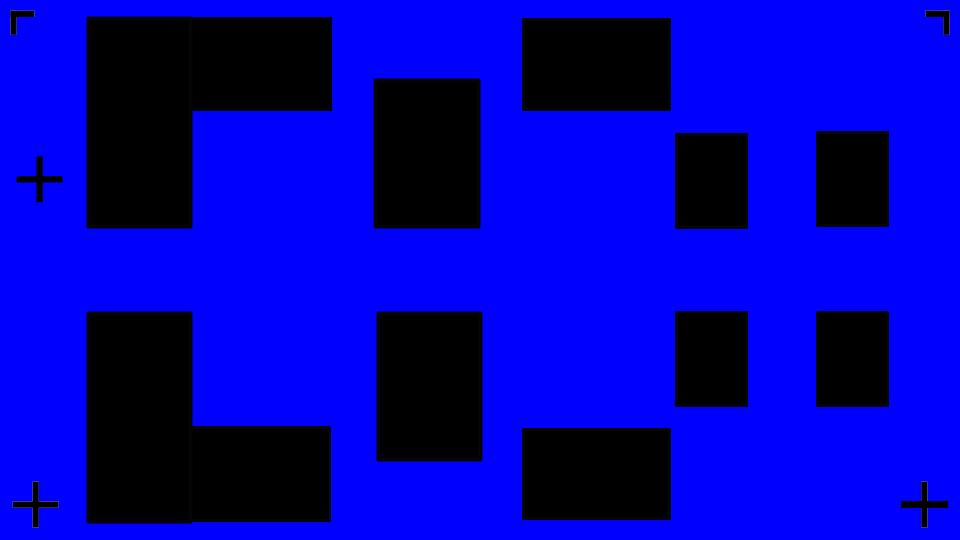


Figure 6. (a) Contact Pads Mask of the NMOS Inverter (left)

(b) Inspection Image After Contact Pads Patterning (right)

3.2 Fabrication Process Flow

The fabrication process flow used to fabricate this Enhancement Load NMOS Inverter is the same as the fabrication process flow used in HackFab S24 Lab sessions. The link to the Fabublox process flow 1 and the mask pattern 2 used to fabricate the device are included in the appendix of the document. The chip view spreadsheets3 documenting the details of the fabrication process are also included there.

1. Results

4.1 Post Fabrication Inspect Image

The final inspection image after the photoresist for aluminum etching is finished is shown below. The pattern matches the design presented in Figure 2.

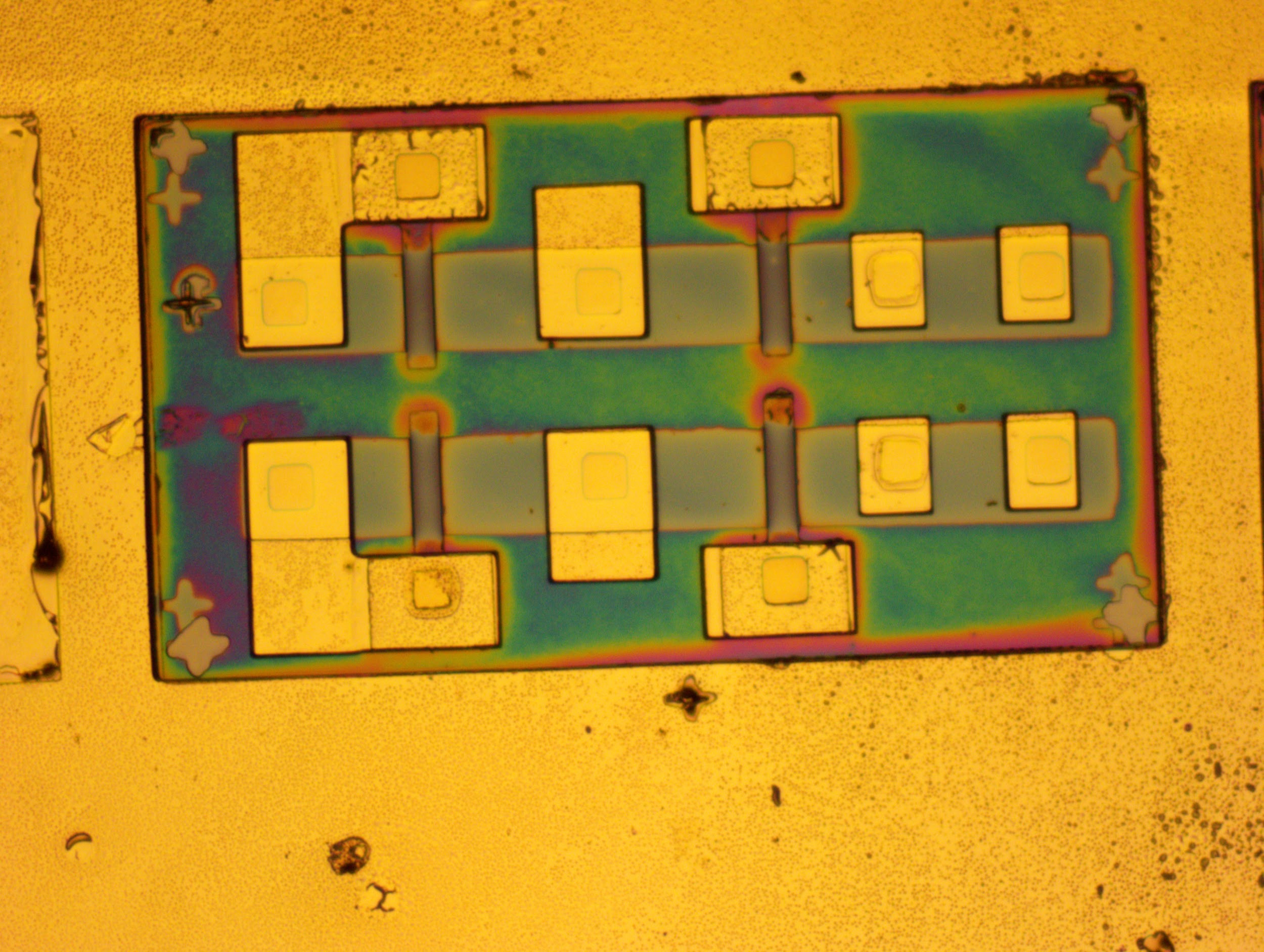


Figure 4. Final Inspection Image of Enhancement Load NMOS Inverter

4.2 SMU Probing Station Set-up and Testing Results

4.2.1 ID-VDS Curve Probing

The probing set-up for the ID-VDS curve of the function transistor (M2) of the Enhancement Load NMOS Inverter is the same as HackerFab probe station SOP. 4 The ID-VDS curves of the transistor M2 at different gate voltages are shown in the blue lines below. The shape of the curve is as expected for NMOS transistors. We can observe that the gate leakage current is very low (ranging from around ±0.1nA) as shown in the red line. The reason why the leakage current is low could be due to the thickness of gate oxide being 20 nm instead of the 10nm oxide wafers that were normally used in previous batches of devices fabricated in HackerFab.

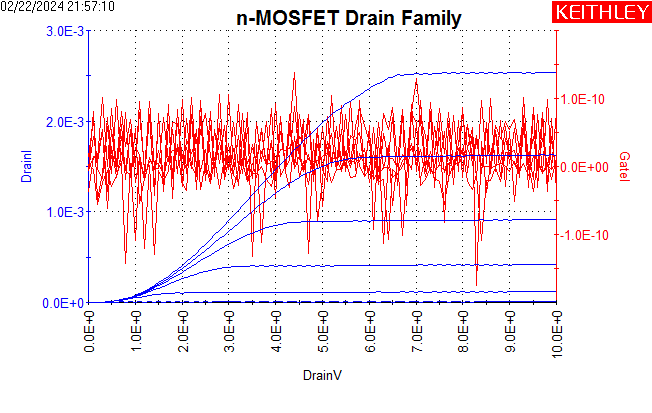
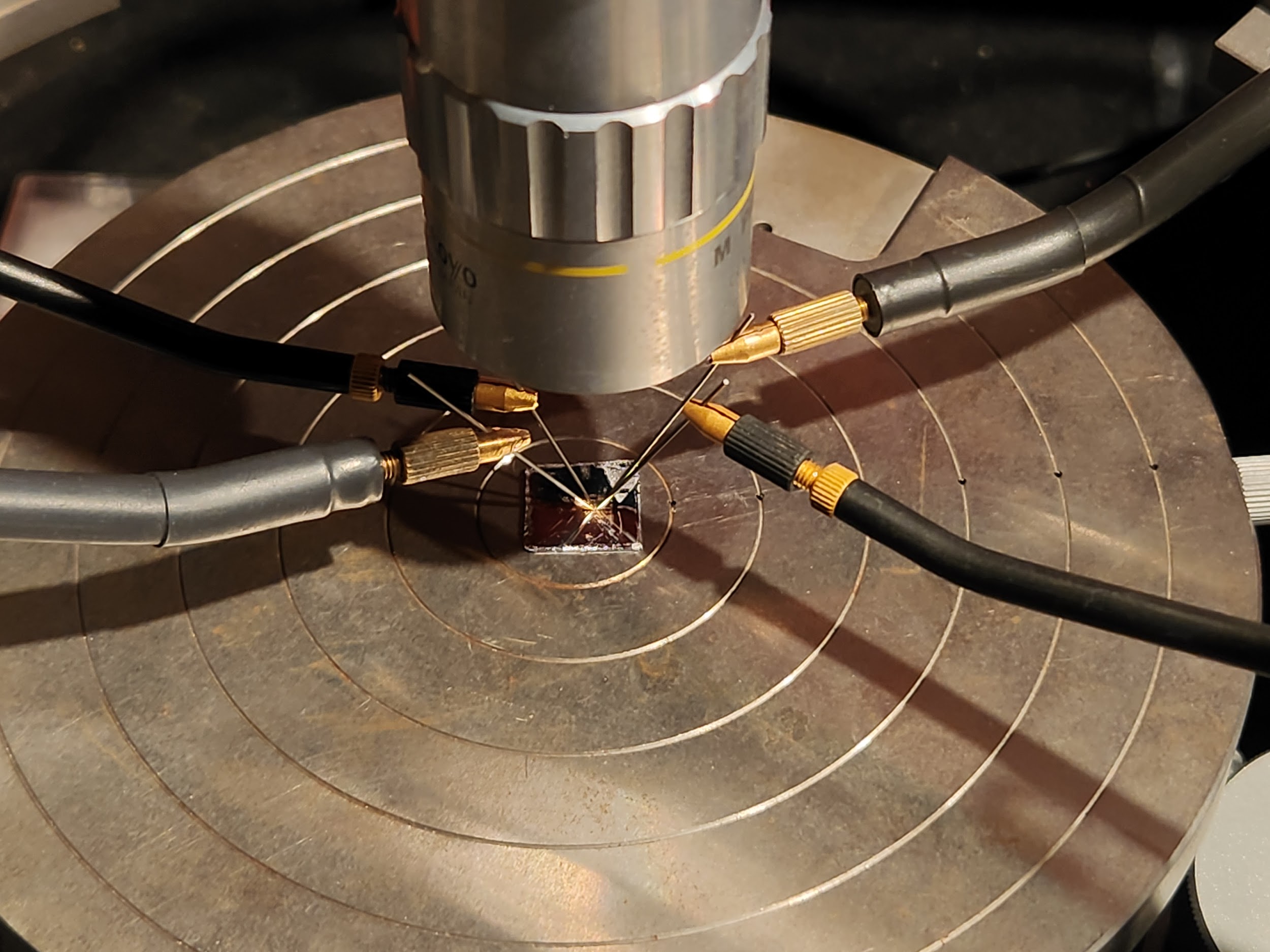


Figure 5. ID-VDS Curve of the M2 transistor

4.2.2 Output Voltage Probing

1. Probe Station Setup

* Add a fourth probe to the original ID-VDS probe setup. Arrange the probes close to the contact pads of the input, output, VDD, and GND terminals of the inverter accordingly as Figure 6 (left) shows.
* Connect the probe on the input terminal to SMU1 or 2 of the probe station.
  + Set “Force function” to “Voltage Sweep” mode. The start voltage is 0V and the end voltage is 5V. This will provide a 0-5V voltage sweep to the input of the inverter (i.e. the gate terminal of transistor M2).
  + In addition, set the voltage measurement for the input for recording the results and plotting.
* Connect the probe on the output terminal to SM1 or SM2 of the prove station.
  + Set “Force function” to “Current Bias (VMU)”. VMU stands for voltage measure unit. The bias current should be set to 0A since we only need to record the output voltage of the device, extra bias current is not needed.
  + Set the voltage measurement for the input for recording the results and plotting.
* Connect the probe on M2’s source terminal to the GND unit.
* Connect the additional fourth probe to an external voltage source to provide a constant 5V bias voltage for the enhancement load transistor M1.
* Run the test and the mode of the test should be “Sweep”.



**Vin**

**Vout**

**Vin**

**VDD**

**Vout**

**VDD**

**GND**

**GND**

Figure 6. Probe Station Setp-up (left) Probe Connected to the Contact Pads (Right)

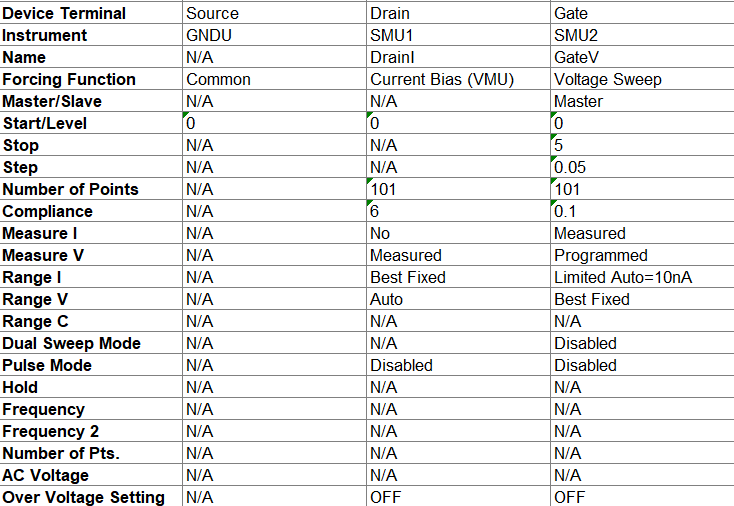
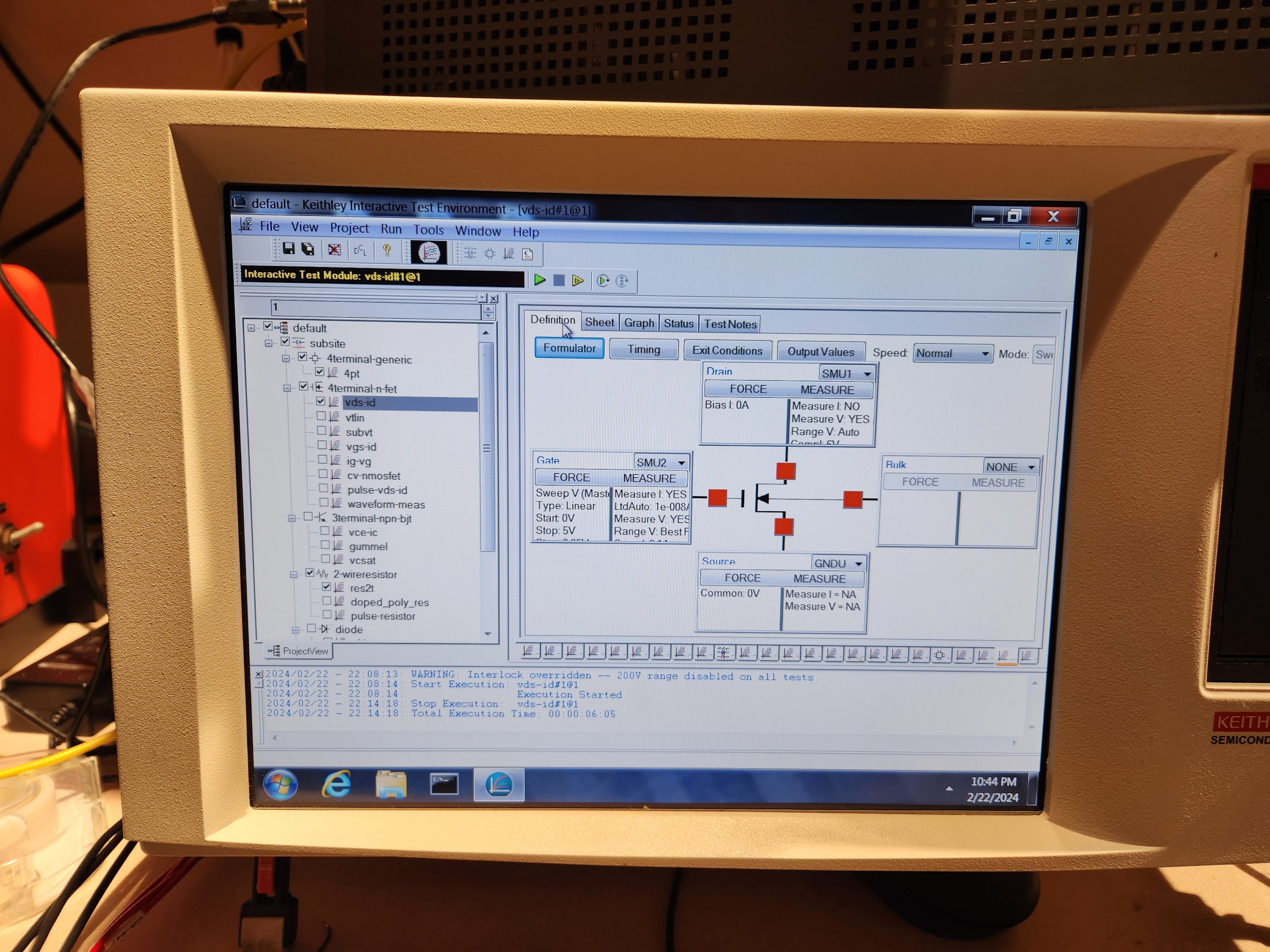


Figure 7. Probe Program Setup (left) Output Log of the Test Set-up (right)

1. Testing Result and Analysis

From Figure 8, when the input of the inverter is low, the output of the inverter is close to the supply voltage which is as expected. When the input voltage starts to increase, the output voltage starts to slowly decrease, and when the input voltage is at 5V the output voltage converges at around 2V. The transition takes longer than expected and the output low voltage is also higher than expected. The reason why this happened could be because the resistance of the load is not high enough and the voltage is divided between the load transistor and the switching transistor.

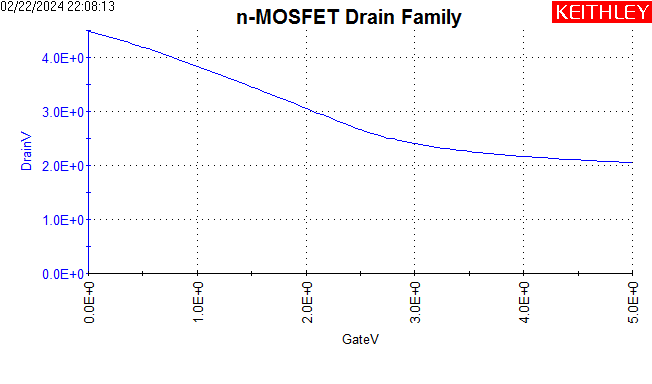


Figure 8. Output of Enhancement Load NMOS Inverter with Input Sweeping from 0 to 5V

1. Conclusion and Future Work

In conclusion, the inverter generally works as expected except for a few things that need to be improved.

One major thing that can be improved in future iterations of NMOS inverter design is to choose the channel lengths of the M1 to be higher. Compare Figure 8 to the output of an ideal inverter, the voltage low is higher than expected and the transition process is also longer. This means that the resistive load is not large enough. Therefore, we can decrease the width-to-length ratio of M1 to increase its effective resistance to have a better performance.

Another thing that can be improved during the fabrication process is to eliminate human error as much as possible to ensure the device can have the electrical characteristics as expected and enhance the yield rate of functioning devices. For example, over-developing during the patterning process and over-etching can enlarge the feature size and affect the functionality of the device.

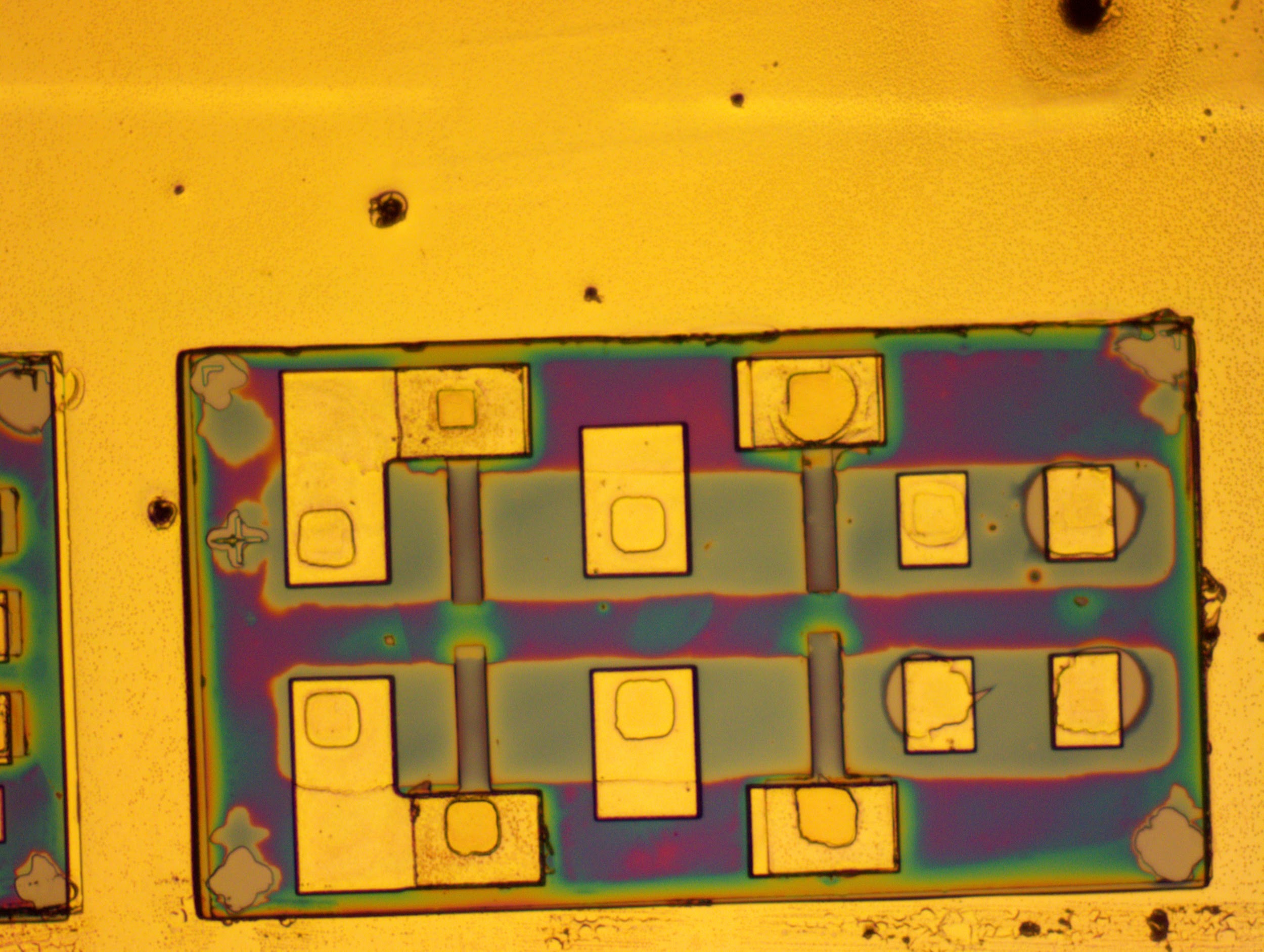


Figure 9. Via Pattern Over Etching

Appendix

1NMOS Inverter Fabublox Process Flow

<https://www.fabublox.com/process-editor/2cae9c94-b49f-4ecf-a23d-a663e2f34de0>

2 NMOS Inverter Mask Pattern [NMOS Inverter Masks](https://docs.google.com/presentation/d/1Q02l-gPsIC7rvnmDtQlWvSO9qyr6oH7joBAHF1w4iB0/edit?usp=sharing)

3 Chip 336 Chip View Spreadsheets [Chip 336 (Chip View)](https://docs.google.com/spreadsheets/d/1jYX2p2FmB2UAPCbBDegczZrLXst202oPel8wEE087Ds/edit?usp=sharing)

4 Probe Station SOP

<https://hacker-fab.gitbook.io/hacker-fab-space/standard-operating-procedures/probe-station-sop>