Features

- Programmable display resolution
- Programmable screen synchronous interrupt
- Displays up to 1024 by 864 pixels at 60 Hz noninterlaced
- Supports video memory address space up to 8K by 8K
- Up to 24 bit planes
- Hardware raster operations—two sources to a destination
- Raster operations at rates of 0.5 to 8 million pixels per second
- Smooth scrolling of rectangular windows
- Hardware clipping to the window boundaries
- Hardware rotation and noninteger scaling of source
- Hardware polygon fill with stipple pattern or solid color
- Addressing of pixels in X- or Z-mode

Description

The 78690 video control (Adder) is an 84-pin, ZMOS VLSI chip used with the 78660 video processor (Viper) chip when building a high-performance, bit-map graphics system with a color or monochrome display system. The video control performs functions common to all bit-map memory planes, such as scan timing, system status generation, and memory address generation for screen refresh and screen updates. The video control sends commands to one or more video processor, which perform the data manipulation for each memory plane. Figure 1 is a block diagram of the video control.

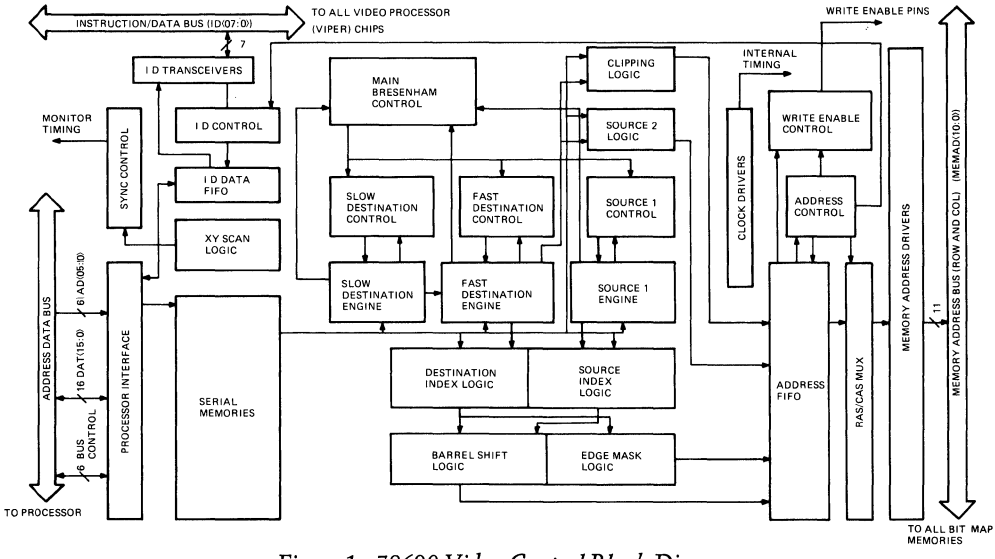

Figure 1 ▪ 78690 Video Control Block Diagram

• Pin and Signal Description

This section provides a brief description of the input and output signals and power and ground connections for the 78690 Video Control 84-pin CERQUAD package. The pin assignments are identified in Figure 2 and the signals are summarized in Table 1.

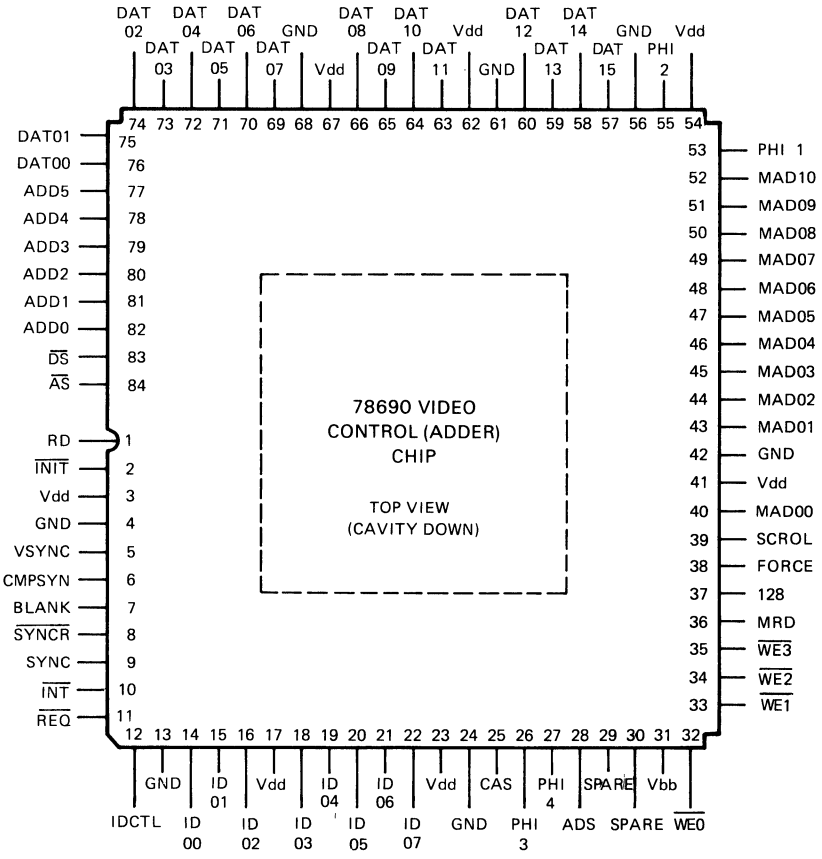

Figure 2 • 78690 Pin Assignments

Table 1 • 78690 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
1	RD	input	Read—Indicates a read or write processor bus cycle.
2	$\overline{\text{INIT}}$	input	Initialize—Initializes the video control and processor bus.
10	$\overline{\text{INT}}$	output	Interrupt—Initiates a processor interrupt request.
11	$\overline{\text{REQ}}$	output	Request—Indicates a DMA access request.
57-60 63-66 69-76	DAT<15:0>	input/output	Data <15:0>—Data bus lines
77-82	ADD<5:0>	input	Address <5:0>—Address bus lines
83	$\overline{\text{DS}}$	input	Data strobe—Enables data transfers on the internal or external data bus.
84	$\overline{\text{AS}}$	input	Address strobe—Initiates an interface transfer.
5	VSYNC	output	Vertical synchronize—A video vertical synchronization signal.
6	CMPSYN	output	Composite synchronize—A video composite horizontal synchronization signal.
7	BLANK	output	Blank—A video composite blank signal.
8	$\overline{\text{SYNCR}}$	output	Synchronize request—A system synchronization cycle request.
9	SYNC	input	Synchronize—Synchronizes the video subsystem.
12	IDCTL	output	ID control—Selects update or scroll select register.
14-16, 18-22	ID<7:0>	input/output	Instruction/Data <7:0>—Instruction/data bus lines.
25	CAS	input	Column address strobe—Bit-map memory address clock signal.
26	PHI3	input	Phase input 3—Phase 3 clock signal.
27	PHI4	input	Phase input 4—Phase 4 clock signal.
28	ADS	input	Address disable—Disables update activity.
29,30	Spare		No external connection recommended.
32-35	$\overline{\text{WE<3:0>}}$	output	Write enable—Enables the writing of the bit-map memory.
36	MRD	output	Map read—Specifies a read or write cycle of the bit-map memory.
37	128/$\overline{16}$	output	128/16—Indicates a major or minor bit-map memory cycle.

Pin	Signal	Input/Output	Definition/Function
38	FORCE	output	Force—Enables a down scrolling write cycle.
39	SCROL	output	Scroll—Selects refresh read memory cycles during scrolling.
40, 43-52	MAD<10:0>	outputs	Memory address <10:0>—Row and column address lines for bit-map memories.
53	PHI1	input	Phase input 1—Phase 1 clock signal.
55	PHI2	input	Phase input 2—Phase 2 clock signal.
31	V_{BB}		Not used.
3,62,67 17,23, 41,54	V_{DD}	input	Voltage—Power supply 5 Vdc.
4,61,68 13,24, 42,56	GND	input	Ground—Ground reference for signals and voltage.

Processor Interface Signals

Read/Write (RD)—This signal informs the video control that the processor access is a read or a write cycle. The processor access is initiated by the assertion of the $\overline{AS}$ signal.

Initialize ($\overline{INIT}$)—This signal causes the video control to be initialized to a known state. The processor interface becomes inactive forcing the ID bus drivers to a high-impedance state until the next SYNC signal is asserted.

Direct Memory Access Request ($\overline{REQ}$)—This signal provides a hardware flag for the bits that are enabled in the status register. The enabled bits are selected by the request register.

Interrupt ($\overline{INT}$)—This signal provides a hardware flag for the bits that are enabled in the status register. The enabled bits are selected by the interrupt register.

Data (DAT<15:0>)—These are bidirectional, parallel data lines, through which the video control interfaces to the processor. During a read operation, the bus master enables the $\overline{DS}$ input and the DAT<15:0> information drives the external data bus. During a write operation when the $\overline{DS}$ signal is asserted, the DAT<15:0> signals drive the internal data bus.

Address (ADD<5:0>)—These inputs select the video control register to be accessed.

Data Strobe ($\overline{DS}$)—During a register read cycle, this signal transfers data to the external data bus. During a register write cycle, it transfers data to the internal data bus.

Address Strobe ($\overline{AS}$)—This signal initiates a video control interfacetransfer. It performs a chip select function and latches the information into the addressed register.

Monitor Timing Signals

Vertical Synchronization (VSYNC)—This signal is a separate vertical SYNC signal for displays that do not use a composite SYNC signal.

Video Composite or Horizontal Synchronization (CMPSYN)—This signal can be programmed as either composite SYNC or horizontal SYNC signal.

Video Composite Blank Signal (BLANK)—The video control uses this signal to blank the monitor.

System Synchronization Request ($\overline{\text{SYNCR}}$)—The video control asserts this signal to request the external clock generation logic to generate a SYNC cycle. The clock logic asserts the SYNC signal and stops the clocks for a predetermined number of serial cycles.

System Synchronization (SYNC)—The external clock generation logic sends this signal to the video control and video processor to synchronize the video subsystem. This signal controls all of the timing generators on the chips.

ID Interface Signals

Chip Select Control (IDCTL)—The ID bus requires two chip select registers to allow independent selection of a video control for ID transactions. When the IDCTL signal is a low level, it selects the update chip selection register. When this signal is a high level, it selects the scroll chip select register.

Instruction/Data Bus (ID<7:0>)—This bus is a communications path between the video control and video processor.

Memory Interface Signals

Address Disable (ADS)—This signal is normally a low level to allow the video control to drive the memory interface. When this signal is high level, all update activity is stopped and all refresh and scroll activities continue. All update cycles on the bus are no operations (NOP) 16-bit read cycles.

Bitmap Memory Write Enable ($\overline{\text{WE}}$<3:0>)—These signals enable writing to groups of four bit map memories.

Memory Read/Write (MRD)—This signal indicates a read or a write cycle. A high level indicates a read cycle and a low level indicates a write cycle.

128/$\overline{16}$ Bit-map Memory Access Width—This signal indicates the type of cycle that the memory interface is about to initiate. A high level specifies the start of a 128-bit major cycle. A low level indicates the start of a 16-bit cycle consisting of two back-to-back minor cycles.

Force Signal for Down Scrolling Write Enables (FORCE)—This signal must occur during a down scroll to cause the write enable signals of the memory planes, with video processor chip plane enables, to write back the data during a scroll write-back cycle.

Scroll Enable (SCROL)—This signal indicates which refresh read memory cycles are to be written back for scrolling.

Bit-map Memory Address (MAD<10:00>—These lines provide the row and column addresses for the bit-map memories that are multiplexed from the video control. An address is available for each column address strobe (CAS) pulse.

Clock Signals

Phase Input 1 to Phase Input 4 (PHI1 to PHI4)—These clock inputs provide the timing control for all operations of the video control.

Column Address Strobe (CAS)—This input is a bit-map memory access strobe.

Power and Ground Connections

Power Supply (V_{DD})—Supplies 5-Vdc power to the 78690 video control.

Ground (GND)—Ground reference for all internal logic except for the output drivers.

• Architecture Summary

A typical bit-map processor system, shown in Figure 3, consists of a local processor or remote processor that performs DMA operations, the 78690 video control, the 78660 video processor, bit-map memory planes, the color map and shift register logic, and high-speed timing logic. The video control performs the functions that are common to memory planes which includes local processor interaction, raster operation computations, scan timing, system status generation, and memory address generation for screen refresh and updates.

The video control communicates with the microprocessor through the microprocessor bus and with the memory through a display memory address bus. It communicates with the video processors through the instruction/data bus.

The video control contains 64 registers that can be directly or indirectly loaded by the local processor to control the scan timing, refresh and scrolling operations. The registers are used to generate interrupts, report status, and to read and write data in the bit-map memory. They also communicate with the instruction/data bus.

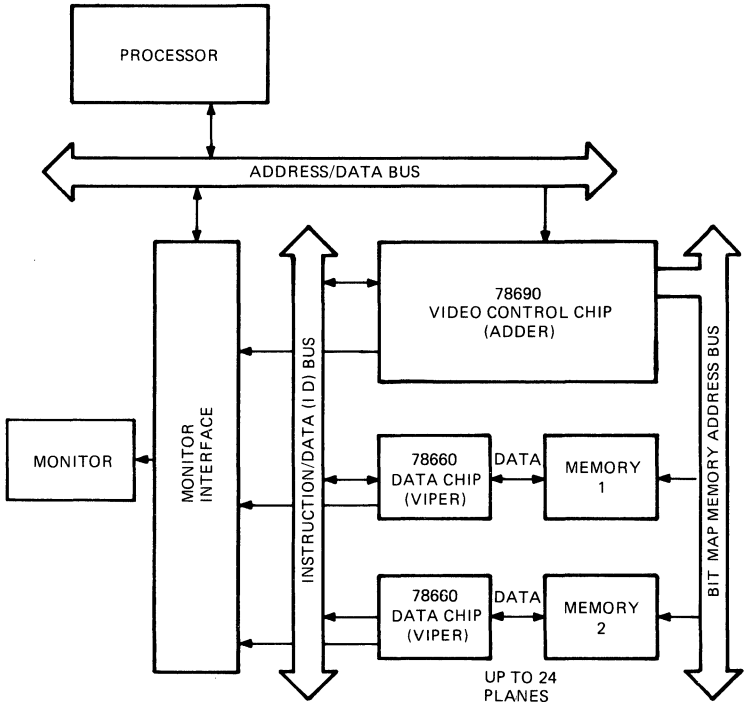

Figure 3 • 78690 Typical Bit-map Graphics System Configuration

The 78690 video control communicates with the processor through the data and address bus, with the bit map memory through the bit-map memory address bus, and with the 78660 video processors through the instruction/data (ID) bus.

The local processor sends the commands to the video control to update memory. The video control performs functions such as local processor interaction, raster computation operations, scan timing, system status generation, and memory address generation to refresh and update the display, that are common to all memory planes.

The display memory address bus transfers the addresses to update the display, to automatically refresh memory, and to scroll the information on the display.

The instruction/data bus loads the registers in the video processor with source, destination, barrel shift constant, and edge mask data. Data is also exchanged through this bus. During a screen update, the new information is transferred to the video processor. During a source operation, the video control sends a code specifying source 1 or source 2 and a barrel shift constant that shifts the source data to align with the destination. During a destination operation, the video control sends a destination code and an edge mask instructing the video processor that specifies which bits of the data bus are to be written.

Hardware Description

The following paragraphs provide a brief description of the major hardware block functions of the video control. Refer to Figure 1.

Processor Interface—This logic receives the parameters and commands from the local processor. The processor interface handles register accesses and controls timing and all necessary bus signals to allow the video control to act as a bus slave to the local processor or DMA device.

ID Control—The ID control selects the chip select registers that determine which video processors will update the bit-map memory and which ones will perform scrolling. The update process uses the ID data first-in/first-out (FIFO) buffer and the scroll process uses the IDS and ICS registers.

ID Data FIFO—During the bit-map memory update process, the video control uses the ID Data FIFO buffer to transfer data to and from the bit maps through the video processor. It is also used to load the video processor registers.

X and Y Scan Logic—The X-scan circuits generate the X components for the monitor display, the system synchronization signals, the refresh and scroll addresses, and the scroll enable signals. The Y-scan circuits generate the Y components for the monitor display, system synchronization signal, refresh and scroll addresses, and determines the active times for scrolling.

Sync Control—This circuit controls horizontal and vertical synchronization.

Serial Memories—The serial memory contains holds the commands and data for update operations.

Main Bresenham Control—This logic controls the serial logic that computes the address sequence for raster operations. It receives command and mode information from the serial memories and generates status bits and control flags for the main control and address collection subsections. A raster operation copies a contiguous section of bit-map memory (source) into a different location of bit-map memory (destination). The modes of raster operations supported are normal raster operations (rasterops), linear patterns, and polygon fill.

Source Generator—The source generator produces a sequence of addresses for the source data during raster operations. In normal mode, it traces a rectangular section of bit-map memory. In linear pattern mode, it loops on a small rectangle to create a repeating pattern until the destination completes its operation. In fill mode, it computes the address sequence for one edge of a polygon.

Destination Generator—The destination generator produces a sequence of addresses for the destination data during raster operations. In the normal and linear pattern modes, it traces a parallelogram by drawing a sequence of arbitrarily oriented parallel lines as the origins follow a trajectory defined by another arbitrarily oriented line. In fill mode, one part of the generator computes the address sequence of the second edge of the polygon and another part of the generator fills the polygon by drawing lines between the two polygon edges.

Source 2 Logic—This logic generates a second sequence of addresses for source data. The video processors may access data from two sources and combine it with the destination data. Source 2 data is generated by adding an offset value to the destination address. It can be used to generate a tile pattern that repeats the modulo of any power of 2 between 16 and 512.

Index Logic—The index logic permits an offset value to be added to the source and destination addresses to support the scrolling process. Scrolling is performed by physically moving data in the bit-map memory. When data is moved, the index may be changed so that the processor is not required to recompute its display list. The index logic allows data to be written into the bit-map memory during the scrolling process.

Clipping Logic—The clipping logic prevents the writing to the bit-map memory locations beyond a predefined rectangular window. Status is generated in the main control section to inform the host processor of the clipping action.

Barrel Shift Constant/Edge Mask Logic—This logic computes the data required by the video processors. The barrel shift constant indicates to the video processor the amount of the source data shift necessary to align it with the destination data. Each source operation generates a barrel shift constant. The edge mask logic defines the left and right edges of the destination. Each destination operation generates an edge mask.

Address FIFO Buffer—This buffer receives the serial logic signals for addresses and flags for destination update writes, source 1 update reads, and source 2 update reads. The FIFO multiplexes this data so it is available when needed.

Address Control—This logic controls the sequence of memory cycles on the memory interface including the refresh (read), scroll (write), and update (read-modify-write) cycles.

Write Enable Control—This logic controls the interface to the bit-map memories. The write enable logic generates the following:

- The timing signals to pass addresses from the RAS/CAS multiplexer to the memories
- The low 3 bits of the CAS addresses during major cycles
- The write enable signals for the memories during both scroll and update read-modify-write memory operations
- The SCROL, MRD and 128/$\overline{16}$ signal for memory
- The memory interface clocks and timing from the CAS clocks

RAS/CAS Multiplexer—This logic combines the X and Y address togenerate the row and column address for the bit-map memories. This multiplexer also assures the refreshing of the bit-map memories.

Programming Functions

When the local processor or DMA controller loads the command register, the video control executes one of the following commands:

Instruction/Data—The instruction/data commands are used to configure and control the video processor.

Raster—The raster commands are used to initiate raster operations as defined by the information previously loaded into registers.

Processor/Bit-map Transfer—These commands are used to to transfer data between the local processor or DMA controller and the video control.

Cancel—The cancel command terminates an update operation in progress and clears all raster operation status registers.

Modes of Operation

The 78690 video control operates in the following modes.

Normal Mode—This mode is used for raster operations when source 1 is a rectangle and the destination is a parallelogram, or source 2 is offset from the destination. Source 1 may be scaled up or down by a noninteger scale factor. When possible, the video control operates on the entire memory bus for operations. Otherwise, it operates on one pixel at a time. This action is transparent to the user.

Pattern Mode—This mode is used to generate dashed lines and thick patterned lines on the display. Scaling is possible in this mode because the source records its own size and is not dependent the destination. In this mode, the video control operates in slow mode.

Fill Mode—This mode is used to fill an area between two vectors. Both the slow source and destination create edge vectors. The fast destination draws either horizontal or vertical lines between the two edge vectors. However, the vectors may intersect each other. In addition, the area to a baseline may be filled so that one edge is a fixed Y value or a fixed X value. The video control uses fast mode for horizontal vectors and slow mode for vertical vectors and the modes can be used together with the fill mode.

Tile Mode—This mode is used to fill intersecting polygons so that the texture of each is continuous across the intersection and applies to source 2 only.

Register Descriptions

The 78690 video control contains 64 registers that can communicate with the processor data/address bus. Three of these registers are reserved for test purposes. The registers may be loaded directly or indirectly through the address counter (register 0) using an autoincrement mode. These registers contain the parameters for raster operations, to set the system timing, and to control the operation of the video control. The following rules apply:

- The registers are write-only unless otherwise specified.
- Local processor coordinates refer to images before adding index values.
- Device coordinates describe a physical position on the screen with 0,0 being the upper-left corner with X increasing to the right and Y increasing downward.
- A DMA controller may load the registers so common combinations are adjacent thereby requiring a minimum of address register loads.

Table 2 • 78690 Register Address Assignments

Address*	Name	Width	Function
Control Registers			
0	Address counter (ADCT)	15:0	DMA device interface to registers
1	Request enable (REQ)	13:0	DMA status flag request enable
2	Interrupt enable (INT)	13:0	Interrupt enable for status flags
3	Status (STAT)	13:0	Video system status
4	Reserved for test		
5	Spare		
6	Reserved for test		
7	ID data (IDD)	15:0	ID bus data
8	Command (CMD)	14:0	Command register (same as command register location A)
9	Mode (MDE)	7:0	Sets various raster operation execution modes
A	Command (CMD)	14:0	Command register
Scroll Registers			
B	Reserved for test		
C	ID scroll data (IDS)	15:0	ID bus scroll data
D	ID scroll command (ICS)	15:0	ID command register for scroll process
E	Scroll X Minimum (PXMN)	13:0	Left boundary of scroll region
F	Scroll X Maximum (PXMX)	13:0	Right boundary of scroll region
10	Scroll Y Minimum (PYMN)	13:0	Top boundary of scroll region
11	Scroll Y Maximum (PYMX)	13:0	Bottom boundary of scroll region
12	Pause (PS)	10:0	Screen coordinate to set pause status
13	Y offset (PYOF)	13:0	Screen to memory coordinate offset
14	Y scroll constant (PYSC)	14:0	Vertical scroll distance in one frame
Update Control Registers			
15	Pending X index (PXI)	13:0	Pending X index
16	Pending Y index (PYI)	13:0	Pending Y index
17	New X index (NXI)	13:0	New X index
18	New Y index (NYI)	13:0	New Y index
19	Old X index (OXI)	13:0	Old X index
1A	Old Y index (OYI)	13:0	Old Y index
1B	Clip X minimum (CXMN)	13:0	Left clipping boundary
1C	Clip X maximum (CXMX)	13:0	Right clipping boundary
1D	Clip Y minimum (CYMN)	13:0	Top clipping boundary
1E	Clip Y maximum (CYMX)	13:0	Bottom clipping boundary
1F	Spare		

Address*	Name	Width	Function
Raster Control Registers			
20	Fast source 1 dX (FSDX)	13:0	Fast delta X for source 1
21	Slow source 1 dY (SSDY)	13:0	Slow delta Y for source 1
22	Source 1 X origin (SXO)	13:0	X coordinate of source 1
23	Source 1 Y origin (SYO)	13:0	Y coordinate of source 1
24	Destination X origin (DXO)	13:0	X coordinate of destination origin
25	Destination Y origin (DYO)	13:0	Y coordinate of destination origin
26	Fast destination dX (FDX)	13:0	X component of fast destination vector
27	Fast destination dY (FDY)	13:0	Y component of fast destination vector
28	Slow destination dX (SDX)	13:0	X component of slow destination vector
29	Slow destination dY (SDY)	13:0	Y component of slow destination vector
2A	Fast scale (FSC)	13:0	Fast vector scale factor
2B	Slow scale (SSC)	13:0	Slow vector scale factor
2C	Source 2 X origin (S2XO)	13:0	X coordinate of source 2
2D	Source 2 Y origin (S2YO)	13:0	Y coordinate of source 2
2E	Source 2 Height and Width (S2HW)	7:0	Size of source 2 tile
2F	Error 1 (ERR1)	13:0	Error adjust for slow destination
30	Error 2 (ERR2)	13:0	Error adjust for fast destination
Screen Format Control Registers			
31	Y scan count 0 (YCT0)	13:0	Vertical timing
32	Y scan count 1 (YCT1)	13:0	Vertical timing
33	Y scan count 2 (YCT2)	13:0	Vertical timing
34	Y scan count 3 (YCT3)	13:0	Vertical timing
35	X scan configuration (XCON)	8:0	Cycles, bus width, number of refresh rows
36	X limit (XL)	13:0	Width limit on refresh
37	Y limit (YL)	13:0	Height limit on refresh
38	X scan count 0 (XCT0)	15:0	X scan count 0
39	X scan count 1 (XCT1)	15:0	X scan count 1
3A	X scan count 2 (XCT2)	15:0	X scan count 2
3B	X scan count 3 (XCT3)	15:0	X scan count 3
3C	X scan count 4 (XCT4)	15:0	X scan count 4
3D	X scan count 5 (XCT5)	15:0	X scan count 5
3E	X scan count 6 (XCT6)	15:0	X scan count 6
3F	Sync phase (SYNP)	14:5	Sync phase adjustment

*Hexadecimal notation

Status and Control Registers

The video control logic contains status and control registers used to initiate requests and interrupts, report status, select modes of operation, and initiate command functions. These registers are described in the following paragraphs. The status and control register formats are shown in Figure 4.

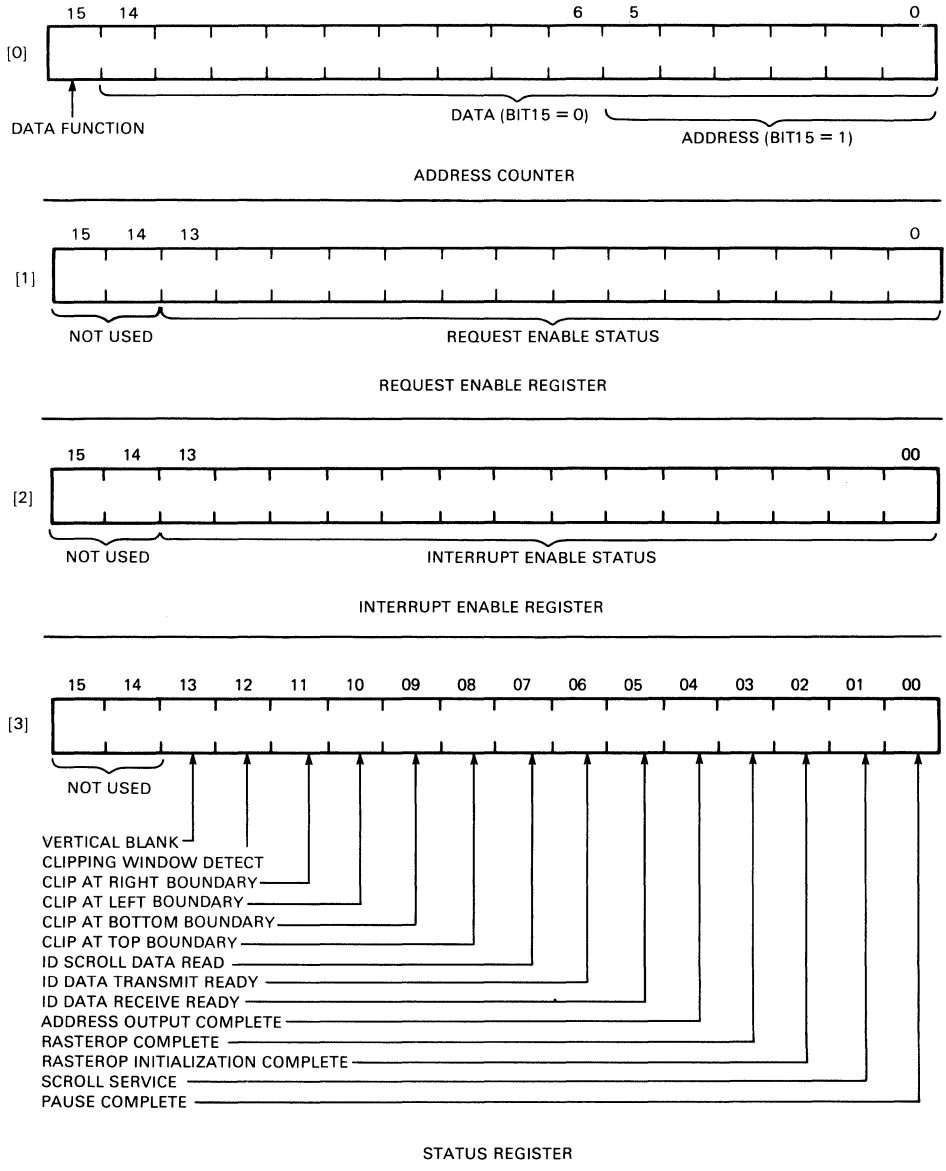

Figure 4 ▪ 78690 Status and Control Register Formats

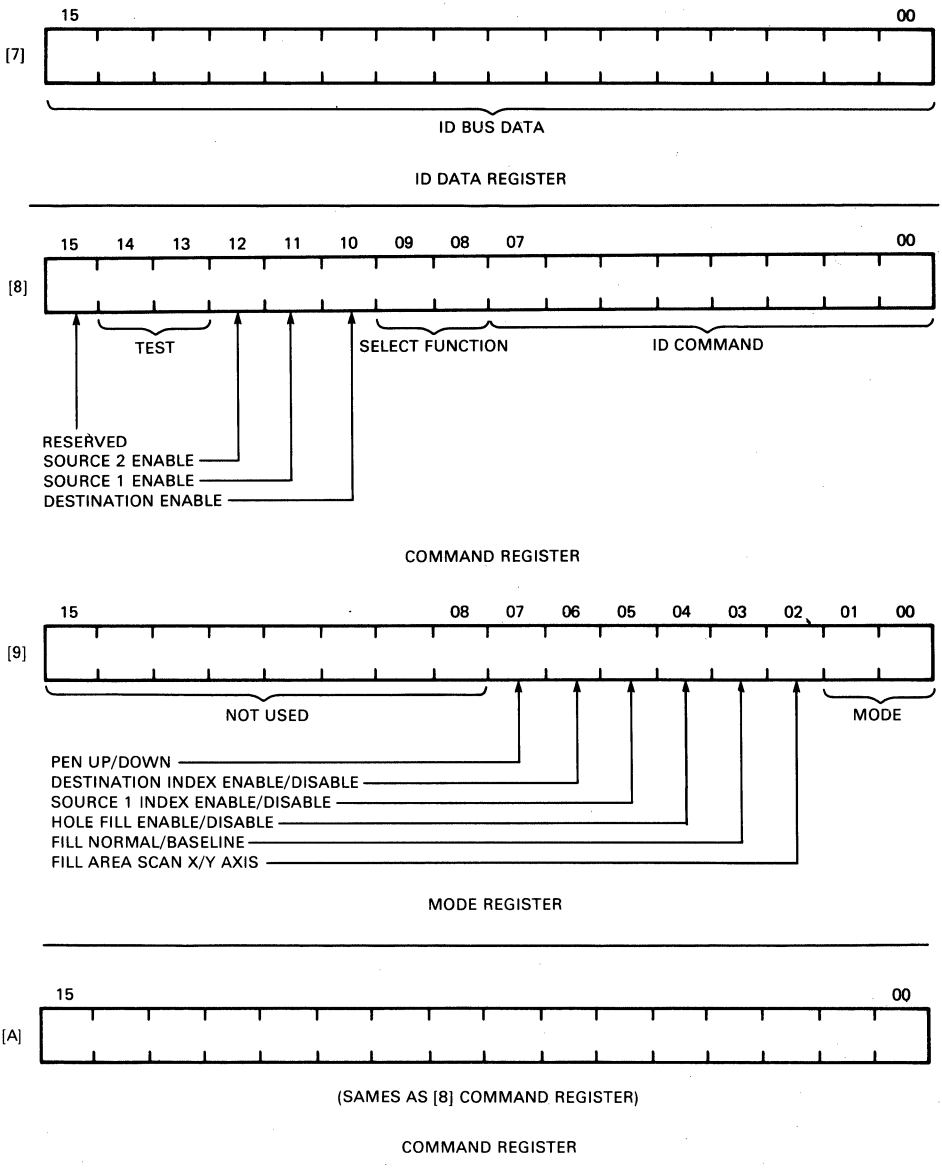

Figure 4 ▪ 78690 Status and Control Register Formats (Continued)

[0] Address Counter—The address counter (ADCT) provides indirect access to the video control registers and is used with standard DMA controllers. The register information is described in Table 3.

Table 3 • 78690 Address Counter Description

Bit	Description
15	Data Function—During write operations, this bit is set to cause the following: Bit 15 = 0: The data in the counter is transferred to the register selected by the counter and the counter is incremented. Bit 15 = 1: The low 6 bits of data replace the original contents of the address counter with the following exception. If the address counter is pointing to either the ID data register (IDD) or to the ID scroll data register (IDS), the most significant bit of the data is ignored and all 16 bits are loaded into the appropriate ID register and the counter is incremented. When reading the address counter, the register that the contents of the address counter points to is accessed and the counter is incremented. The $\overline{\text{INIT}}$ signal clears the counter.
14:0	Data/Address—Contains data in bits 14:0 if data function bit 15 = 0 and address information in bits 6:0 if data function bit 15 = 1.

[1] Request Enable Register—The request enable (REQ) register is used to select any of the corresponding 13 bits of the status register to be enabled to assert a request. When a status condition sets a bit in the status register, a request will be generated if the corresponding request enable bit in this register is also set. The DMA controller normally sets a request bit one at a time as it waits for the specific event to occur. The register information is defined in Table 4.

Table 4 • 78690 Request Enable Register Description

Bit	Description
15,14	Not used
13:0	Request enable—Each bit corresponds to a bit in the status register. When a request bit is set, a request (REQ) signal is generated when the corresponding bit in the status register is set. The request register allows a DMA controller to control data and request status.

[2] Interrupt Enable Register—The interrupt (INT) enable register is used by the local processor to select any of the corresponding 13 bits of the status register. When a status condition sets a bit in the status register, an interrupt will be generated if the corresponding interrupt enable bit in this register is also set. The register information is defined in Table 5.

Table 5 • 78690 Interrupt Enable Register Description

Bit	Description
15,14	Not used
13:0	Interrupt enable (INT)—Each bit corresponds to a bit in the status register. When a interrupt enable bit is set, an interrupt request (INT) signal is generated when the corresponding status condition causes the status bit to be set. The interrupt enable register provides the local processor with interrupt conditions.

[3] Status Register—The status (STAT) register is a read-only register that provides indications of the internal progress of the video control. The register information is described in Table 6.

Table 6 • 78690 Status Register Description

Bit	Description
15:14	Not used
13	Vertical blank—This bit is set at the start of the vertical blank interval and cleared by writing 0 to this bit position.
12	Clipping window detect—Set during a destination write cycle to indicate that part of a raster operation was inside the clipping rectangle. Cleared by writing a zero to this bit position.
11	Clipped right boundary—Set during a destination write cycle to indicate that part of a raster operation was clipped at the right boundary. Cleared by writing a zero to this position.
10	Clipped left boundary—Set during a destination write cycle to indicate that part of a raster operation was clipped at the left boundry. Cleared by writing a zero to this position.
9	Clipped bottom boundary—Set during a destination write cycle to indicate that part of a raster operation was clipped at the bottom boundary. Cleared by writing a zero to this position.
8	Clipped top boundary—Set during a destination write cycle to indicate that part of a raster operation was clipped at the top boundary. Cleared by writing a zero to this position.
7	ID scroll data—Set by the video control when a new data word can be loaded into the ID scroll data register. Cleared by the ID command to the ID scroll command register.

Table 6 • 78690 Status Register Description

6	ID data transmit ready—Set to indicate that data can be loaded into the ID data register during an ID command. Cleared when the new ID data command is loaded. This bit is also set at the completion of a Cancel command to indicate that the ID FIFO buffer is clear to load another command. The Cancel command initially clears this bit. When a raster operation or PBT command is not in progress, loading the ID data register or asserting the $\overline{\text{INIT}}$ signal will set this bit.
5	ID data receive ready—Set when the ID data FIFO buffer has a word to be read. This bit is cleared when the FIFO buffer is empty; when a raster operation, PBT, or cancel command is loaded into the command register; or when bus initialization occurs.
4	Address output complete—Set when all addresses calculated by pending raster operations or PBT commands have been used indicating that update parameters such as clipping boundaries, indexes, ID data, or other commands can be loaded. During a bit-map to processor (BTP) commands, this bit is set when the IDD FIFO buffer is empty. It is also set by the cancel command or $\overline{\text{INIT}}$ signal. Cleared by loading any raster operation or PBT command.
3	Raster operation complete—Set at the completion of raster operations or PBT address calculation when no further command is pending. It indicate that other raster operations can be loaded such as dX and dY pairs, source 2, or scale factor, that the mode register can be loaded, or that a new but not different raster operation can be initiated. It is also set by the Cancel command or $\overline{\text{INIT}}$ signal. Cleared by loading any raster operation or PBT command.
2	Raster operation initialization complete—Set at the completion of the initialization of a raster operation or a processor-to-bit-map transfer. It indicate that the source 1 origin, the destination origin, or a new but not different raster operation command (except PBT command) can be loaded. It is also set by a Cancel command or the $\overline{\text{INIT}}$ signal. Cleared by loading a raster operation or PBT command.
1	Scroll service (frame sync)—Set at the start of frame when new scroll parameters can be loaded. Cleared by writing a zero to this bit.
0	Pause complete—Set when the screen refresh process reaches the Y address of device coordinates in the pause register. Cleared by writing a zero to this bit.

[4] Test Register—Reserved for test purposes.

[5] Spare Register—Not used.

[6] Test Register—Reserved for test purposes.

[7] ID Data Register—The ID data (IDD) register is the ID data bus port from the six-word FIFO buffer. During PBI commands, data is transferred between the processor and bit-map memory through this register.

[8] Command Register—The command (CMD) register is used for all commands by the update process and can be accessed from either address [8] or [A] (hexadecimal). The register information is described in Table 7.

Table 7 • 78690 Command Register Description

Bit	Description
15:13	NOP (No operation)—Reserved and test functions as follows: Bit 15: Reserved and normally zero Bits 14, 13: Test and normally zero
12	S2E (Source 2 enable)—Second source enable
11	S1E (Source 1 enable)—First source enable
10	DTE (Destination enable)—Enable the destination
9:8	(FUNC) Select Function—Selects the function of the command as follows:

Bit 9	Bit 8	Function
0	0	Cancel all active and pending commands
0	1	ID command
1	0	Raster operation command
1	1	Processor bit-map (PBT) transfer command

7:0	ID command—Contains the opcode and address of the ID command.

[9] Mode Register—The mode (MDE) register sets the raster operation execution modes. The register information is described in Table 8.

Table 8 • 78690 Mode Register Description

Bit	Description
7	Pen up/dn—Selects the pen position as follows: Bit 7 = 0: pen up to disable writing Bit 7 = 1: pen down to enable writing
6	Destination indexing—Controls the indexing of the destination as follows: Bit 6 = 0: disable Bit 6 = 1: enable
5	Source 1 indexing—Controls the indexing of source 1 as follows: Bit 5 = 0: disable Bit 5 = 1: enable
4	Hole fill—Controls the hole fill operation as follows: Bit 4 = 0: disable (normal single pixel wide destination) Bit 4 = 1: enable (all other destinations)

Bit	Description
3	Fill area—Selects the fill area as follows: Bit 3 = 0: Normal two-edge fill Bit 3 = 1: Fill to a vertical or horizontal base line depending on the scan direction of the previous bit.
2	Fill area scan axis—Selects the fill area to be scanned as follows: Bit 2 = 0: Scanned parallel to the X axis Bit 2 = 1: Scanned parallel to the Y axis
1:0	Mode—Selects the operating mode as follows:

Bit 1	Bit 0	Mode
0	0	Normal: Source 1 is a scaled destination area.
0	1	Reserved
1	0	Linear pattern: Source 1 is from the dX and dY registers.
1	1	Fill: Destination slow generator computes the "A" edge vector. Source 1 generator computes the "B" edge vector and the video control fills the space between the vectors.

[A] Command Register—The functions of this command (CMD) register are the same as the [8] Command (CMD) register.

Scroll Registers

The scroll registers determine the scroll activity on the display. During active scrolling operations, the scroll registers must be loaded by the scroll process before the start of the vertical blanking. The video processor performs various functions during the vertical blanking depending on the type of scroll activity pending for the next frame. The scroll register formats are shown in Figure 5.

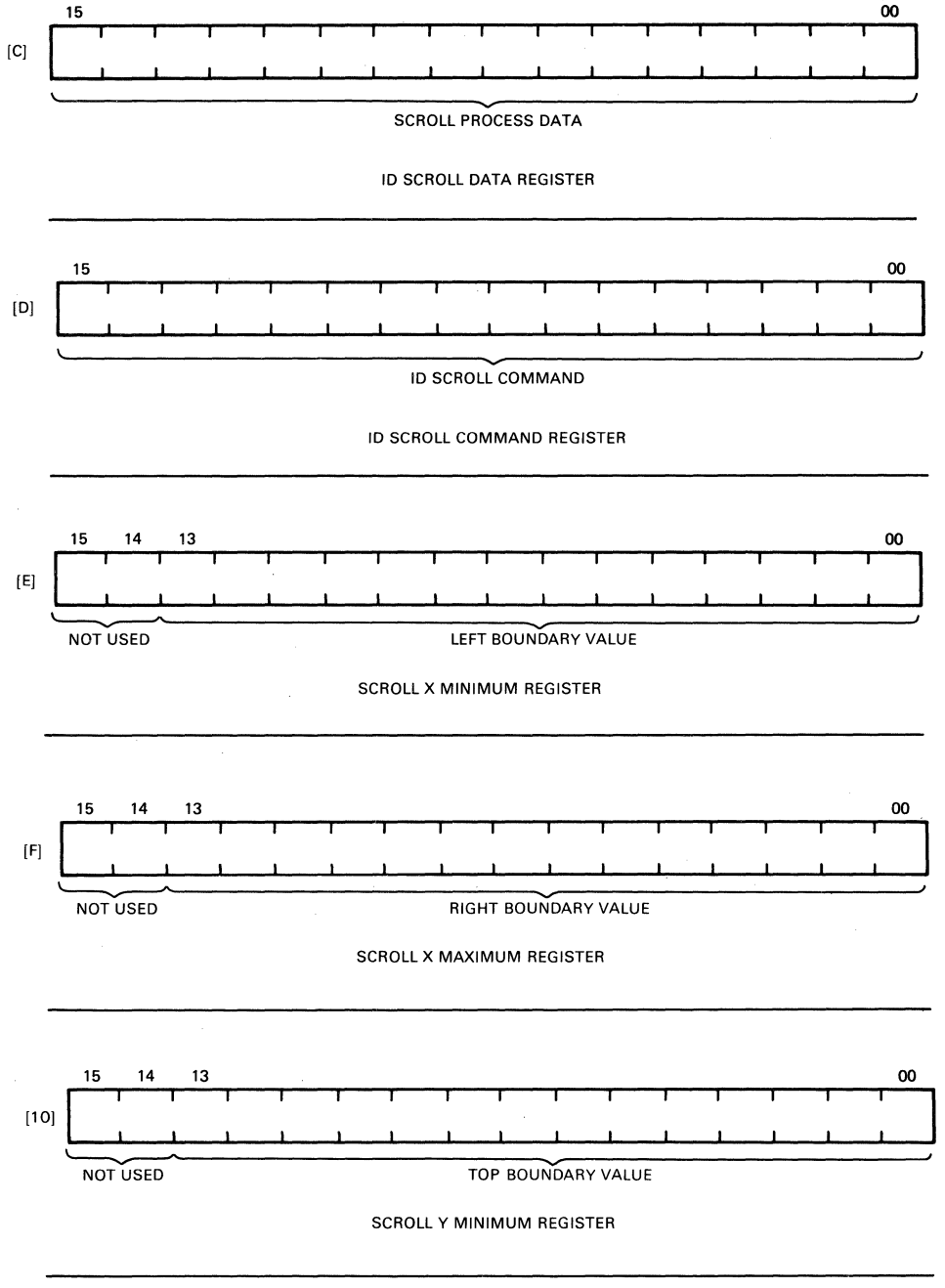

Figure 5 ▪ 78690 ID Scroll Register Formats

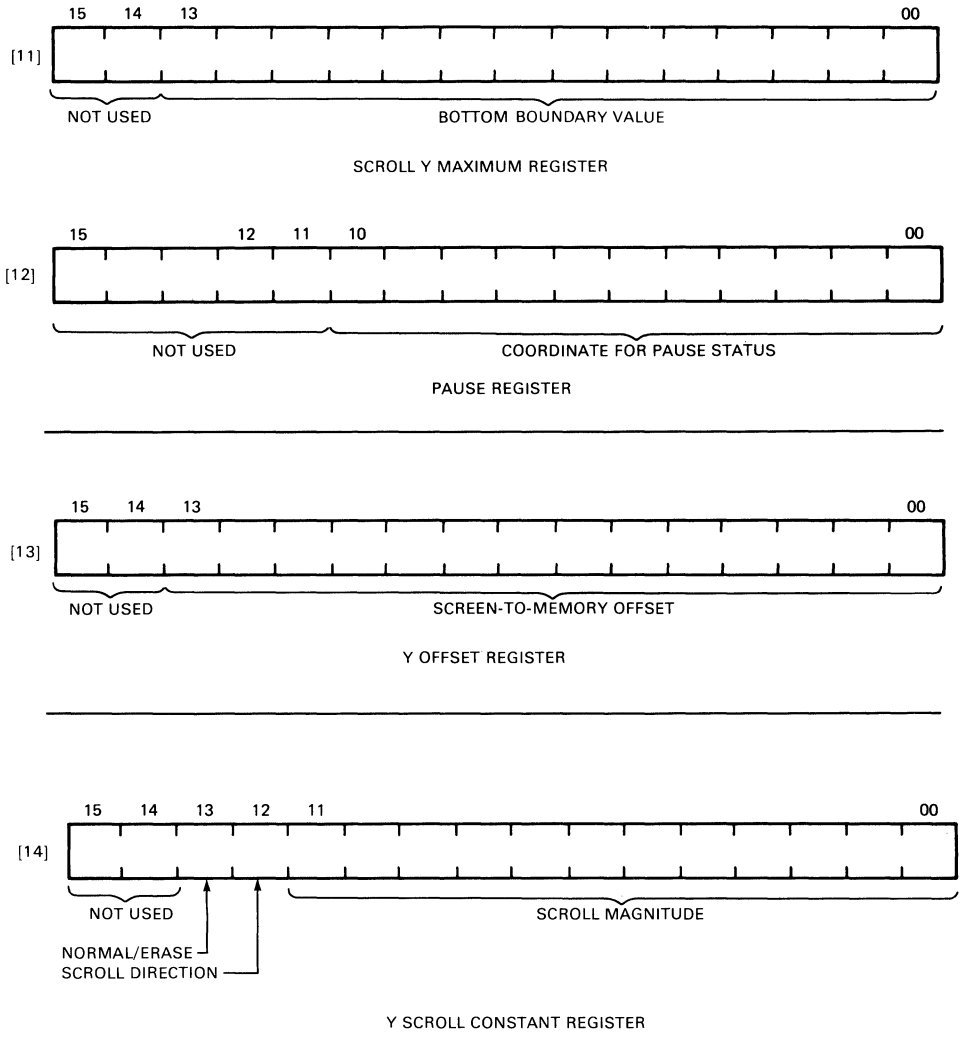

Figure 5 • 78690 ID Scroll Register Formats (Continued)

[B] Test Register—Reserved for test.

[C] ID Scroll Data Register—The ID scroll (IDS) data register contains the data to be transferred to the ID bus during the scroll process ID commands.

[D] ID Scroll Command Register—The ID scroll command (ICS) register is the ID command register for the scroll process. Commands are transferred through this register without interfering with update activities.

[E] Scroll X Minimum Register—The Scroll X minimum (PXMN) register information determines the left boundary of the scroll region and specifies the left-most pixel. The X boundary may only be specified to a multiple of four pixels. The scroll boundaries are not affected by index values and the register is double buffered so that the values loaded become active at the start of the following frame.

[F] Scroll X Maximum Register—The Scroll X maximum (PXMX) register information determines the right boundary of the scroll region. The scroll boundaries are not affected by index values and the register is double buffered so that the values loaded become active at the start of the following frame.

[10] Scroll Y Minimum Register—The Scroll Y minimum (PYMN) register information determines the the top boundary of the scroll region. The scroll boundaries are not affected by index values and the register is double buffered so that the values loaded become active at the start of the following frame.

[11] Scroll Y Maximum Register—The Scroll Y maximum (PYMX) register informatiom determines the bottom boundary of the scroll region. The scroll boundaries are not affected by index values and the register is double buffered so that the values loaded become active at the start of the following frame.

[12] Pause Register—The pause (PSE) register contains a value that specifies which scan, when displayed, will cause the pause complete (bit 0) of the status register to be set or a second pause event to be queued. This register is double buffered so that the new value loaded begins at the start of the following frame and continues through the frame.

[13] Y Offset Register—The Y Offset (PYOF) register contains the value when added to the device coordinates become the memory coordinate ranging from 0 to height of display portion of the bitmap memory. This value is the same as the value stored in the Y limit register minus 1. The register is double buffered so that the values loaded become active at the start of the following frame.

[14] Y Scroll Constant Register—The Y Scroll Constant (PYSC) register specifies the magnitude and direction of the vertical scroll in one frame time. The vertical distance specified by the value in this register and the horizontal distance specified by the value in the scroll constant register of the 78660 video processor will be scrolled. The register information is described in Table 9.

Table 9 • 78690 Y Scroll Constant Register Description

Bit	Description
13	Normal/Erase—Specifies the scroll condition as follows: Bit 13 = 0: Normal scrolling Bit 13 = 1: Erase mode
12	Scroll direction—Specifies the scrolling direction as follows: Bit 12 = 0: Up, left, or right scrolling Bit 12 = 1: Down scrolling.
11:0	Magnitude—Determines the unsigned vertical magnitude of the scroll.

Update Control Registers

The update control registers, shown in Figure 6, contain index values that are added to the raster operation addresses to adjust the addresses for scrolling and to specify location of the regions on the display. The pending values are automatically loaded into the new registers at the start of the next frame. If no scrolling takes place, the loading of the registers is not required. The pending register values are loaded first, followed by the new values, and then the old values.

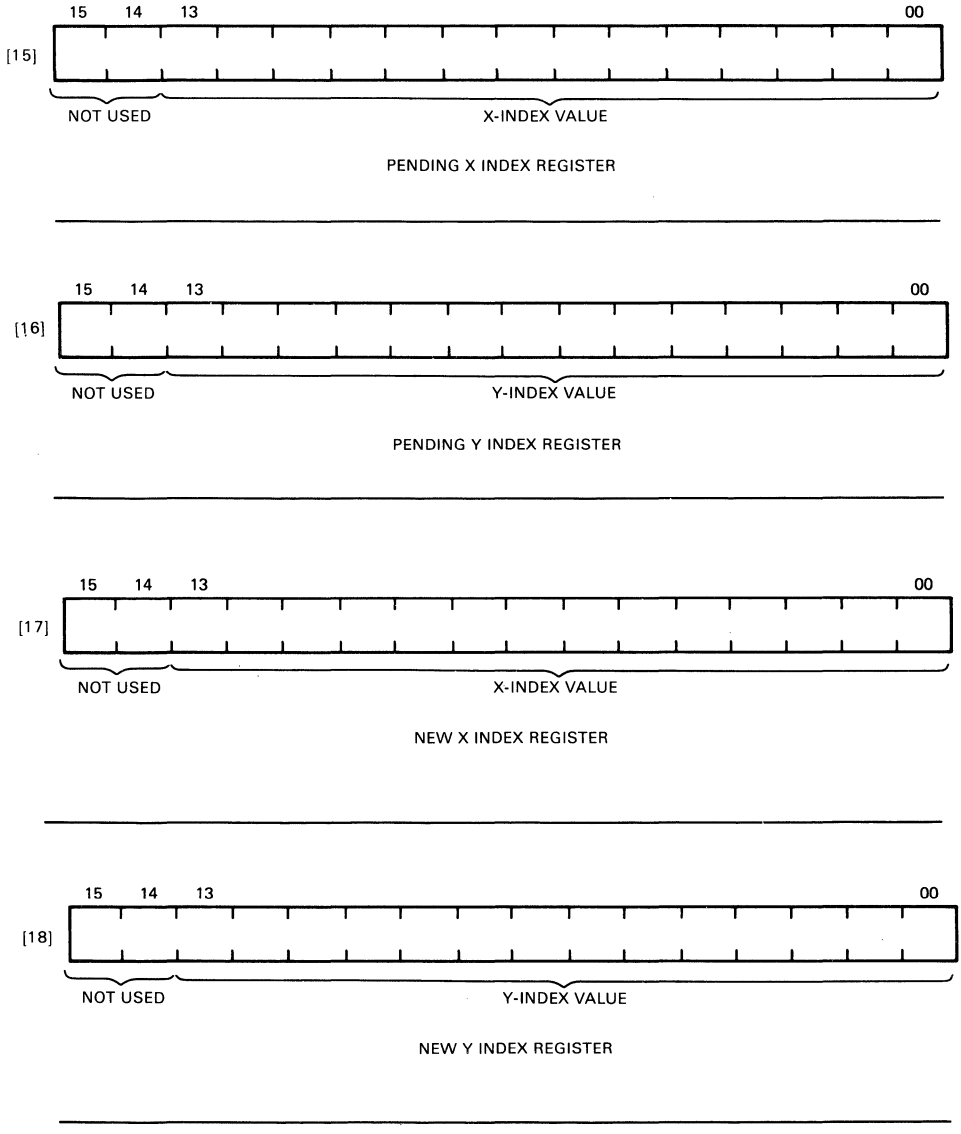

Figure 6 • 78690 Update Control Register Format

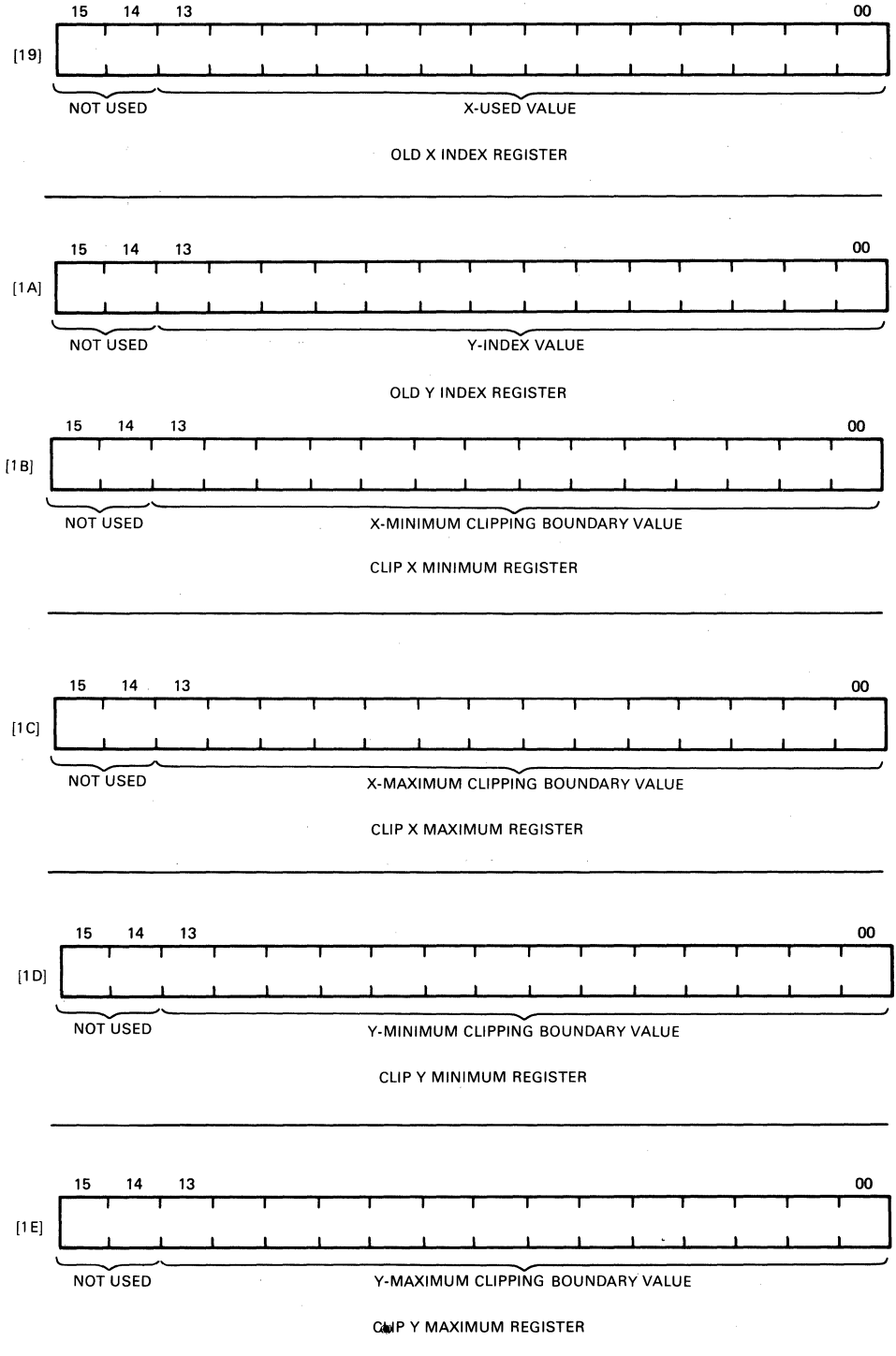

Figure 6 ▪ 78690 Update Control Register Format (Continued)

[15] Pending X Index Register—The pending X index (PXI) register contains the X index value for the next frame.

[16] Pending X Index Register—The pending Y index (PYI) register contains the Y index value for the next frame.

[17] New X Index Register—The new X index (NXI) register contains the new X index value that applies to the data that has been moved during the current frame.

[18] New X Index Register—The new Y index (NYI) register contains the new Y index value that applies to the data that has been moved during the current frame.

[19] Old X Index Register—The old X index (OXI) register contains the old X index value that applies to the data that not been moved.

[1A] Old Y Index Register—The old Y index (OYI) register contains the old X index that applies to the data that has been moved during the current frame.

[1B] Clip X Minimum Register—The clip X minimum (CXMN) register contains the X minimum value of the left clipping boundary. The value is a device coordinate and not affected by the index values.

[1C] Clip X Maximum Register—The clip X maximum (CXMX) register contains the X maximum value of the right clipping boundary. The value is a device coordinate and not affected by the index values.

[1D] Clip Y Minimum Register—The clip Y minimum (CYMN) register contains the Y minimum value of the top clipping boundary. The value is a device coordinate and not affected by the index values.

[1E] Clip Y Maximum Register—The clip Y maximum (CYMX) register contains the Y maximum value of the bottom clipping boundary. The value is a device coordinate and not affected by the index values.

Raster Operation Control Registers

The raster control registers, shown in Figure 7, are used to control the raster by selecting fast and slow operations, the source and destination origins, and scaling.

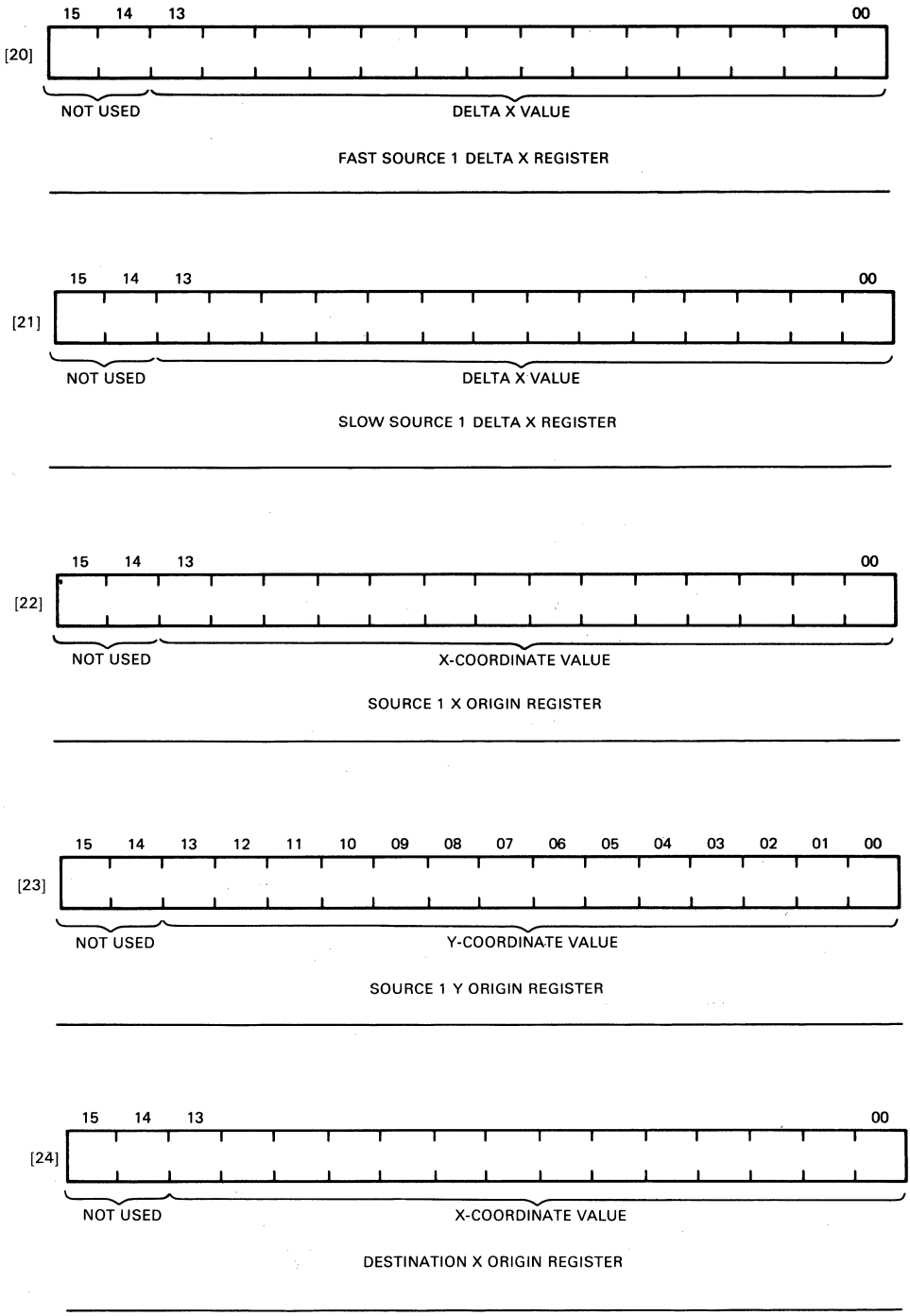

Figure 7 ▪ 78690 Raster Operation Control Register Format

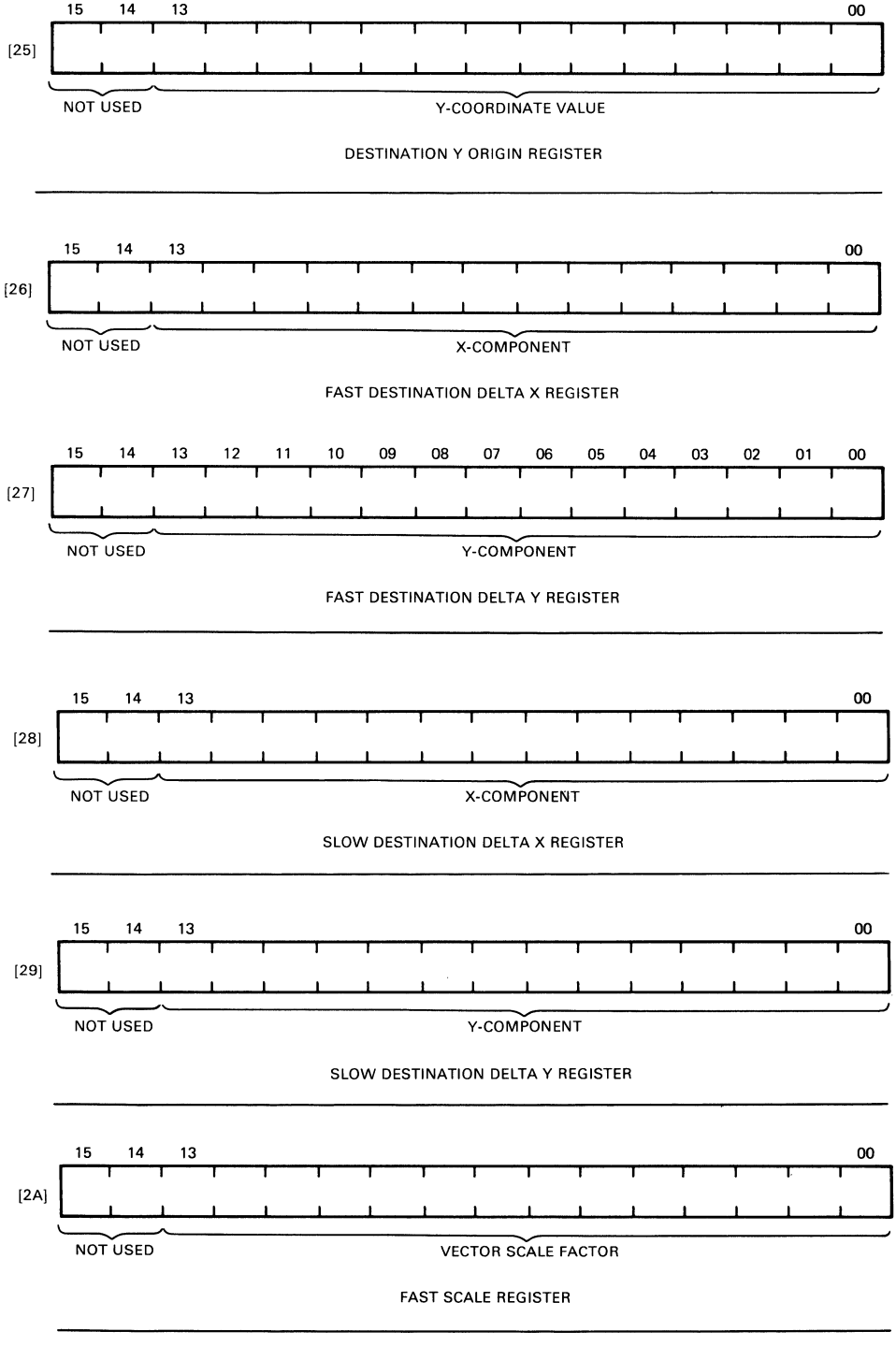

Figure 7 ▪ 78690 Raster Operation Control Register Format (Continued)

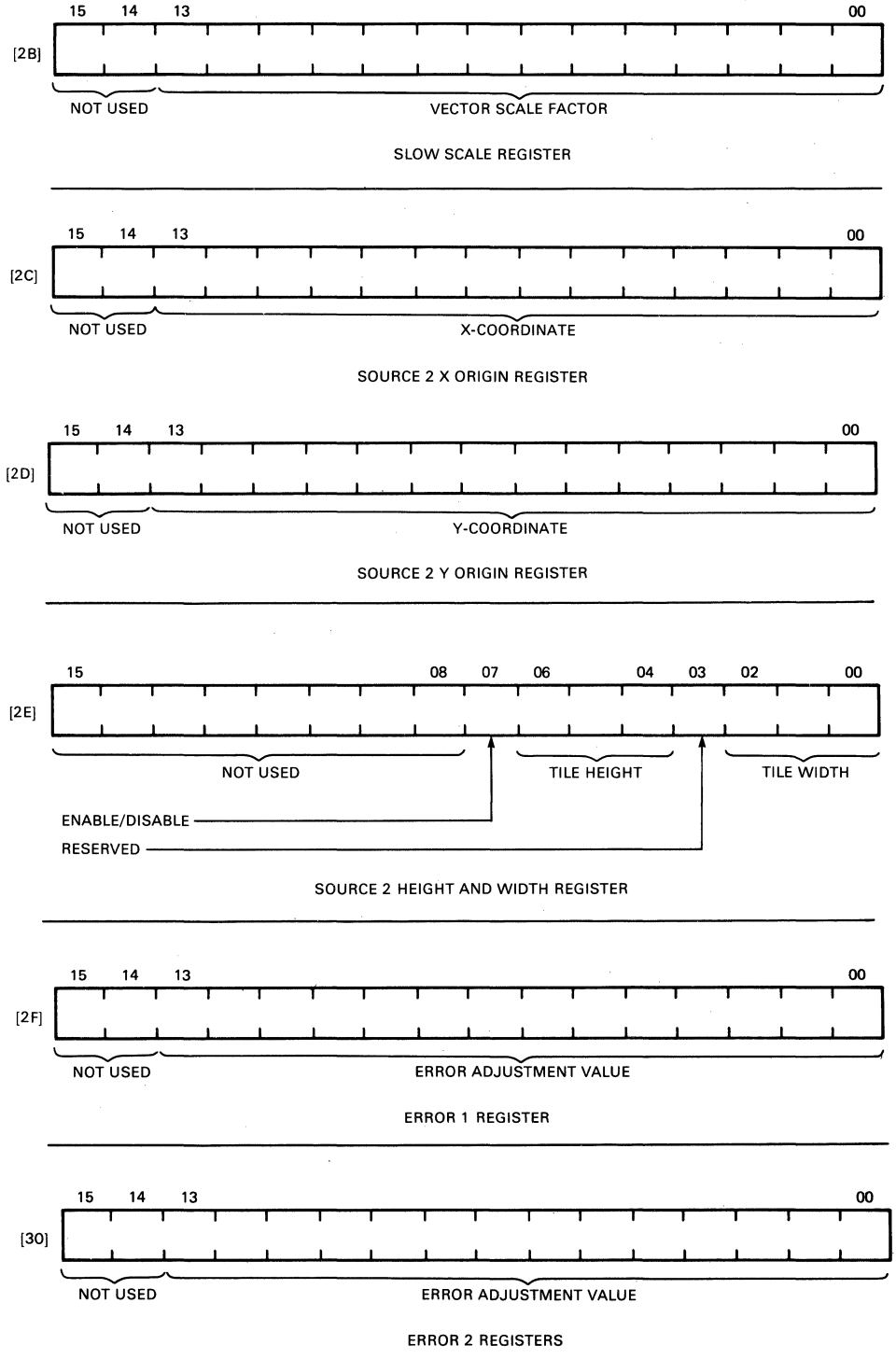

Figure 7 • 78690 Raster Operation Control Register Format (Continued)

[20] Fast Source 1 Delta X Register—The fast source 1 delta X (FSDX) register contains the value for the fast + or–delta X for source 1.

[21] Slow Source 1 Delta Y Register—The slow source 1 delta Y (SSDY) register contains the value for the fast + or–delta Y for source 1.

[22] Source 1 X Origin Register—The source 1 X origin (SX0) register contains the value for the X coordinate of source 1.

[23] Source 1 Y Origin Register—The source 1 Y origin (SY0) register contains the value for the Y coordinate of source 1.

[24] Destination X Origin Register—The destination X origin (DXO) register contains the value for X coordinate of the destination origin.

[25] Destination Y Origin Register—The destination Y origin (DYO) register contains the value for Y coordinate of the destination origin. This value can be a device or world coordinate depending on the destination selected for the index mode.

[26] Fast Destination Delta X Register—The fast destination delta X (FDX) register contains the value for the X component of the fast destination vector.

[27] Fast Destination Delta Y Register—The fast destination delta Y (FDY) register contains the value for the Y component of the fast destination vector.

[28] Slow Destination Delta X Register—The slow destination delta X (SDX) register contains the value for the X component of the slow destination vector.

[29] Slow Destination Delta Y Register—The slow destination delta Y (SDY) register contains the value for the Y component of the slow destination vector.

[2A] Fast Scale Register—The fast scale (FSC) register contains the fast vector scale factor for source 1 and destination in normal and linear pattern mode. Bit 13 = 0 selects upscaling and bit 13 = 1 selects downscaling. The binary point precedes bit 12.

[2B] Slow Scale Register—The slow scale (SSC) register contains the slow vector scale factor for source 1 and destination in normal and linear pattern mode. Bit 13 = 0 selects up scaling and bit 13 = 1 selects down scaling. The binary point precedes bit 12.

[2C] Source 2 X Origin Register—The source 2 X origin (S2XO) register contains the X coordinate of the source 2 origin that is added to the unindexed destination origin. The source 2 X origin is specified as an offset from the destination. No indexing is provided and it can be used to generate objects that are not on the display.

[2D] Source 2 Y Origin Register—The source 2 Y origin (S2YO) register contains the X coordinate of the source 2 origin. The source 2 Y origin is specified as an offset from the destination. No indexing is provided and it can be used to generate objects that are not on the display.

[2E] Source 2 Height and Width Register—The source 2 height and width (S2HW) register determines the size of the source 2 tile. The register bits are defined in Table 11.

Table 10 • 78690 Source 2 Height and Width Register Description

Bit	Description
7	Destination address bit function—Selects the destination address bits as follows: Bit 7 = 0: High bits of destination are truncated before adding to source 2 origin. Bit 7 = 1: All destination address bits are added to source 2 origin.
6:4	Tile height (H)—Selects the tile height. H = 0 to 7 which is $2^{(H+2)}$ from 4 to 512.
3	Reserved
2:0	Tile width (W)—Selects the tile width. W = 0 to 7 which is $2^{(W+2)}$ from 4 to 512. The tile width must not be set to less than the bus width.

[2F] Error 1 Register—The error 1 (ERR1) register contains the error adjustment vector added during raster initialization for the slow destination (B side) fill mode.

[2F] Error 2 Register—The error 2 (ERR2) register contains the error adjustment vector added during raster initialization for the fast destination in normal and linear pattern mode and for the source 1 (B side) in fill mode.

Screen Format Control Registers

The screen format control registers, shown in Figure 8, select the vertical and horizontal timing events, number of read cycles, bus width, and refresh rows.

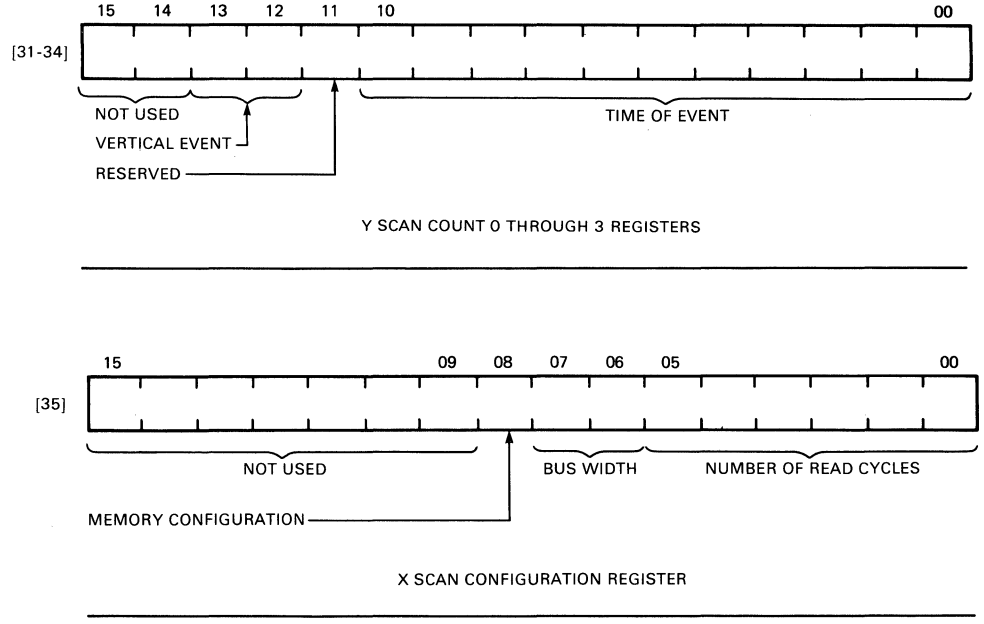

Figure 8 • 78690 Screen Format Control Register Format

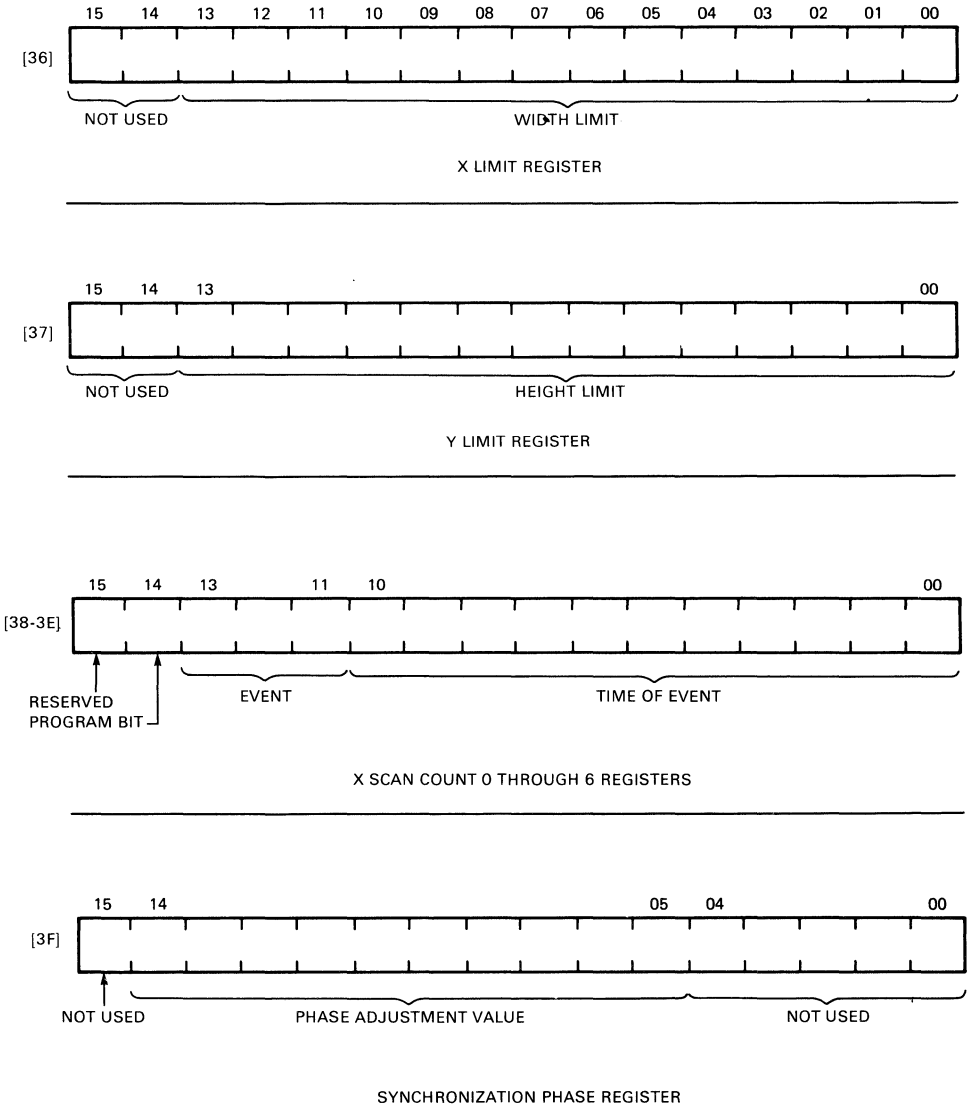

Figure 8 ▪ 78690 Screen Format Control Register Format (Continued)

[31-34] Y Scan Count Registers (0-3)—The Y scan count (YCT0 through YCT3) registers are used to program the vertical events. Each register determines the time for one vertical event, such as vertical blank time, in order of increasing time. If the horizontal period is an odd number of major cycles, the vertical period must be set for an even number of scans in a frame. Table 11 describes the function of the register information.

Table 11 • 78690 Y Scan Count Registers (0-3) Description

Bit	Description
13:12	Vertical event—Selects the vertical sync and blank events as follows: **Bit 13** / **Event 12** 0 0 End vertical period. Set vertical blank low in the following scan. 0 1 Set vertical blank high. 1 0 Set vertical sync low. 1 1 Set vertical sync high. Example: YCT0 sets vertical blank high, YCT1 sets vertical sync high, YCT2 sets vertical sync low, and YCT3 sets vertical blank low and restarts the vertical counter. The video control generates system sync request in the scan prior to deasserting vertical blank. The X scan registers determine the exact timing.
11	Reserved (must be zero)
10:0	Time of event—Determines the time of the event from the deassertion of vertical blank (in scans), except for vertical period, which is set to the number of scans in a frame minus one.

Clock Input Timing

The ac input parameters for the phase input clock signals PHI1 through PHI4 and the CAS signal are shown in Figure 9. The parameters are defined in Table 16.

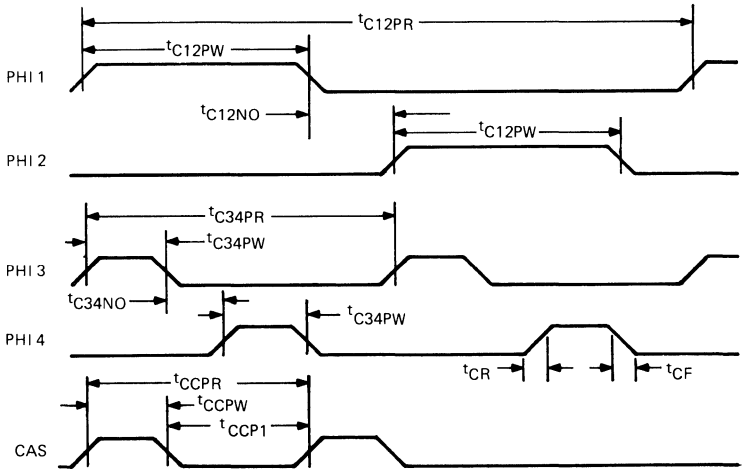

Figure 9 • 78690 Clock Input Timing

Table 16 • 78690 Clock Input Timing Parameters

Symbol	Definition	Requirements (ns) Min.	Max.
t_{C12PR}	Period of PHI1 and PHI2	228	684
t_{C34PR}	Period of PHI3 and PHI4	114	342
t_{CCPR}	Period of CAS	85.5	257
t_{C12PW}	Pulse width of PHI1 and PHI2	85.5	
t_{C34PW}	Pulse width of PHI3 and PHI4	28.5	
t_{CCPW}	Pulse width of CAS	28.5	
t_{CR}*	Rise time of PHI1, PHI2, PHI3, PHI4, CAS		5.0
t_{CF}*	Fall time of PHI1, PHI2, PHI3, PHI4, CAS		5.0
t_{C12NO}	Nonoverlap time of PHI1 and PHI2	23.5	
t_{C34NO}	Nonoverlap time of PHI3, PHI4	23.5	
t_{CCPL}	Low time between CAS pulses	57	

*Rise time is measured from 0.4 V to 2.7 V; fall time, from 2.7 V to 0.4 V.

Processor Interface Timing

The processor interface timing is shown in Figure 10 and the parameters listed on the figure are defined in Table 17.

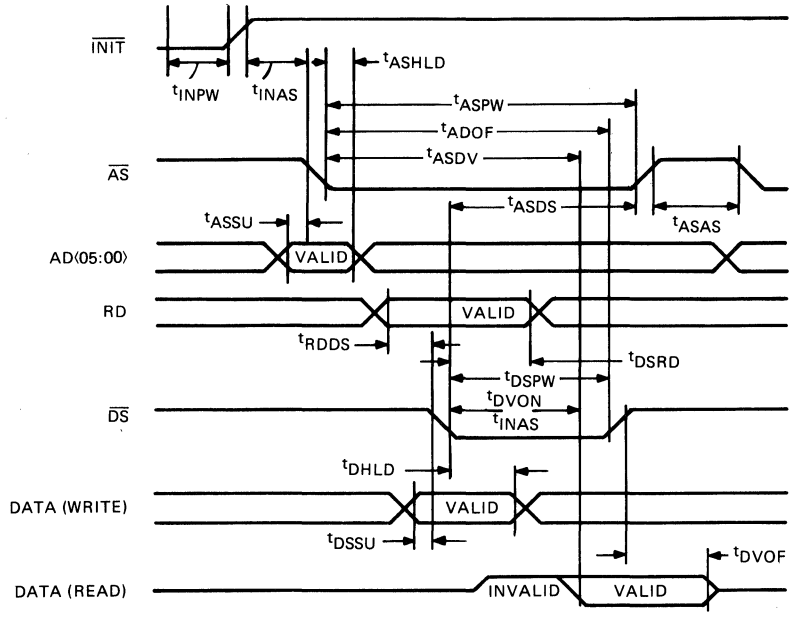

Figure 10 • 78690 Processor Interface Signal Timing

Table 17 • 78690 Processor Interface Timing Parameters

Symbol	Definition	Requirements (ns)* Minimum Read	Minimum Write	Maximum Read	Maximum Write
t_{ASAS}	The time that the $\overline{AS}$ input must not be asserted before being reasserted.	105	105		
t_{ASSU}	Setup time for valid input data on the ADD<5:0> inputs relative to the falling edge of the $\overline{AS}$ input.	0	0		
t_{ASPW}	Pulse width of the $\overline{AS}$ input if the $\overline{DS}$ input is not asserted.	180	180		
t_{ASHLD}	Hold time for valid input data on the ADD<5:0> after the falling edge of the $\overline{AS}$ input.	40	40		

[35] X Scan Configuration Register—The X scan configuration (XCON) register determines the bus widths, the number of read cycles, and the memory configuration. The register information is described in Table 12.

Table 12 • 78690 X Scan Configuration Register Description

Bit	Description
8	Memory configuration—Controls the number of row addresses refreshed on each scan.
7,6	Bus width—This mode is programmed in the video control and video processor before a bitmap memory access is performed as follows:

Bits 7	Bits 6	Bus width
0	0	4-bit
0	1	8-bit
1	0	undefined
1	1	16-bit

5:0	Number of read cycles—The number of major read cycles used for each scan. Normally set to the smallest integer greater than or equal to the number of pixels to be displayed on each scan divided by 128, 64, or 32 in the 16-, 8-, or 4-bit bus width mode, respectively.

[36] X Limit Register—The X limit (XL) register selects the width of the memory that will be read during the refresh process. This value must be the number of read cycles in the X scan configuration register multiplied by 128, 64, or 32 in 16-, 8-, or 4-bit bus width modes, respectively.

[37] Y Limit Register—The Y limit (YL) register selects the height of memory that will be read during the refresh process. This value is set to the memory height plus the number of extra scans required during down scrolling.

[38-3E] X Scan Count Registers (0-6)—The X scan count (XCT0 through XCT6) registers are used to program most of the horizontal timing events such as horizontal blank time. Each register determines the time of one horizontal event and the events are stored in the order of increasing time. The information in the register is defined in Table 12.

Table 13 • 78690 X Scan Count Registers (0-6) Descriptions

Bit	Description
15	Reserved—Reserved fot test. (normally zero)
14	Program bit—Set to one in the X scan count register following the X scan count register that contains the sync request event (bits 11:13). This must be cleared in the remaining X scan count registers.
13:11	Event—Selects the horizontal parameters as follows:

Bits 13	12	11	Event
0	0	0	Set horizontal blank low.
0	0	1	Set horizontal blank high.
0	1	0	Set horizontal sync low except during vertical sync.
0	1	1	Set horizontal sync high except during vertical sync.
1	0	0	Set horizontal sync low
1	0	1	Set horizontal synch high.
1	1	0	End horizontal period.
1	1	1	Set sync request event.

10:0	Time of event—Selects the time of event, in increments of 1/16 of a major cycle, from 3 1/4 major cycles that precede the start of the first memory cycle on a scan. The start of a memory cycle is at the rising edge of the PHI 2 input during the RAS precharge that begins the cycle.

[3F] Sync Phase Register—The sync phase (SYNP) register contains the sync phase adjustment value. This is the value that the video control loads into the horizontal sync counter at each system sync time (once per frame).

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the 78690 video control are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Power supply voltage (V_{DD}): 5.0 V ±5%
- Temperature range (T_A): 0°C to 70°C

Mechanical Configuration

The physical dimensions of the 78690 84-pin CERQUAD package are contained in Appendix E.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Power supply voltage (V_{DD}): −0.5 V to 6.0 V
- Input voltage applied (V_{in}): −0.5 V to 6.0 V
- Output voltage applied (V_{out}): −0.5 V to 6.0 V
- Power dissipation (P_D): 3.5 W at 0°C
- Active temperature (T_A): 0°C to 70°C
- Storage temperature: −55°C to 125°C

Recommended Operating Conditions

- Power supply voltage (V_{DD}): 5 V ±5%
- Temperature (T_A): 0°C to 70°C

dc Electrical Characteristics

The dc electrical parameters of the 78690 video control for the operating voltage and temperature ranges specified are listed in Table 14.

Table 14 • 78690 dc Input and Output Parameters

Symbol	Parameter	Test Condition	Requirements Min.	Max.	Units
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA	2.7		V
V_{OL}	Low-level output voltage DAT<15:0>	I_{OL} = −5 mA		0.5	V
V_{OL}	Low-level output voltage all other outputs	I_{OL} = −5 mA		0.4	V
CLK_{IH}	Clock input high level		2.7		V
CLK_{IL}	Clock input low level			0.4	V
I_{DD}	Active supply current	V_{DD} = max		0.66	mA

Symbol	Parameter	Test Condition	Requirements Min.	Requirements Max.	Units
I_{IH}	Input high leakage current	V_{DD} = max $V_{in} = V_{DD}$(max)		20	μA
I_{IL}	Input low leakage current	V_{DD} = max V_{in} = 0 V		-20	μA
I_{ZH}	Hi-impedance input high leakage current	V_{DD} = max $V_{in} = V_{DD}$(max)		20	μA
I_{ZL}	Hi-impedance input low leakage current	V_{DD} = max V_{in} = 0 V		-20	μA
C_{in}	Input capacitance			10	pF
C_{IO}	Input/output capacitance			10	pF

ac Electrical Characteristics

The ac timing parameters for the 78690 video control are grouped according to clock input, processor interface, instruction/data bus, memory interface, and monitor timing and synchronization request. Table 15 lists the ac input specifications.

Table 15 • 78690 ac Test Limits and Specifications

Symbol	Definition	Requirements Min.	Requirements Max.	Units
C_{in}	Input capacitance		10	pF
C_{io}	Input/output capacitance		10	pF
t_{IR}	Input signal rise time		10	ns
t_{IF}	Input signal fall time		10	ns

The following conditions apply to the ac test conditions unless otherwise stated.

- The delay times extend from the 1.5 V level of the clock input to the V_{OH} or V_{OL} level of the measured signal.
- The rise times are measured from the 10% to 90% level of the signal transitions. Fall times are measured from the 90% to 10% of the signal transitions.
- The measurements are with a 50 pF capacitive load on the outputs. Exceptions to this are outputs ID<07:00> that have a 500 pF load, and DAT<15:00> that have a varying load up to 500 pF.

Symbol	Definition	Requirements (ns)* Minimum Read	Minimum Write	Maximum Read	Maximum Write
t_{ASDS}	The time from assertion of the $\overline{DS}$ input to deassertion of the $\overline{AS}$ input.140	140	75		
t_{DSSU}	Setup time for valid data on the DAT<15:0> inputs relative to the falling edge of the $\overline{DS}$ input during bus write operations.	—	0		
t_{DSPW}	Pulse width of the $\overline{DS}$ input.	140	95		
t_{RDDS}	The time for valid input on the RD input before the assertion of the $\overline{DS}$ input.	30	30		
t_{DSRD}	Hold time for the RD input after the falling edge of the $\overline{DS}$ input until the deassertion of the $\overline{DS}$ input.	40	40		
t_{DHLD}	Hold time for valid data on the DAT<15:0> inputs after the falling edge of $\overline{DS}$ input during bus write operations.	—	40		
t_{DVON}	Delay time for valid data on the DAT<15:0> outputs relative to the falling edge of the $\overline{DS}$ input during bus read operations with a 50-pF capacitive load on the outputs.	—	—	140	
t_{DVONA}†	Delay time for valid data on the DAT<15:0> outputs relative to the falling edge of the $\overline{DS}$ input during bus read operations with a 500-pF capacitive load on the outputs.	—	—	410	
t_{DVOF}	Hold time with previous data valid on the DAT<15:0> outputs after the rising edge of $\overline{DS}$ during bus read operations	0	—	50	
t_{INAS}	The time from deassertion of the $\overline{INIT}$ input to the assertion of the $\overline{AS}$ input.	100	100		
t_{INPW}‡	Pulse width of the $\overline{INIT}$ input.	12×t	12×t		
t_{ADOF}	The time from assertion of the $\overline{AS}$ input to deassertion of the $\overline{DS}$ input.	180	135		
t_{ASDV}	Delay time for valid data on the DAT<15:0> outputs relative to the falling edge of the $\overline{AS}$ during bus read operations.	—	—	180	

*Timing is measured at the V_{OH} and V_{OL} levels

†t_{DVONA} = t_{DVON} +60 ns per 100-pF capacitance additional loading. (Intermediate values may be calculated.)

‡This parameter is 12 × t where t = PHI1 or PHI2 clock period.

Instruction/Data Bus Timing

Figure 11 shows the instruction/data bus signal timing and the timing parameters are listed in Table 18.

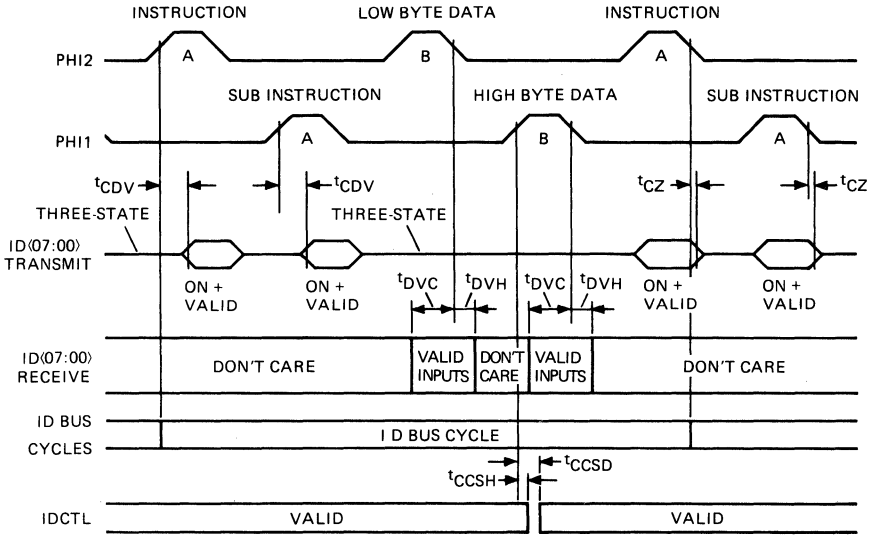

Figure 11 • 78690 Instruction/Data Bus Signal Timing

Table 18 • 78690 Instruction/Data Bus Timing Parameters

Symbol	Definition	Requirements (ns) Min.	Max.
t_{CDV}	Maximum delay time for valid output data on the ID<7:0> lines relative to the rising edge of the PHI1 A and PHI2 A input.		60
t_{CZ}*	Delay time from the falling edge of the PHI1A and PHI2A input to the high-impedance level on the ID<7:0> lines.	5.0	25
t_{DVC}	Minimum setup time for valid input data on the ID<7:0> lines relative to the falling edge of the PHI1 B and PHI2 B input.	20	
t_{DVH}	Minimum hold time for valid input data on the ID<7:0> lines after the falling edge of PHI1 B and PHI2 B input.	5.0	
t_{CCSH}	With previous output data valid, t_{CCSH} is the minimum hold time on the IDCTL output relative to the rising edge of the PHI1 B signal. (PHI1 B is used but time is referenced to the PHI1 signal.)	0	
t_{CCSD}	Maximum delay time for valid data on the IDCTL output relative to the PHI1 B signal going high. (PHI1 B is used but time is referenced to the PHI1 signal.)		75

*t_{CZ} is measured from the deasserted level of the 1.5-V clock input to the high-impedance level of the ID bus.

Memory Interface Timing

Figure 12 shows the memory interface signal timing and the timing parameters are listed in Table 19.

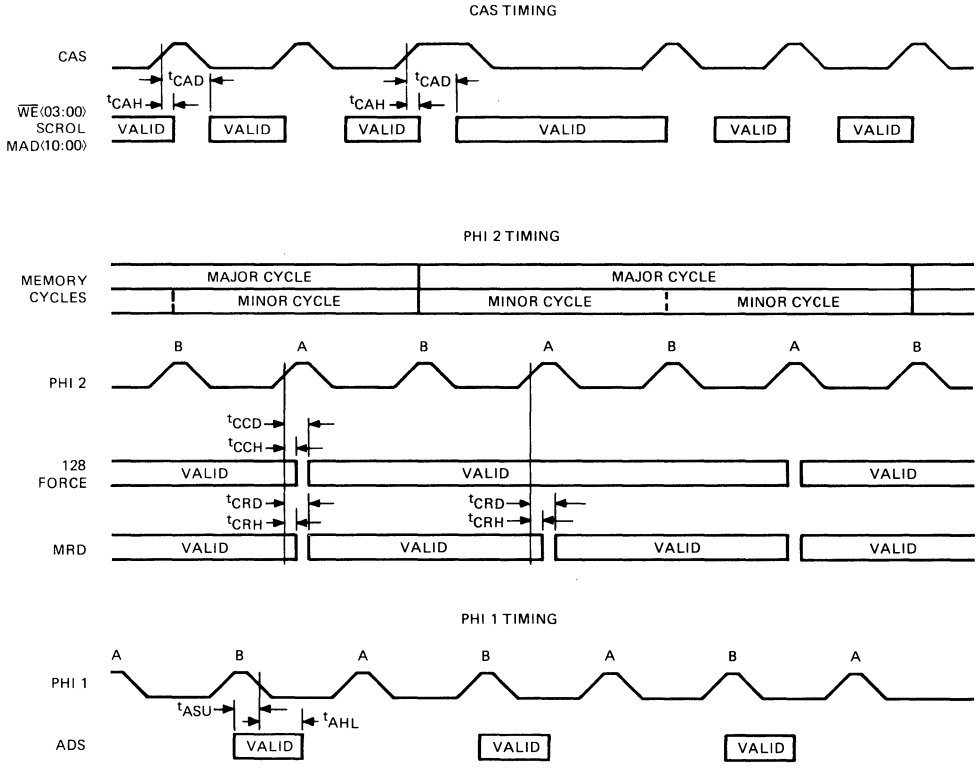

Figure 12 • 78690 Memory Interface Signal Timing

Table 19 • 78690 Memory Interface Timing Parameters

Symbol	Definition	Requirements (ns) Min.	Max.
t_{CAH}	The delay time that the previous output of the MAD<10:0>, $\overline{WE}$<3:0>, and SCROL signals is valid after the rising edge of the CAS input.	8.0	
t_{CAD}	The delay time for valid outputs of the MAD<10:0>, WE, and SCROL signals after the rising edge of the CAS input.		55
t_{CCH}	The delay time that the previous output of the 128/$\overline{16}$ and FORCE signals is valid after the rising edge of PHI2 A input.	5.0	

Symbol	Definition	Requirements (ns) Min.	Max.
t_{CCD}	The delay time for valid output of the 128/$\overline{16}$ and FORCE signals after the rising edge of the PHI2 A input.	55	
t_{CRH}	The time that the previous output of the MRD signal is valid after the rising edge of the PHI2 A input.	5.0	
t_{CRD}	The delay time for valid output of the MRD signal after the rising edge of the PHI2 A input.	55	
t_{ASU}	The setup time for valid input of the ADS signal relative to the falling edge of the PHI2 B input.	50	
t_{AHL}	Minimum hold time for valid input of the ADS signal relative to the falling edge of PHI1 B		27

Monitor Timing and Synchronization Request Timing

During the synchronization interval, the PHI1, PHI2, PHI3, and PHI4 clock inputs are set to a low level, and the CAS input is set to a high level. Figure 13 shows the normal and synchronization clock timing and the parameters are listed in Table 20. The SYNC input parameters are valid for the SYNC request from the video control or from another source. The clocks continue after the SYNC interval.

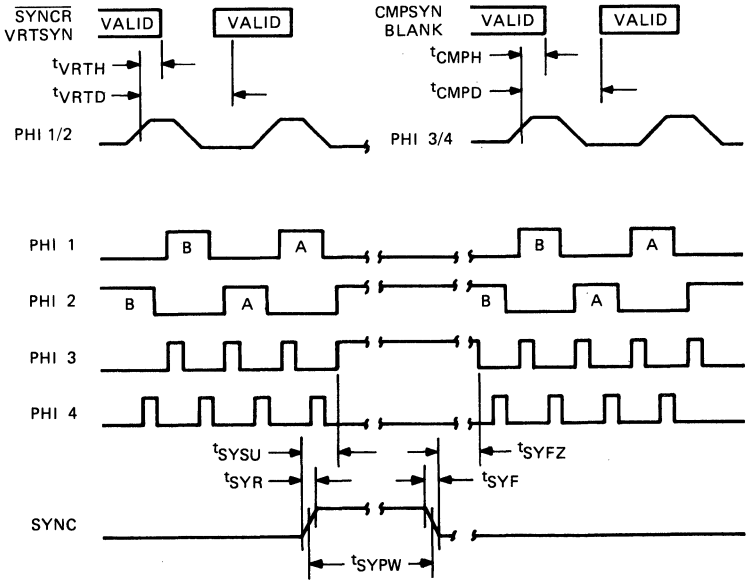

Figure 13 • 78690 Monitor and Synchronization Request Signal Timing

Table 20 • 78690 Monitor and Synchronization Request Timing Parameters

Symbol	Definition	Requirements (ns) Min.	Max.
t_{VRTD}	The delay time for valid output of the VSYNC or $\overline{SYNCR}$ signal relative to the rising edge of the PHI1 or PHI2 input.		90
t_{VRTH}	The delay time that the previous output of the VSYNC or $\overline{SYNCR}$ signals is valid relative to the rising edge of the PHI1 or PHI2 inputs.	0	
t_{CMPD}	The delay time for valid output of the CMPSYN or BLANK signals relative to the rising edge of the PHI3 or PHI4 input.		45
t_{CMPH}	The delay time that the previous output of the CMPSYN or BLANK signals is valid relative to the rising edge of PHI3 or PHI4 inputs.	5.0	
t_{SYSU}	Minimum delay from the assertion of the SYNC signal to the PHI2 input going high. This delay starts the clock freeze period that is a restriction of the external clock generation control.	0	
t_{SYPW}*	The pulse width of the SYNC signal.	800	24 µs
t_{SYFZ}*	The delay time from the deassertion of SYNC to the end of the clock freeze time. This delay is a restriction of the external clock generation control.	400	24 µs
t_{SYR}	Input rise time of the SYNC pulse.		50
t_{SYF}	Input fall time on the SYNC pulse.		50

*t_{SYPW} + t_{SYFZ} must be equal to (or be a multiple of) 16 periods of the PHI1 or PHI2 inputs.

Interrupt and Request Signal Timing

The signal timing for the interrupt and request are listed and defined in Table 21.

Table 21 • Interrupt and Request Timing Parameters

Symbol	Definition	Requirements (ns) Min.	Max.
t_A	The assertion propagation delay for the $\overline{INT}$ or $\overline{REQ}$ signal in response to a status bit being set when the corresponding bit of the Interrupt or Request Enable register has been set previously. Delay t_A is measured from the edge of the $\overline{DS}$ or system clock signal that sets the status bit.	0	140
t_D	The deassertion propagation delay for the $\overline{INT}$ or $\overline{REQ}$ signal in response to a status bit being cleared when the corresponding bit of the Interrupt or Request Enable register has been set previously. Delay t_D is measured from the edge of the $\overline{DS}$ signal that clears the status bit.	0	140
t_{AM}	The assertion propagation delay for the $\overline{INT}$ or $\overline{REQ}$ signal in response to setting a bit of the Interrupt or Request Enable register when the corresponding status bit has been set previously. Delay t_{AM} is measured from the edge of the $\overline{DS}$ signal that sets the Interrupt or Request Enable register bit.	0	180
t_{DM}	The deassertion propagation delay for the $\overline{INT}$ or $\overline{REQ}$ signal in response to clearing a bit of the Interrupt or Request Enable register when the corresponding status bit has been set previously. Delay t_{DM} is measured from the edge of the DS signal that initiates the resetting of the Interrupt or Request register bit.	0	180

• Interfacing Techniques

Up to twenty-four 78660 video processors may be used with each video control. The video control includes a system interface, a bit-map memory interface, and a display interface as shown in Figure 3. Refer to the *Dragon Video System Hardware Specification* for a complete description of a video system using the 78660 video processor and 78690 video control.

The system interface connects the video control to the local processor or DMA controller through the processor interface. The processor interface transfers 16 data bits, 6 address bits and 6 control bits and receives the parameters and commands from the local processor. The interface handles register accesses and controls timing and all necessary bus signals to allow the video control to act as a bus slave to the local processor or DMA device. The system interface also connects the video control to the instruction/data bus through the ID interface.

The ID interface transfers information on the 8-bit bidirectional instruction/data bus and the chip select control line. The instruction/data (ID) bus is used to transfer information within the video processor and to controls its operation. It is used to load and read registers and to execute direct or indirect instructions.

The bit-map memory interface includes the bit-map memory address bus and the signals that control it. It transfers address information on 11 lines, write enable information on 4 lines, and control information on 5 lines.

The display interface connects to the monochrome or color monitor interface for video and timing. The interface signals include the four synchronization and blanking signals.

The video control requires a 5-Vdc power supply.