Features

- Two FIFO buffers for screen refresh and scrolling
- Four-bit wide video serial output
- Background fill on scroll
- Barrel shifter to align and scroll data
- Two mask registers to window write destination data
- 16 logic functions to combine source and destination data
- Two control store RAMs for source 1, source 2 and destination operations
- Data transfer in either X- or Z-mode
  —X-mode, one word = 16 pixels per plane
  —Z mode, one word = 16 planes per pixel

Description

The video processor (Viper) chips are available in two versions. The 78660 video processor is a 68-pin, HMOS VLSI version that provides a frame refresh rate of 60 Hz and has a power consumption of 1.9 W. The 78680 video processor is a 68-pin, CMOS VLSI version that provides a frame refresh rate of 80 Hz and has a power consumption of 0.5 W. Figure 1 is a block diagram of the video processor.

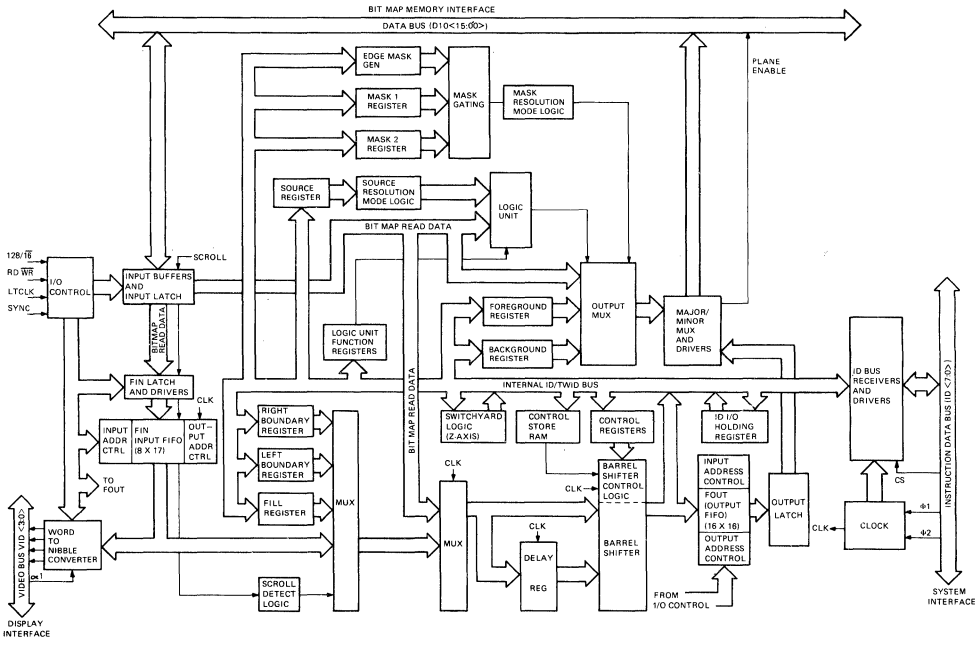

Figure 1 • 78660/78680 Video Processor Block Diagram

The video processor is data-path chip that is used with the 78690 video control (Adder) chip to implement a high-performance, bit-map graphics system with a color or monochrome display. The video processor provides high-speed parallel processing of video data such as transfers of data into and out of a bit map memory plane. The video processor receives commands from the video control and performs the data manipulation required for screen refresh, scrolling of windows, and screen updates.

• Pin and Signal Description

This section provides a brief description of the input and output signals and power and ground connections for the 78660/78680 video processor 68-pin CERQUAD package. The pin assignments are identified in Figure 2 and the signals are summarized in Table 1.

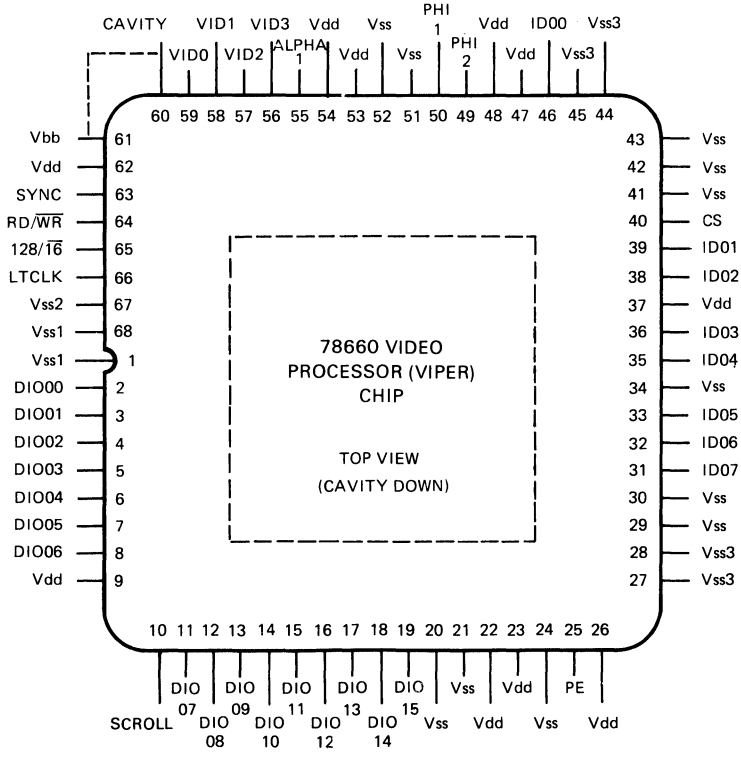

Figure 2 • 78660/78680 Pin Assignments

Table 1 • 78660/78680 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
1,68	V_{SS}	input	Ground—Ground reference for the DIO<15:0> lines.
2-8, 11-19	DIO<15:0>	input/output	Data bus—Bidirectional data lines.
9,22,23, 26,37,47 48,53,54, 62	V_{DD}	input	Voltage—Power supply 5 Vdc
10	SCROLL	input	Scroll—Specifies the word to be scrolled
20,21,24 29,30,34 41-43, 51,52	V_{SS}	input	Ground—Ground reference for internal logic.
25	PE	output	Plane enable—Enables a write to bit-map memory.
27,28, 44,45	V_{SS}	input	Ground—Ground reference ID<7:0> and PE
31-33, 35,36,38 39,46	ID<7:0>	input/output	Instruction/data bus—A bidirectional data bus.
40	CS	input	Chip select—Enables an instruction to be received.
49,50	PH1,PH2	inputs	Phase 1 and Phase 2—Clock signals for timing.
55	ALPHA1	input	Specifies a data transfer on VID<3:0> lines.
56-59	VID<3:0>	output	Video—Video output lines to refresh the display.
60*	CAVITY		Cavity—The 78660/78680 chip substrate.
61*	V_{BB}	output	Voltage—Voltage generator output.
63	SYNC	input	Synchronize—Initializes internal logic and updates registers.
64	RD/$\overline{WR}$	input	Read/write—Specifies a bit-map read or write operation.

Pin	Signal	Input/Output	Definition/Function
65	128/$\overline{16}$	input	Selects a 128-bit process for screen refresh or 16-bit process for updating bit-map memory.
66	LTCLK	input	Latch clock—Clock timing to latch data on DIO<15:0> lines.
67	V_{SS2}	input	Ground—Ground reference for V_{BB}.

*Not bonded after date code 8614.

Bit Map Interface Signals

Bit-map Data Input/Output (DIO<15:0>)—These lines contain the bit-map data input and output data to each bit map memory. When the RD/$\overline{WR}$ signal is high, the DIO<15:0> output drivers are a high-impedance state.

Scroll (SCROLL)—This signal determines which of the data words received on the DIO<15:0> lines are to be scrolled.

Plane Enable (PE)—This signal determines if the bit-map memory may process a write operation.

128 or 16-bit Mode (128/$\overline{16}$)—When high, this signal enables the processing of 128 bits for screen refresh and scrolling operations. When low, 16 bit bit-map update operations are enabled.

Bit-map Memory Read/Bit-map Memory Write (RD/$\overline{WR}$)—When high, this signal allows the video processor to receive bit-map memory data and the DIO<15:0> are a high-impedance state. When low, the falling edge of the RD/$\overline{WR}$ signal latches the bit-map memory data on the DIO<15:0> lines and enables the DIO<15:0> output drivers.

Latch Clock (LTCLK)—When the RD/$\overline{WR}$ and 128/$\overline{16}$ lines are high, the trailing edge of the LTCLK signal latches in bit-map memory data on the DIO<15:0> lines. When this line is low and the 128/$\overline{16}$ line is high, the leading edge of LTCLK causes valid scrolled data to be shifted out on the DIO<15:0> lines.

Synchronize (SYNC)—This pulse initalizes all internal control flip-flops and latches and updates some master-slave registers.This signal does not perform the function of a reset input.

Video Bus Interface Signals

Video (VID<3:0>)—The rising edge of the ALPHA 1 signal shifts the screen refresh data out on these lines.

ALPHA 1—This signal causes the data to be shifted to the VID<3:0> lines.

Instruction/Data Bus Interface Signals

Phase 1 and Phase 2 Clocks (PHI1 and PHI2)—These are nonoverlapping clock inputs that determine the overall timing and control of the video processor.

Chip Select (CS)—When line ID<7> is high, this signal is asserted to allow the incoming instruction to be latched and executed. If line ID<7> is low, the incoming instruction is ignored when the CS signal is asserted. When receiving data on lines ID<7:0>, the polarity of CS and/or ID7 is irrelevant.

Instruction Data (ID<7:0>)—These input and output lines normally remains in a high-impedance state during input instructions and data. The output drivers are enabled by the internal execution of Z-axis or control store RAM instructions.

Power and Ground Connections

Power Supply (V_{DD})—Supplies 5 Vdc power to the 78660/78680 video processor.

Ground (V_{SS})—Ground reference for all internal logic except for the output drivers.

Ground (V_{SS1})—Ground reference for the output drivers of lines DIO<15:0>.

Ground (V_{SS2})—Ground reference for the LTCLK, RD/$\overline{WR}$, 128/$\overline{16}$ and SYNC input signals.

Ground (V_{SS3})—Ground reference for the ID<7:0>, VID<3:0>, and PE signals.

Cavity—Chip substrate that connects to V_{BB} pin 60.

Architecture Summary

A typical bit-map processor system, shown in Figure 3, consists of high-speed timing logic, a local processor or remote processor that performs DMA operations, the 78690 video control, the 78660/78680 video processor, bit-map memory planes, and the color map and shift register logic. The timing logic generates the system clock pulses. The local processor provides the commands to update the video control memory. The video control performs functions that are common to all memory planes such as raster computation operations, scan timing, system status generation, and memory address generation. Each video processor transfers information into and out of its bit-map memory plane. The output data is transferred through the shift register to a color map and digital-to-analog converter to provide the composite video to a monitor.

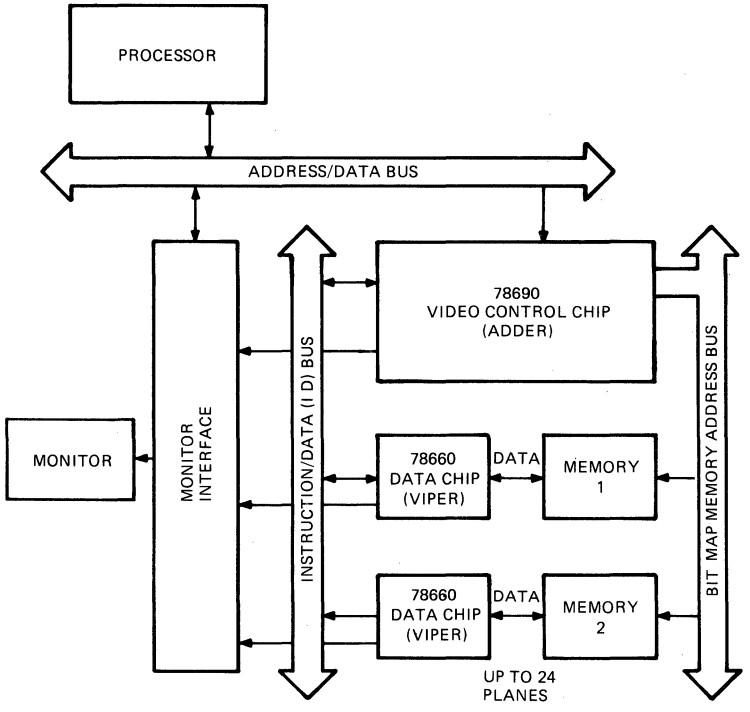

Figure 3 • 78660/78680 Typical Bit-map Graphics System Configuration

The video processor communicates through the instruction/data (ID) bus, the bit-map memory address bus, and the display video bus.

The source, destination, barrel-shift constant, and edge mask data is transferred to the video processor registers through the ID bus which controls the operation of the video processor. The ID bus is used to load and read registers and to execute direct or indirect instructions. Data can be also be exchanged between the registers of other video processors through this bus. During a source operation, the video processor receives the source information from the video control and locates the source in the bit-map memory. During the destination operation, the video processor receives a destination code and an edge mask to determine which bits of the data bus are to be written.

The display memory bus transfers the address required to automatically refresh the memory, the scrolling information, and the screen update information.

The display video bus connects the video processor to the display circuits including the shift registers, color map, and digital-to-analog converters.

Hardware Description

The following paragraphs provide a brief description of the major hardware functions of the video processor shown in Figure 1.

Input FIFO—The 8-bit by 17 word first-in/first-out (FIFO) buffer permits uninterrupted data flow between bit-map memory and the external display circuits for screen refreshing. The maximum data rate into the input FIFO buffer is approximately 11.5 MHz.

Word-to-nibble Converter—This converter reads the input FIFO buffer, divides the word into 4-bit nibbles, and transfers the nibbles to the video output bus. The maximum clocking rate of the converter is approximately 17.2 MHz.

Output FIFO—Because of the timing constraints, the video processor stores the scrolled data in the dynamic 16-bit by 16-word output FIFO buffer before returning the data to the bit-map memory. The maximum data rate from the output FIFO is approximately 11.5 MHz. Data should not remain in the FIFO buffer for more than 30 microseconds. Any test vector rate should therefore be greater than 1.25 Mhz (less than 800 ns per vector).

Barrel Shifter—The 16-bit barrel shifter is used to provide horizontal motion on the screen. The barrel shifter multiplexes the independent processes of scrolling and updating the bit-map memories so they occur concurrently.

Fill Register—During horizontal scrolling, the video procesor creates voids at the left and right edges of the scrolled regions. The fill register holds the data pattern to fill in the voids.

Left and Right Boundary Registers—These registers contain masks that determine the actual bit positions of the edges of the scrolling region.

Logic Unit, Source Register, and Mask Registers—During bit map updates, the logic unit performs logical operations between data in the source register and incoming bit-map memory data. The Mask 1 and Mask 2 registers determine those bits within a 16-bit field that the logic unit will modify. The logic unit performs 16 possible operations by selecting data in the foreground or background register for output to the DIO<15:0> lines.

Switchyard Logic—This logic transfers 1-, 2-, or 4-bits that are received on the ID bus to the 16-bit internal TWID bus. The number of bits received depends on the selection of full-, half-, or quarter-resolution mode. The bits on the TWID bus are transferred to the source, fill, foreground, or background register. The switchyard logic is used for Z-axis bit-map memory update operations.

ID I/O Holding Registers—These registers provide buffering between the 8-bit ID bus and the 16-bit internal TWID bus.

Edge Mask Generator—The edge mask generator converts an 8-bit code into a 16-bit mask, which is a window of variable width and position for raster operations. It may be placed anywhere within a 16-bit field.

Scroll Constant Register—This register stores barrel shifter control data. The scroll constant provides shift magnitude and direction. One register bit determines the up or down scroll direction and one bit enables the memory plane when writing scroll data back to the bit-map memory.

Plane Address Register—This register stores the device address. The video control compares the value in this register to the incoming address to determine if a Z-axis instruction should be executed.

Resolution Mode and Bus-width Mode Registers—These registers control the operating modes of the video processor.

Logic Unit Function Register—Four registers that control the logic unit and logic unit functions.

Control Store RAM (CSR)—Six registers that provide indirect instruction execution to control the origin and destination of data transferred on the internal TWID bus and the external ID bus.

Programming Functions

The following types of instructions are available to the applications programmer.

Register load—The register load instructions are used to load data in one of the 22 addressable registers in the video processor. Two registers are available for mode selection, four registers for direct address control, six registers for data storage, and ten registers for indirect control functions.

Z-dimension color codes—Color information is received from the address processor and is written into one of the four data registers—source, fill, foreground, and background. Up to 16 video processor chips can be addressed in parallel at the same time. During a Z-read cycle, all color data for a specific pixel can be accessed in parallel from the memory planes.

Active cycles—During an indirect data transfer between the bit-map memory planes and the address processor, one video processor transmits the information, and the remaining video processors can receive the data and store it in one of three data registers.

The video processor has a programmable indirect instruction set, which allows the address processor in a video subsystem to command direct memory access (DMA) operations between any memory components of the video subsystem. This enables data to be translated, rotated, and scaled. The video processor performs the following data transfer cycles.

Screen refresh—During this cycle, the data in the video memory is sampled and transferred to the video circuits.

Scroll—During this cycle, data in bit-map memory is read, barrel shifted, and written into the bit-map memory resulting in a scroll operation within a defined window of the display.

Bit-map update—This cycle requires an instruction and data. The type of instruction determines the source of data, indicates the destination of the data, and determines the disposition of the data at the new location.

Modes of Operation

The 78660/78680 video processor operates in the following modes.

Bus width mode—This mode allows the user to select an effective bus width of 4, 8, or 16 bits to optimize the cost advantages from low-density, partial page displays to high-density RAMs.

Resolution mode—This mode enables the programming of color or intensity changes by 1, 2, or 4 bits. An increase in the intensity or color results in a decrease in the resolution on which those changes can be made. The resolution mode can be used effectively with terminals with low plane counts.

Axis mode—This mode provides a method of data transfer to a group of planes that overlap each other in the Z dimension, as opposed to the normal transfer between pixels in the same plane.

Register Descriptions

The video processor contains 22 user-loadable, static registers that combine data and control instructions. The width of the registers is 16 bits. However, many of the registers operate with less than 16 bits. The information written into the registers cannot be read. A register is accessed by the least significant 5 bits of ID<7:0> lines. Figure 4 shows the register load transfer sequence. The ID bus instruction is a one-byte code and most instructions are followed by a 16-bit data transfer or subinstruction as listed:

Parameter	Meaning
IN	Instruction
SI	Shift constant
LB	Data source–low byte
HB	Data source–high byte

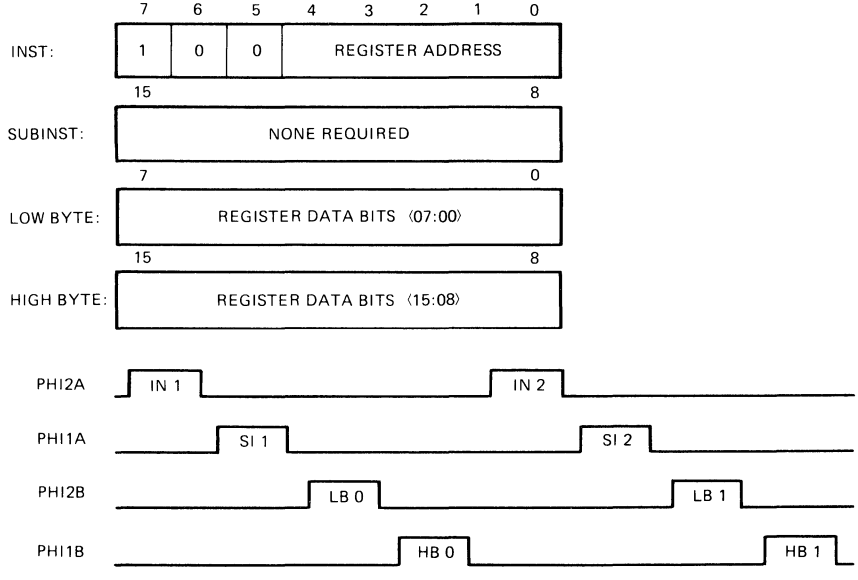

Figure 4 • 78660/78680 Register Load Data Transfer Model

The video processor registers, type, and address assignments are listed in Table 2. Three of the registers are reserved.

Table 2 • 78660/78680 Register Address Assignments

Address (hexadecimal)	Register Name	Width	Type
0	Resolution mode	1:0	Mode
1	Bus width	3:2	Mode
2	Scroll constant	6:0	Direct control
3	Plane address	5:0	Direct control
4	Logic function 0	7:0	Indirect control
5	Logic function 1	7:0	Indirect control
6	Logic function 2	7:0	Indirect control
7	Logic function 3	7:0	Indirect control
8	Data mask 1	15:0	Data
9	Data mask 2	15:0	Data
A	Source	15:0	Data
B	Fill	15:0	Data
C	Left scroll boundary	15:0	Direct control
D	Right scroll boundary	15:0	Direct control
E	Background	15:0	Data
F	Foreground	15:0	Data
10	Control store RAM (CSR0)	6:0	Indirect control
11	Control store RAM (CSR1)	6:0	Indirect control
12	Control store RAM (CSR2)	6:0	Indirect control
13	Reserved		
14	Control store RAM (CSR4)	6:0	Indirect control
15	Control store RAM (CSR5)	6:0	Indirect control
16	Control store RAM (CSR6)	6:0	Indirect control
17	Reserved		
18	Reserved		

The data and direct control registers A through F (hexadecimal) are 16-bit registers that are loaded by the ID bus load register commands. The mask and source registers are loaded by data transfers during the rasterop cycles. The source and fill registers can be loaded with a data constant to select a solid color during Z-axis register load commands. The least significant bit of the word determines the left pixel and the most significant bit determines the right pixel on the display.

Resolution mode—The resolution mode register controls the action of the mask bits (mask 1, mask 2, and edge mask), the source register, the barrel shifter constant, and the Z-axis command. This mode allows the 78660/78680 video processor to respond as 1, 2, or 4 planes. Figure 5 shows the format of the register and Table 3 lists the functions of the register information. Because each video processor can be programmed for a different resolution, the single barrel-shifter constant should be truncated for low-resolution applications except when scrolling. Horizontal scrolling should be used for the lowest-resolution plane to prevent errors caused by truncating to result in the scrolling of an undesired region.

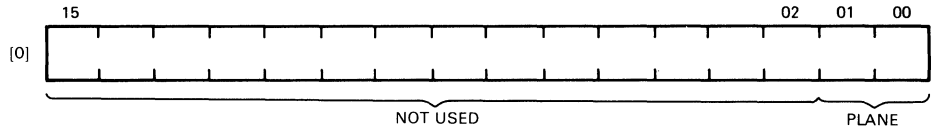

Figure 5 • 78660/78680 Resolution Mode Register Format

Table 3 • 78660/78680 Resolution Mode Register Description

Bit	Description			
15:2	Not used.			
1:0	Planes—Defines the planes of response as follows:			
	Bit 1	**Bit 0**	**Plane**	**Description**
	0	0	1	Full resolution
	0	1	2	Half resolution
	1	0	3	Undefined
	1	1	4	Quarter resolution

Plane 1—When plane 1 is specified, each bit in the mask registers and source register controls its respective mask multiplexer or logic unit bit independently of the remaining bits. The plane address can be programmed to any value and all barrel shifter constants are significant. During Z-axis operations, the video processor receives or transmits the bit that corresponds to its plane address.

Plane 2—When plane 2 is specified, the even and odd mask or source bits are OR gated, and the results are used to control the corresponding mask multiplexer or logic unit bits. The least significant bits of the barrel shifter constant is truncated so that the data will move only by a multiple of 2 bits. During Z-axis operations, the video processor receives or transmits 1 bit that corresponds to its plane address and the next most significant bit. The plane address bit must be programmed to an even value.

Plane 4—When plane 4 is specified, the 4 mask or source bits are OR gated and the results are used to control the corresponding mask multiplexer or logic unit bits. The two least significant bits of the barrel shifter constant are truncated so that the data will move only by a multiple of 4 bits. During Z-axis operations, the video processor receives or transmits the four bits that correspond to its plane address and the next most significant bit. The plane address bit must be programmed to a multiple of four.

Bus width—The bus width register selects the number of video bus bits depending on the number of pixels required for the display. The 78660/78680 video processor and 78690 video control must be set to the same bus width. Figure 6 shows the register format and Table 4 lists the bit selections and the reduction in the video bus speed that results.

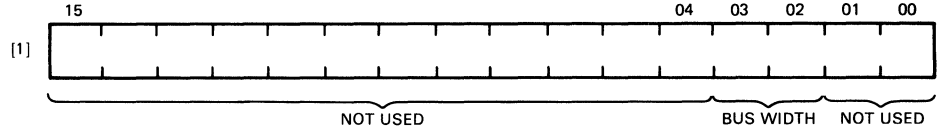

Figure 6 • 78660/78680 Bus Width Register Format

Table 4 • 78660/78680 Bus Width Register Descriptions

Bit	Description			
15:4	Not used.			
3:2	Bus width—Selects the number of video bus bits used for the display as follows:			
	Bit 3	**Bit 2**	**Data bus width**	**Video output**
	0	0	4-bits	4 bits every fourth alpha pulse
	0	1	8-bits	4 bits every other alpha pulse
	1	0	undefined	
	1	1	16-bits	4 bits every alpha pulse
1:0	Not used.			

Scroll constant—The scroll constant register is double buffered and is used to select the left or right horizontal scrolling and vertical scrolling operations. The data entered in the register becomes active on the following frame. Figure 7 shows the register format and Table 5 lists the functions of the register information.

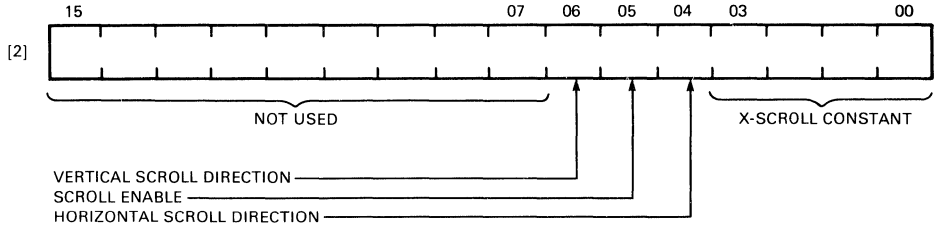

Figure 7 • 78660/78680 Scroll Constant Register Format

Table 5 • 78660/78680 Scroll Constant Register Description

Bit	Description
15:7	Not used.
6	Vertical scroll direction—Selects the direction for the vertical scroll as follows. Used to compensate for the asymmetries between the up and down scrolling directions. 0 = down, 1 = up, left, or right
5	Scroll enable—Set to enable the horizontal or vertical scrolling of the data accessed. Cleared to disable scrolling and the writing of memory planes.
4	Horizontal scroll direction—Control the direction of the X scroll constant specified by bits 3:0 as follows: Cleared when using the Y scroll constant. 0 = left, 1 = right
3:0	X-scroll constant—Selects the number of pixels per frame as follows: For left scrolls: 0 value = 0 pixel and 15 = 15 pixels For right scrolls: 0 value = 1 pixel and 15 = 16 pixels

Plane address—The plane address register determines the Z-axis operation. The plane addresses must be different for each 78660/78680 video processor. Addresses cannot overlap. A permanent plane address is set if the scrolling process loads the fill register in Z-mode. If the fill register is loaded individually by the scrolling process, then different update regions can have different plane address arrangements. The register format is shown in Figure 8 and function of the register information is described in Table 6.

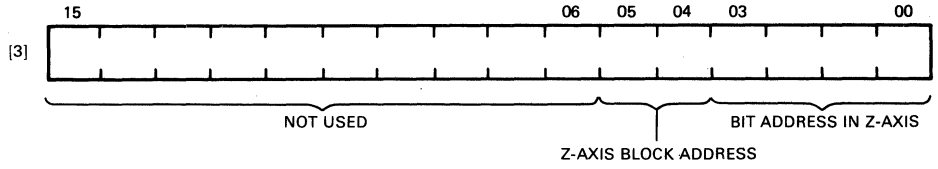

Figure 8 • 78660/78680 Plane Address Register Format

Table 6 • 78660/78680 Plane Address Register Description

Bit	Description
15:6	Not used.
5,4	Z-access block address 0 to 3—Defines the high-order bits of a 6-bit plane address when using more than 16 planes or subplanes within a system.
3:0	Bit address in Z-axis block 0 to 3—This address is set to the bit on which data will be exchanged on the ID bus during Z-mode transfers. For low resolution applications, this bit is the low-order bit and must be a multiple of 2 everything that is a multiple of 4 is a multiple of 2.

Logic unit function (0-3)—Each of the four logic unit function registers (0 through 3) include 8-bits of information. The registers combine the word read from destination (D) during a read-modify-write cycle with the contents of the source (S) register. The results are used to select the color of the foreground and background of the display. The format of the registers are shown in Figure 9 and described in Table 7.

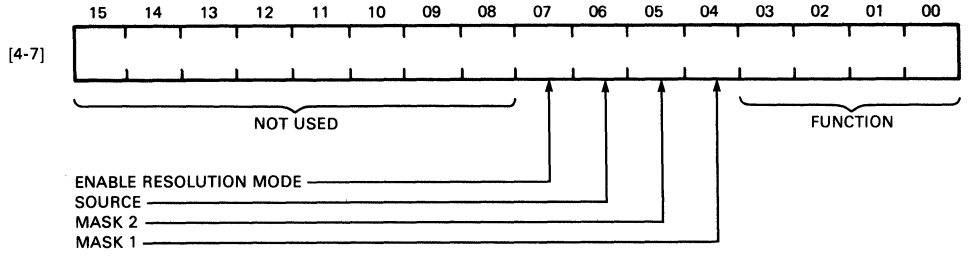

Figure 9 • 78660/78680 Logic Unit Function Registers (0-3) Format

Table 7 • 78660/78680 Logic Unit Function (3-0) Register Description

Bit	Description
15:8	Not used.
7	Enable resolution mode—Cleared to enable the resolution mode for the source register. Set to disable the resolution mode. When disabled, the bits are not combined with the adjacent bits and are transferred through the logic unit regardless of the resolution mode register selections.
6	Source—Set to select the source register word and cleared to select the complement of the source register word.
5	Mask 2—Cleared to use the content of programmable mask register 2 and set to use the complement of mask register 2.
4	Mask 1—Cleared to use the content of programmable mask register 1 and set to use the complement of mask register 1.
3:0	Function—Specifies the contents of the register as follows:

Bits 3	2	1	0	Function
0	0	0	0	zeros
0	0	0	1	not (D or S)
0	0	1	0	(not D) and S
0	0	1	1	not D
0	1	0	0	D and (not S)
0	1	0	1	not S
0	1	1	0	D XOR S
0	1	1	1	not (D and S)
1	0	0	0	D and S
1	0	0	1	not (D XOR S)
1	0	1	0	S
1	0	1	1	(not D) or S
1	1	0	0	D
1	1	0	1	D or (not S)
1	1	1	0	D or S
1	1	1	1	ones

Mask 1 and mask 2—Programmable mask registers 1 and 2 are used to control the bits that a read-modify-write cycle will modify. Loading the data mask register 1 also loads data mask register 2 with the same information. The output of these registers and the edge register determine the bits that will be modified by the 78660/78680 video processor. Figure 10 shows the format of the data mask registers.

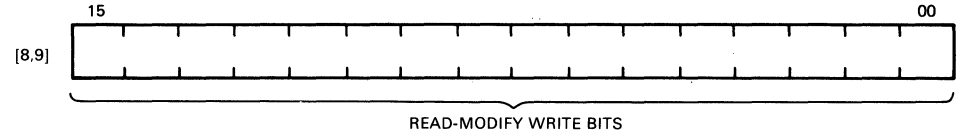

Figure 10 ▪ 78660/78680 Data Mask 1 and 2 Register Format

Source—The source register contains the source word for the logic unit that is combined with the destination information to select the foreground and background color for each pixel. The Z-mode address for this register is 00. The register format is shown in Figure 11.

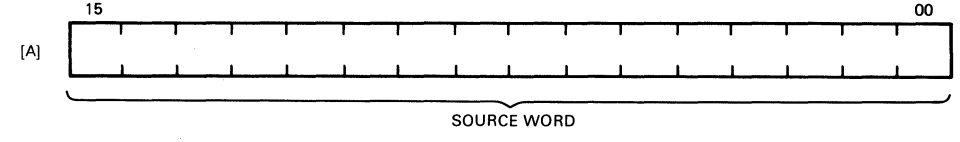

Figure 11 ▪ 78660/78680 Source Register Format

Fill—The fill register is double buffered and determines the fill area or blank space in memory that is created when scrolling. Normally, the Z-axis load command is used to select a solid color. If the register is loaded directly, all bits that correspond to the same subplane are set to the same value. The data from the register becomes active during the frame that follows.

Because the scroll region boundaries can be contained within one word, the leftmost and rightmost word can be programmed to any bit position. The scroll region boundaries of the 78690 video control, however, are limited to a multiple of four. When the video control is used, the boundaries must be selected with groups of 4 bits. Only the low 4 or 8 bits of this register are significant when using the 4- or 8-bit video bus widths, respectively. The register format is shown in Figure 12.

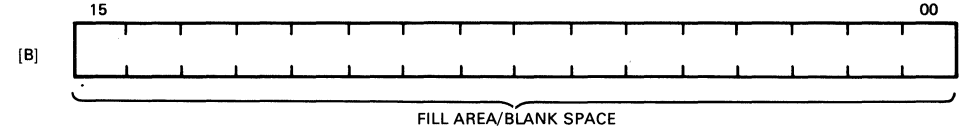

Figure 12 ▪ 78660/78680 Fill Register Format

Left and right scroll boundary—The left scroll boundary register defines the boundary for the left scroll. All bits corresponding to the pixels that contain the left edge of the region are cleared, and all other bits remain set. Normally, all bits from the pixel are cleared on the edge through the most significant bit of the word. If both of the edges are within one word, only the bits from the left edge through the right edge are cleared.

The right scroll boundary register defines the boundary for the right scroll. All bits are cleared from the least significant bit (LSB) of the left edge through the bit corresponding to the rightmost pixel that are to scroll within the word that contains the right edge of the region. All other bits remain set. If the right boundary is between words (LSB not scrolled) or if both edges are within one word, all bits are set. The format of the left and right scroll boundary register is shown in Figure 13.

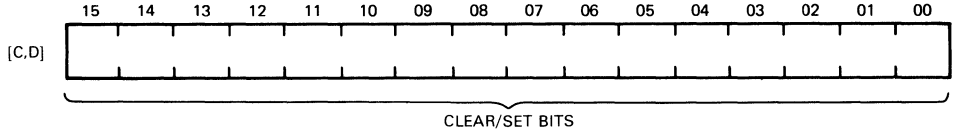

Figure 13 • 78660/78680 Left and Right Scroll Boundary Register Format

Background and foreground—The background and foreground registers are loaded by the ID bus register or Z-axis register load commands. The least significant bit of a word specifies the leftmost pixel and the most significant bit specifies the rightmost pixel. The information in these registers is selected 1 bit at time by the logic unit that transfers the information to the mask multiplexer. The multiplexer selects either this data or the previous destination data. The background register is selected by a zero output and the foreground register by a one output from the logic unit. The register format is shown in Figure 14.

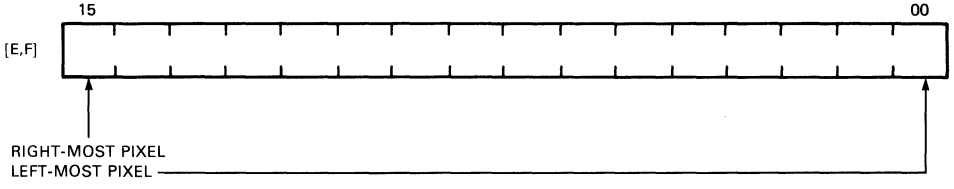

Figure 14 • 78660/78680 Background and Foreground Register Format

Control Store RAM (CSR0-CSR6)—The control store RAM registers are CSR0 through CSR6. Register CSR3 is reserved. During raster operations, these registers control the transfer of data within the 78660/78680 video processor and the data transfer to or from other ID bus devices. During each update memory cycle, the 78690 video control addresses the contents of these registers. When bank 1 is selected by the video control, CSR0 controls the first read source, CSR1 controls the second read source, and CSR3 controls the read-modify-write destination. When bank 2 is selected, CSR4 controls the first read source, CSR5 controls the second read source, and CSR6 controls the read-modify-write destination. Figure 15 shows the format of the control store RAM registers and Table 8 lists the function of the register information.

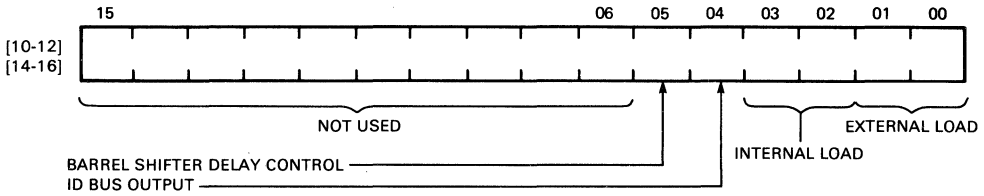

Figure 15 • 78660/78680 Control Store RAM Registers (CSR0-CSR6) Format

Table 8 • 78660/78680 Control Store RAM Description

Bit	Description
15:6	Not used
5	Barrel shifter delay control—Set during a fast mode raster operation to hold the previous word in a delay register so the remainder of each source word forms the next output word. This prevents excessive read operations to the source raster. This bit controls delay register one for CSR0 and CSR4 (for source 1) and delay register 2 for CSR1 and CSR5 (for source 2).
4	ID bus output—When a CSR is addressed during a memory read cycle, this bit is set to enable (one plane at a time is allowed) the transfer of data on the ID bus during a memory read cycle.
3:2	Internal Load—Select the register to receive the data through the barrel shifter from the local memory plane following a memory read operation as follows: **Bit 3 / Bit 2 / Register** 0 0 none 0 1 source 1 0 mask 1 and mask 2 1 1 mask 2
1:0	External load—Selects the register to receive the input data from the ID bus following a memory read operation.

Specifications

The mechanical, electrical, and environmental characteristics and specifications for the 78660/78680 video processor are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Power supply voltage (V_{DD}): 5.0 V
- Temperature range (T_A): 0°C to 70°C
- Ground (V_{SS1}),(V_{SS}),(V_{SS2}),(V_{SS3}): 0 V

Mechanical Configuration

The physical dimensions of the 78660/78680 68-pin CERQUAD package are contained in Appendix E.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Power supply voltage (V_{DD}): −0.5 V to 5.25 V
- Input voltage applied (V_{in}): −0.5 V to 6.0 V
- Output voltage applied (V_{out}): −0.5 V to 6.0 V
- Power dissipation (P_D): 1.9 W at 100°C, 2.8 W at 0°C
- Active temperature (T_A): 0°C to 70°C
- Storage temperature: −55°C to 125°C

Recommended Operating Conditions

- Power supply voltage (V_{DD}): 5 V ±5%
- Temperature (T_J) 0°C to 100°C
- Typical operating voltage: 5.0 V

dc Electrical Characteristics

The dc electrical parameters of the 78660/78680 video processor for the operating voltage and temperature ranges specified are listed in Table 9.

Table 9 • 78660/78680 dc Input and Output Parameters

Symbol	Parameter	Test Condition	Requirements Min.	Max.	Units
V_{IH}	High-level input voltage DIO<15:0>,CS,SCROL, ID<7:0>,SYNC		2.2		V
	RD/WR,128/$\overline{16}$		2.4		V
	LTCLK,ALPHA1,		2.6		V
	PHI1,PHI2		2.7		V
V_{IL}	Low-level input voltage DIO<15:0>,CS,SCROL, ID<7:0>,SYNC			0.8	V
	RD/$\overline{WR}$,128/$\overline{16}$ LTCLK,ALPHA1,			0.7	V
	PHI1,PHI2			0.4	V
V_{OH}	High-level output voltage (all pins except ID<7:0>)	V_{DD}=0 I_{OH}=–200 µA	2.4		V
	ID<7:0>		2.5		V
V_{OL}	Low-level output voltage DIO<15:0>,PE, VID<3:0>	V_{DD}=0 V I_{OL}=4.0 mA	0.4		V
	ID<7:0>	I_{OL}=5.0 mA			
I_{DD}	Active supply current	V_{DD}=max T_A=0°C T_J=20°C		470	mA
I_{IH}	Input leakage current (high)	V_{DD}=max V_{in}=V_{DD} (max.)		30	µA
I_{IL}	Input leakage current (low)	V_{DD}=max. V_{in}=0 V		–30	µA
I_{OS}	Short-circuit output current[1] DIO<15:0>,PE, VID<3:0>	V_{DD}=max.	–10	–90	mA
	ID<7:0>		–15	–140	mA
I_{OZL}	High-Z state output current	V_{DD}=max. V_{out}=0.4 V		30	µA

Symbol	Parameter	Test Condition	Requirements Min.	Max.	Units
I_{OZH}	High-Z state output current[1,2]	V_{DD} = max. V_{out} = 2.4 V		30	µA
C_{in}	Input capacitance except PHI1,PHI2			4	pF
	PHI1,PHI2			18	pF
C_{out}	Output capacitance[3]			5	pF

[1]These are computer simulated measurements and cannot be tested. In the test simulation, only one output at a time may be short circuited to ground.
[2]The outputs include the driver current and input leakage current.
[3]Capacitance loading is for the output drivers and input receivers.

ac Electrical Characteristics

The ac timing parameters for the 78660/78680 video processor are grouped according to major cycle timing, minor cycle timing ID bus and video bus timing, and synchronization cycle timing. The timing parameters in the tables are listed for both the 60 Hz (78660) and 80 Hz (78680) versions are in microseconds unless listed otherwise.

Major Cycle Timing

Table 10 lists the symbols, definitions, and specifications for the major cycle timing shown in Figure 16. A major cycle begins on the rising edge of the PHI2 clock pulse and is equal to four PHI2 clock periods. A refresh read memory cycle has two major cycles—a read cycle and a screen refresh transfer cycle for editing or scrolling. Every second major cycle must be a read cycle. The video processor provides data to the display during the forward scan time of the screen refresh transfer cycle. During this cycle, a refresh read memory cycle transfers data from bit-map memory to the video bus.

Table 10 • 78660/78680 Major Cycle Timing Parameters

Symbol	Definition	Requirements (ns) 60 Hz Min.	60 Hz Max.	80 Hz Min.	80 Hz Max.
t_{CYC1}	Period of LTCLK	82		54.5	
t_{CYC2}	Period of PHI1 or PHI2	228		148	
t_{CYC3}	Period of major cycles	*	10 µs		
t_{D1}	Propagation delay of LTCLK rising to valid data on DIO<15:0>		48		32
t_{HO1}	Hold time of RD/$\overline{WR}$ or 128/$\overline{16}$ switching to the falling edge of LTCLK. This parameter must be met relative to the last falling edge of LTCLK in a major cycle.	15		10	

Symbol	Definition	Requirements (ns) 60 Hz Min.	60 Hz Max.	80 Hz Min.	80 Hz Max.
t_{HO2}	Hold time of DIO<15:0> or SCROLL to the falling edge of LTCLK	20		13	
t_{HZ1}	Propagation delay of RD/$\overline{WR}$ going high to a high-impedance on DIO<15:0>	38	102	36	94
t_{ZL1}	Propagation delay of RD/$\overline{WR}$ going low to valid data on DIO<15:0>	5	45	19	45
t_{NOV}	Nonoverlap time, PHI1 to PHI2		23.5	23	15.5
t_{PWH1}	Pulse width high of LTCLK	27		27	
t_{PWH2}	Pulse width high of PHI1 or PHI2	83		83	
t_{PWL1}	Pulse width low of LTCLK	55		55	
t_{R1}	Input rise time (fall time) for PHI1, PHI2, LTCLK, ALPHA 1,RD/$\overline{WR}$, 128/$\overline{16}$, CS, SYNC, SCROLL, DIO<15:0>	5			5
t_{SU1}	Setup time of RD/$\overline{WR}$ switching to the falling edge of LTCLK. This parameter must be satisfied relative to the first falling edge of LTCLK in a major cycle.	20		20	
t_{SU2}	Setup time of 128/$\overline{16}$ rising to the rising edge of LTCLK. This parameter must be satisfied relative to the first rising edge of LTCLK in a major cycle and applies only to transitions between minor and major write cycles (guaranteed by not exceeding t_{PD2}).	10		10	
t_{SU3}	Setup time of DIO<15:0> or SCROLL to the falling edge of LTCLK	0		0	
t_{SU10}	Setup time of RD/$\overline{WR}$ or 128/$\overline{16}$ switching to the first falling edge of PHI1 in any major cycle	90		90	
t_{ZH1} t_{ZL1}	Propagation delay of RD/$\overline{WR}$ going low to valid data on DIO<15:0>	5.0	45	5.0	45

*Minimum t_{CYC3} = 4 PHI2 cycles or 16 ALPHA cycles

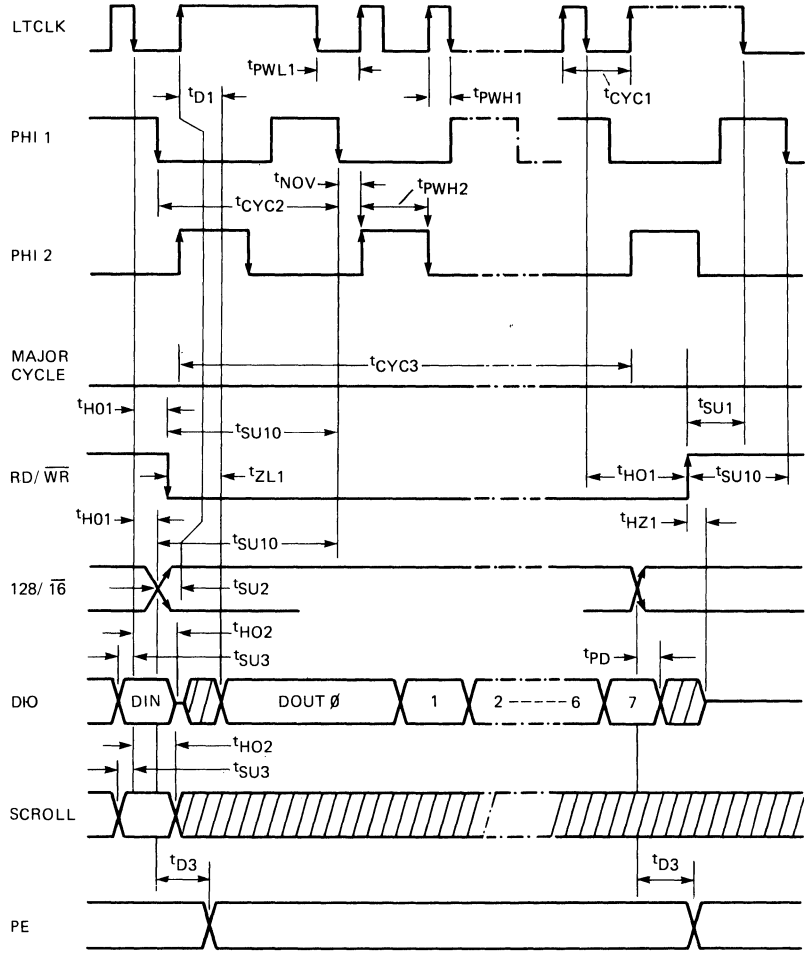

Figure 16 ▪ 78660/78680 Major Cycle Timing

Minor Cycle Signal Timing

Table 11 lists the specifications for the minor cycle events including a memory cycle shown in Figure 14. A memory cycle starts at the beginning of a major cycle and must end by the beginning of the next major cycle. Only one memory cycle must be in progress at a time.

Table 11 • 78660/78680 Minor Cycle Timing Parameters

Symbol	Definition	Requirements (ns) 60 Hz Min.	60 Hz Max.	80 Hz Min.	80 Hz Max.
t_{D2}	Propagation delay of PHI2 rising to valid data on DIO<15:0>. This parameter applies only to Z-axis write operations.		95		63
t_{D3}	Propagation delay of 128/$\overline{16}$ switching to an updated value of PE.		58		37
t_{D5}	Propagation delay of ID data setup to following edge of the second PHI1 in a minor cycle to valid data on DIO<15:0>.		120		79.5
t_{HO3}	Hold time of an asserted CS to the falling edge of PHI2.	60		40	
t_{HO4}	Hold time of DIO<15:0> to the second falling edge of PHI2 in a minor read cycle.		20		13
t_{HO5}	Hold time of DIO<15:0> to the falling edge of RD/$\overline{WR}$.	0		0	
t_{PD}	Propagation delay of the rising edge of 128/$\overline{16}$ to DIO<15:0> rising or falling.	0	58	0	38.5
t_{SU4}	Setup time of an asserted CS to the falling edge of PHI2.	60		40	
t_{SU5}	Setup time of DIO<15:0> to the falling edge of the second PHI2 in a minor cycle.	65		43	
t_{SU6}	Setup time of DIO<15:0> to the falling edge of RD/$\overline{WR}$.	20		13	
t_{ZH1}	Propagation delay of RD/$\overline{WR}$ going low to valid data on DIO<15:0>.	5	45	3.5	30
t_{ZL1}	Propagation delay of RD/$\overline{WR}$ going low to valid data on DIO<15:0>.	5	45	3.5	30

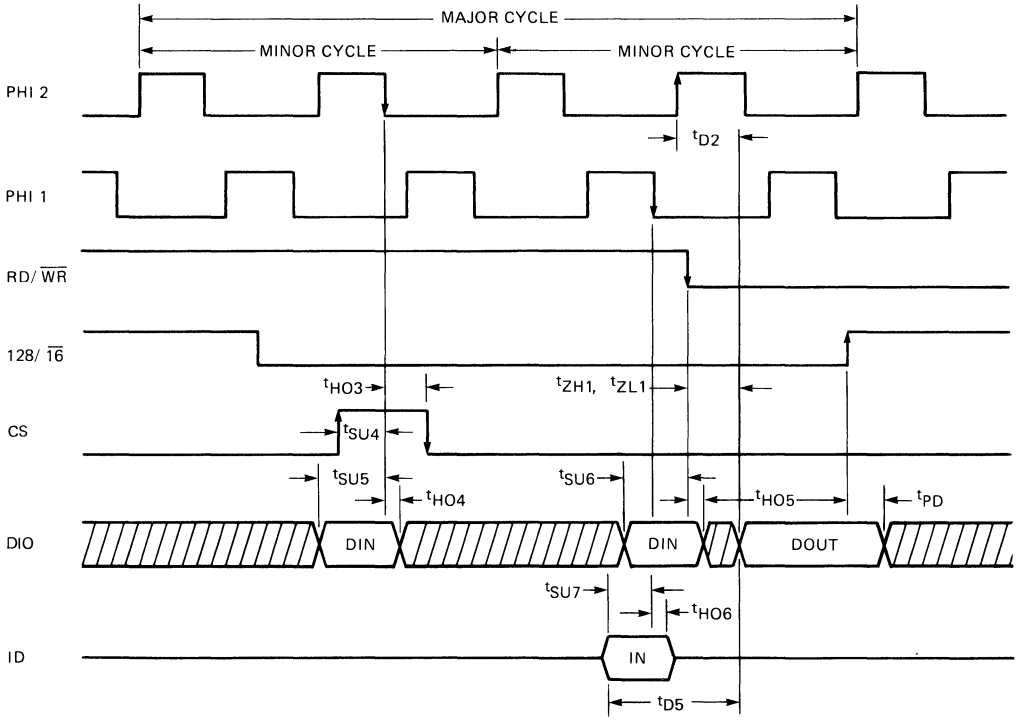

Figure 17 ▪ 78660/78680 Minor Cycle Signal Timing

ID Bus and Video Bus Signal Timing

Table 12 lists the specifications for the ID bus and video bus timing shown in Figure 18. A major cycle begins on the rising edge of the PHI2 clock pulse with 4 PHI2 clock periods. PHI1 and PHI2 must have the same period and must not overlap. The alpha clock has a timing period one-fourth of the PHI2 clock and has coincident rising edges.

Table 12 • 78660/78680 ID Bus and Video Bus Timing Parameters

Symbol	Definition	Requirements (ns) 60 Hz Min.	60 Hz Max.	80 Hz Min.	80 Hz Max.
t_{32}	Time delay to valid data on VID is 10 ALPHA cycles plus t_{D4} after start of present major cycle.				
t_{ACC}	Propagation delay of PHI2 rising to valid data on VID<3:0> while ALPHA is high.		119		85
t_{CYC4}	Period of ALPHA.	54		36	
t_{D4}	Propagation delay of alpha rising to valid data on VID<3:0>. The rate of updating the data depends on the the bus width mode: full page = once/ALPHA clock half page = once/two ALPHA clocks one-fourth page = once/four ALPHA clocks	5.0	42	48	3.0
t_{HO6}	Hold time of ID<7:0> to the falling edge of PHI1 or PHI2.	20		15.5	
t_{HZ2}	Propagation delay of PHI1 or PHI2 going low to a High-Z condition on ID<7:0>.	51	121	49	114.5
t_{LZ2}	Propagation delay of PHI1 or PHI2 going low to a High-Z condition on ID<7:0>.	45	83	44	77
t_{PWH3}	Pulse width high of ALPHA.	27		18	
t_{PWL2}	Pulse width low of ALPHA.	27		18	
t_{R2}	Input rise time (fall time) ID<7:0>		40		26.5
t_{SU7}	Setup time of ID<7:0> to the falling edge of PHI1 or PHI2.	20		13	
t_{ZH2}	Propagation delay of PHI1 or PHI2 rising to valid data on ID<7:0>.	5	60	3.5	40
t_{ZL2}	Propagation delay of PHI1 or PHI2 rising to valid data on ID<7:0>.	5	60	3.5	40

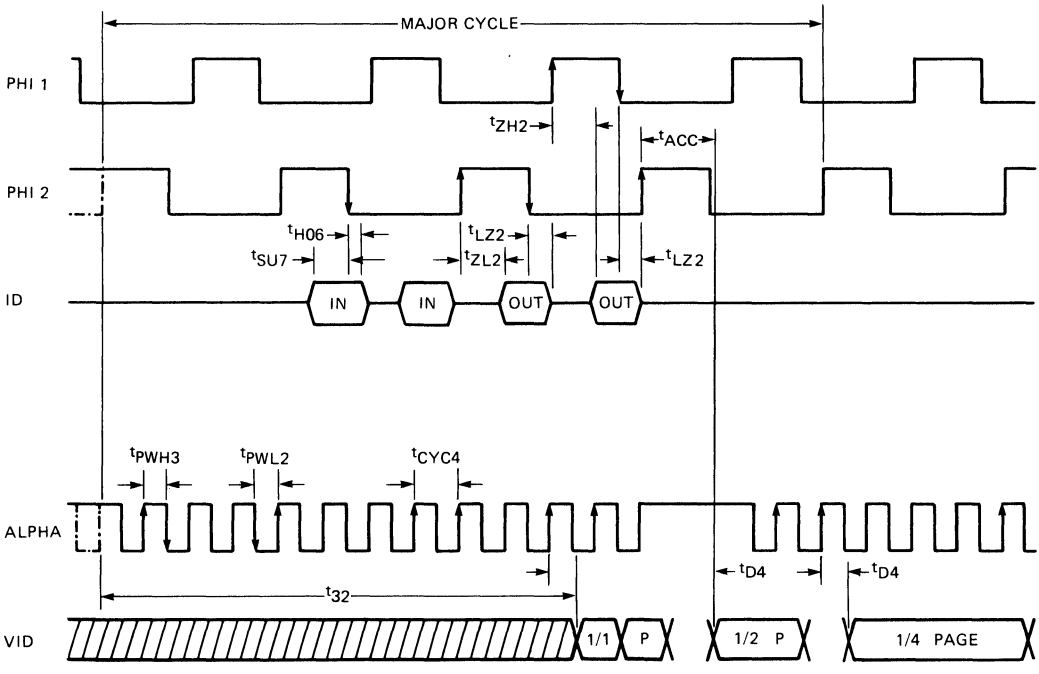

Figure 18 • 78660/78680 ID Bus and Video Bus Signal Timing

Synchronization Cycle Timing

Synchronization occurs once per frame during the vertical retrace period. When the SYNC signal is asserted, all internal clocks halt in a t = 0 + state. The video processor suspends all data processing and resets the counters that are used to transfer data out to the video bus and out of and into the ID and data bus. The LTCLK has eight time periods within a major cycle. These periods can occur within the cycle to accommodate different types of memories. Table 13 lists the synchronization timing parameters shown in Figure 19.

Table 13 • 78660/78680 Synchronization Cycle Timing Parameters

Symbol	Definition	Requirements (ns) 60 Hz Min.	60 Hz Max.	80 Hz Min.	80 Hz Max.
t_{41}	Use the rising edge of PHI2 as the major cycle boundary except after a sync cycle. After a sync cycle, the major cycle boundry occurs three ALPHA states before the falling edge of the " frozen" high PHI2 pulse.				
t_{42}	The number of ALPHA cycles that must elapse before PHI2 goes low for the first time after a SYNC cycle is 1, 5, 9, or 13.				
t_{CYC3}	Period of major cycles.	*		10 µs	
t_{PWH4}	Pulse width high of SYNC.	456		302	
t_{SK}	Skew between PHI2 falling and ALPHA falling.		± 14		8.0
t_{SU8}	Setup time of SYNC going low to the first falling edge of ALPHA.	456	10 µs	302	
t_{SU9}†	Setup time of LTCLK falling to the rising edge of PHI2.	40		26.5	

*Minimum = 4 PHI2 cycles or 16 ALPHA cycles

†In order for the t_{32} specification (Table 12) to be valid, data must have been loaded into the internal FIFO buffers. Therefore, the first falling edge LTCLK and its associated data during a major read cycle must precede the third rising edge of PHI2.

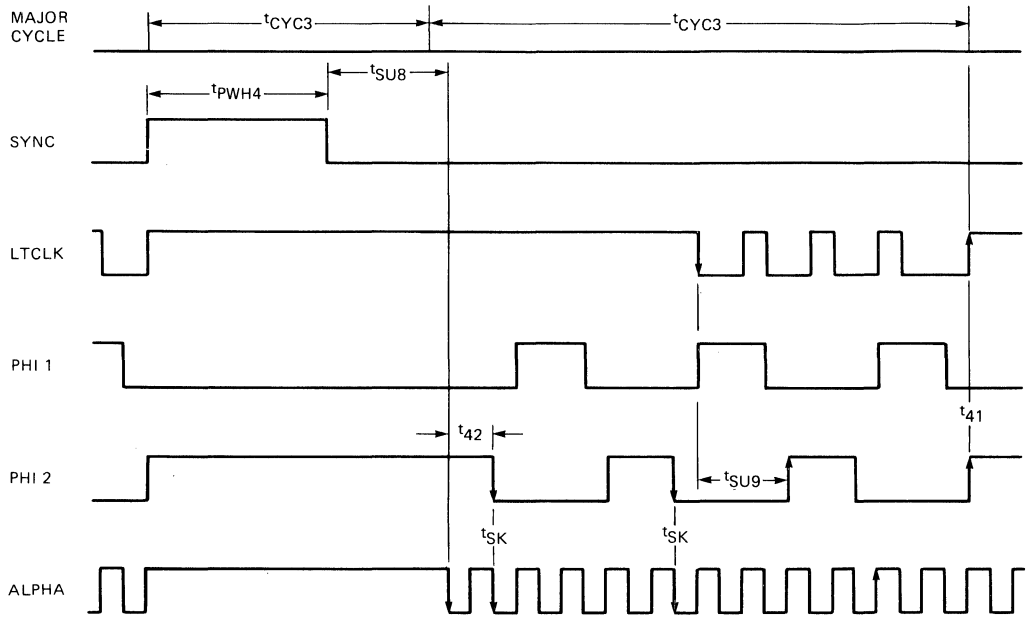

Figure 19 ▪ 78660/78680 Synchronization Cycle Timing

▪ Interfacing Techniques

The video processor communicates with the video subsystem using the three TTL-compatible interfaces shown in Figure 3—the system interface, the bit-map interface, and the display interface.

The system interface lines consist of the chip select (CS), the system clocks, and an 8-bit, bidirectional instruction/data bus. The system interface connects to the address processor memory planes and other memory planes.

The bit-map interface includes the 16-bit bidirectional data bus DIO < 15:0 > and the LTCLK, 128, RD, SCR, OL, PE, PHI1, and PHI2 signals that control data flow on the bus. The bit-map interface connects to the bit-map memory planes.

The display interface includes the video bus and the signals that control it. The video bus VID < 3:0 > connects to the display circuits. The control signals include the ALPHA clock pulses and the PHI1 and PHI2 system clocks pulses. This bus is used during screen refresh cycles.

The instruction/data (ID) bus is used to transfer information between the video processor and controllers. It is used to load and read registers and to execute direct or indirect instructions.

Interface Connections

The following circuit and connections are recommended for the proper operation of the 78660/78680 video processor.

Power—The 78660/78680 video processor operates with a 5 Vdc power supply. Ten of the chip pins connect to V_{DD} and one connects to V_{BB}. No special filtering is required. The 5 Vdc connects to the V_{DD} pins and the power supply ground connects to V_{SS}. Pin 61 (V_{BB}) is the voltage generator output and must be connected to the pin 60 (cavity) which is the substrate.

Powerup latch—The video processor includes a circuit to ensure that the ID bus is in a high-impedence state during the powerup sequence. A latch is set during the powerup sequence to force the ID bus to this state. The deassertion of the CS signal clears the latch.

ID bus lines—Connecting a 50-pF capacitor to ground on each ID bus line compensates for component variations in the interface design. Multiplane single-module systems may not require these capacitors. However, the etch capacitance to ground and to other signals should be evaluated. The noise margin should be limited to 0.2 V to 0.3 V. The total ID bus load capacitance should be less than 400 pF.