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Digital Logic II

Michael C. Hackett

Assistant Professor, Computer Science

COMMUNITY COLLEGE OF PHILADELPHIA

Lecture Topics

- Combinational Circuits
  - Encoders
  - Decoders
  - Multiplexers
  - Demultiplexers

Combinational Circuits

- We've seen the use of logic gates to implement a Boolean function
- With logic gates, we can build **combinational logic circuits** that can perform complex operations
  - They perform Boolean algebra on the circuit's input
- Combinational logic circuits are used in the construction of practical, digital computer circuits (including a computer's CPU)

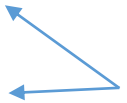
Encoders

- An encoder is a combinational logic circuit with 2^n input pins and n output pins.
  - Only a single input pin is set to 1

- Below is the truth table for a 4x2 encoder
  - $\boldsymbol{I}$ represents the input pins
  - $\boldsymbol{E}$ represents the (encoded) output pins

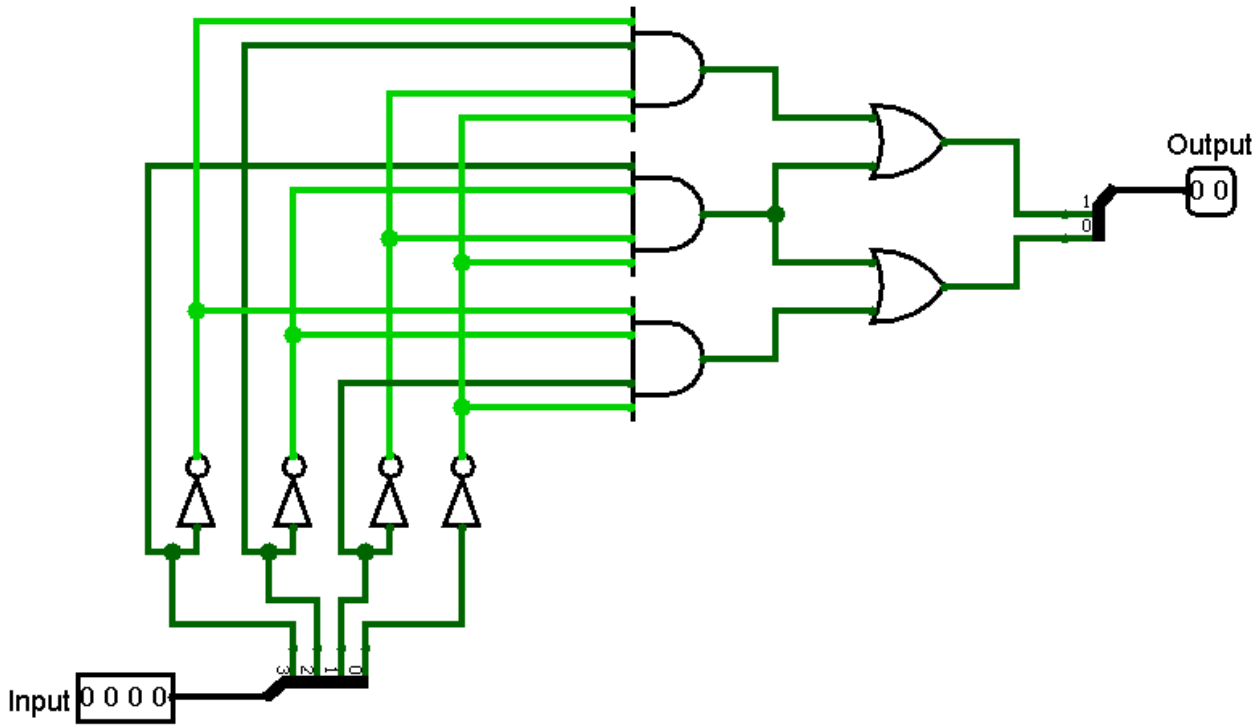
I_3	I_2	I_1	I_0	E_1	E_0
0	0	0	**1**	**0**	**0**
0	0	**1**	0	**0**	**1**
0	**1**	0	0	**1**	**0**
1	0	0	0	**1**	**1**

- SOP Expression: $E_1 = \overline{I_3} I_2 \overline{I_1}\,\overline{I_0} + I_3 \overline{I_2}\,\overline{I_1}\,\overline{I_0}$
- SOP Expression: $E_0 = \overline{I_3}\,\overline{I_2} I_1 \overline{I_0} + I_3 \overline{I_2}\,\overline{I_1}\,\overline{I_0}$



Encoders

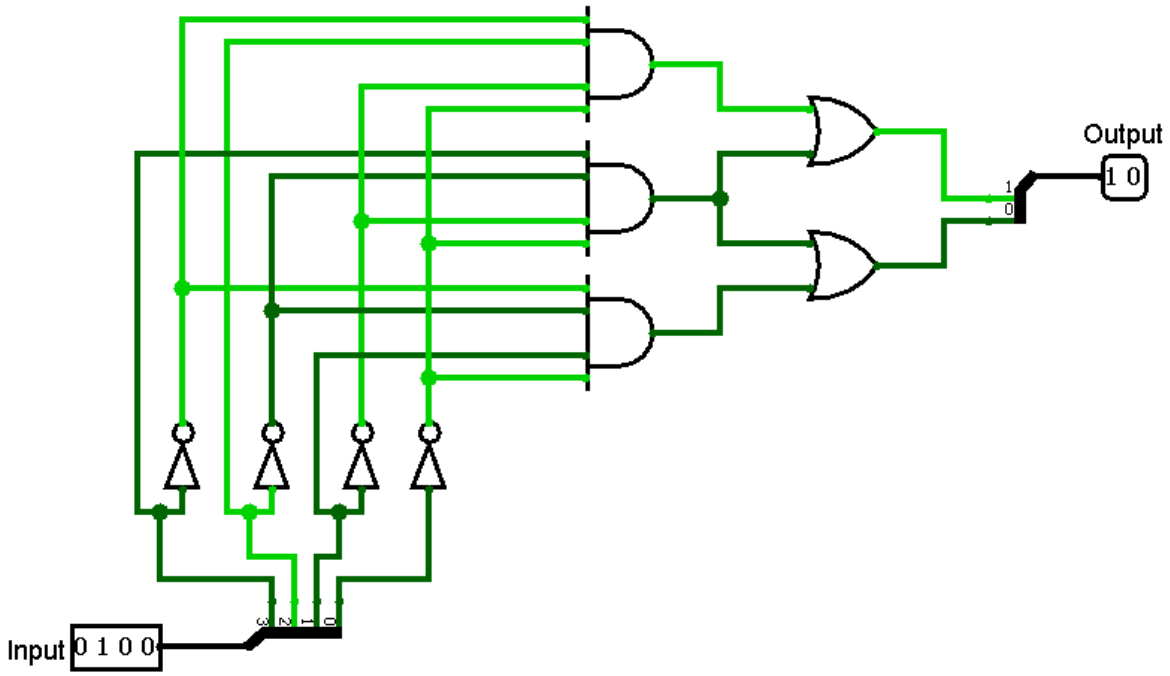
- Logic circuit for a 4x2 encoder:



Encoders

- Logic circuit for a 4x2 encoder:

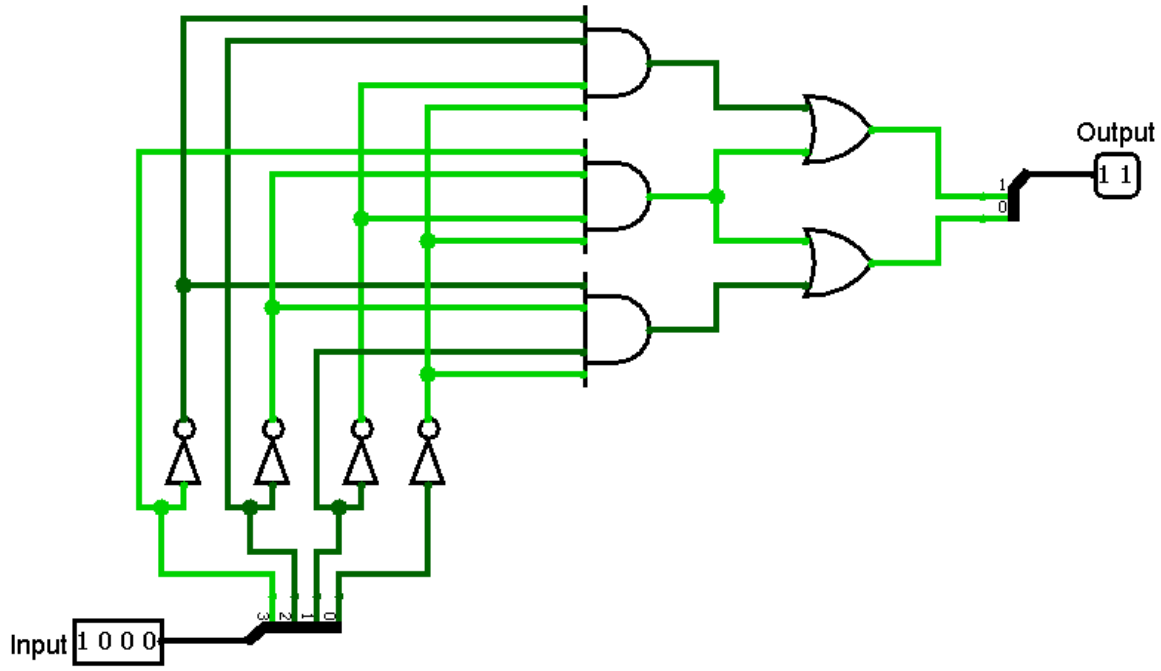
I_3	I_2	I_1	I_0	E_1	E_0
0	0	0	1	0	0
0	0	1	0	0	1
0	**1**	**0**	**0**	**1**	**0**
1	0	0	0	1	1



Encoders

- Logic circuit for a 4x2 encoder:

I_3	I_2	I_1	I_0	E_1	E_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	**0**	**0**	**0**	**1**	**1**



Encoders

- Below is the truth table for an 8x3 encoder

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	E_2	E_1	E_0
0	0	0	0	0	0	0	**1**	**0**	**0**	**0**
0	0	0	0	0	0	**1**	0	**0**	**0**	**1**
0	0	0	0	0	**1**	0	0	**0**	**1**	**0**
0	0	0	0	**1**	0	0	0	**0**	**1**	**1**
0	0	0	**1**	0	0	0	0	**1**	**0**	**0**
0	0	**1**	0	0	0	0	0	**1**	**0**	**1**
0	**1**	0	0	0	0	0	0	**1**	**1**	**0**
1	0	0	0	0	0	0	0	**1**	**1**	**1**

Encoders

- SOP Expressions:

$$E_2 = \overline{I_7}\,\overline{I_6}\,\overline{I_5}I_4\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_7}\,\overline{I_6}I_5\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_7}I_6\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_7\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0}$$

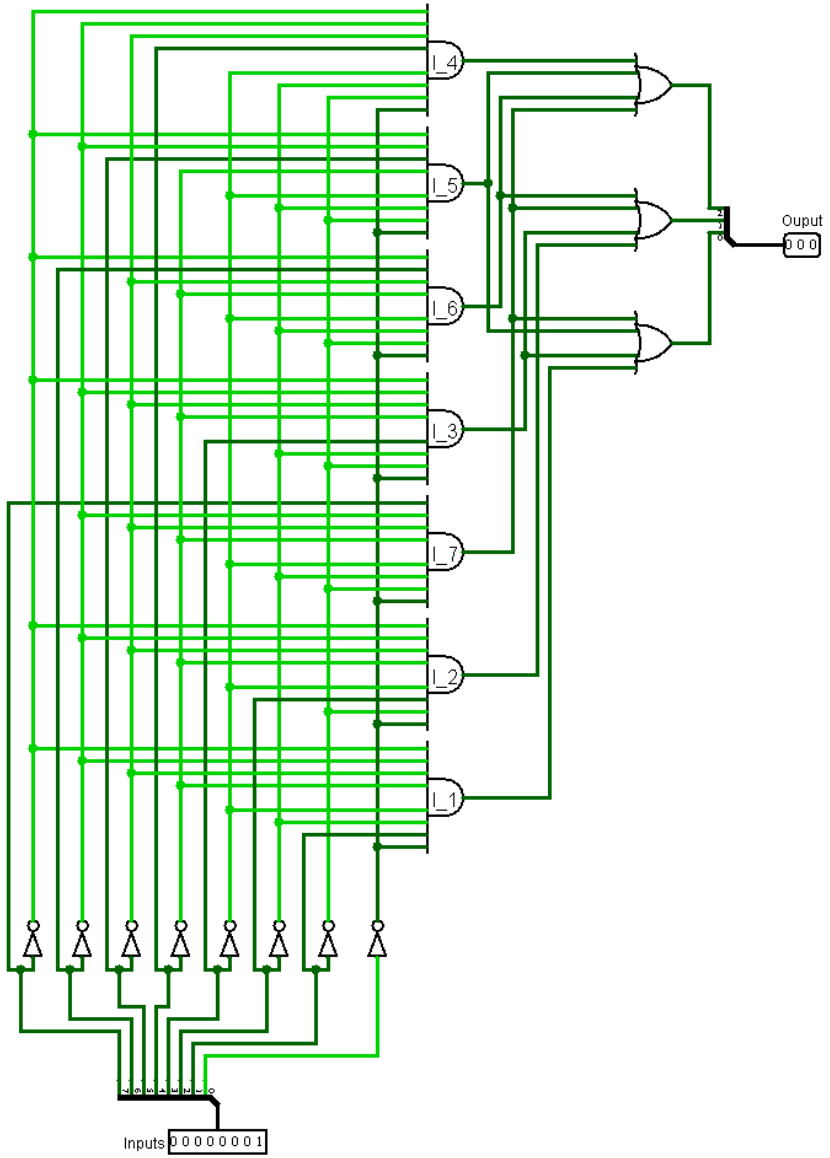
$$E_1 = \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3}I_2\overline{I_1}\,\overline{I_0} + \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4}I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_7}I_6\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_7\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0}$$

$$E_0 = \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2}I_1\overline{I_0} + \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4}I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_7}\,\overline{I_6}I_5\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_7\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0}$$

  - (Boxed terms indicate duplicates)

Encoders

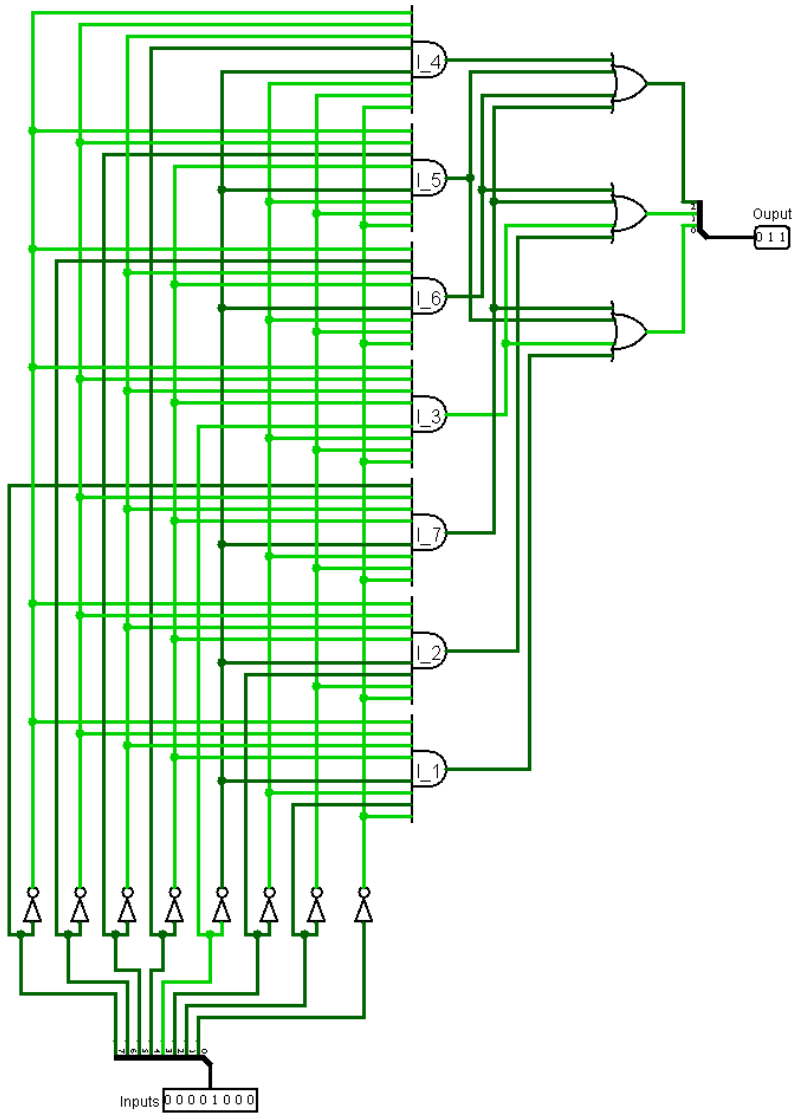
- Logic circuit for an 8x3 encoder:



Encoders

- Logic circuit for an 8x3 encoder:

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	E_2	E_1	E_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1



Decoders

- A decoder is a combinational logic circuit with n input pins and 2^n output pins.
  - For each output, only a single bit is set to 1

- Below is the truth table for a 2x4 decoder
  - ***I*** represents the input pins
  - ***D*** represents the (decoded) output pins

I_1	I_0	D_3	D_2	D_1	D_0
0	**0**	0	0	0	**1**
0	**1**	0	0	**1**	0
1	**0**	0	**1**	0	0
1	**1**	**1**	0	0	0

- SOP Expressions:

$$D_0 = \overline{I_1}\,\overline{I_0}$$

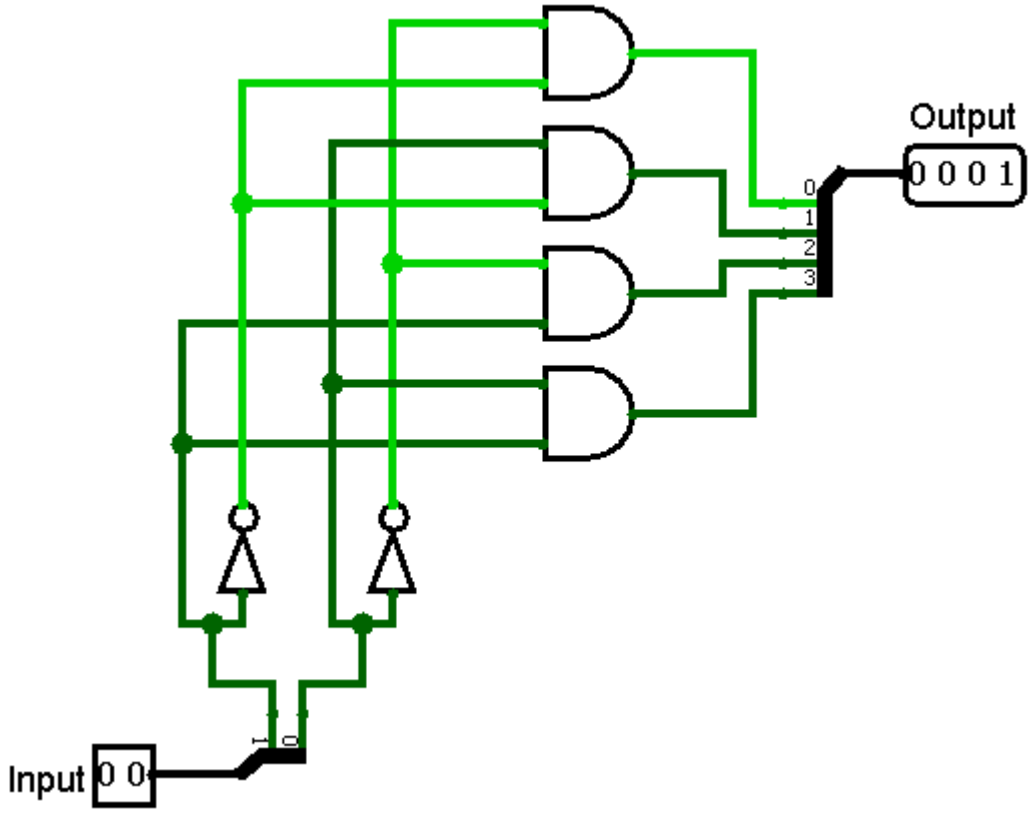
$$D_1 = \overline{I_1} I_0$$

$$D_2 = I_1 \overline{I_0}$$

$$D_3 = I_1 I_0$$

Decoders

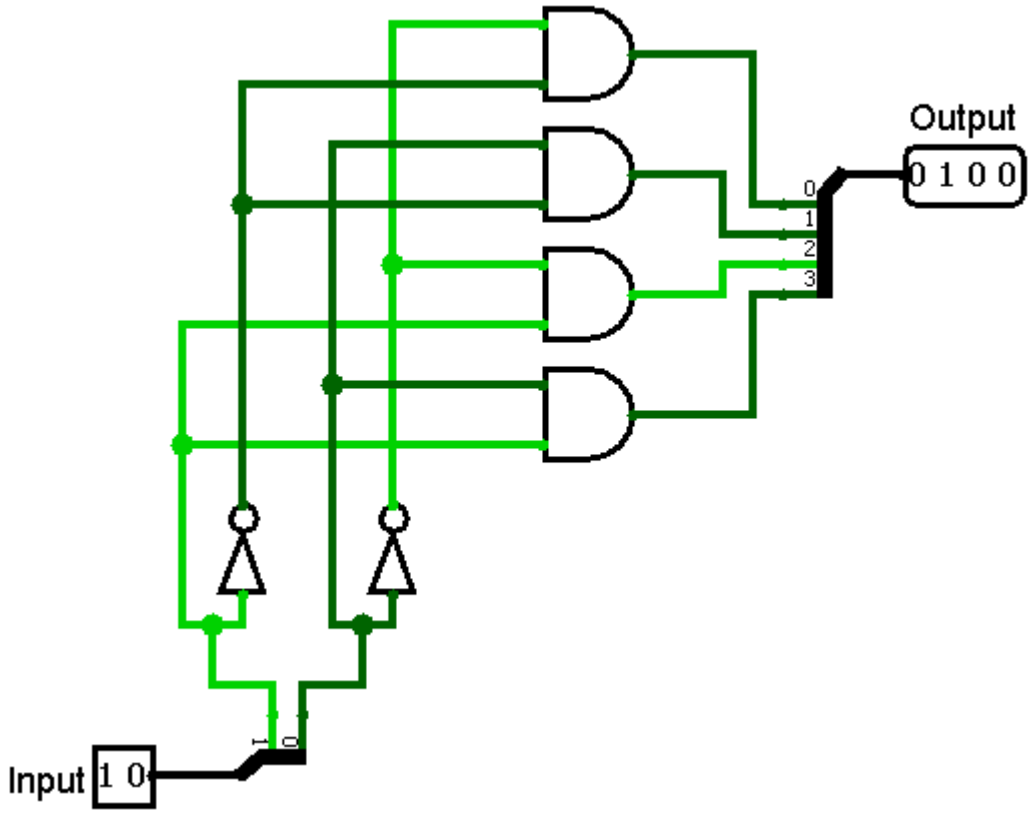
- Logic circuit for a 2x4 decoder



Decoders

- Logic circuit for a 2x4 decoder:

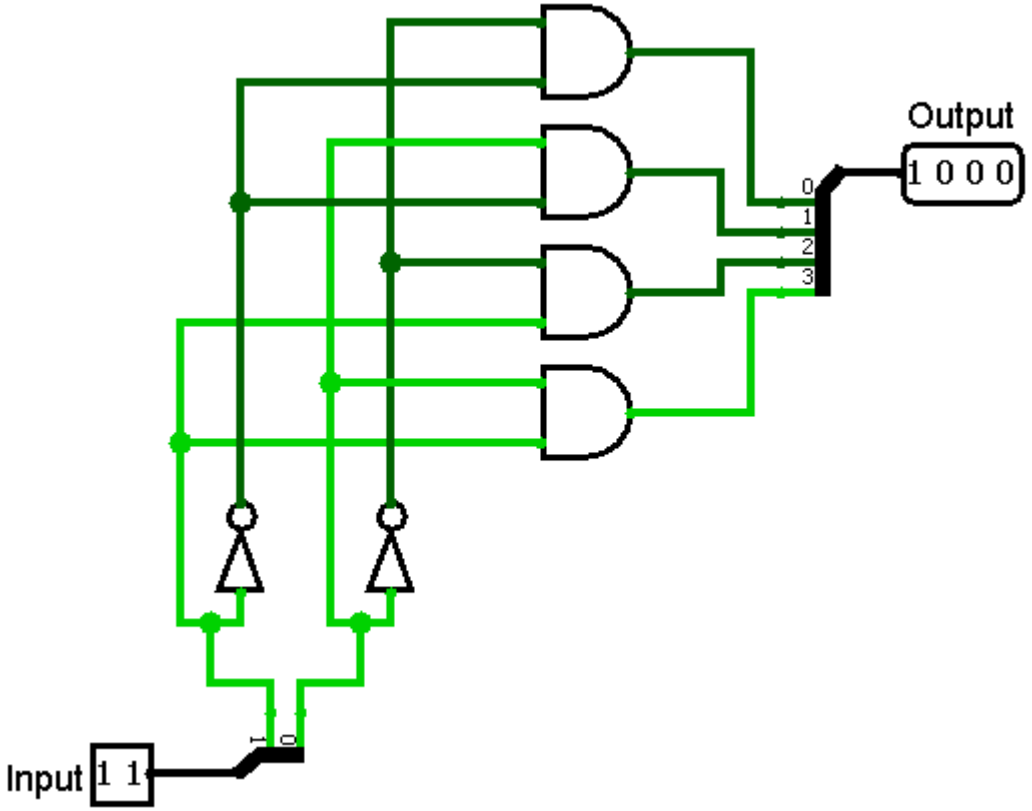
I_1	I_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	**0**	**0**	**1**	**0**	**0**
1	1	1	0	0	0



Decoders

- Logic circuit for a 2x4 decoder:

I_1	I_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	**1**	**1**	**0**	**0**	**0**



Decoders

- Below is the truth table for a 3x8 decoder

I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	**0**	**0**	0	0	0	0	0	0	0	**1**
0	**0**	**1**	0	0	0	0	0	0	**1**	0
0	**1**	**0**	0	0	0	0	0	**1**	0	0
0	**1**	**1**	0	0	0	0	**1**	0	0	0
1	**0**	**0**	0	0	0	**1**	0	0	0	0
1	**0**	**1**	0	0	**1**	0	0	0	0	0
1	**1**	**0**	0	**1**	0	0	0	0	0	0
1	**1**	**1**	**1**	0	0	0	0	0	0	0

Decoders

- SOP Expressions:

$$D_0 = \overline{I_2}\,\overline{I_1}\,\overline{I_0}$$

$$D_1 = \overline{I_2}\,\overline{I_1}\,I_0$$

$$D_2 = \overline{I_2}\,I_1\,\overline{I_0}$$

$$D_3 = \overline{I_2}\,I_1\,I_0$$

$$D_4 = I_2\,\overline{I_1}\,\overline{I_0}$$

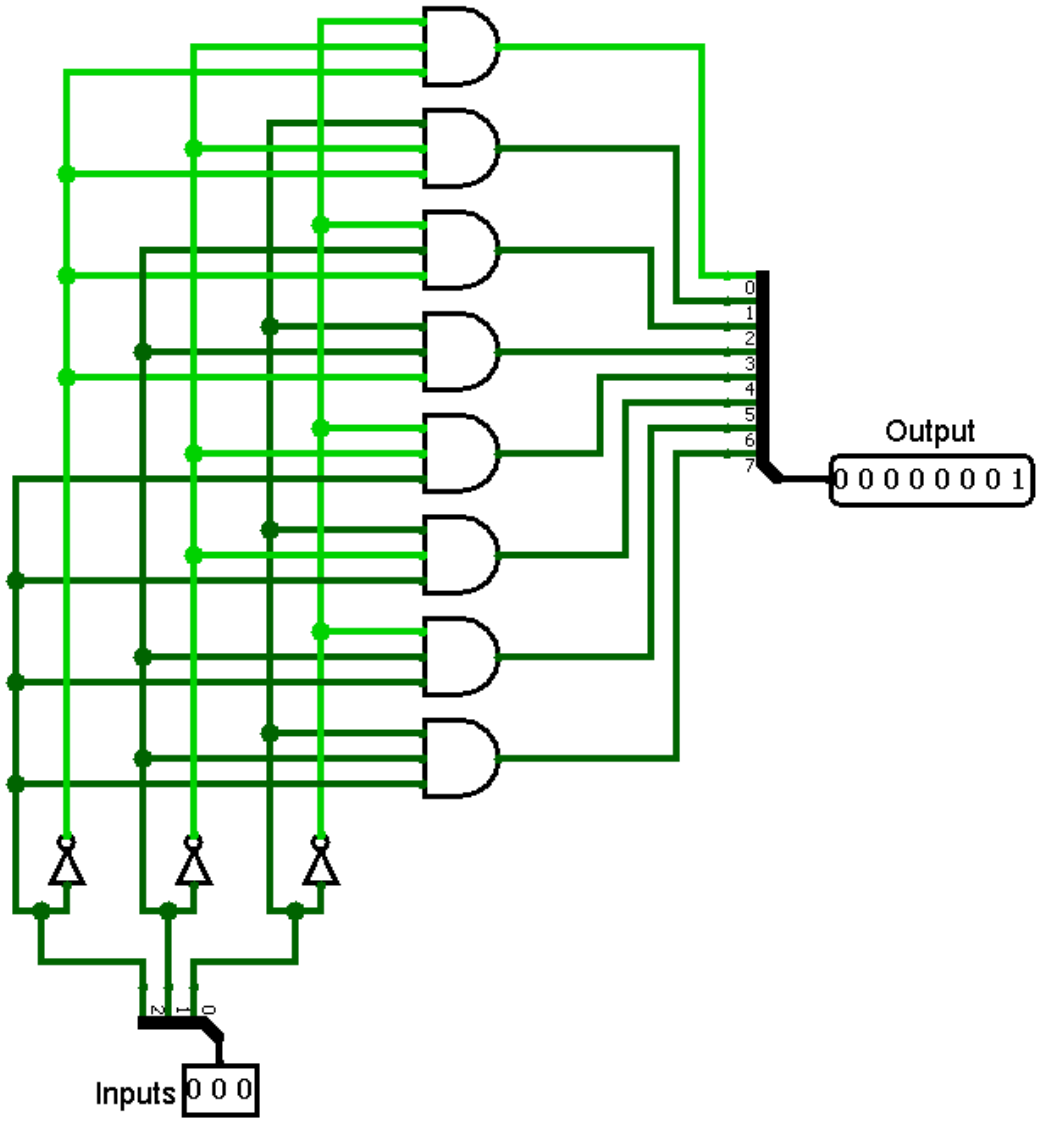
$$D_5 = I_2\,\overline{I_1}\,I_0$$

$$D_6 = I_2\,I_1\,\overline{I_0}$$

$$D_7 = I_2\,I_1\,I_0$$

Decoders

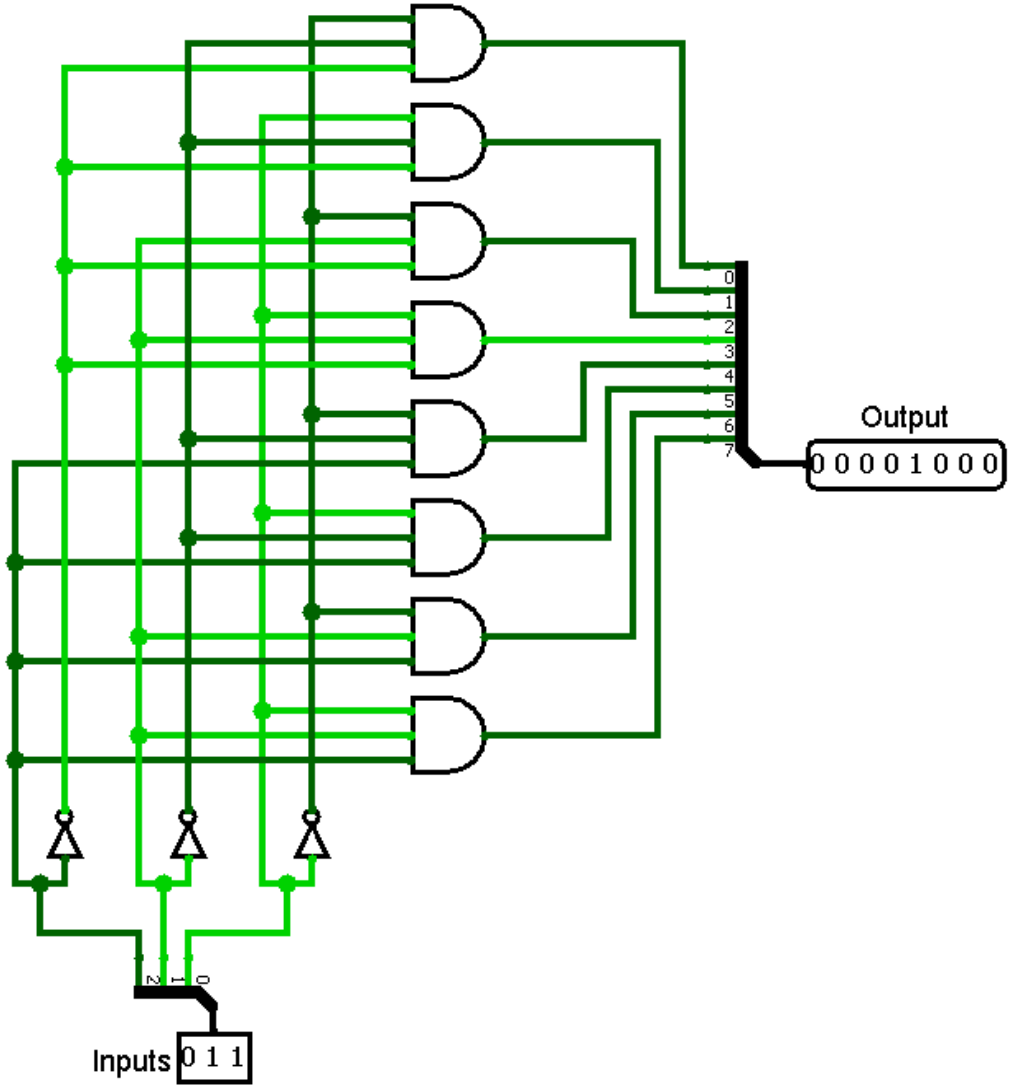
- Logic circuit for a 3x8 decoder:



Decoders

- Logic circuit for a 3x8 decoder:

I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



Multiplexers

- A multiplexer (*MUX*) is a combinational logic circuit used to select one of multiple input lines
- A multiplexer has 2^n input pins, n select pins, and 1 output pin.
  - The output is one of the input pins

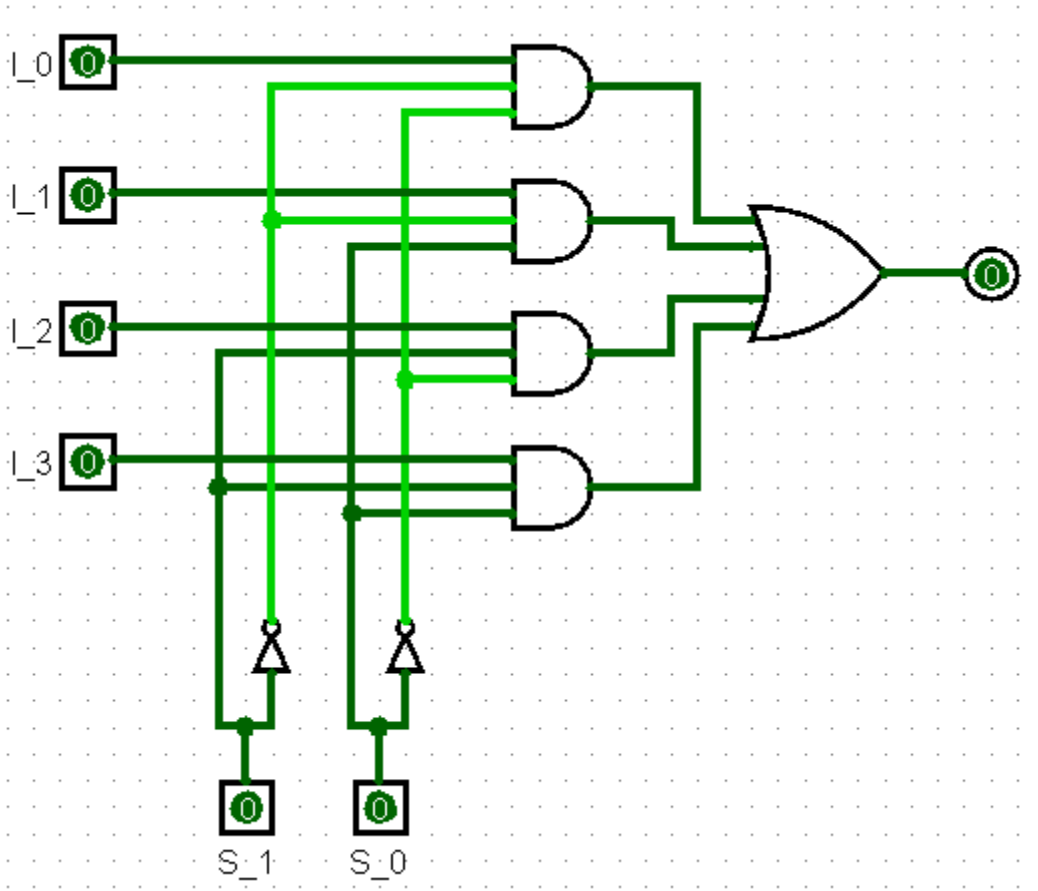
- The truth table for a 4x1 multiplexer:
  - $\boldsymbol{I}$ represents the input pins (4 = 2^2)
  - $\boldsymbol{S}$ represents the select pins (**2**)
  - $\boldsymbol{M}$ represents the output pin

S_1	S_0	M
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

SOP Expression: $M = \overline{S_1}\ \overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$

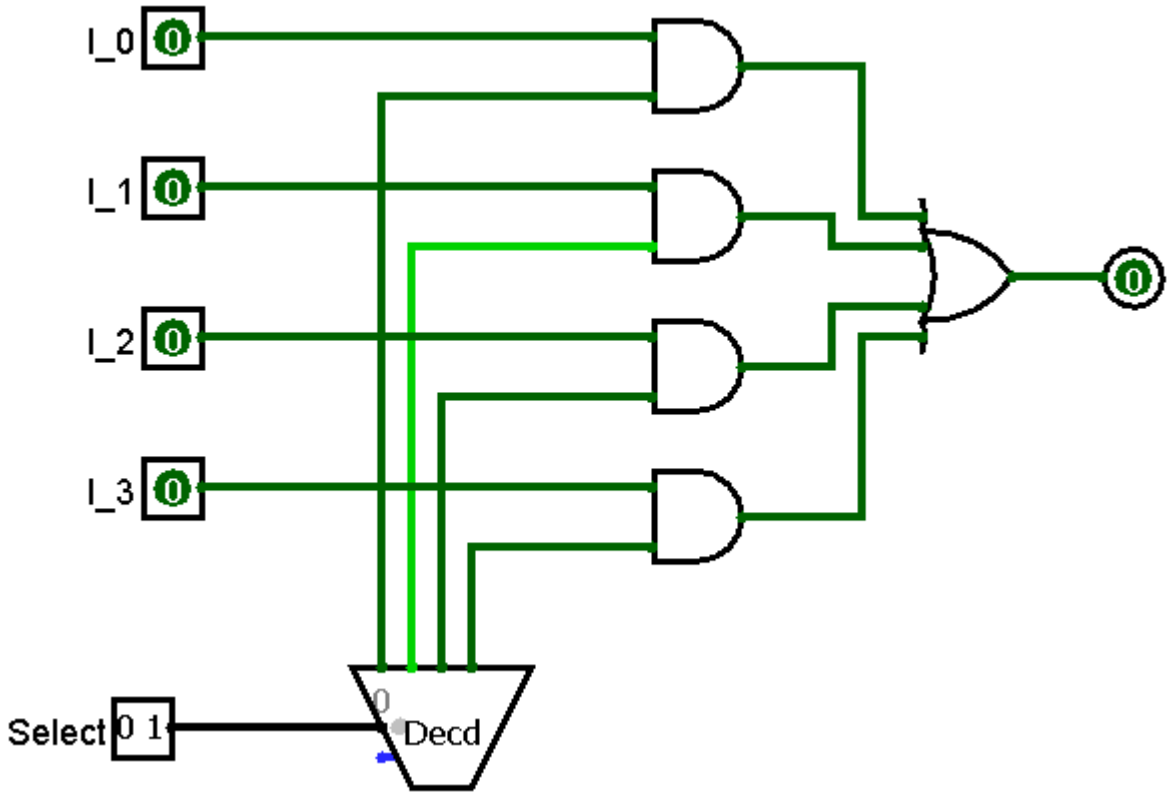
Multiplexers

- Logic circuit for a 4x1 multiplexer:



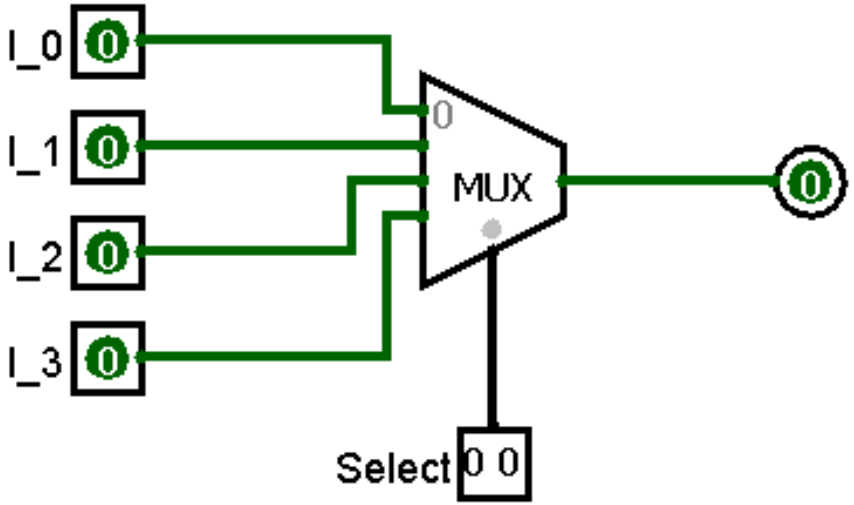
Multiplexers

- 4x1 multiplexer using a decoder:



Multiplexers

- Abstracted 4x1 multiplexer:



Multiplexers

- The truth table for an 8x1 multiplexer:
  - ***I*** represents the input pins (8 = 2^3)
  - ***S*** represents the select pins (**3**)
  - ***M*** represents the output pin

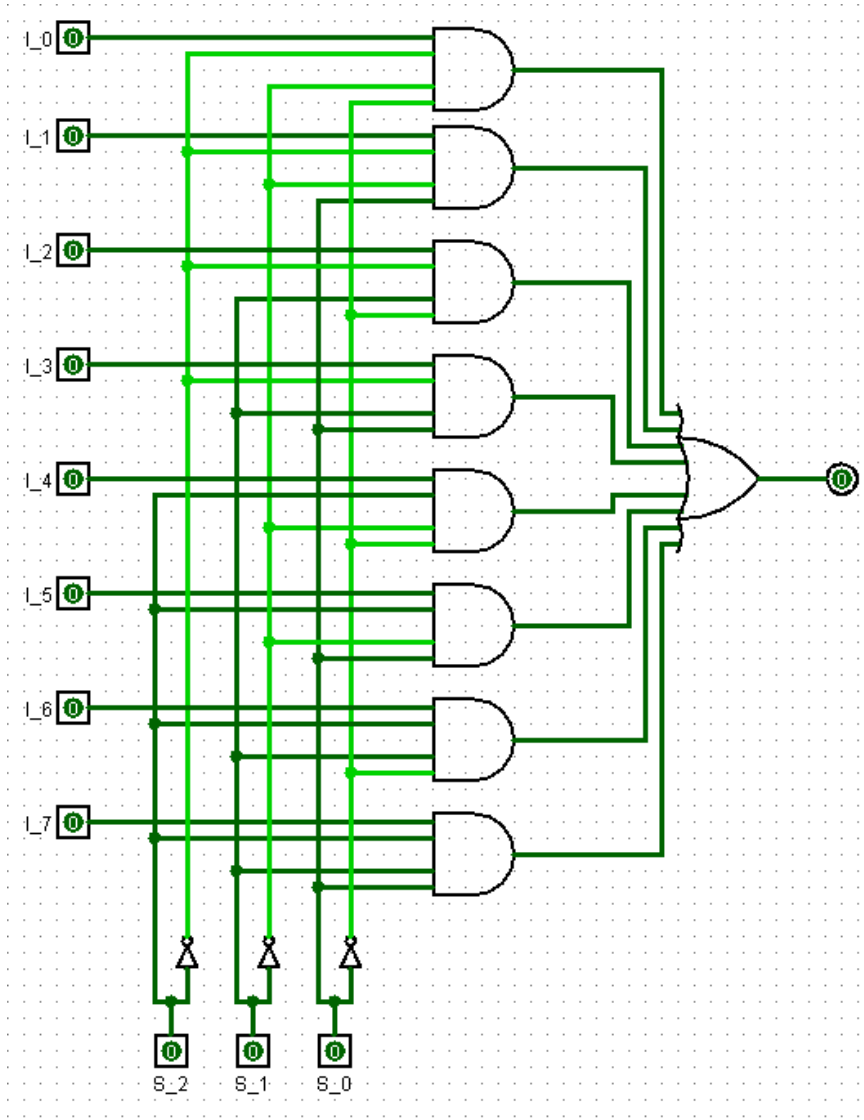
S_2	S_1	S_0	M
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

SOP Expression:

$$M = \overline{S_2}\ \overline{S_1}\ \overline{S_0}\ I_0 + \overline{S_2}\ \overline{S_1} S_0 I_1 + \overline{S_2} S_1 \overline{S_0} I_2 + \overline{S_2} S_1 S_0 I_3 + S_2 \overline{S_1}\ \overline{S_0}\ I_4 + S_2 \overline{S_1} S_0 I_5 + S_2 S_1 \overline{S_0} I_6 + S_2 S_1 S_0 I_7$$

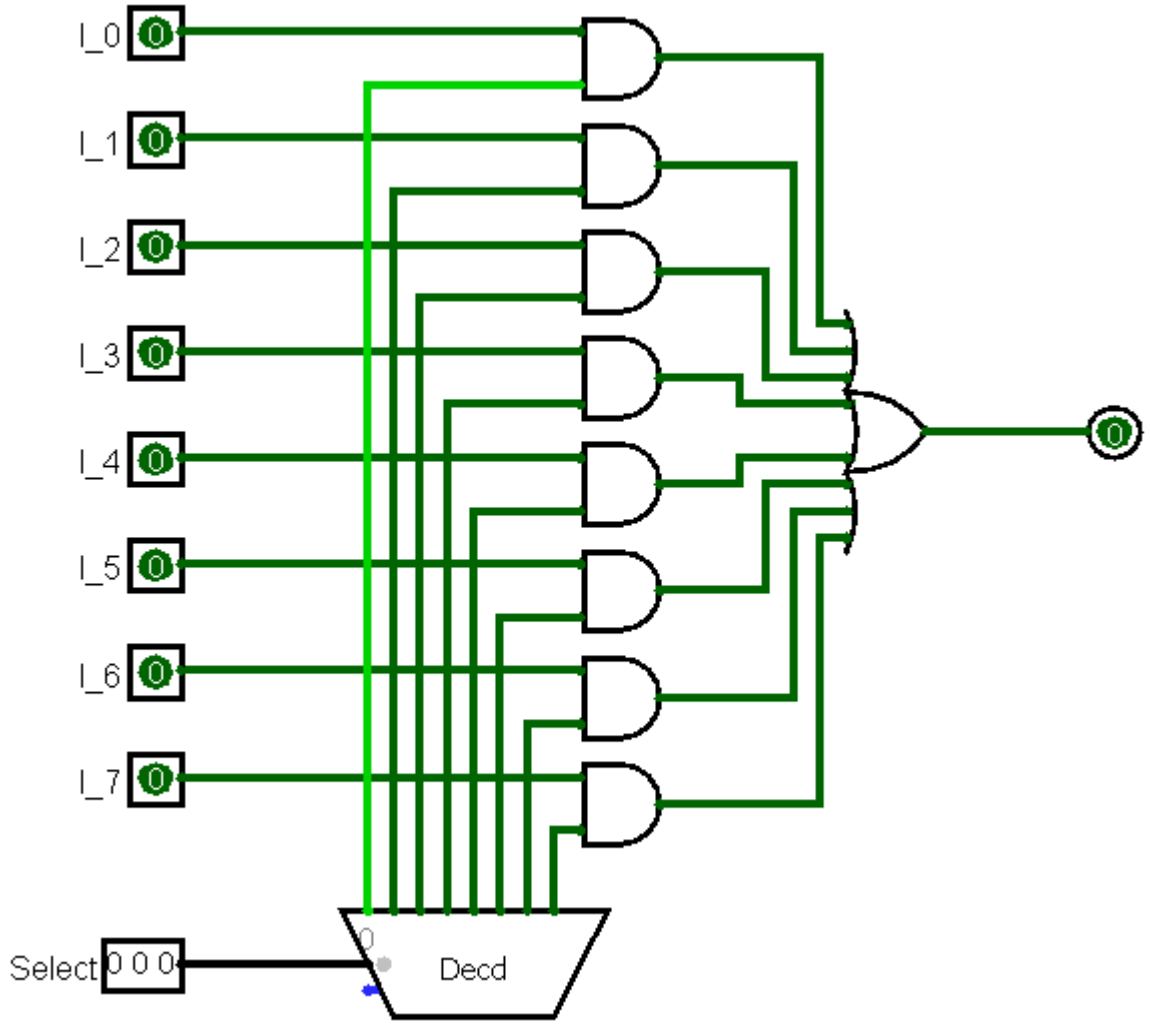
Multiplexers

- Logic circuit for an 8x1 multiplexer:



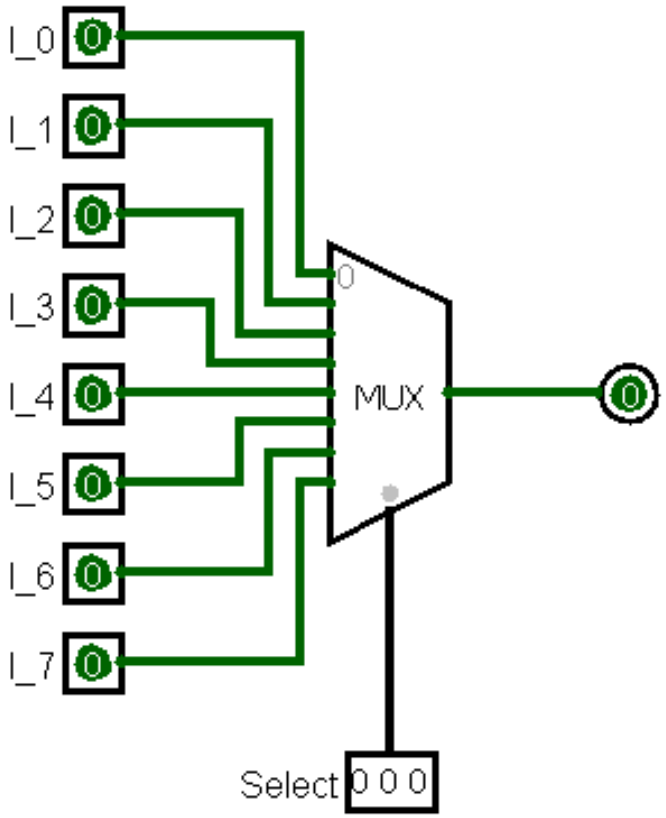
Multiplexers

- 8x1 multiplexer using a decoder:



Multiplexers

- Abstracted 8x1 multiplexer:



Multiplexers

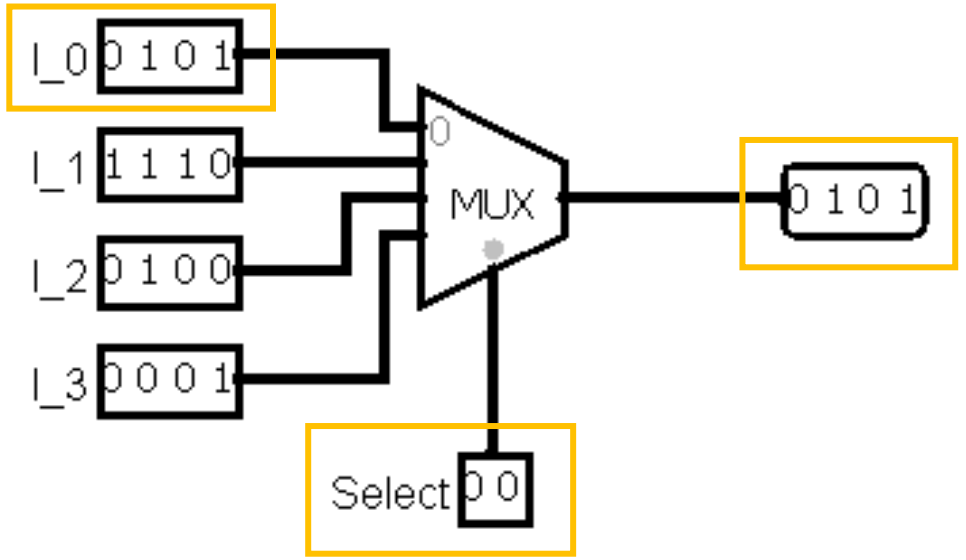
- Buses can be inputs and outputs of a multiplexer.
  - A multiplexer with s select lines and n-bit buses is a 2^s x n multiplexer

- For example, a multiplexer with 2 select lines (implying 4 inputs) where each input is a 4-bit bus
  - 2^s x n = 2^2 x 4 = 4x4 multiplexer

Multiplexers

- 4x4 Multiplexer:

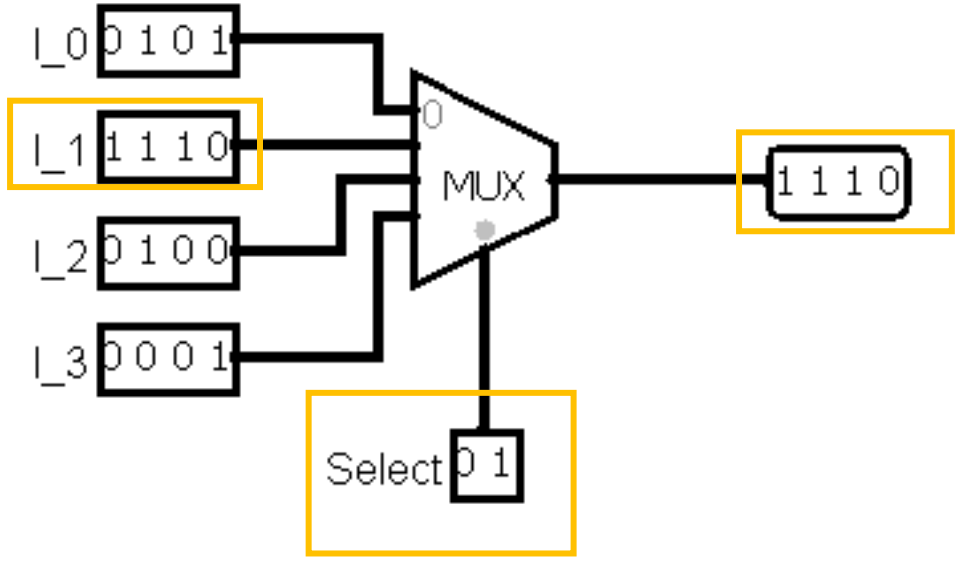
S_1	S_0	M
0	**0**	$\boldsymbol{I_0}$
0	1	I_1
1	0	I_2
1	1	I_3



Multiplexers

- 4x4 Multiplexer:

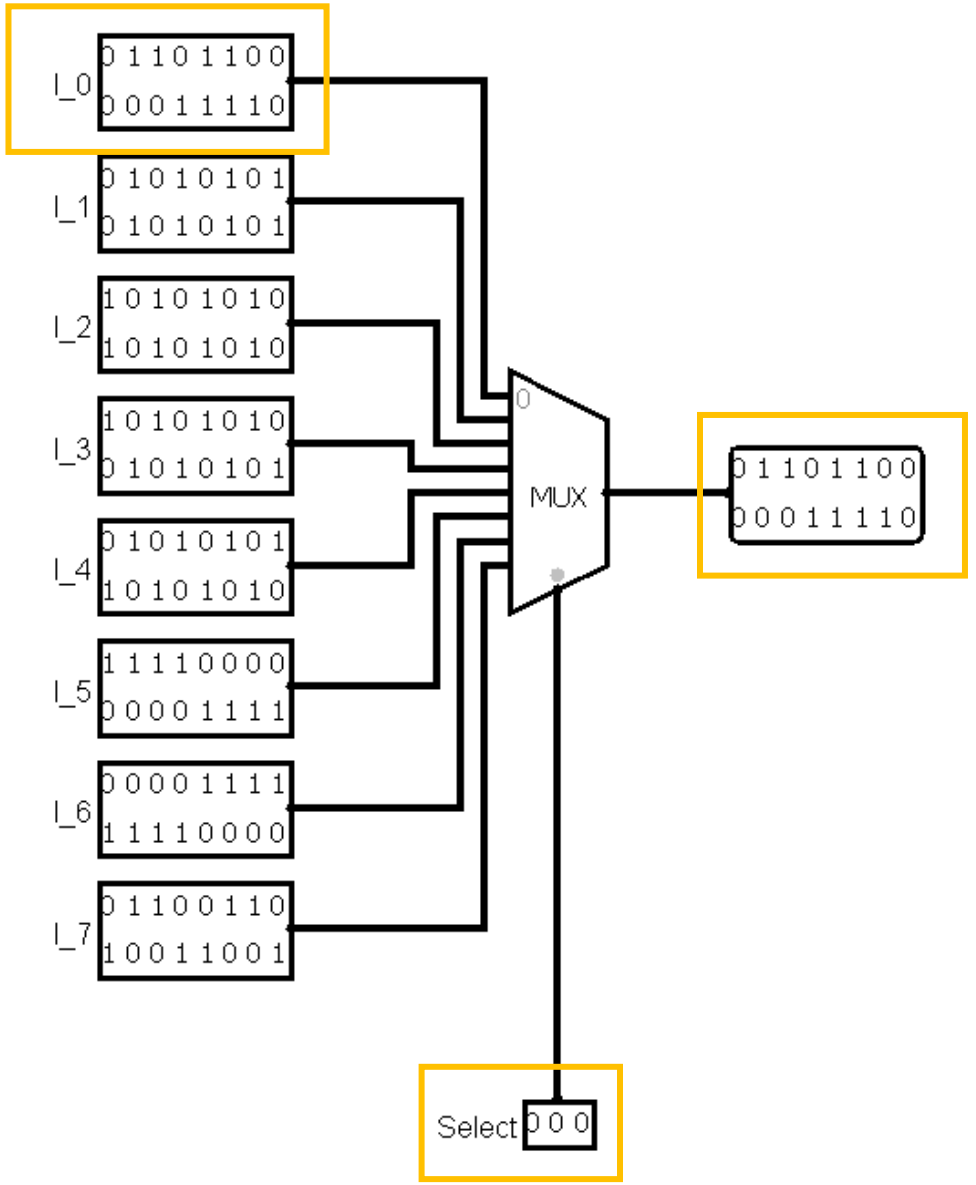
S_1	S_0	M
0	0	I_0
0	**1**	$\boldsymbol{I_1}$
1	0	I_2
1	1	I_3



Multiplexers

- 8x16 Multiplexer:

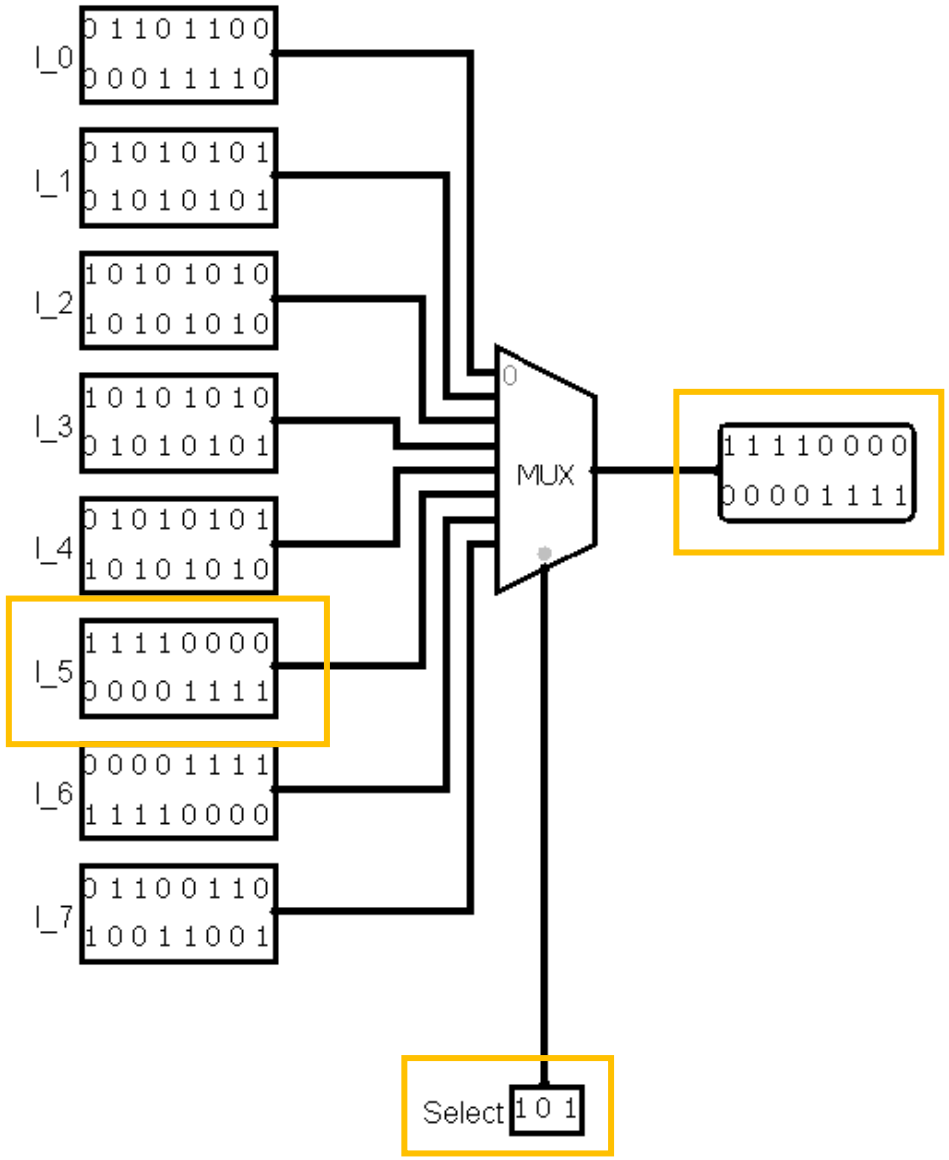
S_2	S_1	S_0	M
0	**0**	**0**	$\boldsymbol{I_0}$
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



Multiplexers

- 8x16 Multiplexer:

S_2	S_1	S_0	M
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	**0**	**1**	$\boldsymbol{I_5}$
1	1	0	I_6
1	1	1	I_7



Demultiplexers

- A demultiplexer (*DMX*) is a combinational logic circuit used to select the output from one input line
- A demultiplexer has 1 input pin, n select pins, and 2^n output pins.

- The truth table for a 1x4 demultiplexer:
  - $\boldsymbol{I}$ represents the input pin
  - $\boldsymbol{S}$ represents the select pins (**2**)
  - $\boldsymbol{D}$ represents the output pins ($4 = 2^2$)

S_1	S_0	D_3	D_2	D_1	D_0
0	**0**	0	0	0	$\boldsymbol{I}$
0	**1**	0	0	$\boldsymbol{I}$	0
1	**0**	0	$\boldsymbol{I}$	0	0
1	**1**	$\boldsymbol{I}$	0	0	0

Demultiplexers

SOP Expressions:

$$D_0 = \overline{S_1}\ \overline{S_0}\ I$$

$$D_1 = \overline{S_1} S_0 I$$

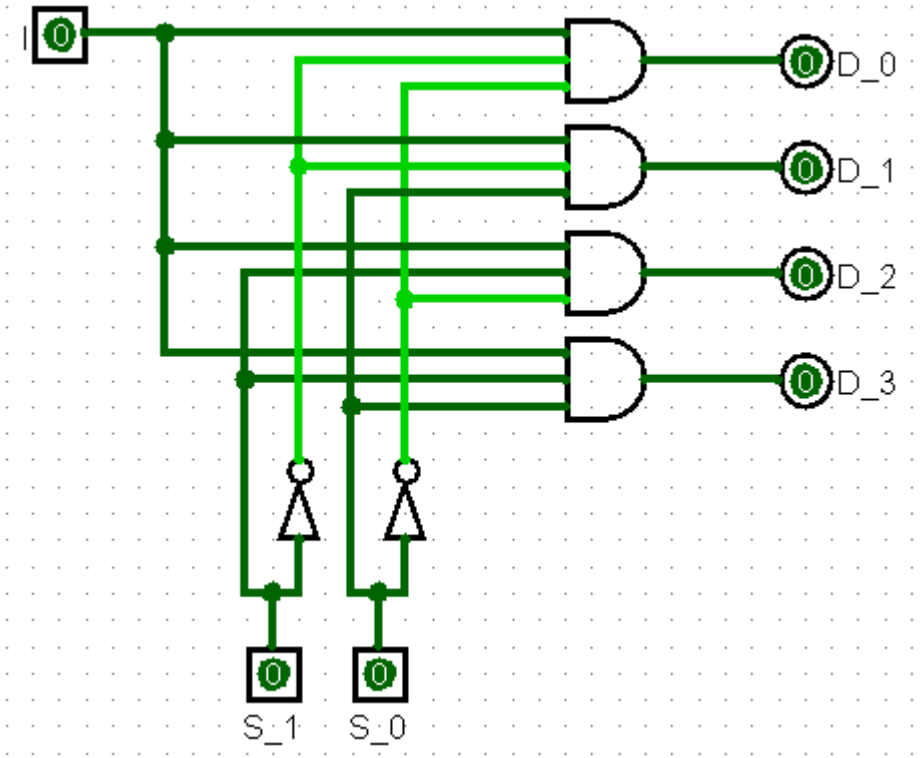
$$D_2 = S_1 \overline{S_0} I$$

$$D_3 = S_1 S_0 I$$

S_1	S_0	D_3	D_2	D_1	D_0
0	**0**	0	0	0	***I***
0	**1**	0	0	***I***	0
1	**0**	0	***I***	0	0
1	**1**	***I***	0	0	0

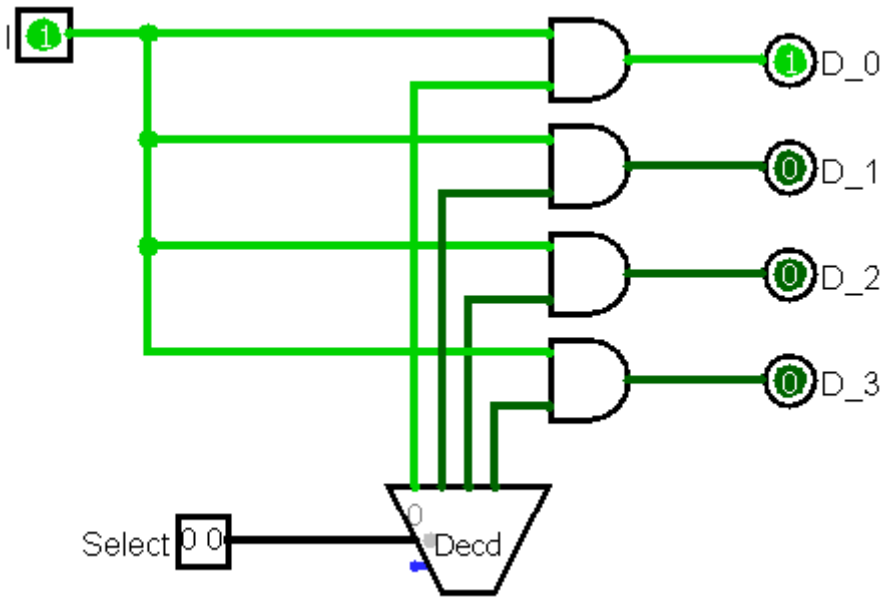
Demultiplexers

- 1x4 Demultiplexer:



Demultiplexers

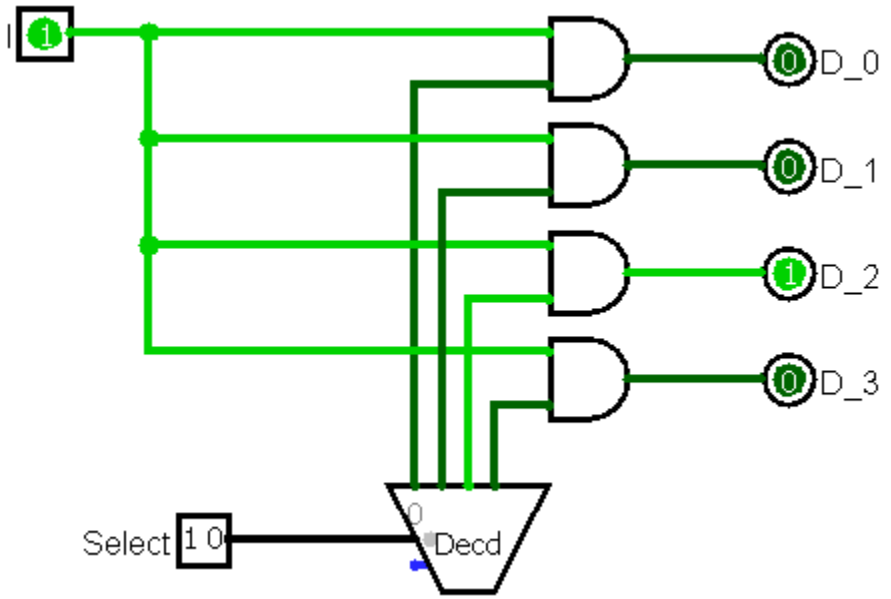
- 1x4 Demultiplexer using a decoder:



Demultiplexers

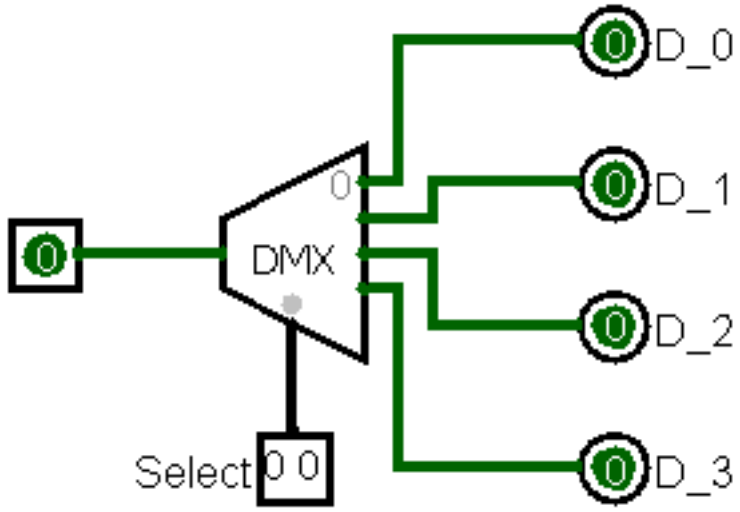
- 1x4 Demultiplexer:

S_1	S_0	D_3	D_2	D_1	D_0
0	0	0	0	0	I
0	1	0	0	I	0
1	**0**	**0**	***I***	**0**	**0**
1	1	I	0	0	0



Demultiplexers

- Abstracted 1x4 demultiplexer:



Demultiplexers

- The truth table for a 1x8 multiplexer:
  - $\boldsymbol{I}$ represents the input pin
  - $\boldsymbol{S}$ represents the select pins (**3**)
  - $\boldsymbol{D}$ represents the output pins (8 = 2^3)

S_2	S_1	S_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	**0**	**0**	0	0	0	0	0	0	0	$\boldsymbol{I}$
0	**0**	**1**	0	0	0	0	0	0	$\boldsymbol{I}$	0
0	**1**	**0**	0	0	0	0	0	$\boldsymbol{I}$	0	0
0	**1**	**1**	0	0	0	0	$\boldsymbol{I}$	0	0	0
1	**0**	**0**	0	0	0	$\boldsymbol{I}$	0	0	0	0
1	**0**	**1**	0	0	$\boldsymbol{I}$	0	0	0	0	0
1	**1**	**0**	0	$\boldsymbol{I}$	0	0	0	0	0	0
1	**1**	**1**	$\boldsymbol{I}$	0	0	0	0	0	0	0

Demultiplexers

SOP Expressions:

$D_0 = \overline{S_2}\,\overline{S_1}\,\overline{S_0}\,I$

$D_1 = \overline{S_2}\,\overline{S_1}\,S_0 I$

$D_2 = \overline{S_2}\,S_1\,\overline{S_0} I$

$D_3 = \overline{S_2}\,S_1 S_0 I$

$D_4 = S_2\,\overline{S_1}\,\overline{S_0}\,I$

$D_5 = S_2\,\overline{S_1}\,S_0 I$

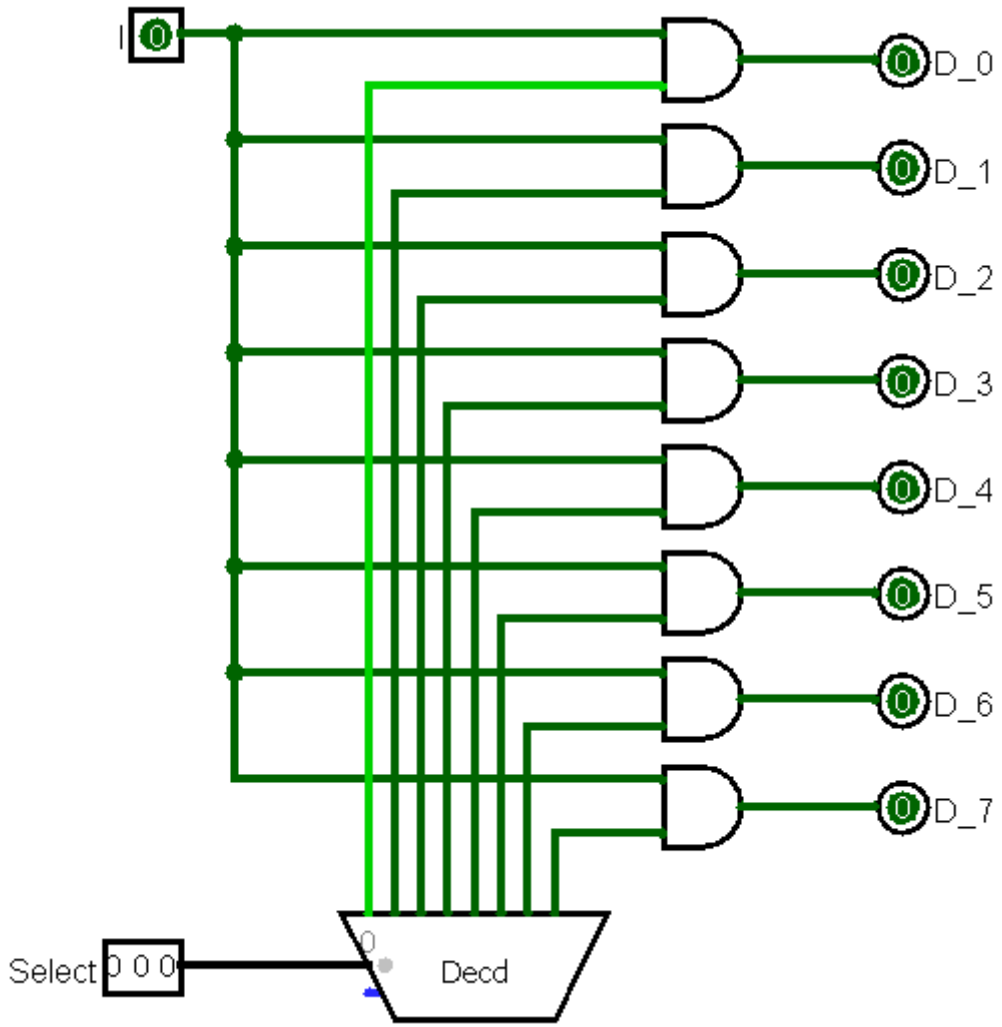
$D_6 = S_2 S_1\,\overline{S_0} I$

$D_7 = S_2 S_1 S_0 I$

S_2	S_1	S_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	**0**	**0**	0	0	0	0	0	0	0	***I***
0	**0**	**1**	0	0	0	0	0	0	***I***	0
0	**1**	**0**	0	0	0	0	0	***I***	0	0
0	**1**	**1**	0	0	0	0	***I***	0	0	0
1	**0**	**0**	0	0	0	***I***	0	0	0	0
1	**0**	**1**	0	0	***I***	0	0	0	0	0
1	**1**	**0**	0	***I***	0	0	0	0	0	0
1	**1**	**1**	***I***	0	0	0	0	0	0	0

Demultiplexers

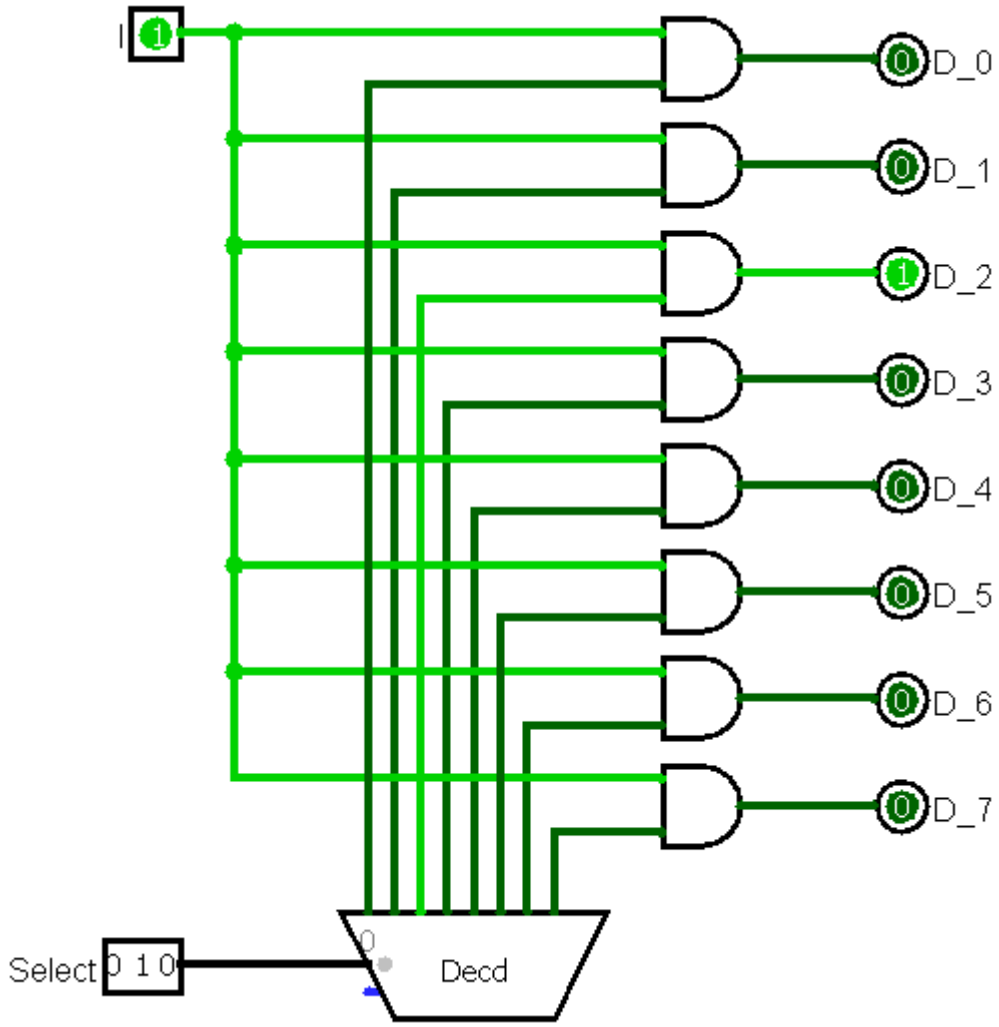
- 1x8 Demultiplexer:



Demultiplexers

- 1x8 Demultiplexer:

S_2	S_1	S_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	$\boldsymbol{I}$	**0**	**0**
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	I	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0



Demultiplexers

- Abstracted 1x8 demultiplexer: