A New Conception of Multilevel Inverter for UPS Application

Lincoln. M. Oliveira, Levy F. Costa, Deivid S. Marins, Sergio Daher, Fernando L. M. Antunes
Energy Processing and Control Group-GPEC, Electrical Engineering Department, Federal University of Ceará
Cx Postal 6001 - Campus do Pici, 60455-700, Fortaleza - CE - Brazil
E-mail: lincolnsobral@yahoo.com.br, deividmarins@yahoo.com.br, fantunes@dee.ufc.br

***Abstract* - This paper presents a single phase, 3 kVA, high efficiency and high power factor on-line Uninterruptible Power Supply (UPS) with 220 Vac input output voltage. The UPS input is composed by an active Power Factor Correction (PFC) boost rectifier which output voltage DC supplies a new conception of multilevel inverter. The multilevel inverter is based on multi-winding transformer with one primary and a several output coils, thus producing several partial AC square waveform. The inverter output stage combines these partial voltage in order to produced the sinusoidal output voltage. Analysis, principles of operation, design example as well as experimental results of the complete UPS system are presented in this paper.**

I. INTRODUCTION

Multilevel converters have been mainly used in medium or high power systems applications, such as static reactive power compensation and adjustable speed drives. In these applications, due to limitations of current available power semiconductor technology, multilevel concepts are usually the unique alternative because it is based on low frequency switching and also provide voltage and/or current sharing between the power semiconductors (H. Ertl, et al., 2002; Calais, et al., 1999; Tolbert, et al., 2000).

On the other hand, for small power systems (<10 kW), multilevel converters have been competing with high frequency PWM converters in applications where high efficiency is of major importance. It is well know that high temperature is one factor that decreases lifetime of many components (Tolbert, et al., 2000 ; Daher, 2006).

Taking this into account, it is expected that high efficiency (therefore less heat and lower temperature) topologies, like multilevel topologies, can reach high degree of reliability. Moreover, lower prices of power switches and new semiconductor technologies, as well as the current demand on high performance inverters have extended the applications of multilevel converters (Daher, 2006).

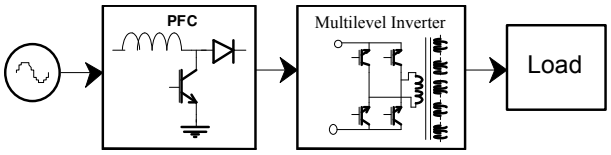

Fig. 1. Block diagram of the complete system

Reference (Daher, 2006) presents the use of multilevel topologies in a 3kVA off-grid PV system with an efficiency of 96%. Aiming to extend the use of multilevel topologies in low power systems this paper presents a single phase 3kVA, low frequency operation, high efficiency, high power factor, and high quality output voltage waveform Uninterruptible Power Supply (UPS). The proposed system consists a double conversion UPS, where the first conversion stage is composed by an active Power Factor Correction (PFC) rectifier and the second conversion stage is composed by a sinusoidal output voltage multilevel inverter, as shown in Fig. 1. Fig. 2 shows the proposed UPS topology. UPS circuit description, operation description topology as well as experimental results for grid mode operation (no battery bank) are presented here.

II. UPS CIRCUIT DESCRIPTION

The proposed UPS is composed by a rectifier with active PFC based on boost converter connected through a DC bus to the multilevel inverter. The multilevel inverter topology proposed by (Daher, 2006) is adopted in this work. The battery charge is based on the classical buck converter. The step-up converter is based on classical boost converter and it is responsible to step of battery voltage bank up to the DC bus voltage. In this paper is made only a grid mode operation analysis.

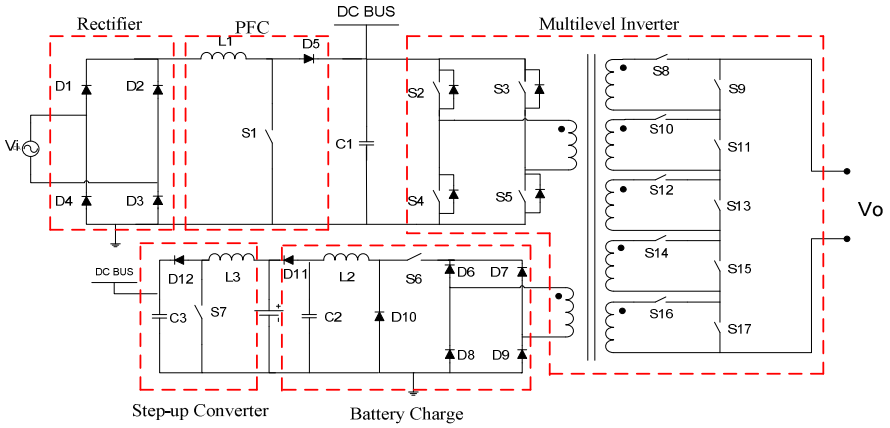

Fig. 2. Proposed UPS Topology

III. PFC ANALYSIS

A. *Circuit Description*

The first stage of the UPS is composed by a classical boost converter. This topology is used because it has the advantage to be simple and to use few component (reducing the weight and space). The Boost converter is controlled using conventional average current-mode-control implemented with the well-known PWM integrated circuit UC3854 for power factor correction (Todd, 1994). Fig. 3 shows the circuit and control block diagram of the boost converter.

B. *Principles of Operation*

The principle of operation of the boost converter is shown in Martins (2006). This paper shows a very simple analysis of the principle of operation of this converter.

- **1º Stage :** The switches Sb is on, thus the voltage across the inductor Lb is positive and the current through the inductor Lb increase linearly. In this stage there is no energy transference. The Fig. 4 (a) shows this stage.
- **2º Stage :** The switches Sb is off, thus the voltage across the inductor Lb is negative and the current through the inductor Lb decrease linearly. In this stage the energy is transference to the output. The Fig. 4 (b) shows this stage.

The main current and voltage waveform of this converter is shown in Fig. 5.

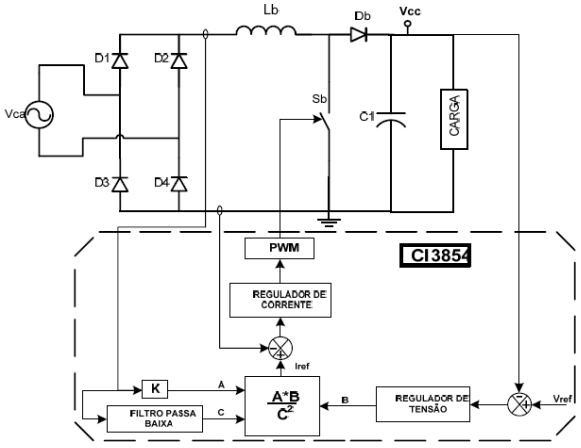

Fig. 3 – PFC Boost converter

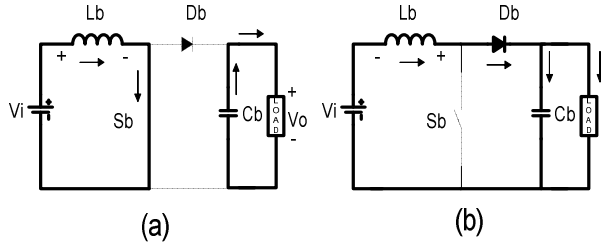

Fig. 4 – Principles of operation of the boost converter

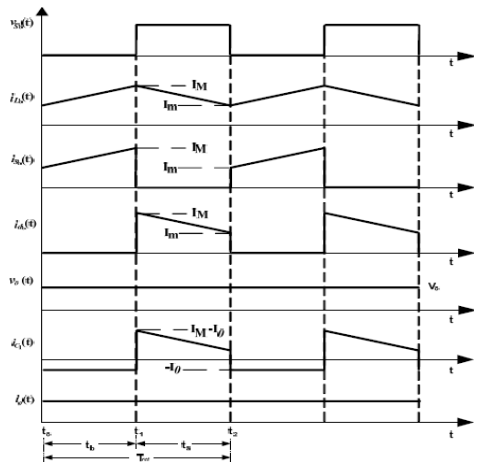

Fig. 5 – Main waveforms of the boost converter

IV. MULTILEVEL INVERTER ANALYSIS

A. *Circuit Description*

As shown in Fig. 2, the used inverter includes 3 main components: one H-bridge converter, one multi-winding transformer and one output stage. The H-bridge converter receives voltage from a DC source, supplied by boost PFC, and generates a square waveform at line frequency that is applied to the primary of the transformer. The transformer operates at line frequency and it has only one primary and a several output coils. These coils are electrically isolated from each other, thus producing several partial AC square waveform. The output stage combines these partial voltage in order to produced the sinusoidal output voltage.

The controller is based on an 8-bit AT90S8535 microcontroller (running at 11.0592 MHz) from ATMEL. The control program was developed in C language, and all switch signals were implemented in lookup tables stored in the microcontroller internal memory. According to the DC bus voltage and output current, it was possible to adjust the output voltage by changing the lookup table. A total of 16

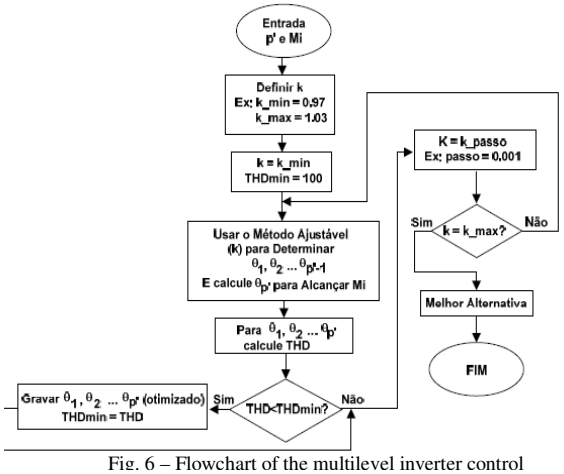

Fig. 6 – Flowchart of the multilevel inverter control

lookup tables were implemented (33, 35, . . . , 63 levels). Fig. 6 shows the flowchart to the inverter control.

B. Principles of Operation

The principle of operation of the inverter will be describe using a structure with an output stage composed by only two cells, as shown in Fig. 7.

- **1º Stage :** The switches Sa, Sb, Sc and Sd are off, thus there is no energy transference, and the output voltage is zero. This operation stage is shown in Fig. 8 (a).
- **2º Stage :** The switches Sa, Sd are on, thus the primary coil receives positive voltage. The switches S2 and S3 are on, then the output voltage is equal the coil 1 voltage. Hence the output voltage is Vi. This operation stage is shown in Fig. 8 (b).
- **3º Stage :** The switches Sa, Sd, thus the primary coil receives positive voltage. The switches S1 and S4 are on, then the output voltage is equal the coil 2 voltage. Hence the output voltage is 2Vi. This operation stage is shown in Fig. 8 (c).
- **4º Stage :** The switches Sa, Sd, thus the primary coil receives positive voltage. The switches S1 and S3 are on. The coil 2 and coil 1 are connected in series, then the output voltage is equal the coil 1 plus coil 2 voltage. Hence the output voltage is 3Vi. This operation stage is shown in Fig. 8 (d).

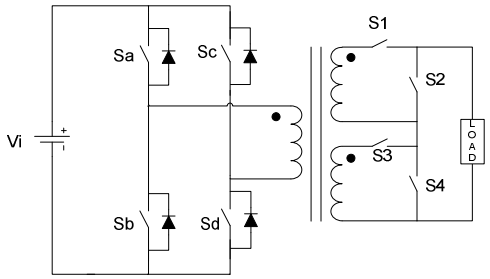

Fig. 7 – Simplified multilevel inverter topology

- **5º Stage :** This stage is equal to stage 3º. In this moment, the output waveform start to down its level. This operation stage is shown in Fig. 8 (c).
- **6º Stage :** This stage is equal to stage 2º. This operation stage is shown in Fig. 8 (b).
- **7º Stage :** This stage is equal to stage 1º. This operation stage is shown in Fig. 8 (d).
- **8º Stage :** The switches Sb, Sc, thus the primary coil receives negative voltage. The switches S2 and S3 are on, then the output voltage is equal the coil 1 voltage. Hence the output voltage is -Vi. This operation mode is shown in Fig. 8 (e).
- **9º Stage :** The switches Sb, Sc, thus the primary coil receives negative voltage. The switches S1 and S4 are on, then the output voltage is equal the coil 2 voltage. Hence the output voltage is -2Vi. This operation stage is shown in Fig. 8 (f).
- **10º Stage :** The switches Sb, Sc, thus the primary coil receives negative voltage. The coil 2 and coil 1 are connected in series, then the output voltage is equal the coil 1 plus coil 2 voltage. Hence the output voltage is -3Vi. This operation stage is shown in Fig. 8 (g).
- **11º Stage :** This stage is equal to stage 9º. This operation stage is shown in Fig. 8 (f).
- **12º Stage :** This stage is equal to stage 8º. This operation stage is shown in Fig. 8 (e).

The Table. 1 shows the resume of the inverter output voltage according to the states of the switches.

TABLE I
INVERTER OUTPUT VOLTAGE

				V =Vi	Vp=0	Vp=-Vi
S1	S2	S3	S4	Vo	Vo	Vo
Off	On	Off	On	0	0	0
Off	On	On	Off	Vi	0	-Vi
On	Off	Off	On	2Vi	0	-2Vi
On	Off	On	Off	3Vi	0	-3Vi

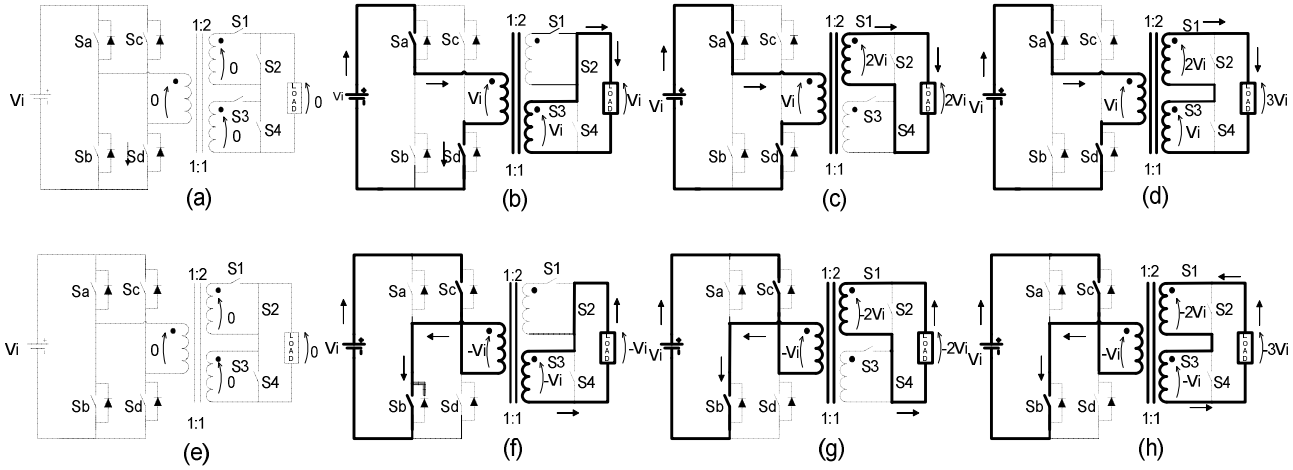

Fig. 8 – Multilevel Inverter Principles of Operation

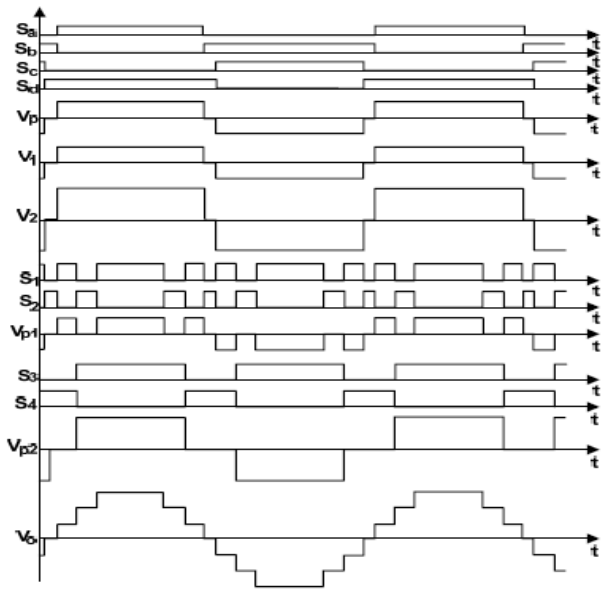

Fig. 9 – Switches signals and voltage waveform for a 2 cells structure

Fig. 9 shows the signal gate-source of all switches and the mains voltages waveform, where is possible to see that the cells work with different frequencies.

V. POWER CIRCUIT DESIGN

The specification of complete system is shown in Table 2. The PFC and inverter design are shown in this section, respectively.

TABLE II
SPECIFICATION OF THE COMPLETE SYSTEM

Output power	Po = 3kVA
Input voltage	V_I = 220 V
Input voltage variation (máx)	$\Delta V_{I\%}$ = 25%
Input current variation (máx)	$\Delta I_{I\%}$ = 15%
Output voltage	Vo = 220 V
Output voltage variation	$\Delta Vo_{\%}$ = 5%
Output voltage frequency	f_R = 60hz
Load power factor	FP = 1
Switching frequency (PFC)	fs_1 = 40kHz
Number of secundary (cells)	N_S = 5
Secundary voltages	V_S= 10, 20, 40, 80 and 160 V
Primary voltage (DC Bus)	V_P=400V
Theorical efficiency (PFC)	η_1 = 95%

A. PFC Design

The maximum and minimum input voltage of the system are given by (1) and (2), respectively:

$$Vi_{MAX} = Vi + (\Delta Vi_{\%} \cdot Vi) = 275V \quad (1)$$

$$Vi_{MIN} = Vi - (\Delta Vi_{\%} \cdot Vi) = 165V \quad (2)$$

The maximum and minimum input current of the system are given by (3) and (4), respectively:

$$Ii_{MAX} = \frac{P_O}{\eta \cdot Vi_{MIN}} = 20.7A \quad (3)$$

$$Ii_{MIN} = \frac{P_O}{\eta \cdot Vi_{MAX}} = 12.4A \quad (4)$$

The duty-cycle for the minimum input voltage is given by (5):

$$D = 1 - \frac{\sqrt{2} \cdot Vi_{MIN}}{V_O} = 0.417 \quad (5)$$

The input current variation is given by (6):

$$\Delta I = \Delta I_{I\%} \frac{P_O}{\eta \cdot V_I} = 4.4A \quad (6)$$

The design of the filter inductor is made according to (ref), thus the value of filter inductance is given by (7):

$$L_1 = \frac{\sqrt{2} \cdot Vi_{MIN} \cdot D}{f_S \cdot \Delta I} = 553\mu H \quad (7)$$

The design of the filter capacitor is made according to (ref), thus the value of filter capacitance is given by (8):

$$C_2 = \frac{2 \cdot P_O}{4 \cdot \pi \cdot f_R \cdot V_O^2 \cdot \Delta V_O} = 3.6mF \quad (8)$$

In this work is used 8 capacitor in parallel with capacitance of 470uF/450V, each other.

B. Inverter Design

The levels number of the inverter is given by (9):

$$n = 2^{N+1} - 1 = 63 \quad (9)$$

The number of steps in a quarter–cycle is given by (10):

$$p' = \frac{n-1}{2} = 31 \quad (10)$$

The output current of the inverter is given by (11):

$$Io = \frac{Vo}{P_O} = 13.6A \quad (11)$$

The maximum relation ratio of the transformer is given by (12) (Daher, 2006) :

$$R_{MAX} = p' \cdot \left(\frac{Vs_{MIN}}{V_P} \right) = 0.93 \quad (12)$$

The current through the primary coil of the transformer is given by (13) (Daher, 2006):

$$I_P = 0.866 \cdot R_{MAX} \cdot Io = 11A \quad (13)$$

The cells frequencies are calculated according to (Daher, 2006) and they are given from (14) to (18), where n_c is the number of the cell:

$$fc_1 = f_R \cdot \left(2^{N-n_C+2} - 2\right) = 3720Hz \quad (14)$$

$$fc_2 = f_R \cdot \left(2^{N-n_C+2} - 2\right) = 1800Hz \quad (15)$$

$$fc_3 = f_R \cdot \left(2^{N-n_C+2} - 2\right) = 840Hz \quad (16)$$

$$fc_4 = f_R \cdot \left(2^{N-n_C+2} - 2\right) = 360Hz \quad (17)$$

$$fc_5 = f_R \cdot \left(2^{N-n_C+2} - 2\right) = 120Hz \quad (18)$$

VI. EXPERIMENTAL RESULTS

In order to verify the operation and evaluate the performance of the proposed UPS, a laboratory prototype was implemented and tested. The prototype was tested with linear and non-linear load, with input voltage of 220V. The components used to assemble the prototype are listed in Table 3, Table 4 and Table 5.

TABLE III
PFC COMPONENTS SPECIFICATION

Rectifier Diode	GBPC3510
Switch S1	IRGP50B60PD1
Diode D1	HFA25PB60
Input Filter Capacitors	8 x 470uF/450V
	Lf = 553uH
Input Filter Inductor	NEE - 76/25
	N = 70 turns (47x26AWG)
	δ = 4.13 mm

TABLE IV
INVERTER COMPONENTS SPECIFICATION

Switches S2 - S5	IRFGP4063D
Switches S8 - S13	IRFP064N
Switches S14 and S15	IRFP4227N
Switches S16 and S17	IRFGP4063D

TABLE V
TRANSFORMER SPECIFICATION

Primary Coil	400V / 11A
Secondary Coil 1	12V / 13.6A
Secondary Coil 2	24V / 13.6A
Secondary Coil 3	48V / 13.6A
Secondary Coil 4	96V / 13.6A
Secondary Coil 5	192V / 13.6A
Frequency	60Hz

A. *Waveform and Curves of the UPS System*

Fig. 10 shows the input voltage and input current waveforms where high power factor is observed. The Fig. 11 show the details of the input voltage where low voltage variation is observed. The output voltages and currents of the inverter are shown in Figs. 12 and 13, where it can be seen a high quality sinusoidal voltage waveform, independently of the characteristic of the connected load. Fig. 14 illustrates the power factor behavior as a function of the output power. Finally, Fig. 15 shows efficiency curve, as a function of output power.

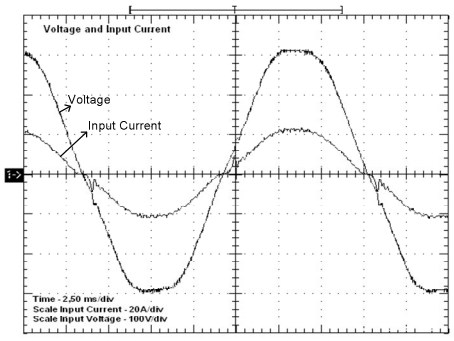

Fig. 10 – Mains input voltage and current
(100V/div.; 20A/div.; 2.5ms/div.)

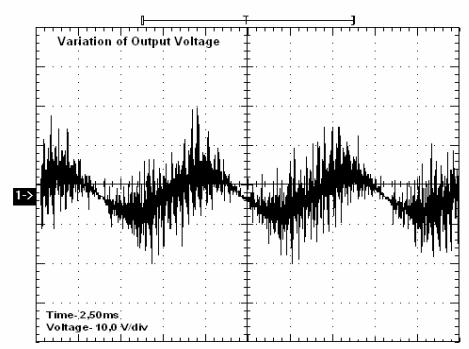

Fig. 11 – Details of the input voltage
(100V/div.; 2.5ms/div.)

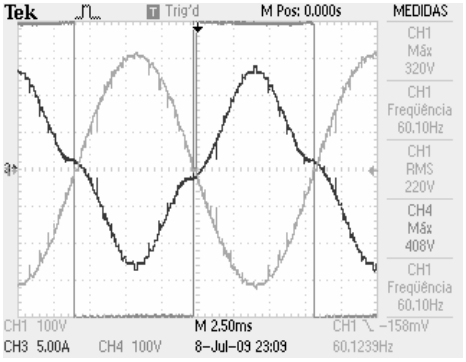

Fig. 12 – Output voltage and current of the inverter for linear load and primary coil voltage of the transformer.
(100V/div.; 20A/div.; 100V/div.; 2.5ms/div.)

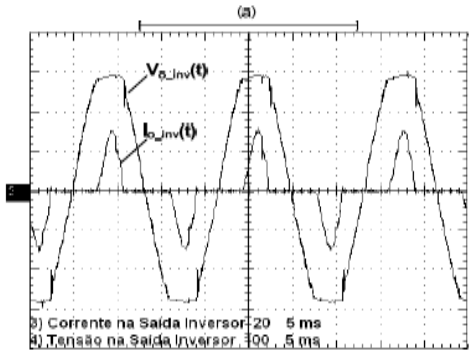

Fig. 13 – Output voltage and current of the inverter for non-linear load.
(100V/div.; 20A/div.; 2.5ms/div.)

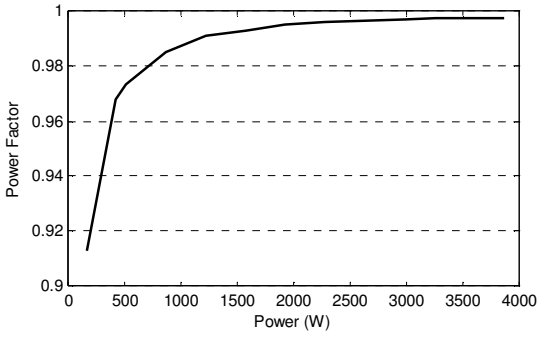

Fig. 14 – Power factor as a function of the output voltage

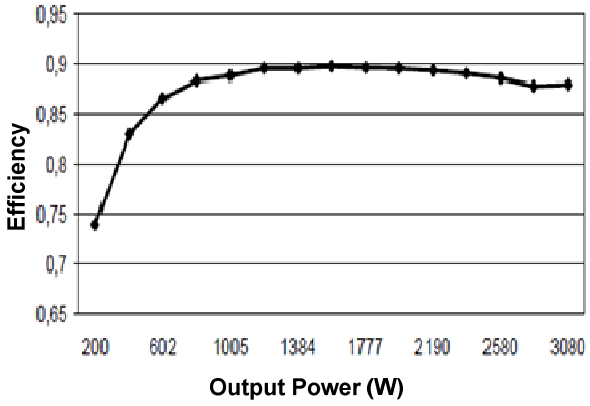

Fig. 15 – Efficiency of the UPS system as a function of the output voltage

Photos of the implemented prototype are shown in Fig. 16 and Fig. 17.

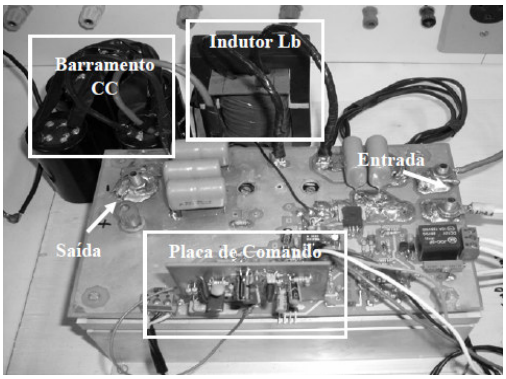

Fig. 16 – PFC Prototype Photograph

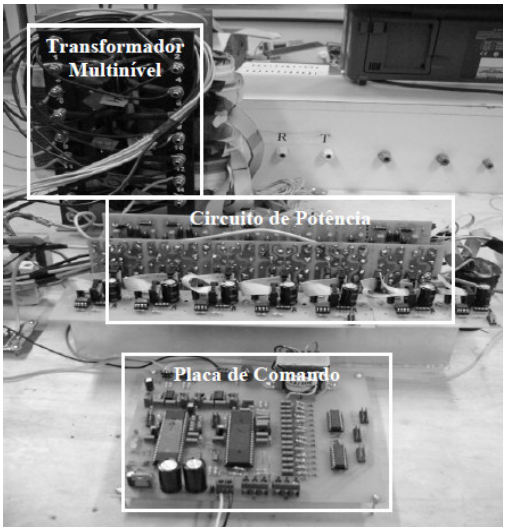

Fig. 17 – Inverter Prototype Photograph

VII. CONCLUSION

A general presentation of a 3kVA uninterrupted power supply on the grid mode operation has been presented. A brief description of the topology in study, the design procedure and the experimental results were performed with the emphasis on the possibility to applied a multilevel inverter to UPS.

The use of multilevel inverters in UPS presents as advantages the high efficiency and robustness added to the system, such as the possibility of using low frequency in the sinusoidal wave generation, which reduces electromagnetic interference generated within the converter thus decreasing the interference possibility in systems with high susceptibility to EMI.

The system has presented a power factor of 0.998, when it operates with nominal load. Moreover, the system has also reached an efficiency of 89.8%.The efficiency of the system was limited by the efficiency of the transformer. The use of a transformer with toroidal core can increase the efficiency of the system.

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