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Xilinx FPGA Based Multilevel PWM Single Phase Inverter

S. Mekhilef and A. Masaoud
Department of Electrical Engineering
University of Malaya, 50603 Kuala Lumpur, Malaysia
Tel: 603-79676851 Fax: 603-7595316 E-mail: saad@um.edu.my

Abstract

In this paper a XILINX FPGA based multilevel PWM single-phase inverter was constructed by adding a bi-directional switchs to the conventional bridge topology. The inverter can produce three and five different output voltage levels across the load. XILINX FPGA is a programmable logic device developed by XILINX which is considered as an efficient hardware for rapid prototyping. It is used as a PWM generator to apply the appropriate signals to inverter switches. In addition to XILINX FPGA, Matlab/Simulink software was used for simulation and verification of the proposed circuit before implementation, Simulation and experimental results show that both are in close agreement.

I. INTRODUCTION

Multilevel inverters have been attracting increasing attention in the past few years as power converters of choice in many applications. They have significant advantages over the conventional one because of the capability to reduce the undesirable harmonics in order to improve the performance and efficiency. Various topologies to realize these inverters have been introduced and studied recently. Waveform synthesis methods for these inverters include staircase modulation, sine-triangle carrier modulation, space vector modulation, and other predictive methods [1-3]. Normally the topological structure of multilevel inverter suggested must cope with the following points:1) It should have less switching devices as far as possible, 2) It should be capable of enduring very high input voltage such as HVDC transmission for high power applications, and 3) Each switching device should have lower switching frequency owing to multilevel approach [4].

PWM generation is considered the more important in the inverter design and Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical (SPWM) with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals [5].

Xilinx field programmable gate arrays (FPGA's) are standard integrated circuits that can be programmed by a user to perform a variety of complex logic functions [6]. The high level of integration available with these devices (currently up to 500,000 gates) means that they can be used to implement complex electronic systems. Furthermore, there are many advantages due to the rapid design process and reprogramable functions. XILINX FPGA enables to produce prototype logic designs right in a short period. It is possible to
create, implement, and verify a new design. This is a sharp contrast to conventional gate array design processes, which can take months to produce working silicon. The FPGA architecture consists of three types of configurable elements - a perimeter of input/output blocks (IOBs), a core array of configurable logic block (CLBs), and resources for interconnection. The IOBs provide a programmable interface between the internal array of logic blocks (CLBs) and the device's external package pins. CLBs perform user-specified logic functions, and the interconnect resources carry signals among the blocks. A configuration program stored in internal static memory cells determines the logic functions and the interconnections. The configuration data is loaded into the device during power-up reprogramming functions [7].

This paper presents a multilevel PWM inverter whose output voltage maybe has three or five levels based on modulation index used. Xilinx WebPack software 4.1 is used to generate PWM pattern by means of both schematic diagrams and VHDL programs. The final design is

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converted in configuration data file and loaded into XS95108 CPLD board.

II. THE PROPOSED CIRCUIT

The multilevel PWM single phase inverter has been clearly presented in Fig.1. A bi-directional switch consists of two switches S5 and S6 and four diodes are added to the conventional full-bridge inverter.

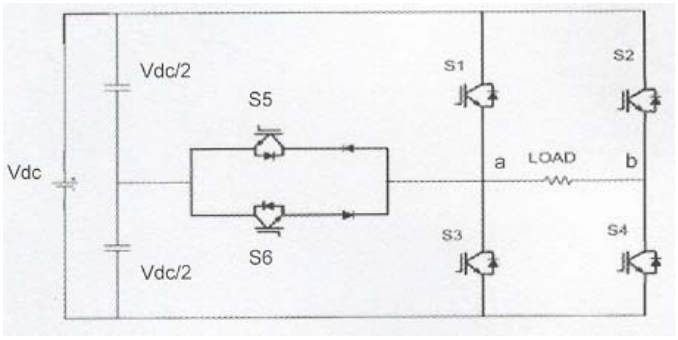

Fig.1 The proposed circuit of the multilevel PWM single phase inverter

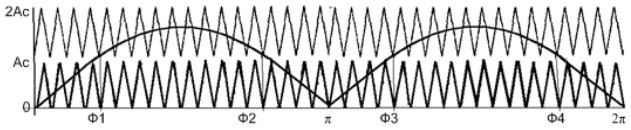

Fig.2 PWM generation technique used for the multilevel PWM single phase inverter.

Two dc capacitors, which are considered as an energy tank for the inverter, are also connected to the dc voltage source. The function of bi-directional switch is to control current flow. The PWM pattern adopted in the proposed inverter makes the inverter producing output voltage with three levels (zero and half supply dc voltage positive and negative respectively) at modulation index (Ma ≤ 0.5) and five levels (zero, half and full supply voltage positive and negative respectively) at modulation index (Ma > 0.5).
The parameters of the modulation process are shown in Fig.2 and defined as following:

1) The modulation index is defined as:

$$\mathrm{Ma} = \frac{\mathrm{Am}}{2\mathrm{Ac}} \tag{1}$$

Where Am is peak value of sinusoidal wave and Ac is the peak is the carrier peak-peak value.

2) The frequency modulation index:

$$\mathrm{Mf} = \frac{fc}{fm} \tag{2}$$

Where fc is the frequency of the carrier wave and fm is the frequency of the sinusoidal wave.

3) The angle of displacement existing between the sinusoidal wave and the first positive carrier wave can be defined as following:

$$\mathrm{Am.Sin}\,(\phi 1) = \mathrm{Ac}$$

$$\phi 1 = \mathrm{Sin}^{-1}\left(\frac{\mathrm{Ac}}{\mathrm{Am}}\right) \tag{3}$$

$$\phi 2 = \pi - \phi 1 \tag{4}$$

$$\phi 3 = \pi + \phi 1 \tag{5}$$

$$\phi 4 = 2\pi - \phi 1 \tag{6}$$

The proposed inverter may be operate in four modes defined as following:

Mode1: $\phi 1 < wt < \phi 2$ (7)

Mode2: $0 < wt \le \phi 1$ and $\phi 2 < wt \le \pi$ (8)

Mode3: $\pi < wt \le \phi 3$ and $\phi 4 < wt \le 2\pi$ (9)

Mode4: $\phi 3 < wt \le \phi 4$ (10)

At modulation index Ma > 0.5 the inverter operates in all modes producing five voltage levels 0, Vdc/2,Vdc, -Vdc/2, -Vdc respectively.
At certain load when the required voltage is Vdc/2 or less the inverter operates at modulation index Ma≤0.5 in two modes 2 and 3 only. The displacement angles become:

$$\phi 1 = \phi 2 = \frac{\pi}{2} \tag{11}$$

$$\phi 3 = \phi 4 = \frac{3\pi}{2} \tag{12}$$

ON SWITCHES	Va	Vb	Vab=Vo
S4,S1	Vdc	0	+Vdc
S4,S6	Vdc/2	0	+Vdc/2
S4,S3	0	0	0
S2,S1	Vdc/2	Vdc/2	0
S2, S5	0	Vdc	-Vdc
S2,S3	0	Vdc/2	-Vdc/2

Table.1 Output voltage based on switches combination

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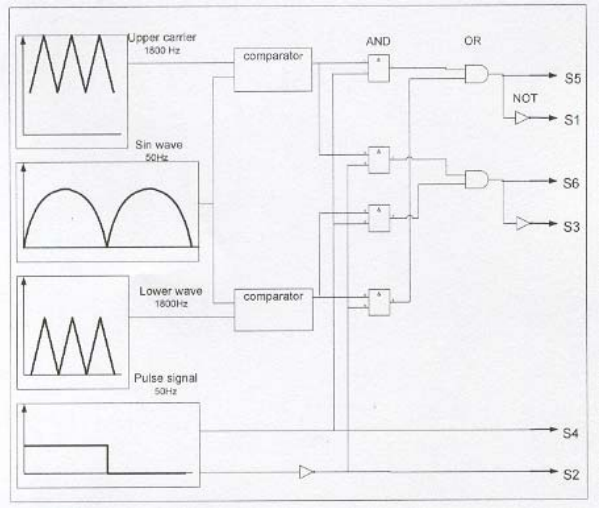

Fig.3 The block diagram of PWM generation strategy

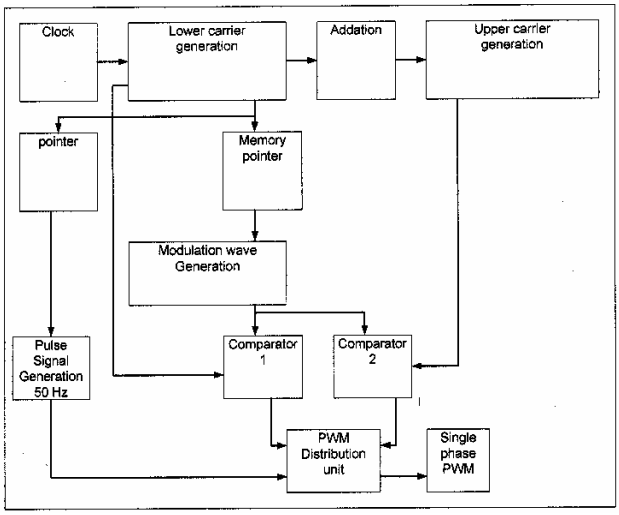

Fig.4 The block diagram of single phase PWM generator in XILINX FPGA

III. PWM GENERATION USING XILINX FPGA

The overall block diagram of the proposed multilevel single-phase inverter PWM generator is shown in Fig.3. The upper and lower carrier waves (1800 Hz) are compared with the sinusoidal wave (50 Hz). In same time a pulse signal has frequency of (50 Hz) is generated and inverted to get its inverse pulse signal.

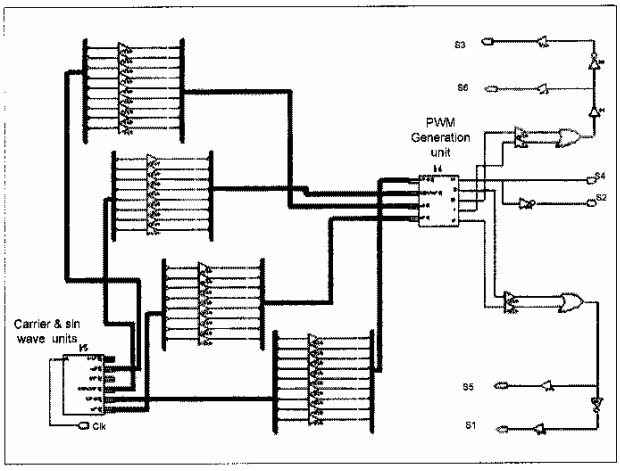

Fig.5 Single phase PWM scheme generator in XILINX FPGA

There are only three control signals S6, S5 and S2 will be needed to derive, another three S3, S1, and S4 are simply generated in method of the logical inverse of S6, S5, and S2 respectively as shown in fig.5.

1- sinusoidal wave generation

The schematic diagram of the sine wave consists of a memory Pointer unit and schematic block includes a VHDL program for sine wave data as shown in Fig.4. The VHDL program includes 19 sine wave data calculated at every 5° degrees, these data cover quarter cycle of sine wave 90° degrees.

As the modulation index depends on the modulation wave amplitude, the sine wave data can be changed to achieve the required modulation index and thus the required output voltage.

2- Carrier wave generation

An 8-bit up-down counter is clocked at 918 KHz to produce 1800Hz carrier frequency and VHDL program includes a simple addition process is also written and converted into schematic block (addition unit) to generate two types of carrier (upper and lower) waves. The main clock frequency is determined by the following formula:

$$fclk = fc\left(2^n - 1\right)^2 \tag{12}$$

Where $fclk$ is the main clock frequency, fc is the carrier (upper and lower) wave frequencies and n is the bit size of the up-down counter.

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3- Pulse signal 50Hz generation

Two inverse pulse signals have same frequency (50Hz) need to be generated; their frequencies are similar to the sinusoidal wave and the output frequency.

Pointer unit consists of an 8 bit counter, some logic gates and VHDL program developed to store data in term of condition statements are the main structure of the pulse signal (50 Hz). These two signals have two functions, first as a switching signal for switches S4 and S2, second to involve with the resultant signals produced from comparators to generate the appropriate switching signals for switches S6, S3, S5 and S1.

4- PWM distribution unit

This unit is used to distribute the PWM output pattern to the switches (S1, S2, S3, S4, S5 and S4). The distribution unit consists of a few logic gates (AND, OR, and NOT) deal with the three main signals produced from comparators and pulse signals 50 Hz generation unit to form the final PWM as shown in Fig.5.

SIMULATION AND EXPERMINTAL RESULTS

The model of the proposed multilevel PWM single phase inverter is simulated by using Matlab/Simulink® simulation tool. The PWM pattern is derived and simulated at different modulation indexes (Ma) as a control signals; the system is tested and simulated by different types of load, resistive, and mixed (resistive and inductive) loads respectively. The waveforms of voltage output and load current are obtained, experimental and simulated results are compared and show satisfactory results.

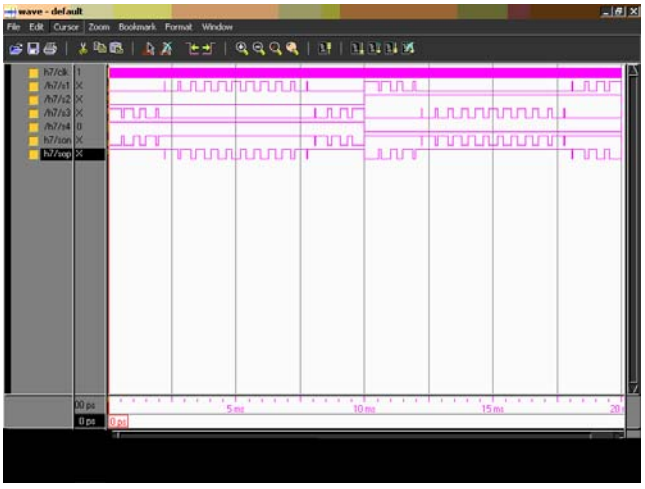


Fig.6 Multilevel PWM single phase simulation results using XILINX FPGA at Ma = 0.8.

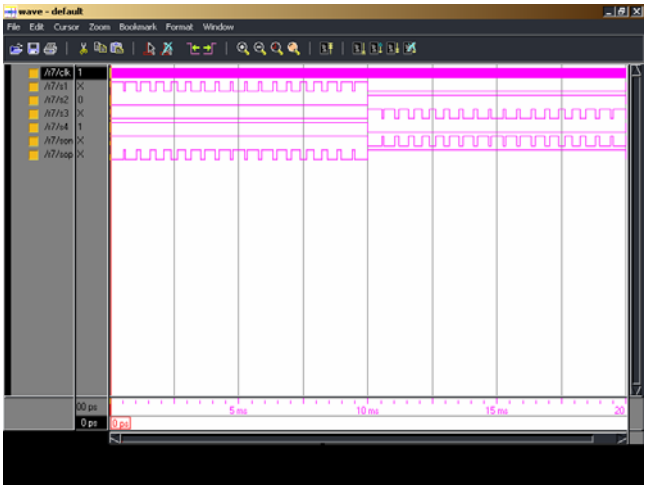
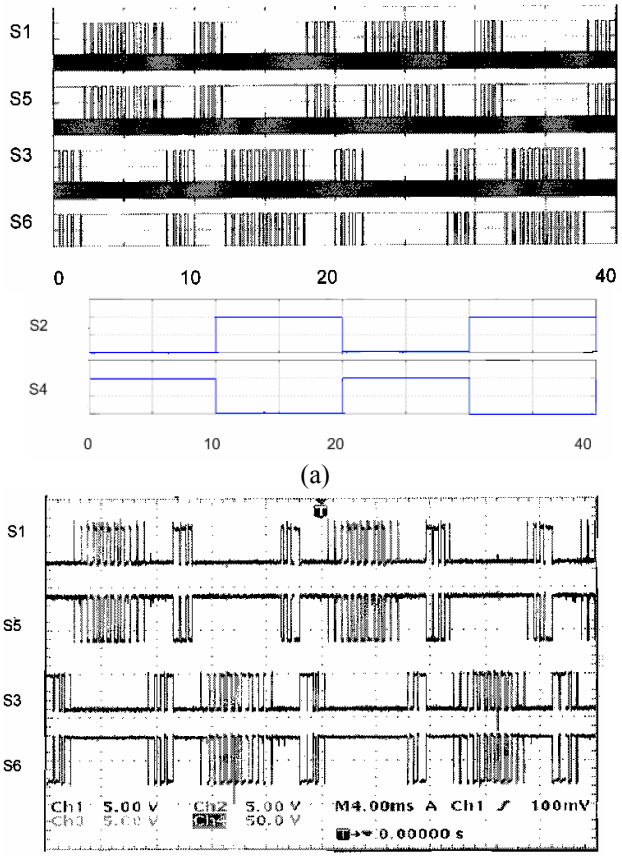


Fig.7 Multilevel PWM single phase simulation results using XILINX FPGA at Ma = 0.4.



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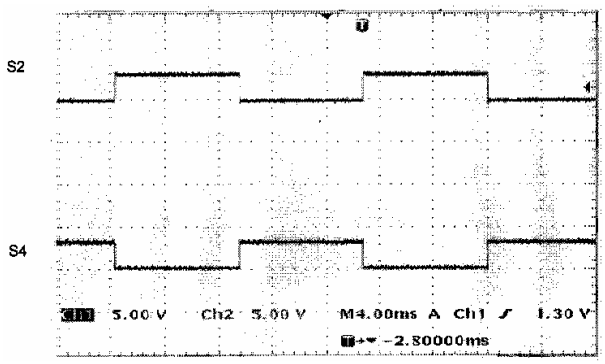
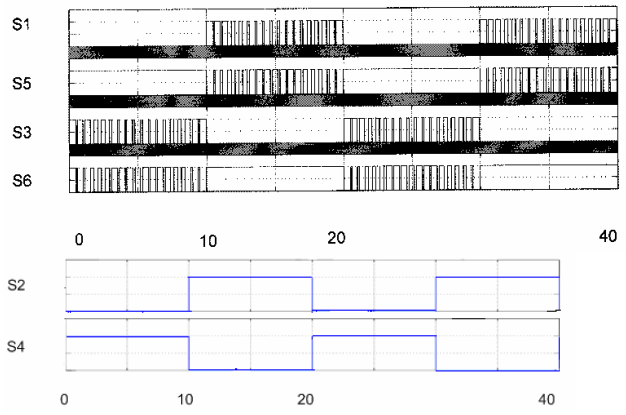
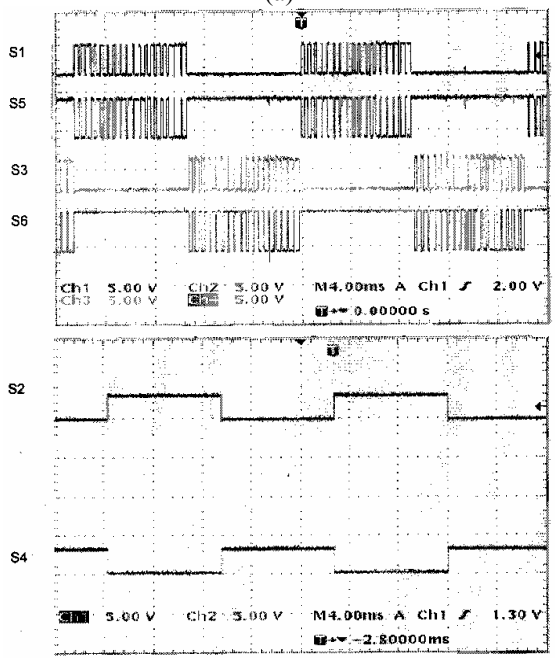


(b)

Fig.8 Multilevel single-phase PWM at Ma=0.8
(a) Simulated, (b) Experimental



(a)



(b)

Fig.9 Multilevel single-phase PWM at Ma=0.4
(a) Simulated, (b) Experimental

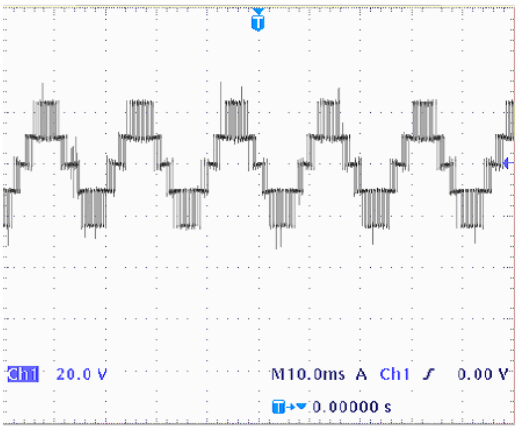


Fig.10 Unfiltered output voltage five levels at Ma=0.8

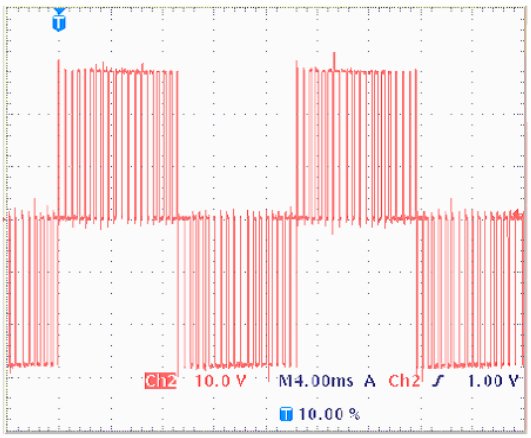
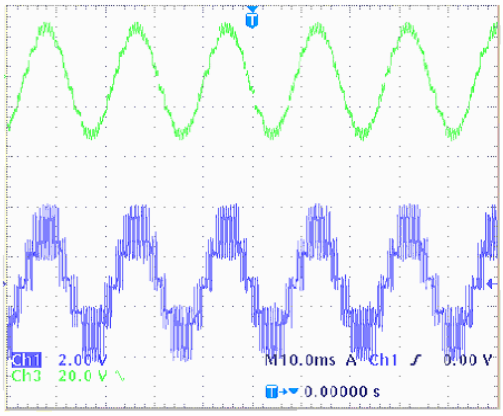


Fig.11 Unfiltered output voltage five levels at Ma=0.4



(a)

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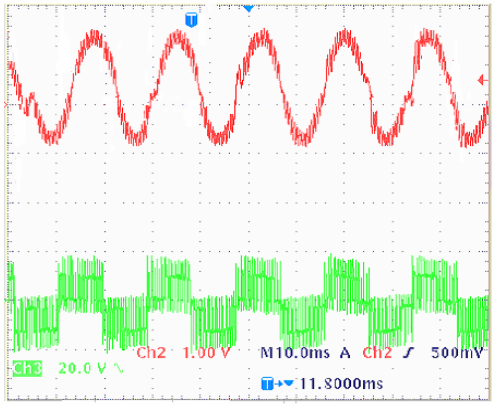

(b)

Fig.12 Ac voltage waveform before and after the filter in the proposed multilevel PWM inverter at modulation indexes (a) 0.8 and (b) 0.4.

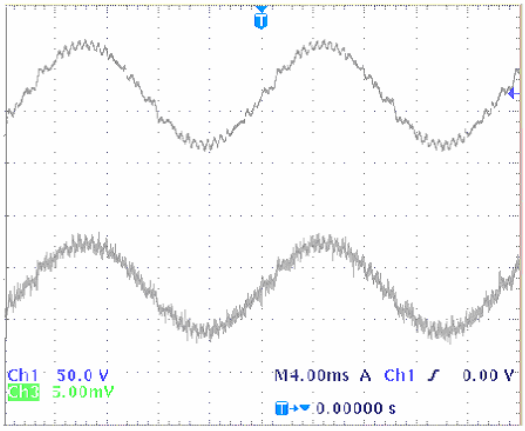

Fig.13 Ac voltage and current output waveforms for resistive load.

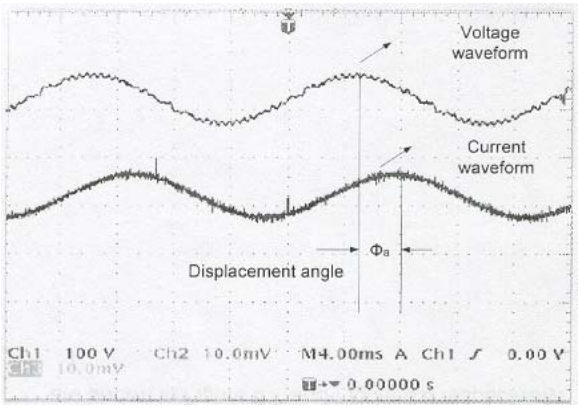

Fig.14 Ac voltage and current output waveforms for (resistive- inductive) load.

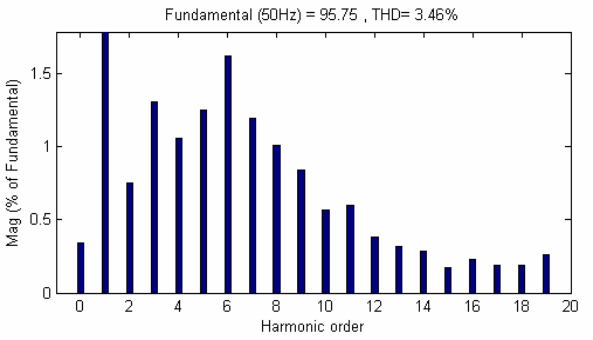

Fig.15 Ac voltage output harmonic spectral after filter

IV. CONCLUSION

The switching patterns adopted are applied at the six inverter switches to generate five or three output voltage levels at different modulation indexes. XILINX FPGA enables to make easy, fast and flexible design and implementation. The experimental and simulated results are show satisfactory results in term of total harmonic distortion and output voltage and current waveform shapes.

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