



# Three-Phase PWM Rectifier with Constant Switching Frequency

S. Begag, N. Belhaouchet and L. Rahmani

**Abstract** - In this paper, a novel adaptive hysteresis band current control technique based on predictive reasoning for three-phase PWM rectifier is presented. A simple and quick prediction of the hysteresis band is added to a phase-locked-loop control to ensure constant switching frequency and synchronization of modulation pulses independently on the system parameters. The proposed technique allows the advantages of quick response, robustness, good current tracking accuracy and minimal supply current ripples. The three-phase PWM rectifier has the characteristic of drawing nearly sinusoidal current with stable switching frequency and tight control of the position of modulation pulses. The simulation results show that the designed technique can improve three-phase PWM rectifier performance noticeably.

**Index Terms**— three-phase PWM rectifier, adaptive HBCC, switching frequency, unity power factor, interaction between the phases.

## I. INTRODUCTION

DIODE rectifiers are widely employed in industrial fields and consumer products thanks to advantages of low cost, simple structure, robustness and absence of control. However, this type of converters results in only unidirectional power flow, low input power factor, high level of harmonic input currents, malfunction of sensitive electronic equipment, increased losses and also contributing to inefficient use of electric energy. To maintain supply quality at acceptable levels, various standards and guidelines (i.e. IEEE 519 and IEC 61000-3) specify limits of current harmonic content for certain types of applications. Recently, many promising power factor correction (PFC) techniques [1-5] have been proposed for rectifiers. Apart from application of active and passive filters, the best solution is in using pulse width modulated (PWM) rectifiers. Research interest in three-phase PWM rectifiers has grown rapidly over the last few years due to some of their important advantages, such as power regeneration capabilities, control of dc-bus voltage over a wide range, and low harmonic distortion of input currents. Since the converter has abilities to control the input currents in sinusoidal waveforms, unity power factor operation can be easily performed by regulating the currents in phase with the power-source voltages.

Various control techniques have been proposed in recent works on this type of PWM rectifier [2-4]. It is well known that in order to obtain better ac supply power quality and

high performance of these converters, it is preferable to directly control the magnitude and phase angle of three-phase supply currents. Among the current control techniques, hysteresis band current control (HBCC) is probably the simplest technique used to forcing the supply current to follow the reference current, because of its ease of implementation, fast current control response, and inherent peak current limiting capability [6,7]. However, the basic conventional HBCC with fixed bandwidth is affected by the drawbacks of a variable switching frequency, a heavy interaction between the phases when the ground is insulated to the capacitors midpoint and an irregularity of the modulation pulses position. These drawbacks provide high current ripples, acoustic noise and difficulty in designing of input filter [5-7].

To overcome these undesirable drawbacks, this paper presents a novel adaptive HBCC technique based on predictive reasoning which demonstrates a viable solution to obtain high performance control of three-phase PWM rectifier in case of the insulating of ground to capacitors midpoint. The analysis of the conventional fixed HBCC technique for three-phase PWM rectifier is described. Next, the novel adaptive HBCC is developed. Then, simulation results obtained by MATLAB/SIMULINK are presented followed by the conclusion.

## II. OPERATION PRINCIPLE OF CONVENTIONAL HBCC FOR THREE-PHASE PWM RECTIFIER

Fig 1 shows the circuit configuration of three-phase PWM rectifier. This latter is composed of a three-phase converter with six IGBT or Mosfet elements, three inductors connected between the ac source and the ac side of converter and two identical series-connected capacitors are used on the dc side.

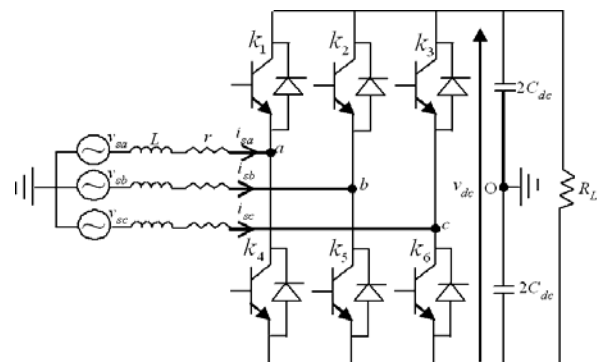


Fig.1. Three-phase PWM rectifier configuration.

The control block diagram of the three-phase PWM rectifier is shown in Fig 2 and it employs a very simple control structure, where a proportional-integral PI controller is used to regulate the dc output voltage and provide the

S. Begag, Department of Electrotechnic, laboratory of Automatic, Ferhat Abbas University-Setif, Algeria (e-mail: begag\_bs@yahoo.fr).

N. Belhaouchet, Department of Electrotechnic, laboratory of Automatic, Ferhat Abbas University-Setif, Algeria (nouri\_belhaouchet@yahoo.fr).

L. Rahmani, Department of Electrotechnic, laboratory of Automatic, Ferhat Abbas University-Setif, Algeria.

magnitude value of the sinusoidal reference currents. The input of this controller is the error between the square of the reference dc voltage  $(v_{dc}^*)^2$  and the dc bus capacitors voltage  $v_{dc}^2$  to have a linear adjustment of the output dc average power, the output is considered as the magnitude of the desired supply currents  $I_{sm}$  and the reference currents are estimated by multiplying this magnitude with the unit sine vectors in phase with the ac main source voltages provided by the phase-locked-loop (PLL). After having found the reference currents, the supply current is sensed and compared with the sinusoidal reference current for each phase. The comparison result is introduced in hysteresis comparator to generate the PWM signal of the rectifier.

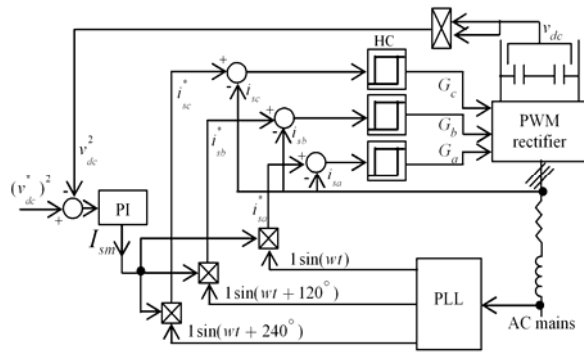


Fig.2. Control block diagram of three-phase PWM rectifier.

The basic structure of three-phase PWM rectifier is shown in Fig. 1. The main objective of this structure is to generate three-phase sinusoidal input currents in phase with the input phase voltages. The analysis of HBCC technique will be considered for the case of midpoint "O" of dc bus capacitors connected to ground as well as when that point is floating.

### II.1. Capacitors midpoint connected to ground

When the midpoint "O" of dc capacitors is connected to ground, the PWM rectifier is symmetrical, and each phase can be regarded as independent. Referring to the topology, the relationship for phase a voltage and current can be formulated as:

$$v_a + L \frac{di_{sa}}{dt} + ri_{sa} = v_{sa} \quad (1)$$

Where  $v_a$  is the voltage of point a referred to the ground.

In practice, it can only take the values of  $\pm V_{dc}/2$  depending on the state of the phase leg switches. However, if the ideal reference current  $i_{sa}^*$  is assumed to flow through phase a of rectifier, then a fictitious reference voltage  $v_a^*$  would exist, given by:

$$v_a^* + L \frac{di_{sa}^*}{dt} + ri_{sa}^* = v_{sa} \quad (2)$$

Now, for HBCC, the difference between the reference and the actual current can be defined as:

$$\delta_a = i_{sa}^* - i_{sa} \quad (3)$$

Subtracting (1) from (2) and substituting from (3), gives:

$$L \frac{d\delta_a}{dt} + r\delta_a = v_a - v_a^* \quad (4)$$

For a reasonably high switching frequency, the effect of the input inductor resistance  $r$  can be neglected, so that (4) becomes:

$$L \frac{d\delta_a}{dt} = v_a - v_a^* \quad (5)$$

The operation of HBCC technique over one switching cycle is shown in Fig. 3.

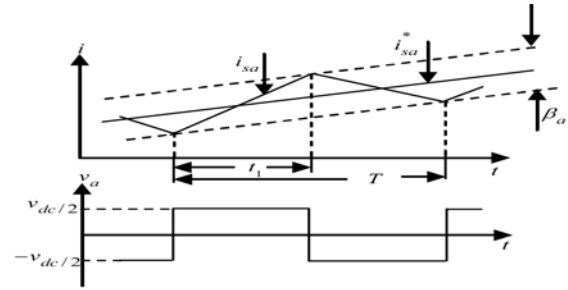


Fig.3. Hysteresis-band current and phase leg voltage waveforms.

From (5), this can be expressed mathematically as:

For the interval  $0 < t < t_1$

$$\begin{aligned} \frac{v_{dc}}{2} - v_a^* &= L \frac{\Delta\delta_a}{\Delta t} = L \left( \frac{\delta_a(t_1) - \delta_a(0)}{t_1 - 0} \right) \\ &= L \left( \frac{\beta_a/2 + \beta_a/2}{t_1} \right) \end{aligned} \quad (6)$$

For the interval  $t_1 < t < T$

$$\begin{aligned} -\frac{v_{dc}}{2} - v_a^* &= L \frac{\Delta\delta_a}{\Delta t} = L \left( \frac{\delta_a(T) - \delta_a(t_1)}{T - t_1} \right) \\ &= L \left( \frac{-\beta_a/2 - \beta_a/2}{T - t_1} \right) \end{aligned} \quad (7)$$

From (6) and (7), the switching period expression is given by:

$$T = \frac{LV_{dc}\beta_a}{\left(\frac{v_{dc}}{2}\right)^2 - (v_a^*)^2} \quad (8)$$

$$T = \frac{4L\beta_a}{v_{dc}(1 - v_{na}^2)} \quad (9)$$

Where:  $v_{na} = v_a^*/(v_{dc}/2)$  is the normalized voltage.

From (9), we note that if the bandwidth  $\beta_a$  is constant, then the switching period  $T$  is variable.

## II.2. Capacitors midpoint without connection to the ground

Since the dc bus capacitors midpoint "O" is normally floating to avoid the third current harmonic in the neutral point, the previous analysis now will be extended to allow for floating point "O".

When point "O" is floating, the relationship for phase a voltage and current can be reformulated as:

$$v_a + v_o + L \frac{di_{sa}}{dt} + ri_{sa} = v_{sa} \quad (10)$$

Where  $v_o$  is the voltage of point "O" referred to the ground; its expression is given as:

$$v_o = \frac{(v_a + v_b + v_c)}{3} \quad (11)$$

Subtracting (10) from (2) gives:

$$L \frac{d\delta_a}{dt} + r\delta_a = v_a - v_a^* + v_o \quad (12)$$

(12) Shows that, due to the action of voltage  $v_o$ , each phase current error is affected by the commutations in the other phases. This interference causes severe irregularities in the ordinary hysteresis operation.

From (3), the current error  $i_{sa}^* - i_{sa}$  can be decoupled into two parts as:

$$\delta_a = i_{sa}^* - i_{sa} = \delta_a' + \delta_a'' \quad (13)$$

where:  $\delta_a'$ : non interacting error and  $\delta_a''$ : interacting error

The equation of interacting error is:

$$L \frac{d\delta_a''}{dt} + r\delta_a'' = v_o \quad (14)$$

An interference-free modulation can be obtained if the hysteresis control is performed on the non interacting error as:

$$L \frac{d\delta_a'}{dt} + r\delta_a' = v_a - v_a^* \quad (15)$$

(15) shows that  $\delta_a'$  only depends on the corresponding voltage  $v_a$ , similar to (5) if the effect of the input inductor resistance  $r$  is neglected. Hence error  $\delta_a'$  can be treated in the same way as the error  $\delta_a$  in the case of capacitive midpoint "O" connected to ground. We can see that the three-phase interacting errors are same ( $\delta_a'' = \delta_b'' = \delta_c''$ ).

## III. DEVELOPMENT OF PREDICTIVE ADAPTIVE HBCC

### III.1. Constant switching frequency control

To obtain a constant switching frequency ( $1/T_d$ ), the hysteresis band  $\beta_a$  has to be dynamically modified according to this equation:

$$\beta_a = \frac{v_{dc} T_d}{4L} (1 - v_{na}^2) \quad (16)$$

The controller maintains its analog structure, but an

adaptive bandwidth digital control is added which ensures constant switching frequency. Fig. 4 shows the adaptation of the hysteresis band for two consecutive modulation periods [5, 8, 9].

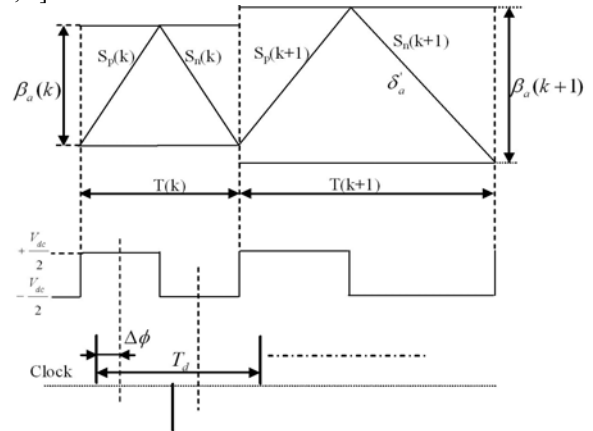


Fig.4. Bandwidth control algorithm.

From Fig.4, we deduce the following equations:

$$\begin{cases} \beta_a = S_p T_{on} = S_n T_{off} \\ T = T_{on} + T_{off} \end{cases} \quad (17)$$

Where  $s_p$  and  $s_n$  are the positive and negative slopes of the non interacting error  $\delta_a'$  in modulation period.

For a switching period corresponding to  $k$ , we have:

$$T(k) = \beta_a(k) \cdot \frac{S_p(k) + S_n(k)}{S_p(k) \cdot S_n(k)} \quad (18)$$

For a switching period corresponding to  $k+1$ , the equation (18) is written:

$$T(k+1) = \beta_a(k+1) \cdot \frac{S_p(k+1) + S_n(k+1)}{S_p(k+1) \cdot S_n(k+1)} \quad (19)$$

For two consecutive switching periods, we have the following simplifying:

$$\begin{aligned} S_p(k) &= S_p(k+1) \\ S_n(k) &= S_n(k+1) \end{aligned} \quad (20)$$

From (18), (19) and (20), we can derive the control equation:

$$\beta_a(k+1) = \beta_a(k) \cdot \frac{T(k+1)}{T(k)} \quad (21)$$

The principle of control given by equation (21) is to keep the switching period constant, where  $T(k+1)$  is the desired switching period which we want to impose and  $T(k)$  is the measured one, i.e. to define the switching period  $T(k+1)$  we predict at time  $k$  the bandwidth  $\beta_a(k+1)$  and hence this reasoning is intended to evaluate the proper bandwidth to achieve the error between the real switching period and the desired switching period equal to zero. This reasoning leads to an algorithm which is equivalent to a first order dead-beat control of the switching period.

The control algorithm is very simple and it is able to ensure a good switching frequency regulation with any knowledge on the system parameters, but it cannot control

the position of modulation pulses. This means that the distribution of the modulation pulses inside the modulation period is random.

### III.2. Switching pulses regulation

Now we make an additional improvement by introducing a synchronization of modulation pulses. This is based on adding a modification to equation (21), where the phase error between an external clock and the control signal contributes to ensure a good regulation of modulation pulses position. The solution is to implement the PLL, generally, this is the effective solution to synchronize two signals if the stability conditions are respected [10, 11].

The PLL is a device which causes one signal to track another one, it keeps the output signal synchronized with a reference input signal in frequency as well as in phase. More precisely, the PLL is simply a servo system, which controls the phase of its output signal in such a way that the phase error between output phase and reference phase reduces to a minimum. The basic fundamental block diagram of PLL consists of a phase detector, a loop filter and a voltage controlled oscillator (VCO). In this case, the PLL block scheme used to modify the equation (21) is shown in Fig. 5 and it is composed of a phase detector to detect the phase error between the reference clock with frequency  $f_d$  and the output switching signal with frequency  $f$ , a proportional-integral (PI) filter and employs the hysteresis comparator (HC) as VCO.

When locked to a suitable clock signal, the PLL not only ensures constant modulation frequency, but also minimizes the phase displacement  $\Delta\phi$  between the output voltage pulses and the external clock. In three-phase insulated ground systems, the optimal reduction of the current ripple corresponds to center of the modulation pulses [12, 13]. In this case, the phase error  $\Delta\phi$  is defined as the time between the center of pulse modulation and the reference clock.

The PLL loop gives the phase error and hence gives the necessary compensating bandwidth to ensure a constant switching frequency and effective lock of modulation pulses to clock as it is well presented in Fig. 5.

Finally, from Fig. 5, it can be derived:

$$\beta_a = \beta_{pa} + \beta_{dba} \quad (22)$$

$$\beta_{pa} = \left( \frac{K_i + sK_p}{s} \right) \cdot \Delta\phi \quad (23)$$

Where  $\left( \frac{K_i + sK_p}{s} \right)$  is the transfer function of PI filter.

Now, the control equation (21) becomes:

$$\beta_{dba}(k+1) = \left( 1 + \frac{K_i + sK_p}{s} \cdot \frac{\Delta\phi}{T_d} \right) \cdot \frac{T_d}{T} \cdot \beta_a(k) \quad (24)$$

(24) shows the modified dead-beat control law with  $\beta_{pa}$  is the compensating bandwidth given by PLL loop,  $\beta_{dba}$  is the bandwidth given by dead-beat control and  $\beta_a$  is the total bandwidth obtained after correction. Similar expressions of hysteresis bands can be written for the other phases b and c.

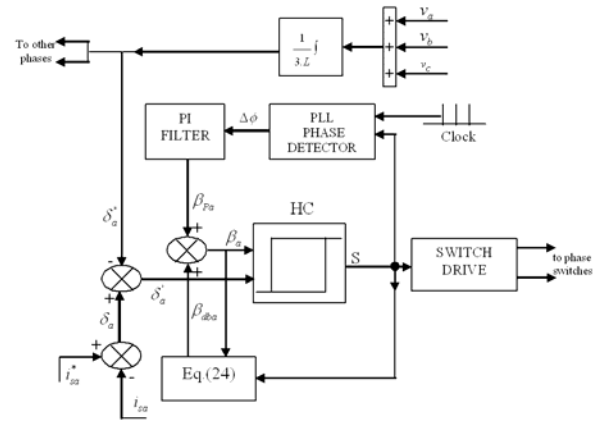


Fig. 5. Block scheme of the predictive adaptive HBCC for phase a.

## IV. SIMULATION RESULTS AND DISCUSSIONS

During this simulation, we used the parameters which are indicated in table 1.

TABLE I  
Design specifications and circuit parameters

Desired switching frequency	5 KHz
Source voltage frequency	50 Hz
ac supply voltage peak	120 V
dc-bus voltage	300V
Input resistance r	0.2 $\Omega$
Input inductance L	11.5 mH
Load resistance R <sub>L</sub>	100 $\Omega$
dc-bus capacitor C <sub>dc</sub>	2000 $\mu$ F

To verify the performances of the proposed predictive adaptive HBCC compared to the conventional fixed HBCC, the simulation results are shown in fig. 6 through fig. 13.

Fig. 6 shows the supply current and current error waveforms of a-phase for conventional fixed HBCC, where the fixed band was set to achieve a maximum switching frequency of 5 KHz when there is no interaction between the phases. Due to the interaction of three-phase current controllers, the supply current instantaneous error can go beyond hysteresis band  $\beta_a$  and reach up to  $2\beta_a$ , this shows that the supply current has high ripples. The supply current and current error waveforms for adaptive HBCC are shown in Fig. 7. In this case the supply current ripples are minimized. The interacting error and non-interacting error waveforms for adaptive HBCC are shown in Fig. 8.

The supply current FFT for conventional HBCC and adaptive HBCC are shown in Fig. 9 and Fig. 10 respectively. In conventional HBCC, the supply current harmonics are widely distributed from hundreds of Hertz to several kiloHertz frequency and the THD (total harmonic distortion) is higher (10.52%). However, for adaptive HBCC, a switching frequency is held in 5 kHz, thus the supply current harmonics are concentrated around 5 kHz frequency and the THD is reduced to 3.78%. This provides predictability of the converter input current harmonics, avoids resonance problem and makes the filter design task easier.

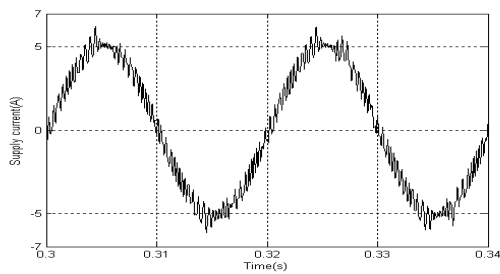


Fig.6. Supply current and current error for conventional HBCC.

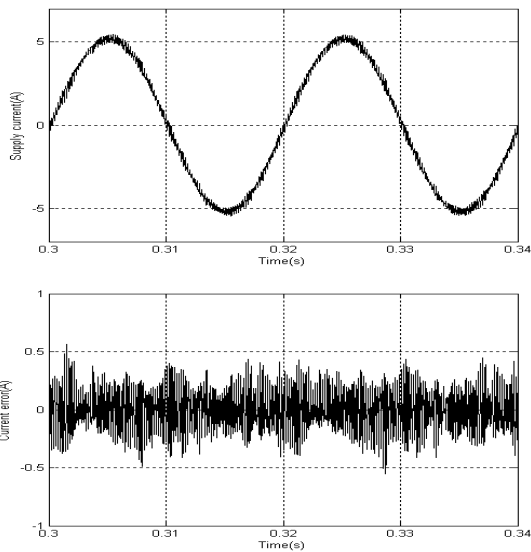


Fig.7. Supply current and current error for proposed adaptive HBCC.

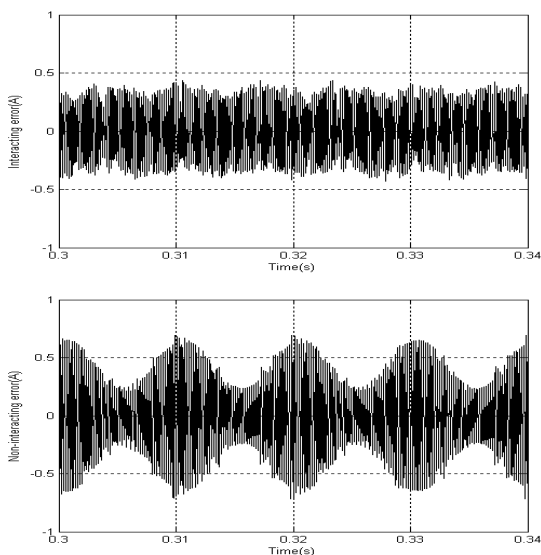


Fig. 8. Interacting error and non-interacting error for adaptive HBCC.

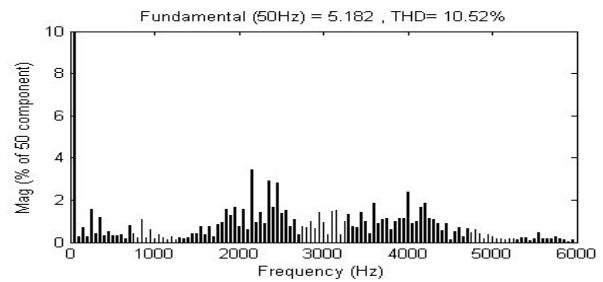


Fig. 9. Supply current FFT for conventional HBCC.

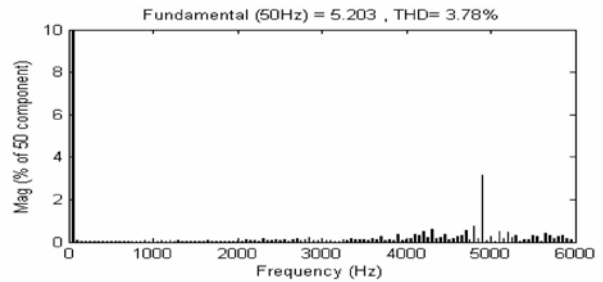


Fig. 10. Supply current FFT for adaptive HBCC.

The instantaneous switching frequencies for conventional HBCC and adaptive HBCC are shown in Fig. 11 and Fig. 12 respectively. In conventional fixed HBCC, the switching frequency varies widely from hundreds of Hertz to several KiloHertz frequency. In adaptive HBCC, the instantaneous switching frequency is stable with little deviation around 5 KHz.

Fig. 13 shows the phase error waveform for the proposed dead-beat algorithm, the phase error is well controlled around zero and it is kept within  $50^\circ$  with a symmetrical waveform. So, we can see that the modulation pulses are well synchronized.

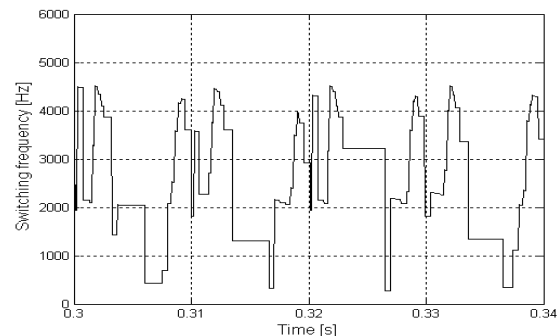


Fig. 11. PWM switching frequency for conventional HBCC.

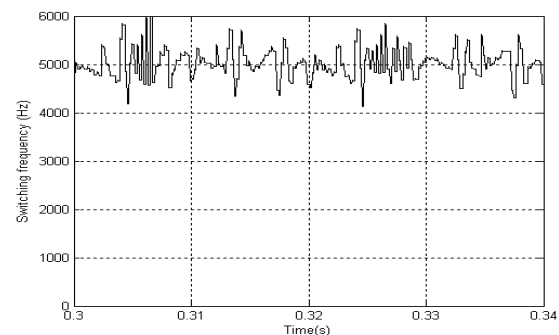


Fig.12. PWM switching frequency for adaptive HBCC.

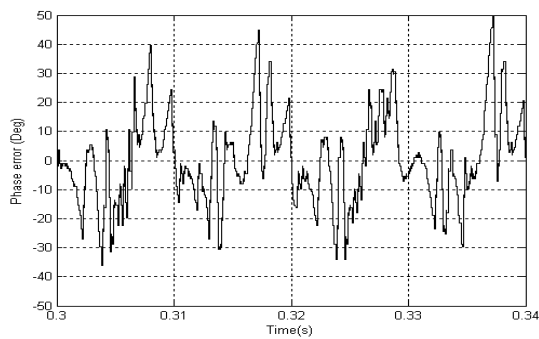


Fig. 13. Phase error waveform for adaptive HBCC.

## V. CONCLUSION

This paper has presented a considerable improvement which offers all the advantages of the hysteresis technique for three-phase PWM rectifier, where a novel adaptive HBCC based on predictive reasoning has been developed which ensures a good regulation of switching frequency and a tight control of the position of modulation pulses. The technique performs by creating an adaptive hysteresis band envelope, and then compensating for the interaction between the phases that occurs when the midpoint of dc bus capacitors is floating. The three-phase PWM rectifier shows excellent features such as unity power factor, high reliability and simple robust control.

## REFERENCES

- [1]. Maswood A.I, Fangrui Liu "A novel variable hysteresis band current control of three-phase three-level rectifier with constant switching frequency", IEEE, Power Engineering Society General Meeting, Vol. 1, Issue , 12-16 June 2005, pp. 23- 27.
- [2]. P. Antoniewicz and M.P. Ka Zmierkowski "Predictive direct power control of three-phase boost rectifier", Bull. Pol. Ac. Tech, Vol. 54, No 3, 2006, pp. 287-292.
- [3]. A. Bouafia and F. Krim "A Fuzzy-Logic-Based Controller for Three-Phase PWM Rectifier With Unity Power Factor Operation", ESR-Groups, Journal of Electrical Systems, Vol. 4, Issue 1, 2008, pp. 36-50.
- [4]. Abdelouahab Bouafia , Fateh Krim, Jean-Paul Gaubert" Design and implementation of high performance direct power control of three-phase PWM rectifier, via fuzzy and PI controller for output voltage regulation", Elsevier , Energy Conversion and Management 50 2009, pp. 6–13.
- [5]. N. Belhaouchet, L. Rahmani and S. Begag "Three-Phase Shunt Active Power Filter with High-Performance Operation", Praise Worthy Prize, International Review of Automatic Control (IREACO), Vol. 1, N° 3, September 2008, pp. 294-302.
- [6]. Q. Yao, D.G. Holmes. A Simple "Novel Method for Variable-Hysteresis-Band Current Control of A Three Phase Inverter with Constant Switching Frequency", IEEE, IAS 93 Ann.Meet Conf Rec, Toronto, October 1993, pp. 1122-1129.
- [7]. M.Kale and E.Ozdenir "A Novel Adaptive Hysteresis Band Current Controller for Shunt Active Power Filter", IEEE, CCA, Istanbul, Turkey, Vol. 2, 23-25, June 2003, pp. 1118-1123.
- [8]. L. Sonaglioni. Predictive Digital Hysteresis Current Control. IEEE, IAC, Orlando, FL, USA, Vol.3, 8-12 Oct 1995, pp. 1879-1886.
- [9]. N. Belhaouchet, L. Rahmani, S. Begag, H. Hamla "Development of Digital Hysteresis Current Control with PLL Loop Gain Compensation Strategy for PWM Inverters with Constant Switching Frequency", ESR-Groups, Journal of Electrical Systems, Vol. 4, Issue 1, 2008, pp. 77-90.
- [10]. L. Malesani, P. Mattavelli, P. Tomasin "High-Performance Hysteresis Modulation Technique for Active Filters", IEEE, APEC, San Jose, CA USA. Vol. 2, 3-7 March 1996, pp. 939-945.
- [11]. L. Malesani, P. Mattavelli, P. Tomasin "Improved Constant Frequency Hysteresis Current Control of VSI Inverters with Simple Feedforward Band with Prediction", IEEE Trans Ind Applicat. Vol.33, n°5, Septemer/October 1997, pp. 1194-1202.
- [12]. D. Wuest, F. Jenni "Space vector based current control schemes for voltage source inverters", IEEE, PESC'93, Conf. Rec, Seattle, 1993, pp. 986-992.
- [13]. H.W. Van der Broeck et al "Analysis and realization of a pulse width modulator based on voltage space vectors", IEEE Trans. Ind. Appl, Vol. 24, n°1, 1988, pp. 142-150.