**Cuk-Based Converter Concepts**
*Part 3: SEPIC Converter Design*
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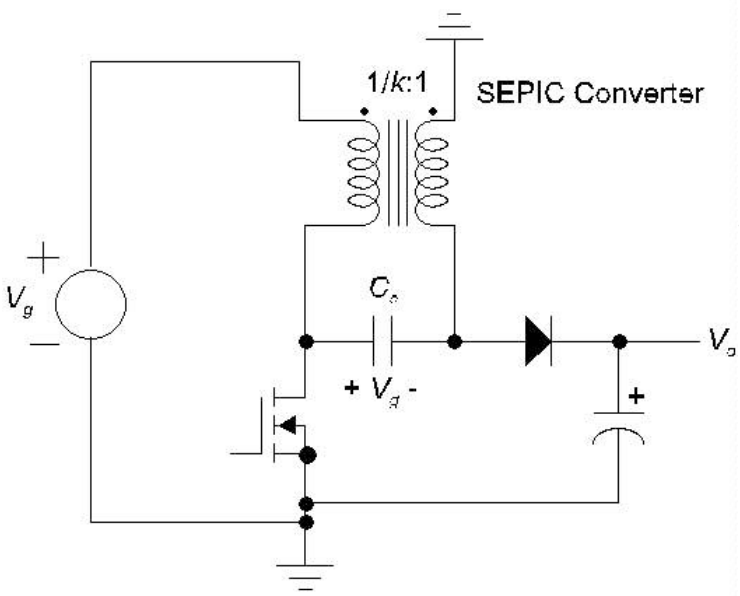
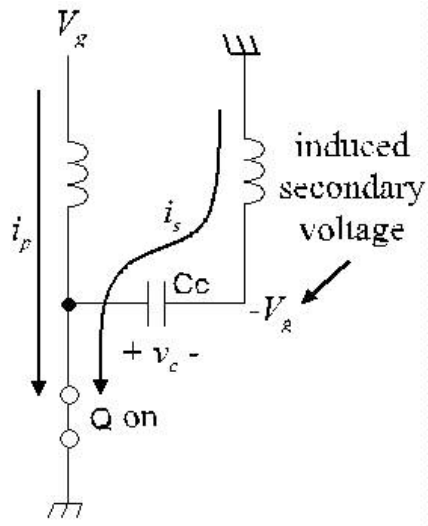
In this part, the engineering formulas needed to design a SEPIC converter are worked out and waveforms determined. In the next part, actual circuit behavior of a prototype converter is observed that can be constructed from commonly available components found in most electronics laboratories.

The basic SEPIC converter topology is repeated below:

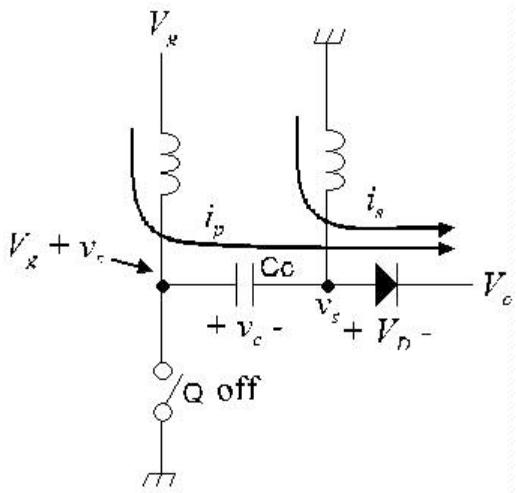



The causal relationships, captured in behavior, are explained as follows: we assume that coupling capacitor, $C_c$, is large enough in value that $\Delta V_c$ is approximately zero. $C_c$ then appears to be a voltage source with an average voltage of $V_g$. (The variation in $v_c$ is important for ripple steering, but that is a refinement of basic behavior.) Initially, $C_c$ charges to $V_g$.

During the on-time of MOSFET Q, which is $D{\cdot}T_s$, $v_Q = 0$, and the induced secondary voltage, $v_s = -v_p$. The primary current, $i_p$, flows through the conducting Q, as does the secondary current, through $C_c$. $C_c$ discharges through leakage inductance $L_l$ toward $v_c = V_g$, as shown below. Magnetizing (mutual) current is $i_p + i_s$, and $i_s$ decreases, opposed by $v_c$.



Then Q turns off for $D' \cdot T_s$. Primary current diverts from Q to $C_c$ and the diode, and secondary current flows also through the diode, as shown below.




The secondary voltage, on the bottom of the winding with respect to ground on top, is:

$$V_s = V_o + V_D$$

The secondary winding is clamped to $v_s$ by the output and diode, and it induces $v_s$ into the primary winding where it adds to $V_g$. $C_c$ charges through the primary-side inductance, $L_p$, to $v_c > V_g$. The magnetizing current also flows to the output. That is the basic behavior of the SEPIC converter.

The design equations will now be derived, or at least presented, and their application discussed. The steady-state voltage and current gain equations are derived by assuming flux balance: the current in the transductor at the beginning of the switching cycle equals that at the end, and no net flux change occurs. This can be expressed in terms of the primary and secondary flux values as:

$$\Delta\lambda_p = -\Delta\lambda_s = 0$$

Averages of quantities are denoted as $\bar{x}$, where $x$ is a voltage or current. The primary-side average voltage over $T_s$ is:

$$\bar{v}_p = V_g \cdot D - V_s \cdot (1 - D) = 0$$

For the secondary winding voltage:

$$\bar{v}_s = \bar{v}_c \cdot D - V_s \cdot (1 - D) = 0$$

Solving these equations for the steady-state voltage gain:

$$M = \frac{\bar{v}_s}{\bar{v}_p} = \frac{D}{1 - D} = \frac{D}{D'}\ ,\ \bar{v}_c = V_g$$

This result could also be derived by beginning with the change in transductor flux for both primary and secondary windings:

$$\Delta\lambda_p = \Delta i_p \cdot L_p = V_g \cdot D \cdot T_s = 0$$

$$-\Delta\lambda_s = -\Delta i_s \cdot L_s = -V_s \cdot D' \cdot T_s = 0$$

These equations are then solved for the voltage gain.

Not only must flux balance occur for steady-state behavior but $C_c$ charge balance must also:

$$\Delta q_c = \Delta(\bar{i}_c \cdot t) = 0 \Rightarrow \bar{i}_c = \bar{i}_p \cdot (1-D) \cdot T_s - \bar{i}_s \cdot D \cdot T_s = 0$$

Then:

$$\bar{i}_p \cdot (1-D) = \bar{i}_s \cdot D$$

and:

$$\frac{\bar{i}_p}{\bar{i}_s} = \frac{D}{1-D} = \frac{D}{D'}$$

Equating this to the voltage gain above:

$$\frac{\bar{i}_p}{\bar{i}_s} = \frac{\bar{v}_s}{\bar{v}_p} \Rightarrow \bar{v}_p \cdot \bar{i}_p = \bar{v}_s \cdot \bar{i}_s$$

The primary and secondary average power over the switching cycle is equal, as it must be; the transductor is not a dissipative circuit element. (Note: generally, when average voltage and current are multiplied, the result is *not* average power. This is an approximation based on the assumption that the averages over $T_s$ can be considered nearly-constant values. Then average and rms values are approximately the same.)

Using the charge balance equation with the $v \cdot i$ relationship for $C_c$, the voltage ripple on $C_c$ can be derived:

$$\Delta v_c = \frac{\Delta q_c}{C_c} = \frac{\bar{i}_p}{C_c} \cdot (1-D) \cdot T_s = \frac{\bar{i}_s}{C_c} \cdot D \cdot T_s$$

The cycle-averaged switch currents are found by applying KCL to transistor and diode:

$$\bar{i}_o = (\bar{i}_p + \bar{i}_s) \cdot (1-D) = \left(\frac{D}{1-D} + 1\right) \cdot \bar{i}_s \cdot (1-D)$$

This reduces to:

$$\bar{i}_o = \bar{i}_s$$

In the primary circuit:

$$\bar{i}_Q = (\bar{i}_p + \bar{i}_s) \cdot D = \left(1 + \frac{1-D}{D}\right) \cdot \bar{i}_p \cdot D$$

This also reduces simply to:

$$\bar{i}_Q = \bar{i}_p$$

It also follows immediately from the circuit that $i_p = i_g$ and that:

$$\bar{i}_p = \bar{i}_g$$

where, all averages are taken over $T_s$ in the steady state.

The following equivalent circuits for the on and off states of Q, with a turns ratio of $n = 1$, are drawn from the circuit with switches in the indicated states. (For $n \neq 1$, refer the impedance of elements from the secondary side of the transductor to the primary side by the referral ratio, $n^2$.) These circuits let us analyze the effects of the transductor inductances. The resonance of the Cuk-derived converter topologies (including the SEPIC) during the on-time can be seen as $C_c$ resonating with the secondary inductance, $L_{s0}$. The primary winding is shorted (through $V_g$) during the on-time. The secondary inductance:

$$L_{s0} = L_{ls} + \frac{M}{n} \| \frac{L_{lp}}{n^2} = L_{ls} + \frac{L_{mp} \| L_{lp}}{n^2}$$

where, $L_{mp}$ is the *magnetizing* or *mutual inductance* referred to the primary side.

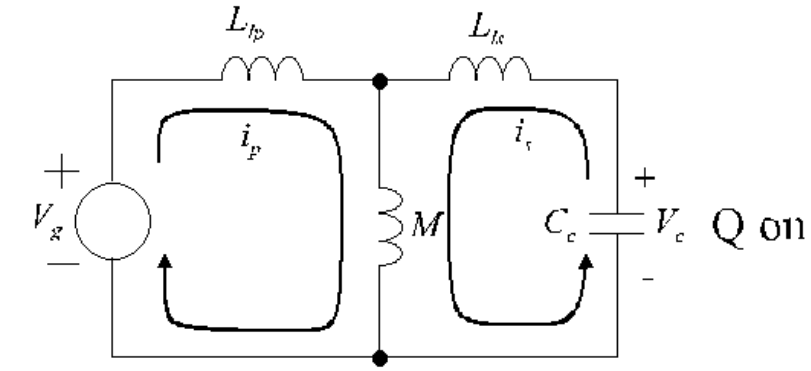
The mutual inductance, $M$, is neither on the primary nor secondary side of the transductor, as shown, but is in between (or is "field-referred") in that:

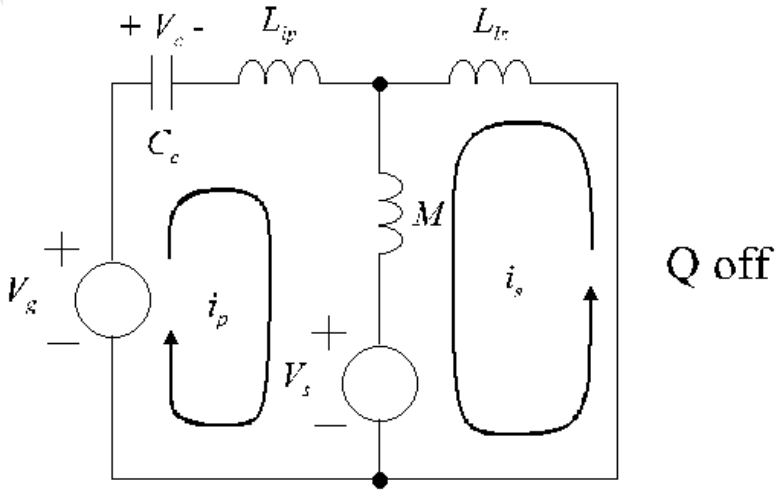
$$M = \frac{L_{mp}}{n} = n \cdot L_{ms} = N_p \cdot N_s \cdot \mathsf{L}$$

L is the field-referred (or per-turn$^2$) inductance of the transductor (usually given in magnetic core catalogs as $A_L$) and $N_x$ is the number of winding turns on side $x$. Then the on-time resonant frequency is:

$$f_r(\text{on}) = \frac{1}{2\pi \cdot \sqrt{L_{s0} \cdot C_c}}$$

During the off-time, $C_c$ resonates with $L_{p0}$ instead of $L_{s0}$.



In both cases, only parasitic winding resistance and $C_c$ series resistance damp these resonances. A frequently used method of adding damping is to shunt $C_c$ with a series RC having a larger $C$ value than $C_c$. The resonance can also be removed in frequency from $f_s$ by making:

$$C_c >> \frac{1}{(2\pi \cdot f_s)^2 \cdot L_{p0}}$$

thus making $f_r << f_s$.

The oscillation of the resonance will then be so slow that a negligible change in resonant voltage or current will occur during the switching cycle. In a later part of this series, an incremental circuit model will be derived that can be used to design the SEPIC control loop.

The transductor inductance value of $L_p$ depends on how much primary-referred magnetizing current, $i_m$, with a peak-to-peak value of $\Delta i_p$, is tolerable. From the *v-i* relationship for inductors:

$$L_p = \frac{V_g \cdot D \cdot T_s}{\Delta i_p} = \frac{V_s}{M+1} \cdot \frac{1}{f_s \cdot \Delta i_p}$$

Then $f_s$ and $\Delta i_p$ are design parameters that affect the value (and hence size and cost) of $L_p$. While transductor bootstrapping diverts current ripple from the input, it still flows in the secondary winding, $C_c$, and transistor.

The average current through $C_c$ must be zero for charge balance, though the rms value is approximately:

$$\tilde{i}_c = \sqrt{D \cdot \bar{i}_s^2 + D' \cdot \bar{i}_p^2} \ , \ i_m = 0$$

The approximation is the small-ripple assumption, that $L_p$ is large enough to make the magnetizing current negligible. Applying the expression for $M$, the $C_c$ rms current can be written in alternative ways:

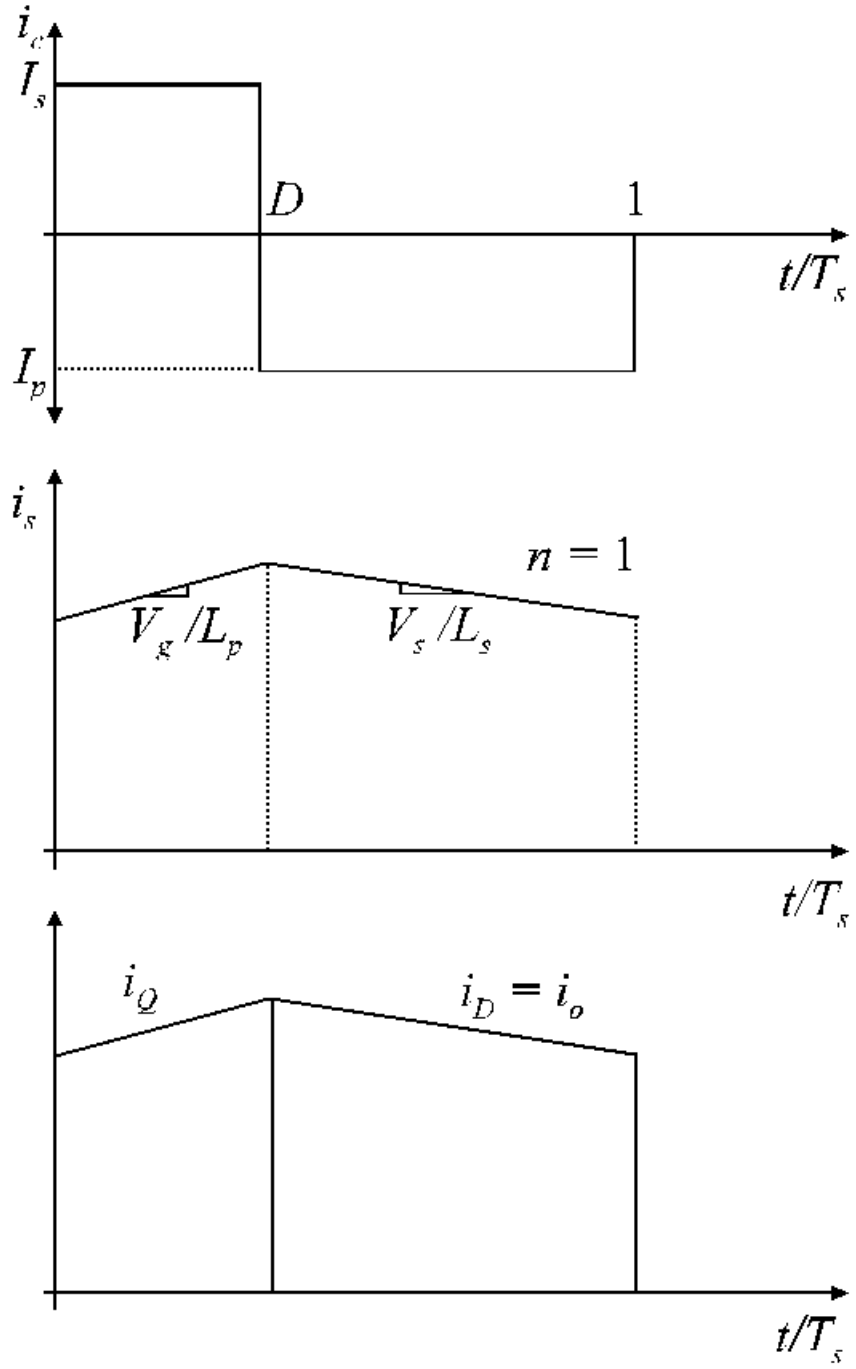
$$\tilde{i}_c = \bar{i}_g \cdot \sqrt{\frac{D'}{D}} = \bar{i}_o \cdot \sqrt{\frac{D}{D'}} = \sqrt{\bar{i}_g \cdot \bar{i}_o}$$

The coupling-capacitor rms current is the geometric mean of the primary and secondary average currents. These averages are, more precisely, the amplitudes of the square-waves of current when they are non-zero, and are amplitudes that are constant under the small-ripple approximation.

Selection of a capacitor is based on both $C_c$ value (from the above equation) and the rms current. To achieve low loss and high efficiency, polypropylene capacitors are a possible choice. Capacitors of larger voltage rating than what is needed may be necessary as the ripple-current requirement increases. Foil rather than metalized film capacitors are also capable of higher currents. These capacitors are expensive and impact circuit cost significantly. They are one of the detractors from Cuk-derived converters as ideal, though with some refinement (in a later article), even the $C_c$ current disadvantage can be overcome to some extent.

The SEPIC (Cuk-cell CP) $C_c$ voltage rating must exceed $V_g$. For the Cuk (Cuk-cell CS) configuration, the voltage rating must exceed $V_g + V_o$, and for the zeta (Cuk-cell CA), $V_o$.

Waveforms for $i_c$, $i_s$, $i_Q$ and $i_o$ are shown below:




In the bottom plot, $i_Q$ is non-zero only during the on-time, and $i_D$ only during the off-time. By including the magnetizing or ripple current, the waveforms correspond to the following design equations:

$$\bar{i}_p = \hat{i}_p - \hat{i}_m$$

where, $\hat{x}$ stands for the peak value.

Then the peak magnetizing current is:

$$\hat{i}_m = \frac{\Delta i_p}{2} = \frac{1}{2} \cdot \frac{V_g}{L} \cdot D \cdot T_s = \frac{1}{2} \cdot \frac{V_s}{L} \cdot D' \cdot T_s$$

Generally it is true for a transductor for which $n \approx 1$ that $L_p \approx L_s \approx L$. The ripple (ac) component of this current is:

$$i_{ac} = \frac{\hat{i}_m}{3}$$

And the rms current is:

$$\tilde{i} = \sqrt{D \cdot (\bar{i}^2 + i_{ac}^2)}$$

where, $i$ is either the primary or secondary current.

The MOSFET current rating depends to some extent on the peak current but for power applications is more dependent upon ohmic heating of the device. It is related to the rms current:

$$\tilde{i}_Q = \sqrt{D \cdot (\bar{i}_p + \bar{i}_s)^2 + i_{ac}^2} = \sqrt{D} \cdot \sqrt{\left(\frac{\bar{i}_p}{D}\right)^2 + i_{ac}^2}$$

For $i_m \approx 0$, this simplifies to:

$$\tilde{i}_Q = \frac{\bar{i}_g}{\sqrt{D}}$$

The transistor current can be reduced and the MOSFET made smaller and cheaper by increasing $D$. However, this decreases $D$' which increases the diode current requirement, for its rms current is:

$$\tilde{i}_D = \sqrt{D' \cdot (\bar{i}_p + \bar{i}_s)^2 + i_{ac}^2} = \sqrt{D'} \cdot \sqrt{\left(\frac{\bar{i}_s}{D'}\right)^2 + i_{ac}^2}$$

Under the small-ripple approximation, $i_m = 0$; then:

$$\tilde{i}_D = \frac{\bar{i}_o}{\sqrt{D'}}$$

Thus there is a tradeoff in selecting the nominal $D$ between transistor and diode current ratings. A figure of demerit useful in assessing converter design optimization is the *form factor*:

$$\kappa = \frac{\tilde{x}}{\bar{x}}$$

where, $x$ is voltage or current.

The average of a quantity is usually what we want. For example, the average output current is the rated current for the supply. The rms is what causes loss due to resistive dissipation of power and is what we want to minimize. Therefore, $\kappa$ is a measure of undesirability of waveform shape. A bipolar square-wave of $D = 1$ has $\kappa = 1$; a sine-wave has $\kappa = 2$ in comparison. $\kappa_Q$ varies inversely with $D$ while $\kappa_D$ varies directly. A compromise minimum is achieved at $D = 0.5$ of $\kappa_Q = \kappa_D = \sqrt{2} \approx 1.414$. At this operating point, the currents of the switch components must be rated about 41% greater than their average current values.

The SEPIC (Cuk-cell CP) voltage ratings of both transistor and diode must exceed $V_g + V_o$. For the Cuk (Cuk-cell CS) configuration, the voltage ratings are only $V_g$, and for the zeta (Cuk-cell CA), $V_o$.

We now have the basic design equations for the SEPIC converter. With them, component ratings can be determined. In the next part, we take to the bench and see whether what has been derived above is true.