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Advanced Three-Phase Multilevel Inverter with Least Number of Devices Operating From Non-Equal DC Sources

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Abstract

Multilevel inverters supplied from equal and constant dc sources almost don't exist in practical applications, even if sources are nominally equal. The variation of the dc sources affects the values of the switching angles required for each specific harmonic profile, as well as increases the difficulty of the harmonic elimination's equations. This paper proposes an advanced generalized configuration of multilevel inverters having the least number of switching devices, and operating from non-equal dc sources. Output voltage control is achieved through controlling the switching angles of the inverter while eliminating the dominant line harmonics. These angles are obtained by solving the relevant equations using the theory of resultant, which is based on solving polynomial equations where all possible solutions are obtained. The solution set which produces the lowest total harmonic distortion is selected. Both computational and simulation work are carried out and experimentally validated for a three-phase 5-level inverter.

Keywords: Multilevel converters, inverters, harmonic elimination, pulse width modulation (PWM).

1 INTRODUCTION

Multilevel inverter is considered as one of the most significant recent advances in power electronics [1]. Multilevel inverters have drawn tremendous interest in the field of high-voltage high-power applications such as laminators, mills, conveyors, compressors, large induction motor drives, UPS systems, and static var compensation. Its concept is based on producing small output voltage steps, resulting in better power quality. Multilevel inverters accomplish the concept of power conversion using small voltage steps, then achieving better power quality. Although this requires a large number of semiconductor devices, which is considered as a primary disadvantage. They are of lower ratings and operate at the fundamental frequency so that the switching loss is reduced and better electromagnetic compatibility is achieved. The fundamental configurations of multilevel inverters include; the diode-clamp topology, the flying-capacitor topology, and the series H-bridge topology [2]. Recently, there has been a great interest in cascaded hybrid topologies dedicated to large drive systems applications [3].

Recent improvement in the speed-power characteristics of power semiconductor switches, and the expected further price reduction in power semiconductor devices and increases in prices of reactive components have increased the interest to incorporate multilevel inverters in the medium and high power-level ranges, particularly in power system control and compensation [4]. This also enhances a movement towards reducing the number of switching devices in multilevel inverter circuits, which saves the gate requirements, diodes, and capacitors, leading to a smaller size, volume and less cost despite the increased voltage stress on the switches within the available range [5].

Multilevel inverters are mostly supplied from dc sources obtained from fuel cells, ultra capacitors, ect. Without external control, the equality of dc sources in multilevel inverter circuits don't exist in reality. Most of the reported work assumed that the dc sources were all equal, which will probably not be the case in applications even if the sources are nominally equal [1]-[5].

Practical capacitors, which provide the voltage divider task, can't guarantee to establish equal dc sources across different inverter levels even if they are nominally similar. This will affect the modulation process of the inverter and may lead to the presence of some unwanted low order harmonics. Despite their complexity, capacitor voltage balancing techniques are worth noting for this situation [6]. On the other hand, taking the inequality of the dc voltage sources into consideration would be a better solution, and would keep the simplicity of the circuit configuration.

This paper proposes an advanced new configuration of three-phase multilevel inverter circuit having the least number of components and operating from non-equal dc sources. A three-phase five-level inverter is used to illustrate the proposed configuration, where its associated waveforms

and modes of operation are outlined. Obviously, similar waveforms and modes can be realized for higher levels, where reduced voltage stress and better waveforms can be obtained. Also, the percentage saving in switching devices is increased by the increase of the number of levels. The modulation process is performed by controlling the switching angles of the inverter in order to obtain the required fundamental output voltage and, at the same time, eliminates the dominant low order line harmonics. This is achieved by first converting the transcendental equations describing the inverter output voltage into an equivalent set of polynomial equations. Then using the mathematical theory of resultant, all solution sets of switching angles can be found. The solution set which produce the lowest total harmonic distortion (THD) is selected. Computations and simulations of the proposed inverter configuration are conducted and experimentally verified.

2 THE NEW THREE-PHASE MULTILEVEL INVERETER CONFIGURATION

The principle objective of the proposed configuration of multilevel inverter power circuit is to reach at the minimum possible number of switching devices, without affecting the staircase output voltage waveform characterized by conventional multilevel topologies. However, there is a small penalty have to be paid, which is the increased rating of the four main switches as they have to withstand the whole dc bus. The continued and increased advances in high power semiconductor technology allowed the working range of IGBTs to reach 6.5kV, which will indeed increase the popularity of the presented configuration.

The generalized configuration of the proposed three-phase multilevel inverter is shown in Fig.1. Each phase consists of 4 main switches in an H-bridge configuration connected across the dc bus. A group of capacitors are connected across the dc bus to achieve voltage divider task for the different number of inverter levels. A number of bi-directional switches are connected from the supply voltage divider points to the phase voltage point of the main bridge. The generalized multilevel inverter of Fig.1 can be developed for any required number of levels. However, in order to simplify the computational work and experimental implementation, a three-phase 5-level inverter operating from non-equal dc sources is considered where similar modes can be realized for circuits with extra number of levels. The power circuit of the proposed three-phase 5-level inverter is shown in Fig.2. Each phase is composed of the main H-bridge inverter, a bi-directional switch, and two capacitors representing the non-equal dc sources.

On a per-phase basis, the proposed 5-level topology is using only five controlled power switches instead of eight required by any of the three fundamental configurations; thus achieving a 37.5% reduction in the number of main power switches. It also reduces the number of diodes by 60% (8 instead of 20 per phase), and the number of capacitors by 50% (2 instead of 4 per phase) as compared to the diode clamped configuration. The auxiliary switch voltage and current ratings are lower than the ones required by the main controlled switches. The proposed topology can be extended to any desired number of levels. Each extra level requires an additional bi-directional auxiliary switch and a dc capacitor to establish the additional dc voltage step. The possible saving in the number of IGBTs switches per phase of the proposed topology compared to existing cascaded H-bridge inverter versus the number of inverter levels is shown in Fig. 3. Actually, this is not the only saving, as the size and cost of gate drivers, isolators, diodes and capacitors will also be saved.

The modes of operation depend on the polarity of the output voltage and load current. Therefore, the following modes of operation (for phase *A*) can be identified:

1- Powering mode (Maximum level phase voltage): Switch pairs Q_{1A}, Q_{4A} or Q_{2A}, Q_{3A} are conducting to produce maximum positive or maximum negative level respectively, where the whole dc bus is applied to the load terminals.

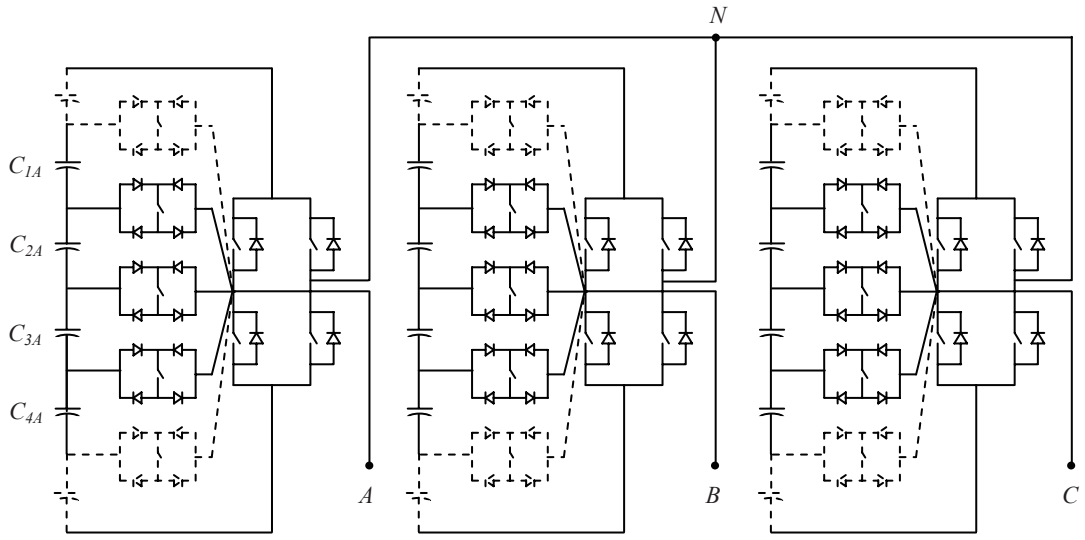

Fig. 1. Generalized circuit configuration of the new topology of multilevel inverters

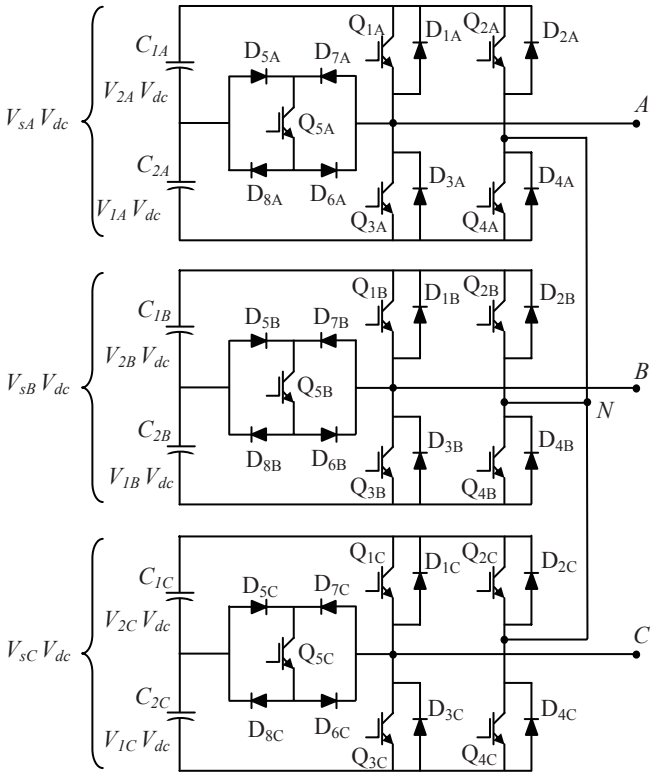

Fig. 2. The proposed three-phase 5-level inverter

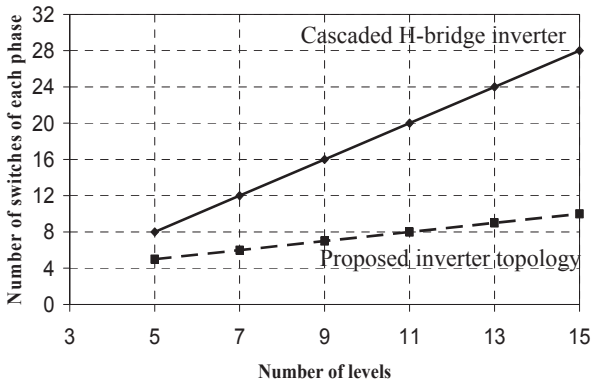

Fig. 3. Savings in number of switches of the new topology

2- Powering mode (nominal half-level output phase voltage): The bi-directional switch Q_{5A}, D_{5A} and D_{6A} and Q_{4A} are conducting for nominal positive half-level output phase voltage level, while the combination Q_{5A}, D_{7A}, D_{8A} and Q_{2A} are conducting for nominal negative half-level output phase voltage level.

3- Free-Wheeling mode (Zero output voltage level): In the positive half cycle of the load voltage, Q_{4A} and D_{3A} or Q_{1A} and D_{2A} are conducting, short circuiting the load, and all other devices are off, such that its voltage is zero. In the negative half cycle of the load voltage Q_{2A} and D_{1A} or Q_{3A} and D_{4A} are conducting, short circuiting the load and all other switches are off.

4- Regenerating mode: The circuit has the ability for regeneration, where energy can be returned back to a supply cell through the bi-directional switch depending on the polarity of load voltage and current.

3 PROBLEM FORMULATION AND ANALYSIS

Assuming that the non-equal dc sources are known, and taking into consideration the characteristics of the inverter waveform shown in Fig. 4, from its odd nature and half- and quarter-wave symmetry, the Fourier series expansion of the stepped output voltage waveform of the multilevel inverter with non-equal dc sources can be expressed as [7]:

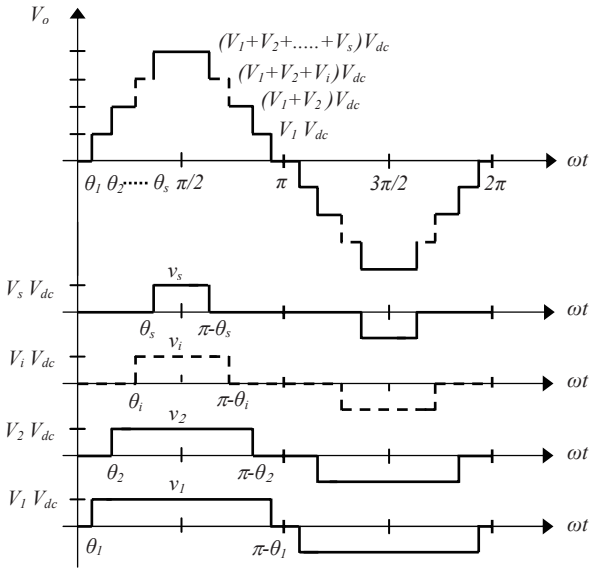

Fig. 4. Generalized output voltage waveform of multilevel inverters with non-equal dc sources

$$V_o(\omega t)=\sum_{n=1,3,5,\ldots}^{s}\frac{4V_{dc}}{n\pi}\left(V_1\cos(n\theta_1)+V_2\cos(n\theta_2)+\ldots.+V_s\cos(n\theta_s)\right)\sin(n\omega t) \qquad (1)$$

Where s is the number of dc sources, and the product V_iV_{dc} is the value of the i^{th} dc source. If all the dc sources have the same value V_{dc}, then $V_1=V_2=\cdots\cdots=V_s=1$. Equation (1) has s variables (θ_1, θ_2, θ_3,……, θ_s), where $0\le\theta_1<\theta_2<\cdots<\theta_s\le\pi/2$, and a set of solutions is obtainable by equating s-1 harmonics to zero and assigning a specific value to the fundamental component, as given below:

$$\left.\begin{aligned}
&V_1\cos(\theta_1)+V_2\cos(\theta_2)+\cdots\cdots+V_s\cos(\theta_s)=m\\
&V_1\cos(5\theta_1)+V_2\cos(5\theta_2)+\cdots\cdots+V_s\cos(5\theta_s)=0\\
&V_1\cos(7\theta_1)+V_2\cos(7\theta_2)+\cdots\cdots+V_s\cos(7\theta_s)=0\\
&\qquad\vdots\\
&V_1\cos(n\theta_1)+V_2\cos(n\theta_2)+\cdots\cdots+V_s\cos(n\theta_s)=0
\end{aligned}\right\} \qquad (2)$$

Where $m=V_1/(4V_{dc}/\pi)$, and the modulation index m_a is given by $m_a=m/s$.

The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Then the resultant method is employed to find the solutions when they exist [7]. These sets of solutions have to be examined for its corresponding THD in order to select the set which generate the lowest harmonic distortion (mostly due to the 11th and 13th harmonics). The computed THD in percent is defined by:

$$\%THD = \sqrt{\frac{V_3^2 + V_5^2 + V_7^2 + \cdots\cdots + V_{19}^2}{V_1^2}} \times 100 \qquad (3)$$

Considering the case of solving 3 equations such that the fundamental component can be controlled, and the 5th and 7th harmonics can be eliminated. The 3rd harmonic, and its multiples, are not taken into consideration as they are automatically eliminated in the line-line voltage. Transforming the transcendental equations (2) into polynomial equations using the change of variables:

$$x_1 = \cos\theta_1, \quad x_2 = \cos\theta_2, \quad x_3 = \cos\theta_3 \qquad (4)$$

And the trigonometric identities:

$$\cos(5\theta) = 5\cos\theta - 20\cos^3\theta + 16\cos^5\theta \qquad (5)$$

$$\cos(7\theta) = -7\cos\theta + 56\cos^3\theta - 112\cos^5\theta + 64\cos^7\theta \qquad (6)$$

To transfer (2) into the equivalent conditions:

$$p_1(x) = V_1x_1 + V_2x_2 + V_3x_3 - m = 0 \qquad (7)$$

$$p_5(x) = \sum_{i=1}^{3} V_i\left(5x_i - 20x_i^3 + 16x_i^5\right) = 0 \qquad (8)$$

$$p_7(x) = \sum_{i=1}^{3} V_i\left(-7x_i + 56x_i^3 - 112x_i^5 + 64x_i^7\right) = 0 \qquad (9)$$

Equations (7), (8), and (9) forming a set of three polynomial equations in three unknowns x_1, x_2, and x_3, where $x = (x_1, x_2, x_3)$, and the angles condition must satisfy $0 \le x_3 \le x_2 \le x_1 \le 1$.

Equation (7) can be rewritten as:

$$x_3 = \frac{m - (V_1x_1 + V_2x_2)}{V_3} \qquad (10)$$

Substituting from (10) in (8) and (9) yields to a system of polynomial equations. A systematic procedure to obtain the solutions of these polynomial systems is known as elimination theory and uses the notion of resultants. A detailed explanation of this procedure can be found in [7].

4 COMPUTATIONAL AND SIMULATION RESULTS

Since 5-level inverter has only two switching angles θ_1 and θ_2 per quarter cycle, therefore the fundamental component can be controlled and a low order harmonic can be eliminated. Since the 3rd harmonic and its multiples will be automatically eliminated in the line-line voltage, therefore the 5th harmonic is the first existing low order harmonic such that it will be considered for elimination. Assuming that the values of the dc sources can be measured, the polynomial equations are solved, using the above mentioned technique, for all possible solutions (sets of switching angles) for any given value of m. The THD produced by output waveform using each of these sets of switching angles is computed, and the particular solution which produces the smallest THD is chosen. In order to obtain general solutions, computations were performed in the per unit basis. Since infinite number of case studies can be exited depending on the values of the dc sources of the three phases, the presented work considers the values of dc voltages given in Table I.

Computation for the given values of the dc sources was performed for the three-phases over the entire operating range of m. Fig. 5 illustrates the variation of the obtained switching angles of phase A versus m, where solutions only exist in the range $0.6 \le m \le 1.65$ and no optimal solutions can't be found outside this range. Similar computations were done to obtain the switching angles for phases B and C. The results of the case study of the three phases are also given in Table I.

TABLE I
CASE STUDY OF NON-EQUAL DC SOURCES AND CORRESPONDING SWITCHING ANGLES

Phase	V_1V_{dc} (p.u.)	V_2V_{dc} (p.u.)	m= 1.5	
			θ_1	θ_2
A	1	0.9	17.048°	52.815°
B	0.95	0.88	13.448°	49.11°
C	0.98	0.94	17.187°	53.148°

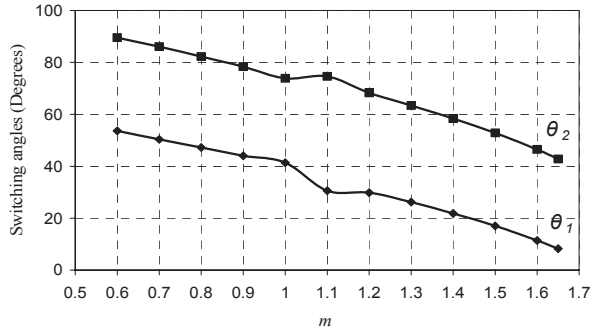

Fig. 5. Solutions for 2 angles of phase A versus m (5th harmonic eliminated)

The inverter circuit was simulated using PSIM for the values given in Table I. Figs. 6 and 7 show the inverter output phase and line-line voltages, where the 30º between the respective phase and line voltages is clearly seen, which reflects the soundness of the modulation strategy. The line-line voltage

has a nine-step waveform, where this is a natural phenomenon in 3-phase multilevel inverters as the number of steps in the line-line voltage exceeds that of the phase voltage by four step levels. Beside the increased voltage level, this has the effect of improving the harmonic profile of the line-line voltages. The corresponding harmonic spectrum of the phase voltage V_A and line-line voltage V_{AB} are shown in Figs. 8 and 9 respectively. Similar FFT for phases *B* and *C* were also obtained. It is clear that the targeted 5th harmonic is eliminated from the phase voltages and the fundamental component is equal to 1.9 p.u. as desired (s=2, m=1.5, V_{dc}=1 p.u., $V_f = (4mV_{dc}/\pi)$ =1.9 p.u.). Also, the first low order harmonic appears in the line-line voltages is the 7th harmonic as the 3rd harmonic is automatically eliminated, and the fundamental component equals $\sqrt{3} \times 1.9 = 3.29$ p.u. The THD for the voltage waveform of V_A and V_{AB} were computed from the FFT of Figs. 8 and 9 and found to be 5.7% and 4.8% respectively.

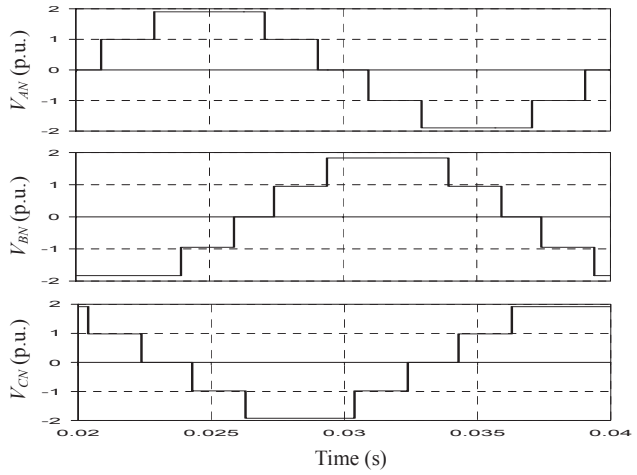

Fig. 6. The inverter output phase voltages (for values given in Table I)

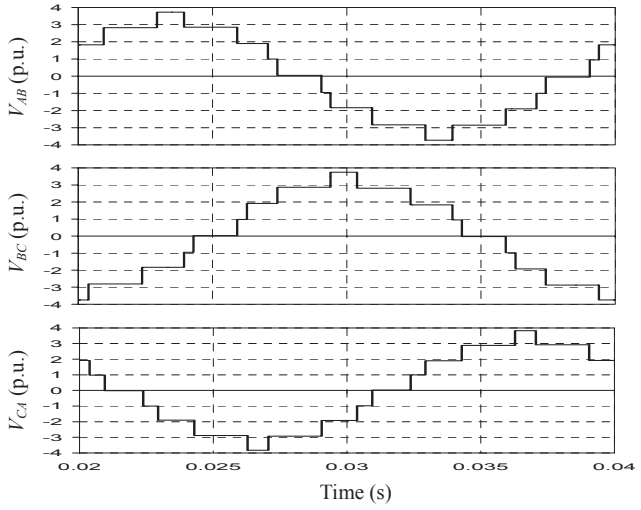

Fig. 7. The inverter output line-line voltages (for values given in Table I)

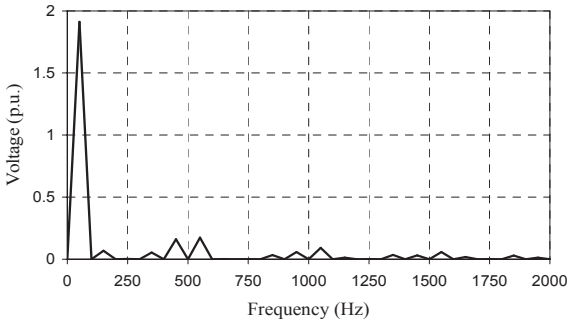

Fig. 8. FFT of inverter phase voltage V_A (V_1=1 p.u., V_2= 0.9 p.u., m=1.5)

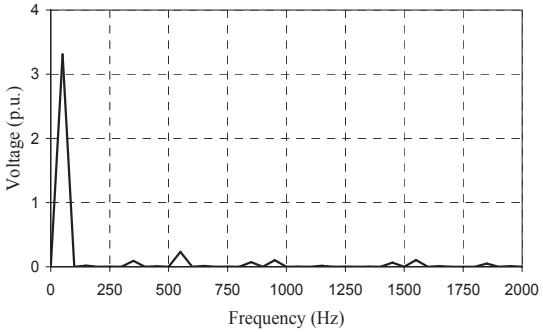

Fig. 9. FFT of inverter line-line voltage V_{AB} (V_1=1 p.u., V_2= 0.9 p.u., m=1.5)

5 EXPERMENTAL RESULTS

A prototype three-phase 5-level inverter was built using 600-V, 20-A GT20J321 IGBTs as the switching devices. A separate dc sources of 60V dc (nominally) was used to individually supply each inverter level. The data shown in Fig. 5 and those of the other two phases *B* and *C* were put in a look-up table format, and the generation of the PWM gating signals is obtained by cycling through a delay loop. A real-time controller based on MCB-1A Hampden microprocessor kit is used to implement the programmed PWM technique. The switching angles are converted into switching patterns using a down-counter and some logic operations. The switching patterns obtained from the controller are interfaced to the inverter power switches through optocoupler isolators and drivers. To verify the presented simulation results, the hardware implementation is developed for the same case study of simulation given in Table I. The three-phase inverter output voltages were measured, where phase voltage V_A, line-line voltage V_{AB}, and their corresponding FFT are shown in Figs. 10-13. The phase and line-line voltages are almost identical to those of simulations. The 5th harmonic is eliminated from both phase and line-line voltages, while the 3rd harmonic and its multiples are suppressed from the line-line voltages. The THD for the voltage waveforms of V_A and V_{AB} were computed from the FFT of Figs. 11 and 13 and found to be in the same range as those from simulations.

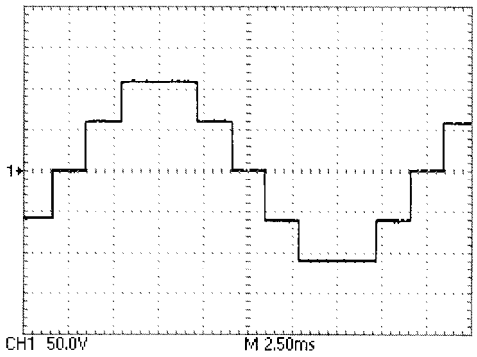

Fig. 10. Phase voltage V_A at the values of Table I, (V_{dc}= 60V)

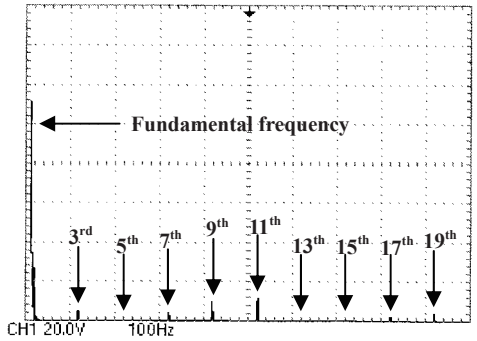

Fig. 11. FFT of output phase voltage V_A at the values of Table I, (V_{dc}= 60V)

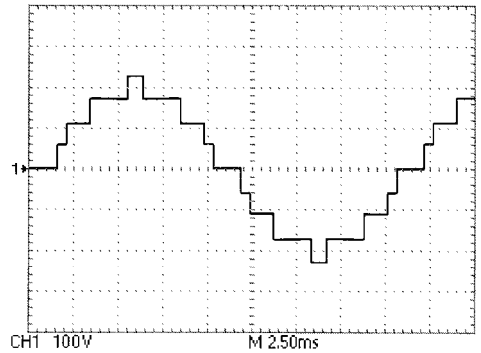

Fig. 12. Line-line voltage V_{AB} at the values of Table I, (V_{dc}= 60V)

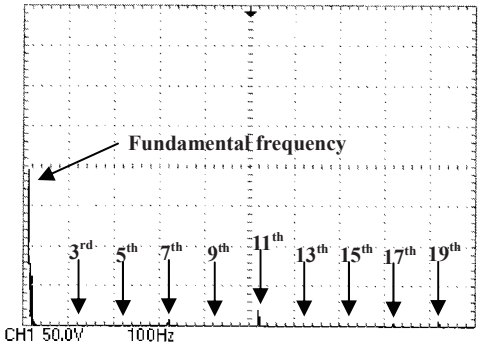

Fig. 13. FFT of output line-line voltage V_{AB} at the values of Table I, (V_{dc}= 60V)

6 CONLUSIONS

An advanced configuration of three-phase multilevel inverter topology having the minimum number of switching devices and operating from non-equal dc sources has been presented. The study was focused on a 5-level inverter, where similar results can be obtained for higher levels. A programmed PWM algorithm, based on the theory of resultant, is used to achieve the modulation process. For each case study defined by the values of the dc sources, optimal solution can be found over a definite range of modulation index. Both simulation and experimental implementation proved the soundness and effectiveness of both the new inverter topology and the programmed PWM technique, where both output voltage control and harmonic elimination are achieved and result in a dramatic decrease in the output voltage and current THD. This inverter configuration may be applied to large drive systems, UPS systems, static VAR compensation schemes, and distributed power generation involving fuel cells and photovoltaic cells.

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