

Appendices

Appendix A

RMS Values of Commonly Observed Converter Waveforms

The waveforms encountered in power electronics converters can be quite complex, containing modulation at the switching frequency and often also at the ac line frequency. During converter design, it is often necessary to compute the rms values of such waveforms. In this appendix, several useful formulas and tables are developed which allow these rms values to be quickly determined.

RMS values of the doubly-modulated waveforms encountered in PWM rectifier circuits are discussed in Section 18.5.

A.1 SOME COMMON WAVEFORMS

DC, Fig. A.1:

$$rms = I \quad (A.1)$$

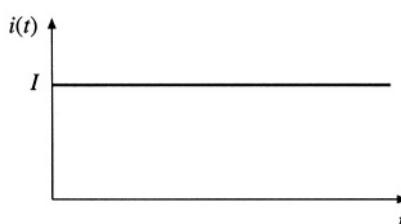


Fig. A.1

DC plus linear ripple, Fig. A.2:

$$rms = I \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I} \right)^2} \quad (A.2)$$

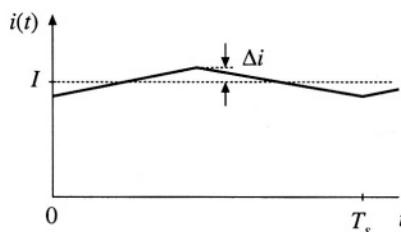


Fig. A.2

Square wave, Fig. A.3:

$$rms = I_{pk} \quad (A.3)$$

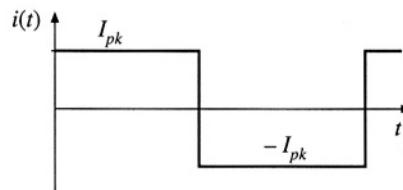


Fig. A.3

Sine wave, Fig. A.4:

$$rms = \frac{I_{pk}}{\sqrt{2}} \quad (A.4)$$

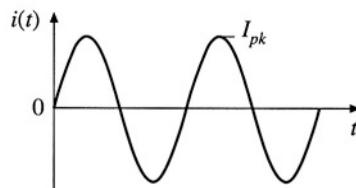


Fig. A.4

Pulsating waveform, Fig. A.5:

$$rms = I_{pk} \sqrt{D} \quad (A.5)$$

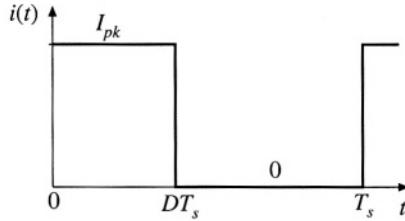


Fig. A.5

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I \sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I} \right)^2} \quad (\text{A.6})$$

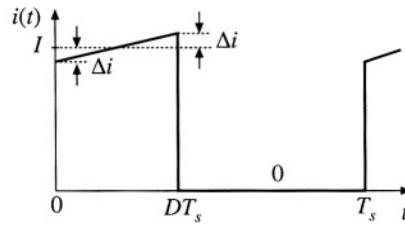


Fig. A.6

Triangular waveform, Fig. A.7:

$$rms = I_{pk} \sqrt{\frac{D_1 + D_2}{3}} \quad (\text{A.7})$$

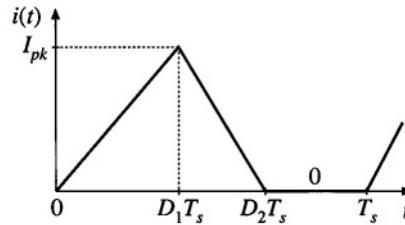
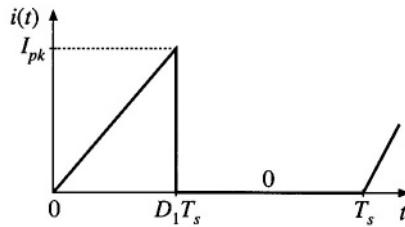


Fig. A.7

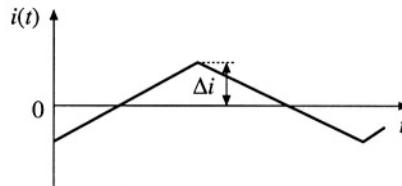
Triangular waveform, Fig. A.8:

$$rms = I_{pk} \sqrt{\frac{D_1}{3}} \quad (\text{A.8})$$

**Fig. A.8**

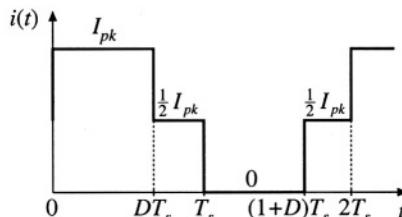
Triangular waveform, no dc component, Fig. A.9:

$$rms = \frac{\Delta i}{\sqrt{3}} \quad (A.9)$$

**Fig. A.9**

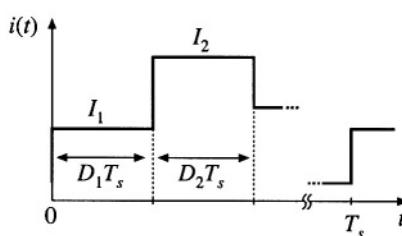
Center-tapped bridge winding waveform, Fig. A.10:

$$rms = \frac{1}{2} I_{pk} \sqrt{1+D} \quad (A.10)$$

**Fig. A.10**

General stepped waveform, Fig. A.11:

$$rms = \sqrt{D_1 I_1^2 + D_2 I_2^2 + \dots} \quad (A.11)$$

**Fig. A.11**

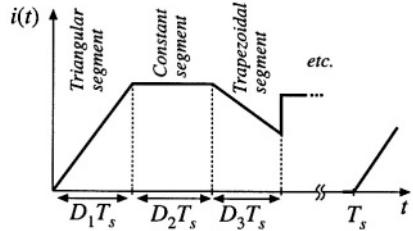


Fig. A.12 General piecewise waveform.

A.2 GENERAL PIECEWISE WAVEFORM

For a periodic waveform composed of n piecewise segments as in Fig. A.12, the rms value is

$$rms = \sqrt{\sum_{k=1}^n D_k u_k} \quad (\text{A.12})$$

where D_k is the duty cycle of segment k , and u_k is the contribution of segment k . The u_k s depend on the shape of the segments—several common segment shapes are listed below:

Constant segment, Fig. A.13:

$$u_k = I_1^2 \quad (\text{A.13})$$

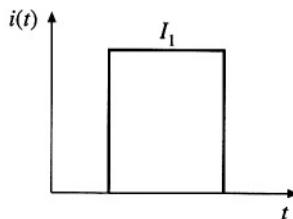


Fig. A.13

Triangular segment, Fig. A.14:

$$u_k = \frac{1}{3} I_1^2 \quad (\text{A.14})$$

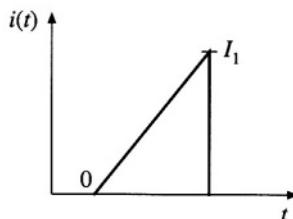


Fig. A.14

Trapezoidal segment, Fig. A.15:

$$u_k = \frac{1}{3} (I_1^2 + I_1 I_2 + I_2^2) \quad (\text{A.15})$$

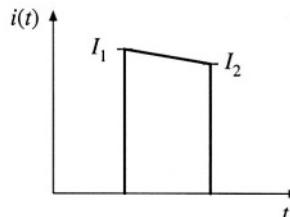


Fig. A.15

Sinusoidal segment, half or full period, Fig. A.16:

$$u_k = \frac{1}{2} I_{pk}^2 \quad (\text{A.16})$$

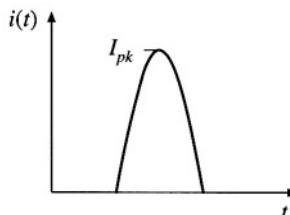


Fig. A.16

Sinusoidal segment, partial period: as in Fig. A.17, a sinusoidal segment of less than one half-period, which begins at angle θ_1 and ends at angle θ_2 . The angles θ_1 and θ_2 are expressed in radians:

$$u_k = \frac{1}{2} I_{pk}^2 \left(1 - \frac{\sin(\theta_2 - \theta_1) \cos(\theta_2 + \theta_1)}{(\theta_2 - \theta_1)} \right) \quad (\text{A.17})$$

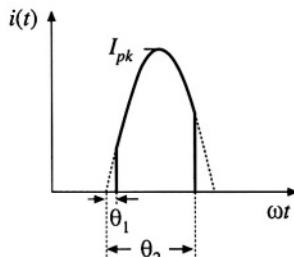


Fig. A.17

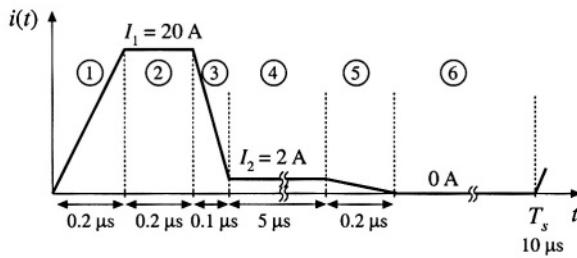


Fig. A.18 Example: an approximate transistor current waveform, including estimated current spike due to diode stored charge.

Example

A transistor current waveform contains a current spike due to the stored charge of a freewheeling diode. The observed waveform can be approximated as shown in Fig. A1.18. Estimate the rms current.

The waveform can be divided into six approximately linear segments, as shown. The D_k and u_k for each segment are

1. Triangular segment:

$$D_1 = (0.2 \mu s)/(10 \mu s) = 0.02$$

$$u_1 = I_1^2/3 = (20 \text{ A})^2/3 = 133 \text{ A}^2$$

2. Constant segment:

$$D_2 = (0.2 \mu s)/(10 \mu s) = 0.02$$

$$u_2 = I_1^2 = (20 \text{ A})^2 = 400 \text{ A}^2$$

3. Trapezoidal segment:

$$D_3 = (0.1 \mu s)/(10 \mu s) = 0.01$$

$$u_3 = (I_1^2 + I_2^2 + I_3^2)/3 = 148 \text{ A}^2$$

4. Constant segment:

$$D_4 = (5 \mu s)/(10 \mu s) = 0.5$$

$$u_4 = I_2^2 = (2 \text{ A})^2 = 4 \text{ A}^2$$

5. Triangular segment:

$$D_5 = (0.2 \mu s)/(10 \mu s) = 0.02$$

$$u_5 = I_2^2/3 = (2 \text{ A})^2/3 = 1.3 \text{ A}^2$$

6. Zero segment:

$$u_6 = 0$$

The rms value is

$$rms = \sqrt{\sum_{k=1}^6 D_k u_k} = 3.76 \text{ A} \quad (\text{A.18})$$

Even though its duration is very short, the current spike has a significant impact on the rms value of the current—without the current spike, the rms current is approximately 2.0 A.

Appendix B

Simulation of Converters

Computer simulation can be a powerful tool in the engineering design process. Starting from design specifications, an initial design typically includes selection of system and circuit configurations, as well as component types and values. In this process, component and system models are constructed based on vendor-supplied data, and by applications of analysis and modeling techniques. These models, validated by experimental data whenever possible, are the basis upon which the designer can choose parameter values and verify the achieved performance against the design specifications. One must take into account the fact that actual parameter values will not match their nominal values because of inevitable production tolerances, changes in environmental conditions (such as temperature), and aging. In the design verification step, worst-case analysis (or other reliability and production yield analysis) is performed to judge whether the specifications are met under all conditions, i.e., for expected ranges of component parameter values. Computer simulation is very well suited for this task: using reliable models and appropriate simulation setups, the system performance can be tested for various sets of component parameter values. One can then perform design iterations until the worst-case behavior meets specifications, or until the system reliability and production yield are acceptably high.

In the design verification of power electronic systems by simulation, it is often necessary to use component and system models of various levels of complexity:

1. *Detailed, complex models that attempt to accurately represent physical behavior of devices.* Such models are necessary for tasks that involve finding switching times, details of switching transitions and switching loss mechanisms, or instantaneous voltage and current stresses. Component vendors often provide libraries of such device models. To complete a detailed circuit model, one must also carefully examine effects of packaging and board interconnects. With fast-switching power semiconductors, simulation time steps of a few nanoseconds or less may be required, especially during on/off switching transitions. Because of the complexity of detailed device models, and the fine time resolution, the simulation tasks can be very time consuming. In practice, time-domain simulations using detailed device models are usually performed only

on selected parts of the system, and over short time intervals involving a few switching cycles at most. Devices for power converters, and detailed physical device modeling, are areas of active research and development beyond the scope of this book.

2. *Simplified device models.* Since an on/off switching transition usually takes a small fraction of a switching cycle, the basic operation of switching power converters can be explained using simplified, idealized device models. For example, a MOSFET can be modeled as a switch with a small (ideally zero) on-resistance R_{on} when on, and a very large off-resistance (ideally an open circuit) when off. Such simplified models yield physical insight into the basic operation of switching power converters, and provide the starting point for developments of analytical models described throughout this book. Simplified device models are also useful for time-domain simulations aimed at verifying converter and controller operation, switching ripples, current and voltage stresses, and responses to load or input transients. Since device models are simple, and details of switching transitions are ignored, tasks that require simulations over many switching cycles can be completed efficiently using general-purpose circuit simulators. In addition, specialized tools have been developed to support fast transient simulation of switching power converters based on idealized, piecewise-linear device models [1-7], or a combination of piecewise-linear and nonlinear models [8].
3. *Averaged converter models.* Averaged models that are well suited for prediction of converter steady-state and dynamic responses are discussed throughout this book. These models are essential design tools because they provide physical insight and lead to analytical results that can be used in the design process to select component parameter values for a given set of specifications. In the design verification step, simulations of averaged converter models can be performed to test for losses and efficiency, steady-state voltages and currents, stability, and large-signal transient responses. Since switching transitions and ripples are removed by averaging, simulations over long time intervals and over many sets of parameter values can be completed efficiently. As a result, averaged models are also well suited for simulations of large electronic systems that include switching converters. Furthermore, since large-signal averaged models are nonlinear, but time-invariant, small-signal ac simulations can be used to generate various frequency responses of interest. Selected references on averaged converter modeling for simulation are listed at the end of this chapter [9-18].

Averaged models for computer simulation are covered in this appendix. Based on the material presented in Section 7.4, averaged switch models for computer simulation of converters operating in continuous conduction mode are described in Section B.1. Application examples include finding SEPIC dc conversion ratio and efficiency, and large-signal transient responses of a buck-boost converter. Section B.2 describes an averaged switch model suitable for simulation of converters that may operate either in continuous conduction mode or in discontinuous conduction mode. Application examples include finding SEPIC open-loop frequency responses in CCM and DCM, loop-gain, phase margin and closed-loop responses of a buck voltage regulator, and current harmonics in a DCM boost rectifier. Based on the results from Chapter 12, a simulation model for converters with current programmed control is described in Section B.3, together with a buck converter example that compares control-to-output frequency responses with current programmed control against duty-cycle control.

It is assumed that the reader is familiar with basics of Spice circuit simulations. All simulation models and examples in this appendix are prepared using the PSpice circuit simulator [19]. Netlists are included to help explain details of model implementation and simulation analysis options. Usually, instead of writing netlists, the user would enter circuit diagrams and analysis options from a front-end schematic capture tool. The examples and the library *switch.lib* of subcircuit models described in this appendix are available on-line. Similar models and examples can be constructed for use with other simulation tools.

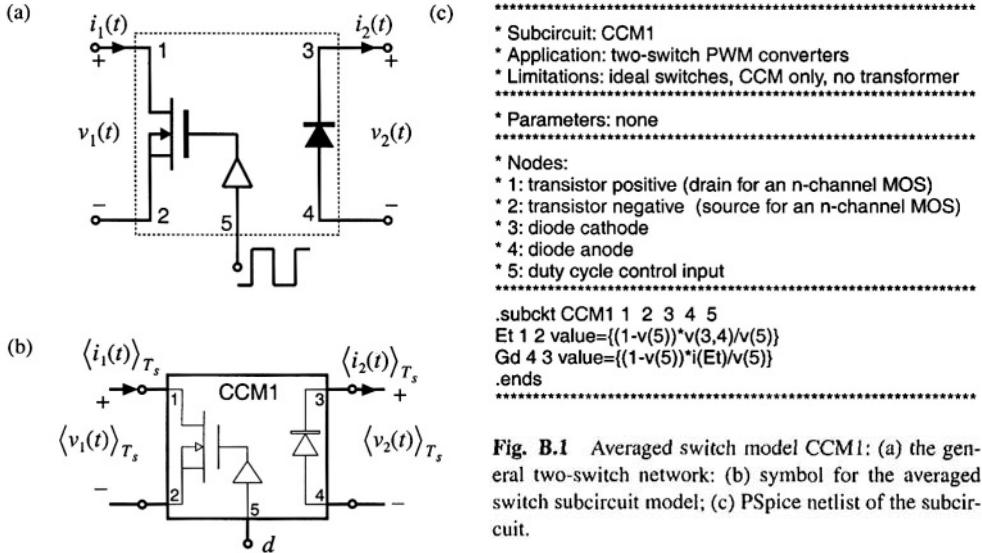


Fig. B.1 Averaged switch model CCM1: (a) the general two-switch network; (b) symbol for the averaged switch subcircuit model; (c) PSpice netlist of the subcircuit.

B.1 AVERAGED SWITCH MODELS FOR CONTINUOUS CONDUCTION MODE

The central idea of the *averaged switch modeling* described in Section 7.4 is to identify a switch network in the converter, and then to find an averaged circuit model. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete model of the converter. An important feature of the averaged switch modeling approach is that the same model can be used in many different converter configurations; it is not necessary to rederive an averaged equivalent circuit for each particular converter. This feature is also very convenient for construction of averaged circuit models for simulation. A general-purpose subcircuit represents a large-signal nonlinear averaged switch model. The converter averaged circuit for simulation is then obtained by replacing the switch network with this subcircuit. Based on the discussion in Section 7.4, subcircuits that represent CCM averaged switch models are described in this section, together with application examples.

B.1.1 Basic CCM Averaged Switch Model

The large-signal averaged switch model for the general two-switch network of Fig. 7.39(a) is shown in Fig. 7.39(c). A PSpice subcircuit implementation of this model is shown in Fig. B.1. The subcircuit has five nodes. The transistor port of the averaged switch network is connected between the nodes 1 and 2, while the diode port is comprised of nodes 3 and 4. The duty ratio $d = v(5)$ is the control input to the subcircuit at the node 5. The quantity $v(5)$ is a voltage that is equal to the duty cycle, and that lies in the range zero to one volt. Figure B.1(c) shows the netlist of the subcircuit. The netlist consists of only four lines of code and several comment lines (the lines starting with *). The .subckt line defines the name (CCM1) of the subcircuit and the interface nodes. The value of the controlled voltage source E_t , which

models the transistor port of the averaged switch network, is written according to Eq. (7.136):

$$\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s} \quad (\text{B.1})$$

Note that $v(3,4)$ in the subcircuit of Fig. B.1 is equal to the switch network independent input $\langle v_2(t) \rangle_{T_s}$. Also, $d(t) = v(5)$, and $d'(t) = 1 - d(t) = 1 - v(5)$. The value of the controlled current source G_d , which models the diode port, is computed according to Eq. (7.137):

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (\text{B.2})$$

The switch network independent input $\langle i_1(t) \rangle_{T_s}$ equals the current $i(E_t)$ through the controlled voltage source E_t . The ends line completes the subcircuit netlist. The subcircuit CCM1 is included in the model library *switch.lib*.

An advantage of the subcircuit CCM1 of Fig. B.1 is that it can be used to construct an averaged circuit model for simulation of any two-switch PWM converter operating in continuous conduction mode, subject to the assumptions that the switches can be considered ideal, and that the converter does not include a step-up or step-down transformer. The subcircuit can be further refined to remove these limitations. In converters with an isolation transformer, the right-hand side of Eqs. (B.1) and (B.2) should be divided by the transformer turns ratio. Inclusion of switch conduction losses is discussed in the next section.

A disadvantage of the model in Fig. B.1 is that Eqs. (B.1) and (B.2) have a discontinuity at duty cycle equal to zero. In applications of the subcircuit, it is necessary to restrict the duty-cycle to the range $0 < D_{\min} \leq d \leq 1$.

Following the approach of this section, subcircuits can be constructed for the large-signal averaged models of the buck switch network (see Fig. 7.50(a), and Eqs. (7.150)), and the boost switch network (see Fig. 7.46(a) and Eqs. (7.146)). An advantage of these models is that their defining equations do not have the discontinuity problem at $d = 0$.

B.1.2 CCM Averaged Switch Model that Includes Switch Conduction Losses

Let us modify the model of Fig. B.1 to include switch conduction losses. Figure B.2 shows simple device models that include transistor and diode conduction losses in the general two-switch network of Fig. B.1(a). The transistor is modeled as an ideal switch in series with an on-resistance R_{on} . The diode is modeled as an ideal diode in series with a forward voltage drop V_D and resistance R_D .

Construction of dc equivalent circuits to find dc conversion ratio and efficiency of converters is discussed in Chapter 3. Derivation of an averaged switch model that includes conduction losses arising from R_{on} and V_D is described in Section 7.4.5. Following the same averaged switch modeling approach, we can find the following relationships that describe the averaged switch model for the switch network of Fig. B.2:

$$\langle v_1(t) \rangle_{T_s} = \left(\frac{R_{on}}{d(t)} + \frac{d'(t)R_D}{d^2(t)} \right) \langle i_1(t) \rangle_{T_s} + \frac{d''(t)}{d(t)} \left(\langle v_2(t) \rangle_{T_s} + V_D \right) \quad (\text{B.3})$$

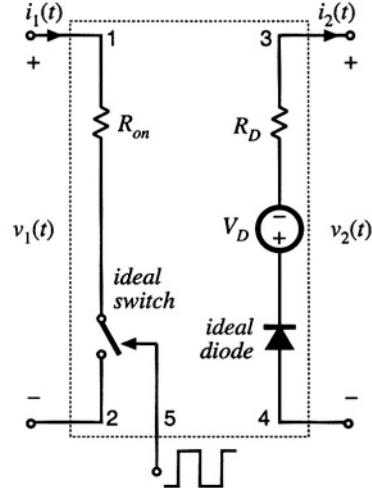


Fig. B.2 Switch network model that includes conduction loss elements R_{on} , V_D and R_D .

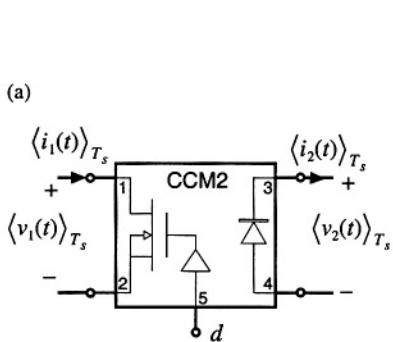


Fig. B.3 Subcircuit implementation of the CCM averaged switch model that includes conduction losses: (a) circuit symbol; (b) PSpice netlist for the subcircuit.

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (\text{B.4})$$

A subcircuit implementation of the averaged switch model described by Eqs. (B.3) and (B.4) is shown in Fig. B.3. The subcircuit terminal nodes are the same as in the CCM1 subcircuit: the transistor port is between the nodes 1 and 2; the diode port is between the nodes 3 and 4; the duty ratio $d = v(5)$ is the con-

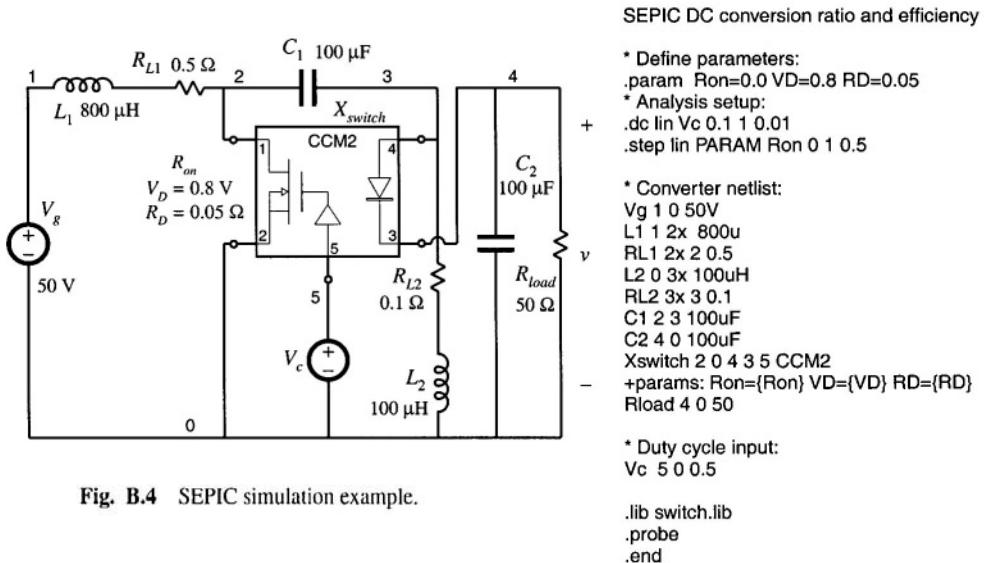


Fig. B.4 SEPIC simulation example.

trol input to the subcircuit at the node 5. Two controlled voltage sources in series, E_r and $E_{r'}$, are used to generate the port 1 (transistor) averaged voltage according to Eq. (B.3). The controlled voltage source E_r models the voltage drop across the equivalent resistance $R_{on}/d(t) + d'(t)R_D/d^2(t)$ in Eq. (B.3). Note that this equivalent resistance is a nonlinear function of the switch duty cycle $d(t)$. The controlled voltage source E_r shows how the port 1 (transistor) averaged voltage depends on the port 2 (diode) averaged voltage. The controlled current source G_d models the averaged diode current according to Eq. (B.4). The subcircuit CCM2 has three parameters (R_{on} , V_D , and R_D) that can be specified when the subcircuit is used in a converter circuit. The default values of the subcircuit parameters, $R_{on} = 0$, $V_D = 0$, and $R_D = 0$, are defined in the .subckt line. These values correspond to the ideal case of no conduction losses. The subcircuit CCM2 is included in the model library *switch.lib*.

The model of Fig. B.3 is based on the simple device models of Fig. B.2. It is assumed that inductor current ripples are small and that the converter operates in continuous conduction mode. Many practical converters, however, must operate in discontinuous conduction mode at low duty cycles where the diode forward voltage drop is comparable to or larger than the output voltage. In such cases, the model of Fig. B.2, which includes V_D as a fixed voltage generator, gives incorrect, physically impossible results for polarities of converter voltages and currents, losses and efficiency.

B.1.3 Example: SEPIC DC Conversion Ratio and Efficiency

Let us consider an example of how the subcircuit CCM2 can be used to generate dc conversion ratio and efficiency curves for a CCM converter. As an example, Figure B.4 shows a SEPIC averaged circuit model. The converter circuit can be found in Fig. 6.38(a), or in Fig. 7.37. To construct the averaged circuit model for simulation, the switch network is replaced by the subcircuit CCM2. In the converter netlist shown in Fig. B.4, the X_{switch} line shows how the subcircuit is connected to other parts of the converter. The switch duty cycle is set by the voltage source V_c . All other parts of the converter circuit are simply copied to the averaged circuit model. Inductor winding resistances $R_{L1} = 0.5 \Omega$ and $R_{L2} = 0.1 \Omega$ are

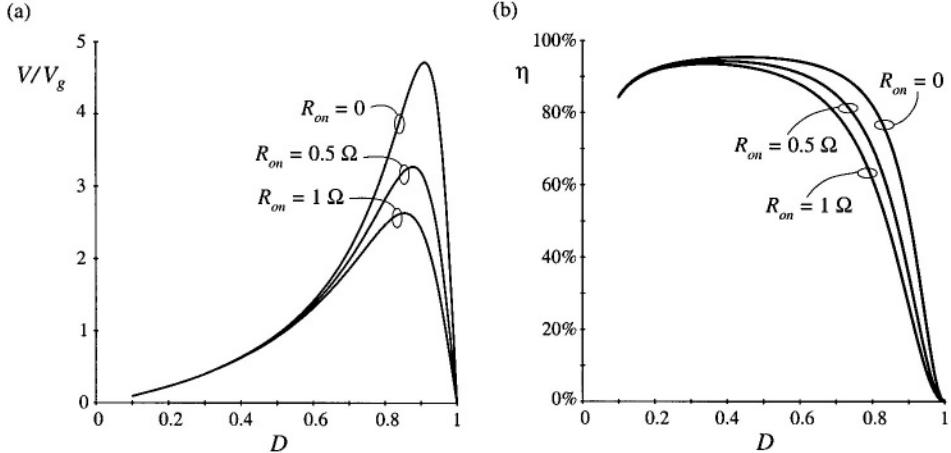


Fig. B.5 SEPIC simulation example: (a) dc conversion ratio and (b) efficiency.

included to model copper losses of the inductors L_1 and L_2 , respectively. The switch conduction loss parameters are defined by the .param line in the netlist: $R_{on} = 0$, $V_D = 0.8$ V, $R_D = 0.05$ Ω . Notice how these values are passed to the subcircuit CCM2 in the X_{switch} line. In this example, all other losses in the converter are neglected. A dc sweep analysis (see the .dc line in the netlist) is set to vary the dc voltage source V_c from 0.1 V to 1 V, in 0.01 V increments, which corresponds to varying the switch duty cycle over the range from $D = 0.1$ to $D = 1$. The range of duty cycles from zero to 0.1 is not covered because of the model discontinuity problem at $D = 0$ (discussed in Section B.1.1), and because the model predictions for conduction losses at low duty cycles are not valid, as discussed in Section B.1.2. The dc sweep analysis is repeated for values of the switch on-resistance in the range from $R_{on} = 0 \Omega$ to $R_{on} = 1 \Omega$ in 0.5Ω increments (see the .step line in the netlist). The .lib line refers to the *switch.lib* library, which contains definitions of the subcircuit CCM2 and all other subcircuit models described in this appendix.

Simulation results for the dc output voltage V and the converter efficiency η are shown in Fig. B.5. Several observations can be made based on the modeling approach and discussions presented in Chapter 3. At low duty cycles, efficiency drops because the diode forward voltage drop is comparable to the output voltage. At higher duty cycles, the converter currents increase, so that the conduction losses increase. Eventually, for duty cycles approaching 1, both the output voltage and the efficiency approach zero. Given a desired dc output voltage and efficiency, the plots in Fig. B.5 can be used to select the transistor with an appropriate value of the on-resistance.

B.1.4 Example: Transient Response of a Buck–Boost Converter

In addition to steady-state conversion characteristics, it is often of interest to investigate converter transient responses. For example, in voltage regulator designs, it is necessary to verify whether the output voltage remains within specified limits when the load current takes a step change. As another example, during a start-up transient when the converter is powered up, converter components can be exposed to significantly higher stresses than in steady state. It is of interest to verify that component stresses are

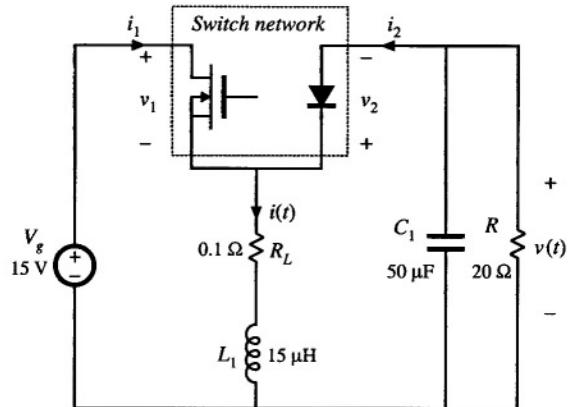


Fig. B.6 Buck-boost converter example.

within specifications or to make design modifications to reduce the stresses. In these examples, transient simulations can be used to test for converter responses.

Transient simulations can be performed on the converter switching circuit model or on the converter averaged circuit model. As an example, let us apply these two approaches to investigate a start-up transient response of the buck-boost converter shown in Fig. B.6.

Figure B.7 shows a switching circuit model of the buck-boost converter. The inductor winding resistance R_L is included to model the inductor copper losses. The MOSFET is modeled as a voltage-controlled switch S_{q1} controlled by a pulsating voltage source v_c . The switch .model line specifies the switch on-resistance $R_{on} = 50 \text{ m}\Omega$, and the switch off-resistance $R_{off} = 10 \text{ M}\Omega$. The switch is on when the controlling voltage v_c is greater than $V_{on} = 6 \text{ V}$, and off when the controlling voltage v_c is less than $V_{off} = 4 \text{ V}$. The pulsating source v_c has the pulse amplitude equal to 10 V. The period is $T_s = 1/f_s = 10 \mu\text{s}$, the rise and fall times are $t_r = t_f = 100 \text{ ns}$, and the pulse width is $t_p = 7.9 \mu\text{s}$. The switch duty cycle is $D = (t_p + 0.5(t_r + t_f))/T_s = 0.8$. The built-in nonlinear Spice model is used for the diode. In the diode .model statement, only the parameter I_s is specified, to set the forward voltage drop across the diode. The switch and the diode models used in this example are very simple. Conduction losses are modeled in a simple manner, and details of complex device behavior during switching transitions are neglected.

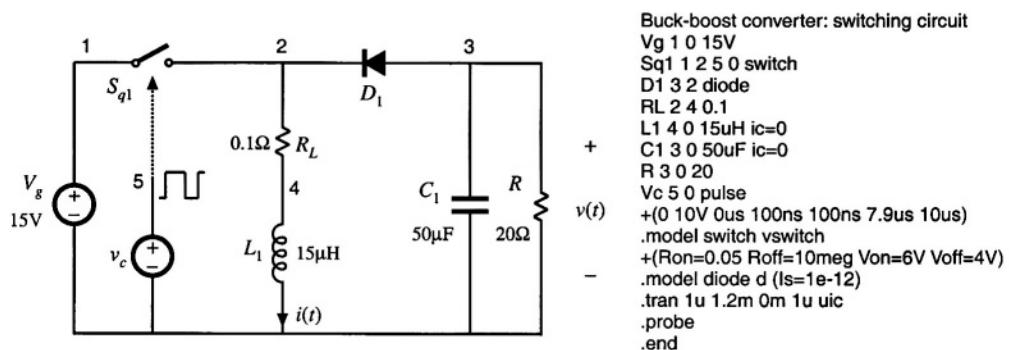


Fig. B.7 Buck-boost converter simulation example, switching circuit model.

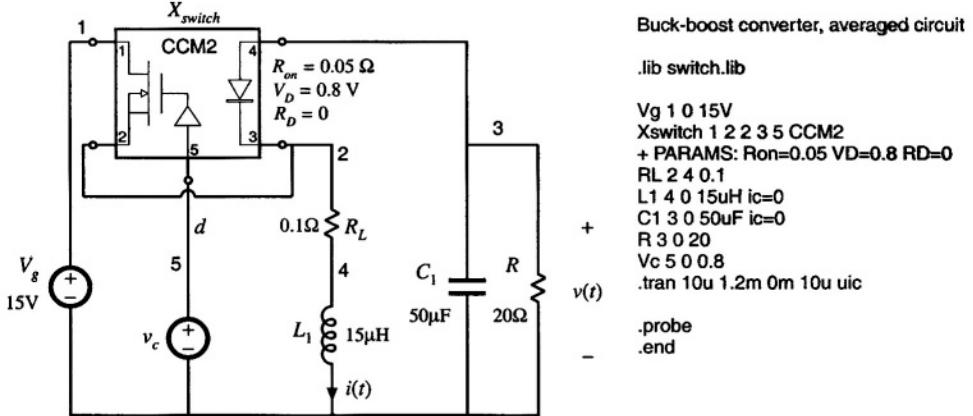


Fig. B.8 Buck-boost converter simulation example, averaged circuit model.

Therefore, the circuit model of Fig. B.7 cannot be used to examine switching transitions or to predict switching losses in the converter. Nevertheless, basic switching operation is modeled, and a transient simulation can be used to find out how the converter waveforms evolve in time over many switching cycles. Transient simulation parameters are defined by the .tran line: the output time step is 1 μ s, the final simulation time is 1.2 ms, the output waveforms are generated from the start of simulation at time equal to zero, and the maximum allowed time step is 1 μ s. The uic (“use initial conditions”) option tells the simulator to start with all capacitor voltages and inductor currents equal to the specified initial values. For example, ic=0 in the L_1 line sets the initial inductor current to zero. In Spice, the default initial conditions are always zero, so that ic=0 statements can be omitted.

An averaged circuit model of the buck-boost converter is shown in Fig. B.8. This circuit model is obtained by replacing the switch network in the converter of Fig. B.6 by the CCM2 subcircuit. Notice that the circuits and the netlists of Figs. B.7 and Fig. B.8 are very similar. The only difference is that the switching devices in the converter circuit of Fig. B.7 are replaced by the CCM2 subcircuit X_{switch} in Fig. B.8. Also, the pulsating source $v_c(t)$ in the switching circuit is replaced by a constant voltage source v_c equal to the switch duty cycle $D = 0.8$.

The inductor current and the capacitor voltage waveforms during the start-up transient are shown in Fig. B.9. For comparison, the waveforms obtained by transient simulation of the switching converter circuit shown in Fig. B.7, and by simulation of the averaged circuit model of Fig. B.8 are shown. Switching ripples can be observed in the waveforms obtained by simulation of the switching circuit model. The converter transient response is governed by the converter natural time constants. Since these time constants are much longer than the switching period, the converter start-up transient responses in Fig. B.9 take many switching cycles to reach the steady state. In the results obtained by simulation of the averaged circuit model, the switching ripples are removed, but the low-frequency portions of the converter transient responses, which are governed by the natural time constants of the converter network, match very closely the responses obtained by simulation of the switching circuit.

Based on the results shown in Fig. B.9, we can see that converter components are exposed to significantly higher current stresses during the start-up transient than during steady state operation. The problem of excessive stresses in the start-up transient is quite typical for switching power converters. Practical designs usually include a “soft-start” circuit, where the switch duty cycle is slowly increased

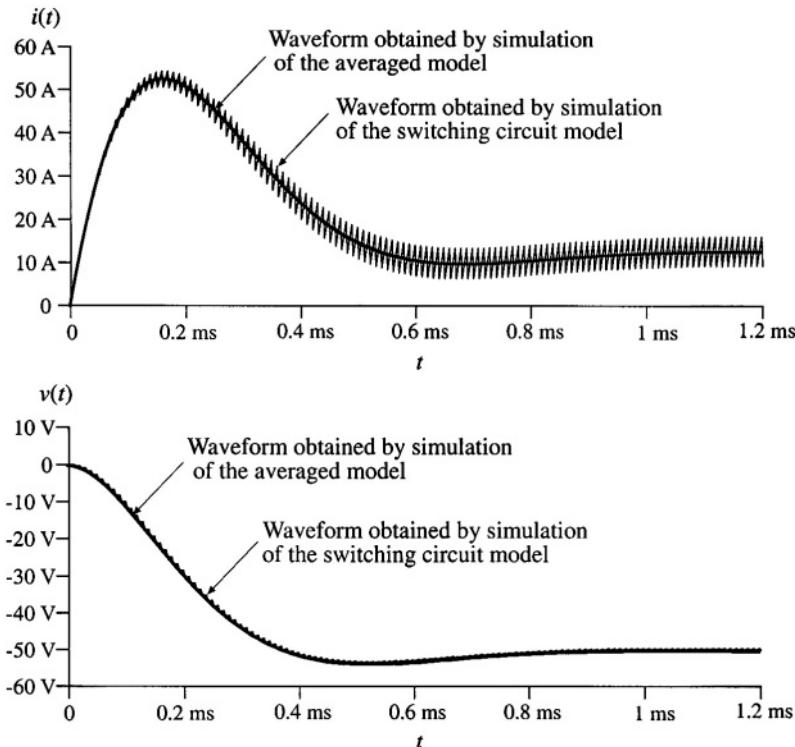


Fig. B.9 Inductor current and output voltage waveforms obtained by transient simulation of the switching converter circuit shown in Fig. B.7, and by simulation of the averaged circuit model of Fig. B.8

from zero to the steady-state value to reduce start-up transient stresses.

This simulation example illustrates how an averaged circuit model can be used in place of a switching circuit model to investigate converter large-signal transient responses. An advantage of the averaged circuit model is that transient simulations can be completed much more quickly because the averaged model is time invariant, and the simulator does not spend time computing the details of the fast switching transitions. This advantage can be important in simulations of larger electronic systems that include switching power converters. Another important advantage also comes from the fact that the averaged circuit model is nonlinear but time-invariant: ac simulations can be used to linearize the model and generate small-signal frequency responses of interest. This is not possible with switching circuit models. Examples of small-signal ac simulations can be found in Sections B.2 and B.3.

B.2 COMBINED CCM/DCM AVERAGED SWITCH MODEL

The models and examples of Section B.1 are all based on the assumption that the converters operate in continuous conduction mode (CCM). As discussed in Chapters 5 and 11, all converters containing a diode rectifier operate in discontinuous conduction mode (DCM) if the load current is sufficiently low. In some cases, converters are purposely designed to operate in DCM. It is therefore of interest to develop

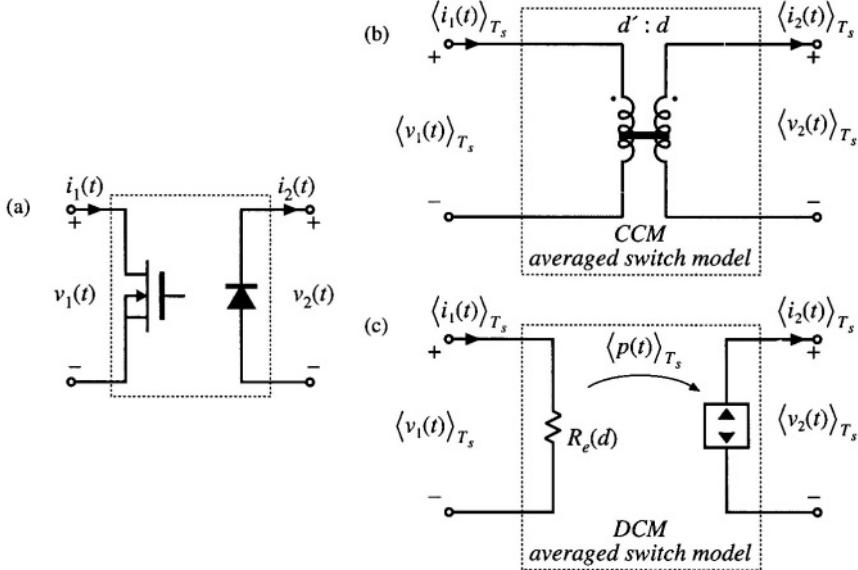


Fig. B.10 Summary of averaged switch modeling: (a) general two-switch network, (b) averaged switch model in CCM, and (c) averaged switch model in DCM.

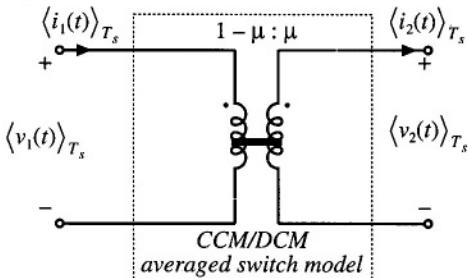


Fig. B.11 A general averaged switch model using the equivalent switch conversion ratio μ .

averaged models suitable for simulation of converters that may operate in either CCM or DCM.

Figure B.10 illustrates the general two-switch network, and the corresponding large-signal averaged models in CCM and DCM. The CCM averaged switch model, which is derived in Section 7.4, is an ideal transformer with $d' : d$ turns ratio. In DCM, the large-signal averaged switch model is a loss-free resistor, as derived in Section 11.1. Our objective is to construct a combined CCM/DCM averaged switch model that reduces to the model of Fig. B.10(a) or to the model of Fig. B.10(c) depending on the operating mode of the converter. Let us define an effective switch conversion ratio $\mu(t)$, so that the averaged switch model in both modes has the same form as in CCM, as shown in Fig. B.11. If the converter operates in CCM, then the switch conversion ratio $\mu(t)$ is equal to the switch duty cycle $d(t)$,

$$\mu = d \quad (B.5)$$

If the converter operates in DCM, then the effective switch conversion ratio can be computed so that the terminal characteristics of the averaged-switch model of Fig. B.11 match the terminal characteristics of the loss-free resistor model of Fig. B.10(c). Matching the port 1 characteristics gives

$$\langle v_1(t) \rangle_{T_s} = \frac{1-\mu}{\mu} \langle v_2(t) \rangle_{T_s} = R_e \langle i_1(t) \rangle_{T_s} \quad (B.6)$$

which can be solved for the switch conversion ratio μ ,

$$\mu = \frac{1}{1 + \frac{R_e \langle i_1(t) \rangle_{T_s}}{\langle v_2(t) \rangle_{T_s}}} \quad (B.7)$$

It can be verified that matching the port 2 characteristics of the models in Figs. B.10(c) and B.11 gives exactly the same result for the effective switch conversion ratio in DCM.

The switch conversion ratio $\mu(t)$ can be considered a generalization of the duty cycle $d(t)$ of CCM switch networks. Based on this approach, models and results developed for converters in CCM can be used not only for DCM but also for other operating modes or even for other converter configurations by simply replacing the switch duty cycle $d(t)$ with the appropriate switch conversion ratio $\mu(t)$ [21-24]. For example, if $M(d)$ is the conversion ratio in CCM, then $M(\mu)$, with μ given by Eq. (B.7), is the conversion ratio in DCM. The switch conversion ratio in DCM depends on the averaged terminal voltage and current, as well as the switch duty cycle d through the effective resistance $R_e = 2L/d^2T_s$. If the converter is completely unloaded, then the average transistor current $\langle i_1(t) \rangle_{T_s}$ is zero, and the DCM switch conversion ratio becomes $\mu = 1$. As a result, the dc output voltage attains the maximum possible value $V = V_g M(1)$. This is consistent with the results of the steady-state DCM analyses in Chapter 5 and Section 11.1.

To construct a combined CCM/DCM averaged switch model based on the general averaged switch model of Fig. B.11, it is necessary to specify which of the two expressions for the switch conversion ratio to use: Eq. (B.5), which is valid in CCM, or Eq. (B.7), which is valid in DCM. At the CCM/DCM boundary, these two expressions must give the same result, $\mu = d$. If the load current decreases further, the converter operates in DCM, the average switch current $\langle i_1(t) \rangle_{T_s}$ decreases, and the DCM switch conversion ratio in Eq. (B.7) becomes greater than the switch duty cycle d . We conclude that the correct value of the switch conversion ratio, which takes into account operation in CCM or DCM, is the larger of the two values computed using Eq. (B.5) and Eq. (B.7).

Figure B.12 shows an implementation of the combined CCM/DCM model as a PSpice subcircuit CCM-DCM1. This subcircuit has the same five interface nodes as the subcircuits CCM1 and CCM2 of Section B.1. The controlled sources E_t and G_d model the port 1 (transistor) and port 2 (diode) averaged characteristics, as shown in Fig. B.11. The switch conversion ratio μ is equal to the voltage $v(u)$ at the subcircuit node u . The controlled voltage source E_u computes the switch conversion ratio as the greater of the two values obtained from Eqs. (B.5) and (B.7). The controlled current source G_a , the zero-value voltage source V_a , and the resistor R_a form an auxiliary circuit to ensure that the solution found by the simulator has the transistor and the diode currents with correct polarities, $\langle i_1(t) \rangle_{T_s} > 0$, $\langle i_2(t) \rangle_{T_s} > 0$. The subcircuit parameters are the inductance L relevant for CCM/DCM operation, and the switching frequency f_s . The default values in the subcircuit are arbitrarily set to $L = 100 \mu\text{H}$ and $f_s = 100 \text{ kHz}$.

The PSpice subcircuit CCM-DCM1 of Fig. B.12 can be used for dc, ac, and transient simula-

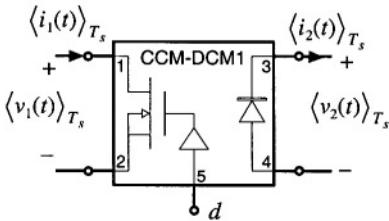


Fig. B.12 Implementation of the combined CCM/DCM averaged switch model.

```
*****
* MODEL: CCM-DCM1
* Application: two-switch PWM converters, CCM or DCM
* Limitations: ideal switches, no transformer
*****
* Parameters:
*   L = equivalent inductance for DCM
*   fs = switching frequency
*****
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
*****
.subckt CCM-DCM1 1 2 3 4 5
+ params: L=100u fs=1E5
Et 1 2 value={(1-v(u))*v(3,4)/v(u)}
Gd 4 3 value={(1-v(u))*i(Et)/v(u)}
Ga 0 a value=[MAX(i(Et),0)]
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5),
+ v(5)*v(5)/(v(5)*v(5)+2*L*fs*i(Va)/v(3,4)))} (0 0) (1 1)
.ends
*****
```

tions of PWM converters containing a transistor switch and a diode switch. This subcircuit is included in the model library *switch.lib*. It can be modified further for use in converters with isolation transformer.

B.2.1 Example: SEPIC Frequency Responses

As an example, Fig. B.13 shows a SEPIC circuit and the averaged circuit model obtained by replacing the switch network with the CCM-DCM1 subcircuit of Fig. B.12. A part of the circuit netlist is included in Fig. B.13. The connections and the parameters of the CCM-DCM1 subcircuit are defined by the *X_{switch}* line. In the SEPIC, the inductance parameter $L = 83.3 \mu\text{H}$ is equal to the parallel combination of L_1 and L_2 . The voltage source v_c sets the quiescent value of the duty cycle to $D = 0.4$, and the small-signal ac value to $\hat{d} = 1$. Ac simulation is performed on a linearized circuit model, so that amplitudes of all small-signal ac waveforms are directly proportional to the amplitude of the ac input, regardless of the input ac amplitude value. For example, the control-to-output transfer function is $G_{vd} = \hat{v}/\hat{d}$, where $\hat{v} = v(4)$ in the circuit of Fig. B.13(b). We can set the input ac amplitude to 1, so that the control-to-output transfer function G_{vd} can be measured directly as $v(5)$. This setup is just for convenience in finding small-signal frequency responses by simulation. For measurements of converter transfer functions in an experimental circuit (see Section 8.5), the actual amplitude of the small-signal ac variation \hat{d} would be set to a fraction of the quiescent duty cycle D . Parameters of the ac simulation are set by the .ac line in the netlist: the signal frequency is swept from the minimum frequency of 5 Hz to the maximum frequency of 50 kHz in 201 points per decade.

Figure B.14 shows magnitude and phase responses of the control-to-output transfer function obtained by ac simulations for two different values of the load resistance: $R = 40 \Omega$, for which the converter operates in CCM, and $R = 50 \Omega$, for which the converter operates in DCM. For these two operating

points, the quiescent (dc) voltages and currents in the circuit are nearly the same. Nevertheless, the frequency responses are qualitatively very different in the two operating modes. In CCM, the converter exhibits a fourth-order response with two pairs of high- Q complex-conjugate poles and a pair of complex-conjugate zeros. Another RHP (right-half plane) zero can be observed at frequencies approaching 50 kHz. In DCM, there is a dominant low-frequency pole followed by a pair of complex-conjugate poles and a pair of complex-conjugate zeros. The frequencies of the complex poles and zeros are very close in value. A high-frequency pole and a RHP zero contribute additional phase lag at higher frequencies.

In the design of a feedback controller around a converter that may operate in CCM or in DCM, one should take into account that the crossover frequency, the phase margin, and the closed-loop responses can be substantially different depending on the operating mode. This point is illustrated by the example of the next section.

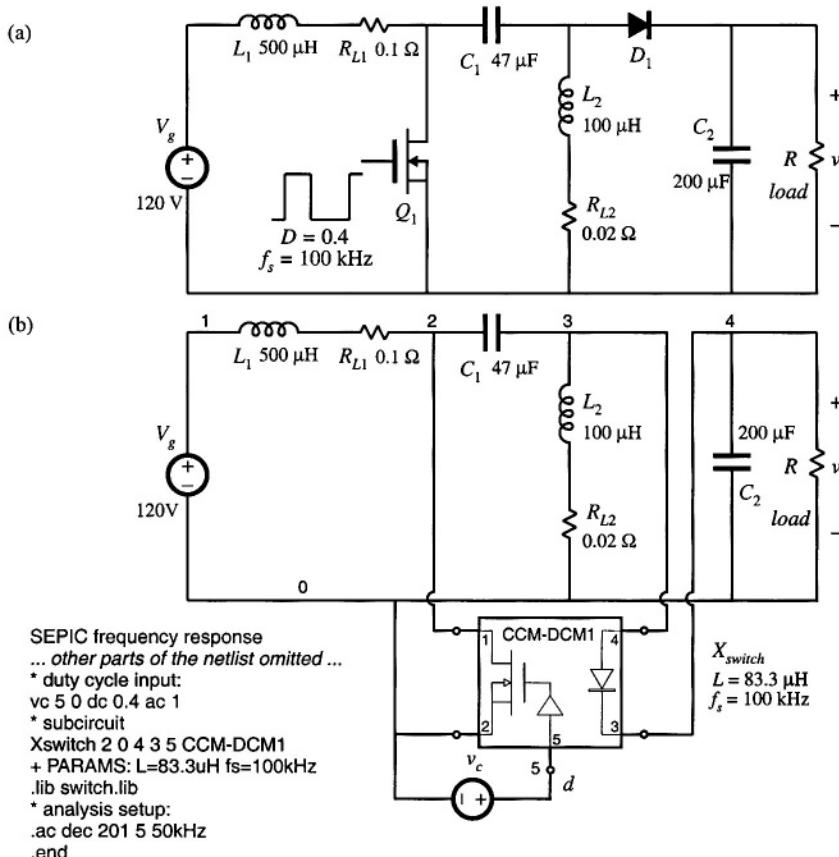


Fig. B.13 SEPIC simulation example: (a) converter circuit, (b) averaged circuit model for simulation.

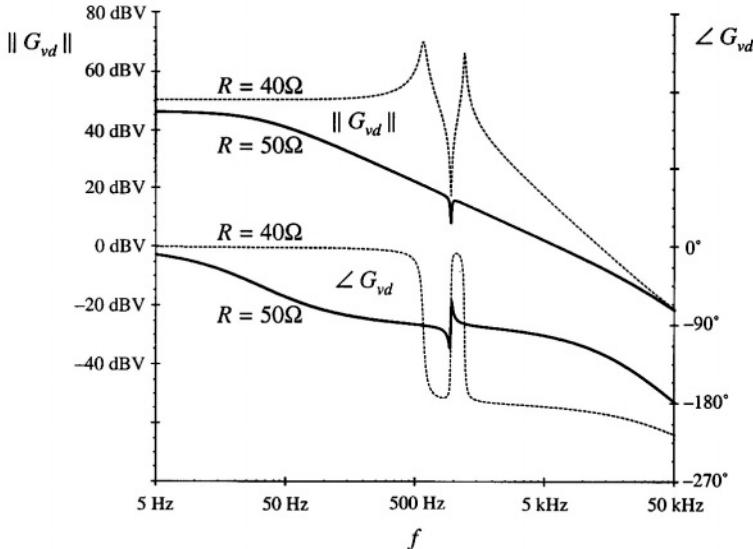


Fig. B.14 Magnitude and phase responses of the control-to-output transfer function obtained by simulation of the SEPIC example, for two values of the load resistance. For $R = 50 \Omega$, the converter operates in DCM (solid lines), and for $R = 40 \Omega$, the converter operates in CCM (dotted lines).

B.2.2 Example: Loop Gain and Closed-Loop Responses of a Buck Voltage Regulator

A controller design for a buck converter example is discussed in Section 9.5.4. The converter and the block diagram of the controller are shown in Fig. 9.22. This converter system is designed to regulate the dc output voltage at $V = 15$ V for the load current up to 5 A. Let us test this design by simulation. An averaged circuit model of a practical realization of the buck voltage regulator described in Section 9.5.4 is shown in Fig. B.15. The MOSFET and the diode switch are replaced by the averaged switch model implemented as the CCM-DCM1 subcircuit. The pulse-width modulator with $V_M = 4$ V is modeled according to the discussion in Section 7.6 as a dependent voltage source E_{pwm} controlled by the PWM input voltage v_x . The value of E_{pwm} is equal to $1/V_M = 0.25$ times the PWM input voltage v_x , with a limit for the minimum value set to 0.1 V, and a limit for the maximum value set to 0.9 V. The output of the pulse-width modulator is the control duty-cycle input to the CCM-DCM1 averaged switch subcircuit. Given the specified limits for E_{pwm} , the switch duty cycle $d(t)$ can take values in the range:

$$D_{\min} \leq d(t) \leq D_{\max} \quad (\text{B.8})$$

where $D_{\min} = 0.1$, and $D_{\max} = 0.9$. Practical PWM integrated circuits often have a limit $D_{\max} < 1$ for the maximum possible duty cycle. The voltage sensor and the compensator are implemented around an op-amp LM324. With very large loop gain in the system, the steady-state error voltage is approximately zero, i.e., the dc voltages at the plus and the minus inputs of the op-amp are almost the same,

$$v(5) = v_{ref} \quad (B.9)$$

As a result, the quiescent (dc) output voltage V is set by the reference voltage v_{ref} and the voltage divider comprised of R_1 , R_2 , R_4 :

$$V \frac{R_4}{R_1 + R_2 + R_4} = v_{ref} = 5 \text{ V} \quad (B.10)$$

By setting the ac reference voltage \hat{v}_{ref} to zero, the combined transfer function of the voltage sensor and the compensator can be found as:

$$H(s)G_c(s) = \frac{\hat{v}_y}{\hat{v}} = \frac{R_3 + \frac{1}{sC_3}}{R_1 + R_2 \parallel \frac{1}{sC_2}} \quad (B.11)$$

This transfer function can be written in factored pole-zero form as

$$G_{cm}H \frac{\left(1 + \frac{s}{\omega_i}\right)\left(1 + \frac{\omega_L}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \quad (B.12)$$

where

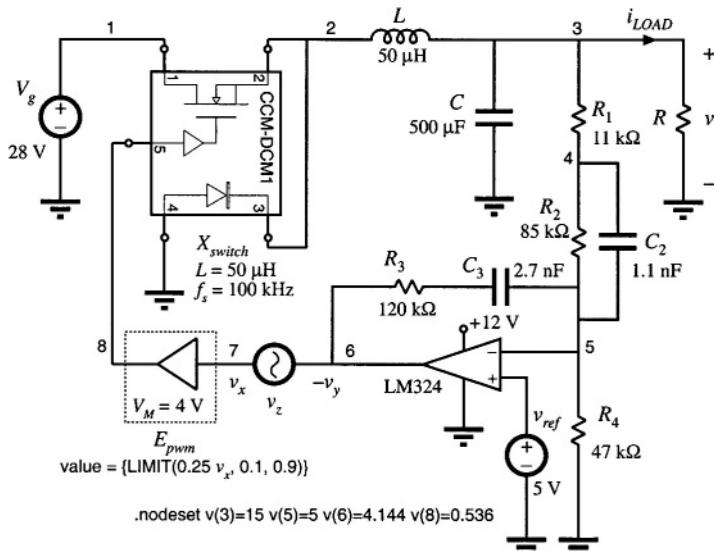


Fig. B.15 Buck voltage regulator example.

$$G_{cm}H = \frac{R_3}{R_1 + R_2} \quad (B.13)$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi R_2 C_2} \quad (B.14)$$

$$f_L = \frac{\omega_L}{2\pi} = \frac{1}{2\pi R_3 C_3} \quad (B.15)$$

and

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi(R_1 \parallel R_2)C_2} \quad (B.16)$$

The design described in Section 9.5.4 resulted in the following values for the gain and the corner frequencies:

$$G_{cm}H = 3.7(1/3) = 1.23, f_z = 1.7 \text{ kHz}, f_L = 500 \text{ Hz}, f_p = 14.5 \text{ kHz} \quad (B.17)$$

Eqs. (B.10) and (B.13) to (B.17) can be used to select the circuit parameter values. Let us (somewhat arbitrarily) choose $C_2 = 1.1 \text{ nF}$. Then, from Eq. (B.14), we have $R_2 = 85 \text{ k}\Omega$, and Eq. (B.16) yields $R_1 = 11 \text{ k}\Omega$. From Eq. (B.13) we obtain $R_3 = 120 \text{ k}\Omega$, and Eq. (B.15) gives $C_3 = 2.7 \text{ }\mu\text{F}$. Finally, $R_4 = 47 \text{ k}\Omega$ is found from Eq. (B.10). The voltage regulator design can now be tested by simulations of the circuit in Fig. B.15.

Loop gains can be obtained by simulation using exactly the same techniques described in Section 9.6 for experimental measurement of loop gains [20]. Let us apply the voltage injection technique of Section 9.6.1. An ac voltage source v_z is injected between the compensator output and the PWM input. This is a good injection point since the output impedance of the compensator built around the op-amp is small, and the PWM input impedance is very large (infinity in the circuit model of Fig. B.15). With the ac source amplitude set (arbitrarily) to 1, and no other ac sources in the circuit, ac simulations are performed to find the loop gain as

$$T(s) = \frac{\hat{v}_y}{\hat{v}_x} = -\frac{v(6)}{v(7)} \quad (B.18)$$

To perform ac analysis, the simulator first solves for the quiescent (dc) operating point. The circuit is then linearized at this operating point, and small-signal frequency responses are computed for the specified range of signal frequencies. Solving for the quiescent operating point involves numerical solution of a system of nonlinear equations. In some cases, the numerical solution does not converge and the simulation is aborted with an error message. In particular, convergence problems often occur in circuits with feedback, especially when the loop gain at dc is very large. This is the case in the circuit of Fig. B.15. To help convergence when the simulator is solving for the quiescent operating point, one can specify approximate or expected values of node voltages using the .nodeset line as shown in Fig. B.15. In this case, we know by design that the quiescent output voltage is close to 15 V ($v(3) = 15$), that the negative input of the op-amp is very close to the reference ($v(5) = 5$), and that the quiescent duty cycle is approximately $D = V/V_g = 0.536$, so that $v(8) = 0.536 \text{ V}$. Given these approximate node voltages, the numerical solution converges, and the following quiescent operating points are found by the simulator for two values of the load resistance R :

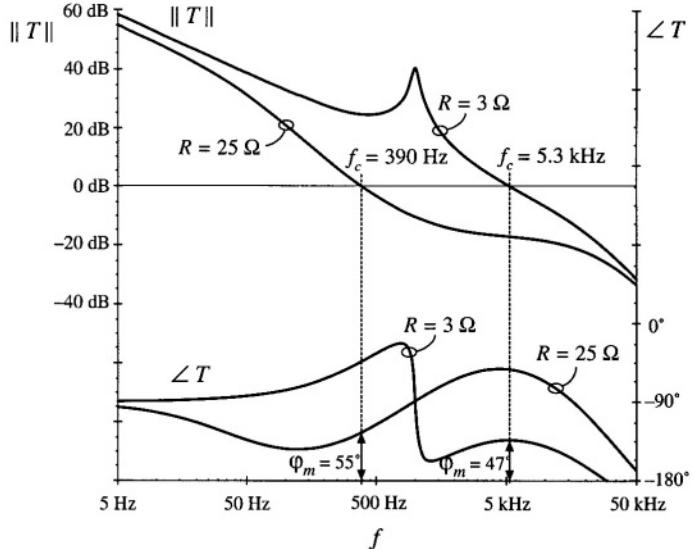


Fig. B.16 Loop gain in the buck voltage regulator example.

$$R = 3 \Omega, v(3) = 15.2 \text{ V}, v(5) = 5.0 \text{ V}, v(7) = 2.173 \text{ V}, v(8) = 0.543 \text{ V}, D = 0.543 \quad (\text{B.19})$$

$$R = 25 \Omega, v(3) = 15.2 \text{ V}, v(5) = 5.0 \text{ V}, v(7) = 2.033 \text{ V}, v(8) = 0.508 \text{ V}, D = 0.508 \quad (\text{B.20})$$

For the nominal load resistance $R = 3 \Omega$, the converter operates in CCM, so that $D = V/V_g$. For $R = 25 \Omega$, the same dc output voltage is obtained for a lower value of the quiescent duty cycle, which means that the converter operates in DCM.

The magnitude and phase responses of the loop gain found for the operating points given by Eqs. (B.19) and (B.20) are shown in Fig. B.16. For $R = 3 \Omega$, the crossover frequency is $f_c = 5.3 \text{ kHz}$, and the phase margin is $\phi_M = 47^\circ$, very close to the values ($f_c = 5 \text{ kHz}$, $\phi_M = 52^\circ$) that we designed for in Section 9.5.4. At light load, for $R = 25 \Omega$, the loop gain responses are considerably different because the converter operates in DCM. The crossover frequency drops to $f_c = 390 \text{ Hz}$, while the phase margin is $\phi_M = 55^\circ$.

The magnitude responses of the line-to-output transfer function are shown in Fig. B.17, again for two values of the load resistance, $R = 3 \Omega$ and $R = 25 \Omega$. The open-loop responses are obtained by braking the feedback loop at node 8, and setting the dc voltage at this node to the quiescent value D of the duty cycle. For $R = 3 \Omega$, the open-loop and closed-loop responses can be compared to the theoretical plots shown in Fig. 9.32. At 100 Hz, the closed-loop magnitude response is $0.012 \Rightarrow -38 \text{ dB}$. A 1 V, 100 Hz variation in $v_g(t)$ would induce a 12 mV variation in the output voltage $v(t)$. For $R = 25 \Omega$, the closed loop magnitude response is $0.02 \Rightarrow -34 \text{ dB}$, which means that the 1 V, 100 Hz variation in $v_g(t)$ would induce a 20 mV variation in the output voltage. Notice how the regulator performance in terms of rejecting the input voltage disturbance is significantly worse at light load than at the nominal load.

A test of the transient response to a step change in load is shown in Fig. B.18. The load current is initially equal to 1.5 A, and increases to $i_{LOAD} = 5 \text{ A}$ at $t = 0.1 \text{ ms}$. When the converter is operated in

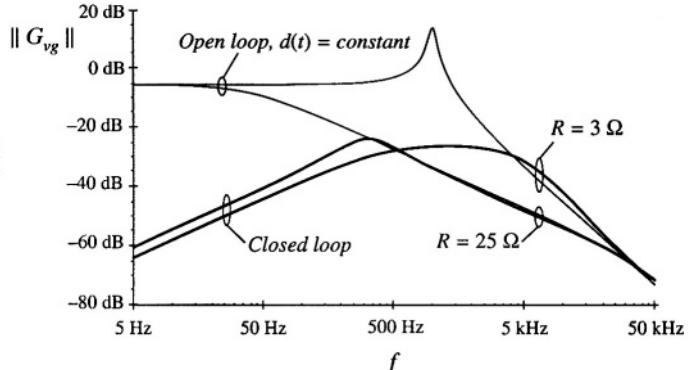


Fig. B.17 Line to output response of the buck voltage regulator.

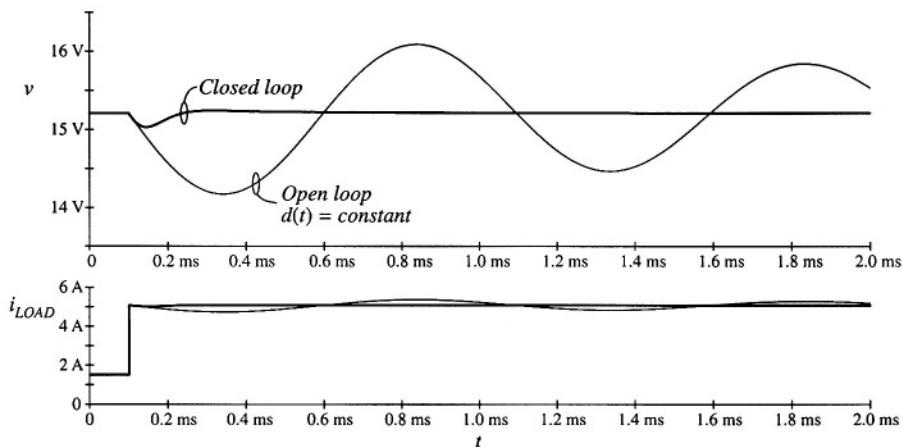


Fig. B.18 Load transient response of the buck voltage regulator example.

open loop at constant duty cycle, the response is governed by the natural time constants of the converter network. A large undershoot and long lightly-damped oscillations can be observed in the output voltage. With the feedback loop closed, the controller dynamically adjusts the duty cycle $d(t)$ trying to maintain the output voltage constant. The output voltage drops by about 0.2 V, and it returns to the regulated value after a short, well-damped transient.

The voltage regulator example of Fig. B.15 illustrates how the performance can vary significantly if the regulator is expected to supply a wide range of loads. In practice, further tests would also be performed to account for expected ranges of input voltages, and variations in component parameter values. Design iterations may be necessary to ensure that performance specifications are met under worst case conditions.

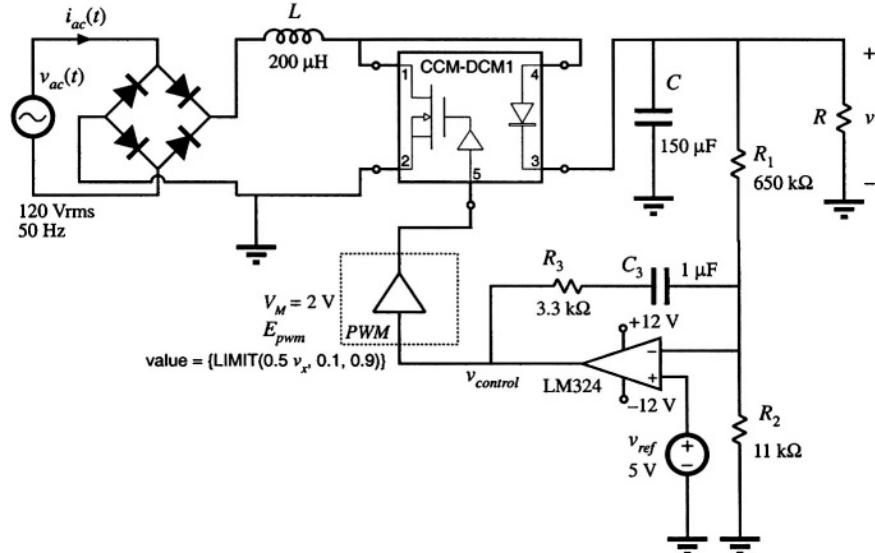


Fig. B.19 DCM boost rectifier example.

B.2.3 Example: DCM Boost Rectifier

Converters switching at frequencies much above the ac line frequency can be used to construct near-ideal rectifiers where power is taken from the ac line without generation of line current harmonics. Approaches to construction of low-harmonic rectifiers are discussed in Chapter 18. One simple solution is based on the boost converter operating in discontinuous conduction mode, as described in Section 18.2.1. When a boost DCM converter operates at a constant switch duty cycle, the input current approximately follows the input voltage. The DCM effective resistance $2L/d^2(t)T_s$ is an approximation of the emulated resistance R_e of the DCM boost rectifier. Ac line current harmonics are not zero, but the rectifier can still be designed to meet harmonic limits. In this section we consider a DCM boost rectifier example and test its performance by simulation.

An averaged circuit model of the boost DCM rectifier is shown in Fig. B.19. Full-wave rectified 120 Vrms, 50 Hz ac line voltage is applied to the input of the boost converter. The converter switches are replaced by the CCM-DCM1 averaged switch subcircuit. It is desired to regulate the dc output voltage at $V = 300$ V at output power up to $P_{out} = 120$ W across the load R . The switching frequency is $f_s = 100$ kHz. Let us select the inductance L so that the converter always operates in DCM. From Eq. (18.24), the condition for DCM is:

$$L < \frac{\left(1 - \frac{V_M}{V}\right)R_e}{2f_s} \quad (\text{B.21})$$

where R_e is the emulated resistance of the rectifier and V_M is the peak of the ac line voltage. When line

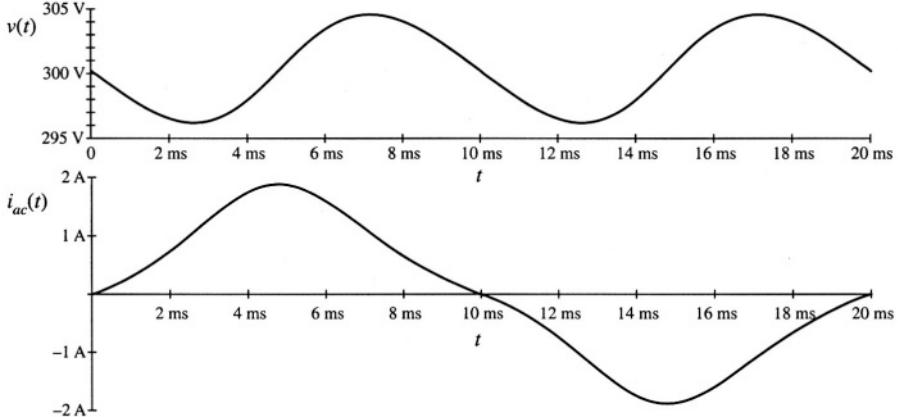


Fig. B.20 Output voltage and ac line current in the DCM boost rectifier example.

current harmonics and losses are neglected, the rectifier emulated resistance R_e at the specified load power P is

$$R_e = \frac{V_M^2}{2P} \quad (\text{B.22})$$

Given $V_M = 170$ V and R_e found from Eq. (B.22), Eq. (B.21) gives $L < 260$ μH . The selected inductance is $L = 200$ μH . A low-bandwidth voltage feedback loop is closed around the converter to regulate the dc output voltage. The output voltage is sensed and compared to the reference v_{ref} . A PI compensator is constructed around the LM324 op-amp. The output $v_{control}$ of the compensator is the input to the pulse-width modulator. By adjusting the switch duty ratio d , $v_{control}$ adjusts the emulated resistance $R_e = 2L/d^2T_s$ of the rectifier, and thereby controls the power taken from the ac line. In steady state, the input power matches the output power. The dc output voltage V is regulated at the value set by the reference voltage v_{ref} and the voltage divider composed of R_1 and R_2 , as follows:

$$V = v_{ref} \frac{R_1 + R_2}{R_1} = 300 \text{ V} \quad (\text{B.23})$$

Modeling of the low-bandwidth voltage regulation loop is discussed in Section 18.4.2.

It is of interest to find ac line current harmonics. First, a long transient simulation is performed to reach steady-state operation. Then, current harmonics are computed using Fourier analysis applied to the ac line current waveform $i_{ac}(t)$ during one line cycle in steady state. Figure B.20 shows the steady-state ac line current and output voltage obtained for $R = 900 \Omega$, i.e., for 100 W of output power. The output voltage has a dc component equal to 300 V, and an ac ripple component at twice the line frequency. The peak-to-peak voltage ripple at twice the line frequency is approximately 8 V, which compares well with the value (7 V) found from Eq. (18.91). The ac line current has noticeable distortion. The spectrum of the ac line current is shown in Fig. B.21. The largest harmonic, the third, has an amplitude of 16.6% of the fundamental, and the total harmonic distortion is 16.7%.

We can also examine what happens if the rectifier is overloaded. The steady-state ac line current waveform for the case when the load resistance is $R = 500 \Omega$, and the output power is 180 W, is shown in

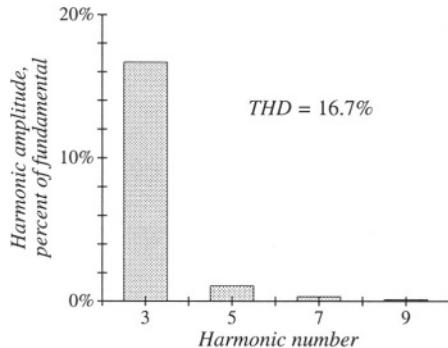


Fig. B.21 Spectrum of the ac line current in the DCM boost rectifier.

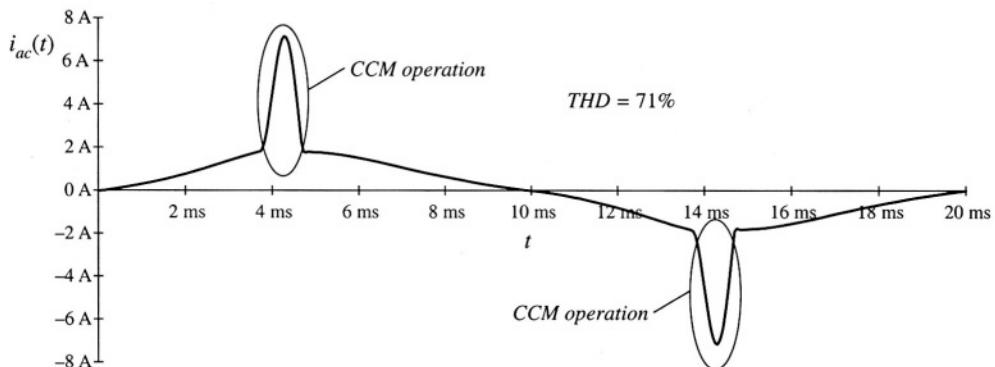


Fig. B.22 Ac line current of the DCM boost rectifier example, when the output is overloaded.

Fig. B.22. The boost converter operates in CCM near the peak of the ac line voltage; this results in current spikes and significant harmonic distortion.

B.3 CURRENT PROGRAMMED CONTROL

In the current programmed mode (CPM), which is studied in Chapter 12, the transistor switching is controlled so that the peak transistor current follows a control signal. The transistor duty cycle $d(t)$ is not directly controlled, but depends on the CPM control input as well as on other converter voltages and currents. In this section, large-signal averaged relationships in CPM are written in a form suitable for implementation as a subcircuit for simulation.

B.3.1 Current Programmed Mode Model for Simulation

Typical inductor current and voltage waveforms of CPM converters operating in continuous conduction mode or in discontinuous conduction mode are shown in Fig. B.23. Signal $i_c(t)$ is the CPM control input. An artificial ramp having slope $-m_a$ is added to the control input. In the first subinterval,

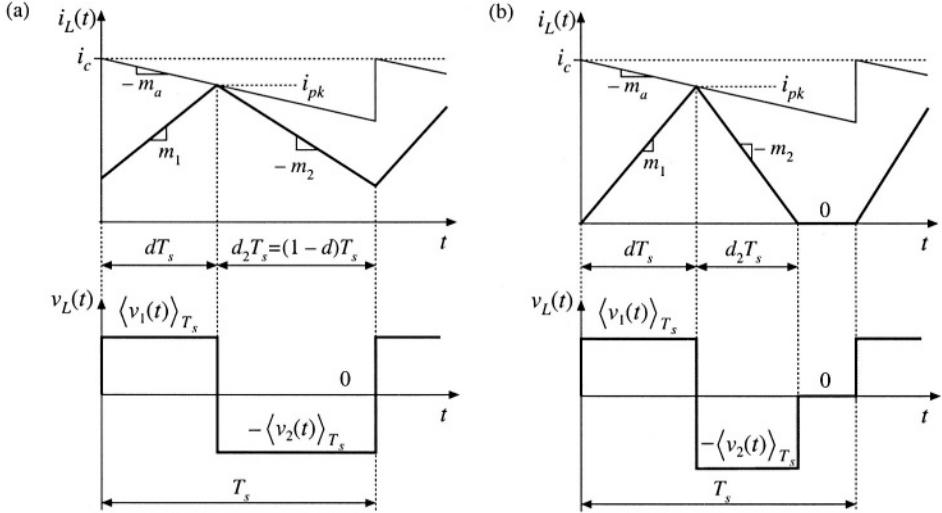


Fig. B.23 Current programmed mode waveforms: (a) continuous conduction mode; (b) discontinuous conduction mode.

when the transistor is on, the inductor current increases with slope m_1 given by:

$$m_1 = \frac{\langle v_1(t) \rangle_{T_s}}{L} \quad (\text{B.24})$$

It is assumed that voltage ripples are small so that the voltage $v_1(t)$ across the inductor is approximately equal to the averaged value $\langle v_1(t) \rangle_{T_s}$. The length of the first subinterval is $d(t)T_s$. The transistor is turned off when the inductor current reaches the peak value i_{pk} equal to:

$$i_{pk} = i_c - m_a d T_s \quad (\text{B.25})$$

In the second subinterval, when the transistor is off and the diode is on, the inductor current decreases with a negative slope $-m_2$. With the assumption the voltage ripples are small, the slope m_2 is given by:

$$m_2 = \frac{\langle v_2(t) \rangle_{T_s}}{L} \quad (\text{B.26})$$

The length of the second subinterval is $d_2(t)T_s$. In CCM, the second subinterval lasts until the end of the switching cycle. Therefore:

$$d_2 = 1 - d \quad (\text{B.27})$$

In DCM, the current drops to zero before the end of the switching period. The length of the second subinterval can be computed from:

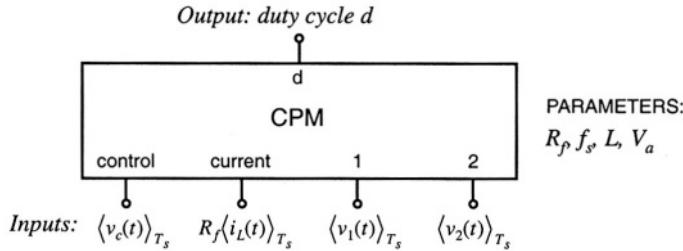


Fig. B.24 Current programmed mode (CPM) subcircuit.

$$d_2 = \frac{i_{pk}}{m_2 T_s} \quad (B.28)$$

If the converter operates in DCM, d_2 computed from Eq. (B.28) is smaller than $1 - d$. If the converter operates in CCM, $1 - d$ is smaller than d_2 computed from Eq. (B.28). In general, the length of the second subinterval can be found as the smaller of the two values computed using Eqs. (B.27) and (B.28).

The average inductor current can be found by computing the area under the inductor current waveform in Fig. B.23:

$$\langle i_L(t) \rangle_{T_s} = d \left(i_{pk} - \frac{m_1 d T_s}{2} \right) + d_2 \left(i_{pk} - \frac{m_2 d_2 T_s}{2} \right) \quad (B.29)$$

The relationship given by Eq. (B.29) is valid for both CCM and DCM provided that the second subinterval length is computed as the smaller of the values obtained from Eqs. (B.27) and (B.28).

Based on Eqs. (B.24) to (B.29), an averaged CPM subcircuit model is constructed in the form shown in Fig. B.24. The inputs to the CPM subcircuit are the control input $\langle v_r(t) \rangle_{T_s} = R_f \langle i_c(t) \rangle_{T_s}$, the measured inductor current $R_f \langle i_L(t) \rangle_{T_s}$, and the inductor voltages $\langle v_1(t) \rangle_{T_s}$ and $\langle v_2(t) \rangle_{T_s}$ of the two subintervals. The output of the subcircuit is the switch duty cycle d . The parameters of the CPM subcircuit are the equivalent current-sense resistance R_f , the inductance L , the switching frequency $f_s = 1/T_s$, and the amplitude V_a of the artificial ramp:

$$V_a = m_a T_s R_f \quad (B.30)$$

In the subcircuit implementation, the length of the second subinterval is computed as the smaller of the values given by Eqs. (B.27) and (B.28):

$$d_2 = \text{MIN} \left(1 - d, \frac{i_{pk}}{m_2 T_s} \right) \quad (B.31)$$

Next, the switch duty cycle is found by solving Eq. (B.29). There are many different ways the switch duty cycle can be expressed in terms of other quantities. Although mathematically equivalent to Eq. (B.29), these different forms of solving for d result in different convergence performance of the numerical solver in the simulator. In the CPM subcircuit available in the *switch.lib* library, the duty cycle is found from:

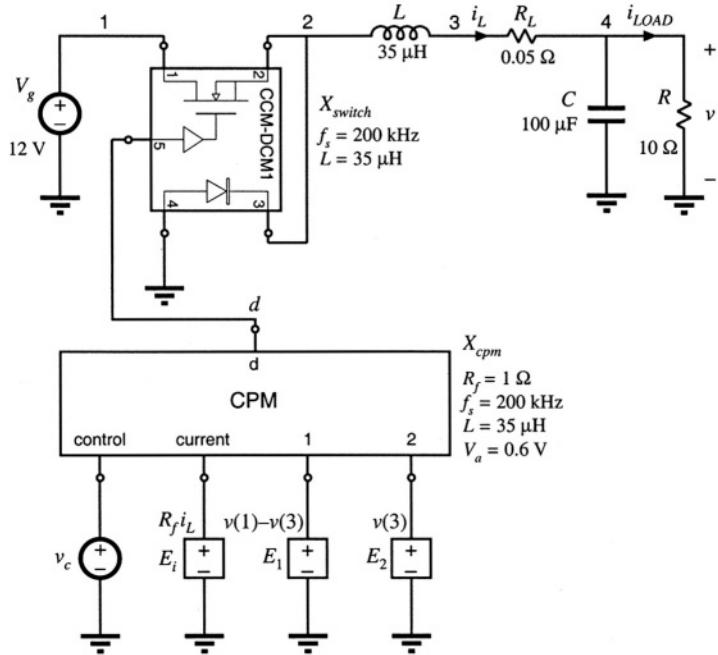


Fig. B.25 CPM buck converter example.

$$d = \frac{2i_c(d + d_2) - 2\langle i_L(t) \rangle_{T_s} - m_2 d^2 T_s}{2m_a(d + d_2)T_s + m_1 d T_s} \quad (\text{B.32})$$

which is obtained by inserting Eq. (B.25) into Eq. (B.29). This implicit expression (notice that d is on both sides of the equation) is used by the numerical solver in the simulator to compute the switch duty cycle d .

B.3.2 Example: Frequency Responses of a Buck Converter with Current Programmed Control

To illustrate an application of the CPM subcircuit, let us consider the example buck converter circuit model of Fig. B.25. To construct this averaged circuit model, the switches are replaced by the CCM-DCM1 averaged switch subcircuit. The control input to the CPM subcircuit is the independent voltage source v_c . Three dependent voltage sources are used to generate other inputs to the CPM subcircuit. The controlled voltage source E_i is proportional to the inductor current i_L . The controlled voltage source E_1 is equal to $v(1) - v(3)$, which is equal to the voltage $\langle v_1(t) \rangle_{T_s}$ applied across the inductor during the first subinterval when the transistor is on and the diode is off. The controlled voltage source E_2 is equal to $v(3)$, which is equal to the voltage $\langle v_2(t) \rangle_{T_s}$ applied across the inductor during the second subinterval when the transistor is off and the diode is on.

Ac simulations are performed at the quiescent operating point obtained for the dc value of the

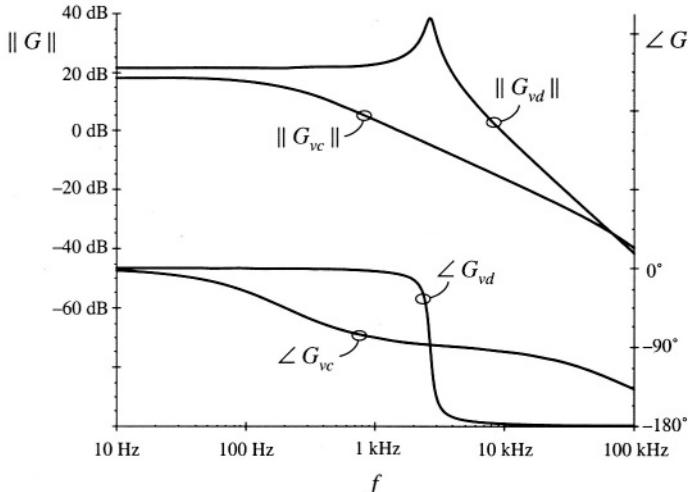


Fig. B.26 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

control input equal to $V_c = 1.4$ V. At the quiescent operating point, the switch duty cycle is $D = 0.676$, the dc output voltage is $V = 8.1$ V, and the dc component of the inductor current is $I_L = 0.81$ A. The converter operates in CCM.

Magnitude and phase responses of the control-to-output transfer functions $G_{vc}(s) = \hat{v}/\hat{v}_c$ and $G_{vd}(s) = \hat{v}/d$ are shown in Fig. B.26. The duty-cycle to output voltage transfer function $G_{vd}(s)$ exhibits the familiar second-order high-Q response. Peaking in the magnitude response and a steep change in phase from 0° to -180° occur around the center frequency of the pair of complex-conjugate poles. In contrast, the CPM control-to-output response has a dominant low-frequency pole. The phase lag is around -90° in a wide range of frequencies. A high frequency pole contributes to additional phase lag at higher frequencies. The frequency responses of Fig. B.26 illustrate an advantage of CPM control over duty-cycle control. Because of the control-to-output frequency response dominated by the single low-frequency pole, it can be much easier to close a wide-bandwidth outer voltage feedback loop around the CPM controlled power converter than around a converter where the duty cycle is the control input.

Another advantage of CPM control is in rejection of input voltage disturbances. Line-to-output frequency responses for duty-cycle control and CPM control in the buck example are compared in Fig. B.27. At practically all frequencies of interest, CPM control offers more than 30 dB better attenuation of input voltage disturbances.

It is also interesting to compare the output impedance of the converter with duty-cycle control versus CPM control. The results are shown in Fig. B.28. At low frequencies, duty-cycle controlled converter has very low output impedance determined by switch and inductor resistances. As the frequency goes up, the output impedance increases as the impedance of the inductor increases. At the resonant frequency of the output LC filter, significant peaking in the output impedance of the duty-cycle controlled converter can be observed. At higher frequencies, the output impedance is dominated by the impedance of the filter capacitor, which decreases with frequency. In the CPM controlled converter, the low-frequency impedance is high. It is equal to the parallel combination of the load resistance and the CPM out-

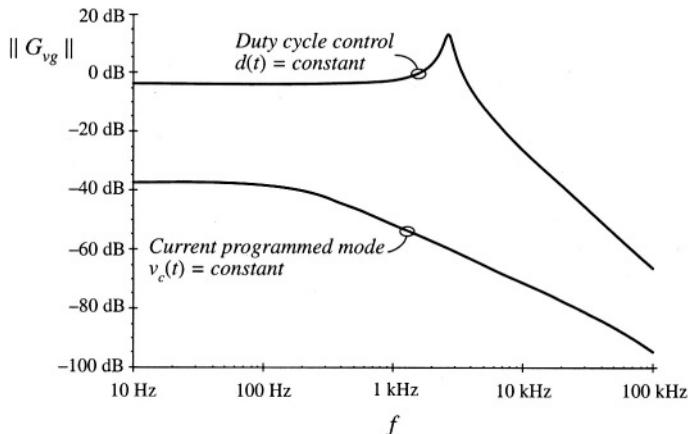


Fig. B.27 Comparison of CPM control with duty-cycle control, for the line-to-output frequency response of the buck converter example.

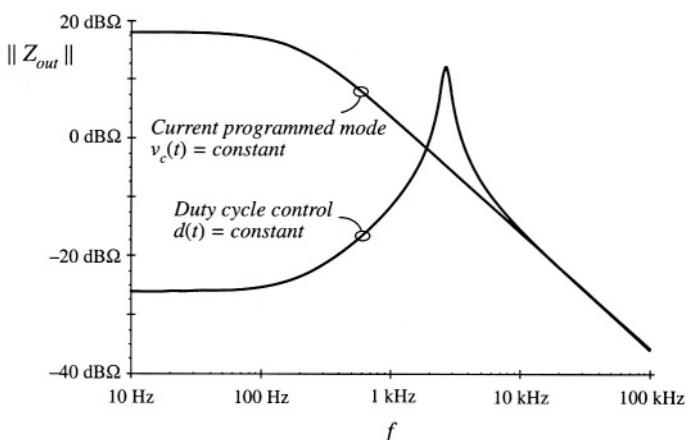


Fig. B.28 Comparison of CPM control with duty-cycle control, for the output impedance of the buck converter example.

put resistance. Because of the lossless damping introduced by CPM control, the series inductor does not affect the output impedance. As the frequency goes up, the output impedance becomes dominated by the output filter capacitor and it decreases with frequency. At high frequencies the output impedances of the duty-cycle and CPM controlled converters have the same asymptotes.

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Appendix C

Middlebrook's Extra Element Theorem

The *Extra Element Theorem* of R. D. Middlebrook [1–3] shows how a transfer function is changed by the addition of an impedance to the network. The theorem allows one to determine the effects of this extra element on any transfer function of interest, without solving the system all over again. The Extra Element Theorem is a powerful technique of design-oriented analysis. It leads to impedance inequalities which guarantee that an element does not substantially alter a transfer function. The Extra Element Theorem is employed in Chapter 10, where it leads to a relatively simple methodology for designing input filters that do not degrade the loop gains of switching regulators. It is also employed in Section 19.4, to determine how the load resistance affects the properties of a resonant inverter. In this appendix, Middlebrook's Extra Element Theorem is derived, based on the principle of superposition. Its application is illustrated via examples.

C.1 BASIC RESULT

Consider the linear circuit of Fig. C.1(a). This network contains an input $v_{in}(s)$ and an output $v_{out}(s)$. In addition, it contains a port whose terminals are open-circuited. It is assumed that the transfer function from $v_{in}(s)$ to $v_{out}(s)$ is known, and is given by

$$\frac{v_{out}(s)}{v_{in}(s)} = G(s) \Big|_{Z(s) \rightarrow \infty} \quad (\text{C.1})$$

The Extra Element Theorem tells us how the transfer function $G(s)$ is modified when an impedance $Z(s)$ is connected between the terminals at the port, as in Fig. C.1(b). The result is

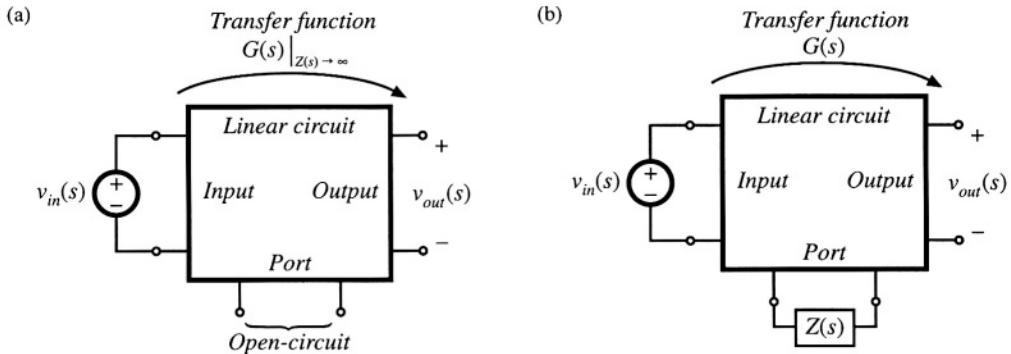


Fig. C.1 How an added element changes a transfer function $G(s)$: (a) original conditions, before addition of the new element; (b) addition of element having impedance $Z(s)$.

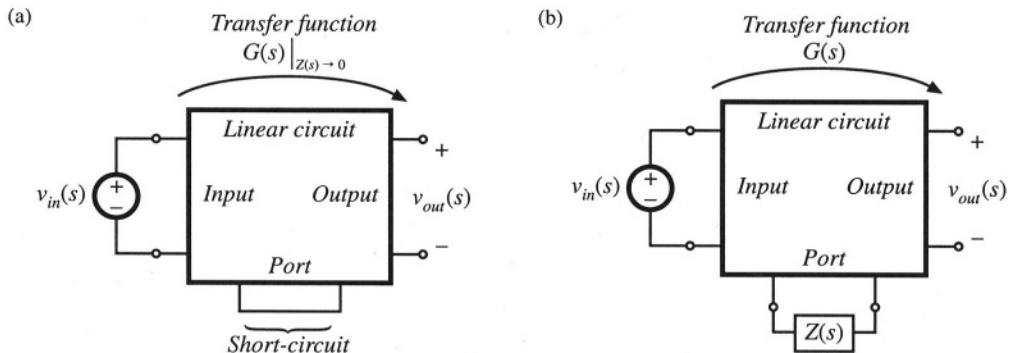


Fig. C.2 The dual form of the Extra Element Theorem, in which the extra element replaces a short circuit: (a) original conditions, (b) addition of element having impedance $Z(s)$.

$$\frac{v_{out}(s)}{v_{in}(s)} = \left(G(s) \Big|_{Z(s) \rightarrow \infty} \right) \left(\frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (\text{C.2})$$

The right-hand side terms involving $Z(s)$ account for the influence of $Z(s)$ on $G(s)$, and are known as the *correction factor*.

The Extra Element Theorem also applies to the dual form illustrated in Fig. C.2. In this form, the transfer function is initially known under the conditions that the port is short-circuited. In Fig. C.2(b), the short-circuit is replaced by the impedance $Z(s)$. In this case, the addition of the impedance $Z(s)$ causes the transfer function to become

$$\frac{v_{out}(s)}{v_{in}(s)} = \left(G(s) \Big|_{Z(s) \rightarrow 0} \right) \left(\frac{1 + \frac{Z(s)}{Z_N(s)}}{1 + \frac{Z(s)}{Z_D(s)}} \right) \quad (\text{C.3})$$

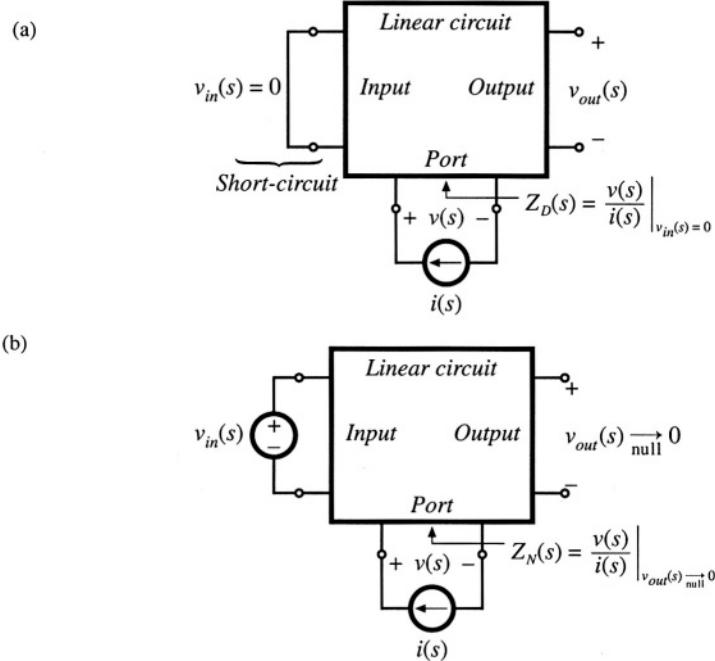


Fig. C.3 Determination of the quantities $Z_N(s)$ and $Z_D(s)$: (a) $Z_D(s)$ is the Thevenin-equivalent impedance at the port, and is measured with the input $v_{in}(s)$ set to zero; (b) $Z_N(s)$ is the impedance seen at the port under the condition that the output is nulled.

The $Z_N(s)$ and $Z_D(s)$ terms in Eqs. (C.2) and (C.3) are identical. By equating the $G(s)$ expressions of Eqs. (C.2) and (C.3), one can show that

$$\frac{G(s)|_{Z(s) \rightarrow \infty}}{G(s)|_{Z(s) \rightarrow 0}} = \frac{Z_D(s)}{Z_N(s)} \quad (\text{C.4})$$

This is known as the *reciprocity relationship*.

The quantities $Z_N(s)$ and $Z_D(s)$ can be found by measuring impedances at the port. The term $Z_D(s)$ is the Thevenin equivalent impedance seen looking into the port, also known as the driving-point impedance. As illustrated in Fig. C.3(a), this impedance is found by setting the independent source $v_{in}(s)$ to zero, and then measuring the impedance between the terminals of the port:

$$Z_D(s) = \frac{v(s)}{i(s)} \Big|_{v_{in}(s) = 0} \quad (\text{C.5})$$

Thus, $Z_D(s)$ is the impedance between the port terminals when the input $v_{in}(s)$ is set to zero.

Determination of the impedance $Z_N(s)$ is illustrated in Fig. C.3(b). The term $Z_N(s)$ is found under the conditions that the output $v_{out}(s)$ is nulled to zero. A current source $i(s)$ is connected to the terminals of the port. In the presence of the input signal $v_{in}(s)$, the current $i(s)$ is adjusted so that the output $v_{out}(s)$ is nulled to zero. Under these conditions, the quantity $Z_N(s)$ is given by

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{v_{out}(s) \rightarrow 0} \quad (C.6)$$

Note that *nulling* the output is not the same as *shorting* the output. If one simply shorted the output, then a current would flow through the short, which would induce voltage drops and currents in other elements of the network. These voltage drops and currents are not present when the output is nulled. The null condition of Fig. C.3(b) does not employ any connections to the output of the circuit. Rather, the null condition employs the adjustment of the independent sources $v_{in}(s)$ and $i(s)$ in a special way that causes the output $v_{out}(s)$ to be zero. By superposition, $v_{out}(s)$ can be expressed as a linear combination of $v_{in}(s)$ and $i(s)$; therefore, for a given $v_{in}(s)$, it is always possible to choose an $i(s)$ that will cause $v_{out}(s)$ to be zero. Under these null conditions, $Z_N(s)$ is measured as the ratio of $v(s)$ to $i(s)$. In practice, the circuit analysis to find $Z_N(s)$ is simpler than analysis of $Z_D(s)$, because the null condition causes many of the signals within the circuit to be zero. Several examples are given in Section C.4.

The input and output quantities need not be voltages, but could also be currents or other signals that can be set or nulled to zero. The next section contains a derivation of the Extra Element Theorem with a general input $u(s)$ and output $y(s)$.

C.2 DERIVATION

Figure C.4(a) illustrates a general linear system having an input $u(s)$ and an output $y(s)$. In addition, the system contains an electrical port having voltage $v(s)$ and current $i(s)$, with the polarities illustrated. Initially, the port is open-circuited: $i(s) = 0$. The transfer function of this system, with the port open-circuited, is

$$G_{old}(s) = \left. \frac{y(s)}{u(s)} \right|_{i(s)=0} \quad (C.7)$$

The objective of the extra element theorem is to determine the new transfer function $G(s)$ that is obtained when an impedance $Z(s)$ is connected to the port:

$$G(s) = \frac{y(s)}{u(s)} \quad (C.8)$$

The situation is illustrated in Fig. C.4(b). It can be seen that the conditions at the port are now given by

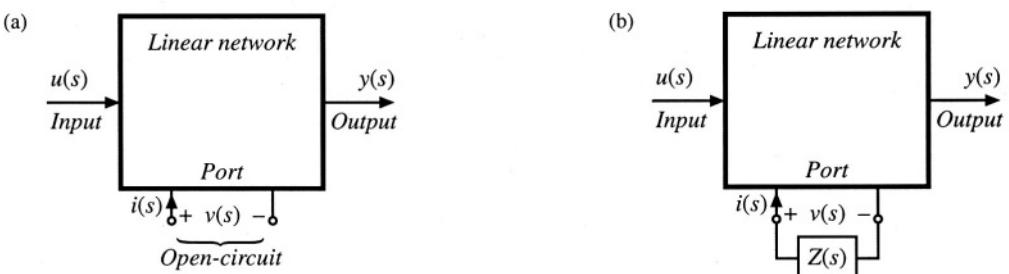


Fig. C.4 Modification of a linear network by addition of an extra element: (a) original system, (b) modified system, with impedance $Z(s)$ connected at an electrical port.

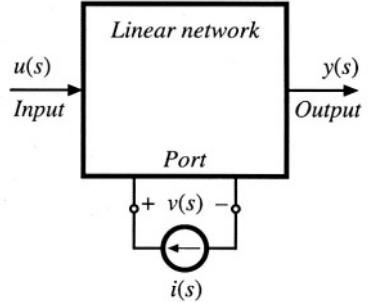


Fig. C.5 Current injection at the electrical port, by addition of independent current source $i(s)$.

$$v(s) = -i(s)Z(s) \quad (\text{C.9})$$

To express the new transfer function $G(s)$ in Eq. (C.8) in terms of the original transfer function $G_{old}(s)$ of Eq. (C.7), we use current injection at the port, as illustrated in Fig. C.5. There are now two independent inputs: the input $u(s)$ and the independent current source $i(s)$. The dependent quantities $y(s)$ and $v(s)$ can be expressed as functions of these independent inputs using the principle of superposition:

$$y(s) = G_{old}(s)u(s) + G_i(s)i(s) \quad (\text{C.10})$$

$$v(s) = G_v(s)u(s) + Z_D(s)i(s) \quad (\text{C.11})$$

where

$$G_{old}(s) = \frac{y(s)}{u(s)} \Big|_{i(s)=0} \quad (\text{C.12})$$

$$G_i(s) = \frac{y(s)}{i(s)} \Big|_{u(s)=0} \quad (\text{C.13})$$

$$Z_D(s) = \frac{v(s)}{i(s)} \Big|_{u(s)=0} \quad (\text{C.14})$$

$$G_v(s) = \frac{v(s)}{u(s)} \Big|_{i(s)=0} \quad (\text{C.15})$$

are the transfer functions from the independent inputs to the respective dependent quantities $y(s)$ and $v(s)$.

The transfer function $G(s)$ can be found by elimination of $v(s)$ and $i(s)$ from the system of equations (C.9) to (C.11), and solution for $y(s)$ as a function of $u(s)$. The result is

$$G(s) = \frac{y(s)}{u(s)} = G_{old}(s) - \frac{G_v(s)G_i(s)}{Z(s) + Z_D(s)} \quad (\text{C.16})$$

This intermediate result expresses the new transfer function $G(s)$ as a function of the original transfer function $G_{old}(s)$ and the extra element $Z(s)$, as well as the quantities $Z_D(s)$, $G_v(s)$, and $G_i(s)$.

Equation (C.14) gives a direct way to find the quantity $Z_D(s)$. $Z_D(s)$ is the driving-point impedance at the port, when the input $u(s)$ is set to zero. This quantity can be found either by conventional circuit analysis or simulation, or by laboratory measurement.

Although $G_v(s)$ and $G_i(s)$ could also be determined from the definitions (C.13) and (C.15), it is preferable to eliminate these quantities, and instead express $G(s)$ as a function of the impedances at the given port. This can be accomplished via the following thought experiment. In the presence of the input $u(s)$, we adjust the independent current source $i(s)$ in the special way that causes the output $y(s)$ to be nulled to zero. The impedance $Z_N(s)$ is defined as the ratio of $v(s)$ to $i(s)$ under these null conditions:

$$Z_N(s) = \frac{v(s)}{i(s)} \Big|_{y(s) \xrightarrow{\text{null}} 0} \quad (\text{C.17})$$

The value of $i(s)$ that achieves the null condition $y(s) \xrightarrow{\text{null}} 0$ can be found by setting $y(s) = 0$ in Eq. (C.10), as follows:

$$\left[G_{old}(s)u(s) + G_i(s)i(s) \right] \xrightarrow{\text{null}} 0 \quad (\text{C.18})$$

Hence, the output $y(s)$ is nulled when the inputs $u(s)$ and $i(s)$ are related as follows:

$$u(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} = -\frac{G_i(s)}{G_{old}(s)} i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \quad (\text{C.19})$$

Under this null condition, the voltage $v(s)$ is given by

$$\begin{aligned} v(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} &= G_v(s) u(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} + Z_D(s) i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \\ &= \left(-\frac{G_v(s)G_i(s)}{G_{old}(s)} + Z_D(s) \right) i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \end{aligned} \quad (\text{C.20})$$

which follows from Eqs. (C.11) and (C.19). Substitution of Eq. (C.17) into Eq. (C.20) yields

$$v(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} = Z_N(s) i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} = \left(-\frac{G_v(s)G_i(s)}{G_{old}(s)} + Z_D(s) \right) i(s) \Big|_{y(s) \xrightarrow{\text{null}} 0} \quad (\text{C.21})$$

Hence,

$$Z_N(s) = Z_D(s) - \frac{G_v(s)G_i(s)}{G_{old}(s)} \quad (\text{C.22})$$

Solution for the quantity $G_v(s)G_i(s)$ yields

$$G_v(s)G_i(s) = (Z_D(s) - Z_N(s))G_{old}(s) \quad (\text{C.23})$$

Thus, the unknown quantities $G_v(s)$ and $G_i(s)$ can be related to $Z_N(s)$ and $Z_D(s)$, which are properties of the port at which the new impedance $Z(s)$ will be connected, and to the original transfer function $G_{old}(s)$.

The final step is to substitute Eq. (C.23) into Eq. (C.16), leading to

$$G(s) = G_{old}(s) - \frac{Z_D(s) - Z_N(s)}{Z(s) + Z_D(s)} G_{old}(s) \quad (C.24)$$

This expression can be simplified as follows:

$$G(s) = G_{old}(s) \frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \quad (C.25)$$

or,

$$G(s) = \left(G(s) \Big|_{Z(s) \rightarrow \infty} \right) \left(\frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (C.26)$$

This is the desired result. It states how the transfer function $G(s)$ is modified by addition of the extra element $Z(s)$. The right-most term in Eq. (C.26) is called the *correction factor*; this term gives a quantitative measure of the change in $G(s)$ arising from the introduction of $Z(s)$.

Derivation of the dual result, Eq. (C.3), follows similar steps.

C.3 DISCUSSION

The general form of the extra element theorem makes it useful for designing a system such that unwanted circuit elements do not degrade the desirable system performance already obtained. For example, suppose that we already know some transfer function or similar quantity $G(s)$, under simplified or ideal conditions, and have designed the system such that this quantity meets specifications. We can then use the extra element theorem to answer the following questions:

What is the effect of a parasitic element $Z(s)$ that was not included in the original analysis?

What happens if we later decide to add some additional components having impedance $Z(s)$ to the system?

Can we establish some conditions on $Z(s)$ that ensure that $G(s)$ is not substantially changed?

A common application of the extra element theorem is the determination of conditions on the extra element that guarantee that the transfer function $G(s)$ is not significantly altered. According to Eqs. (C.2) and (C.26), this will occur when the correction factor is approximately equal to unity. The conditions are:

$$\begin{cases} \|Z(j\omega)\| \gg \|Z_N(j\omega)\| \\ \|Z(j\omega)\| \gg \|Z_D(j\omega)\| \end{cases} \quad (C.27)$$

This gives a formal way to show when an impedance can be ignored: one can plot the impedances $\|Z_N(j\omega)\|$ and $\|Z_D(j\omega)\|$, and compare the results with a plot of $\|Z(j\omega)\|$. The impedance $Z(s)$ can be ignored over the range of frequencies where the inequalities (C.27) are satisfied.

For the dual case in which the new impedance is inserted where there was previously a short circuit, Eq. (C.3), the inequalities are reversed:

$$\begin{aligned} \|Z(j\omega)\| &\ll \|Z_N(j\omega)\| \\ \|Z(j\omega)\| &\ll \|Z_D(j\omega)\| \end{aligned} \quad (C.28)$$

This equation shows how to limit the magnitude $\|Z(j\omega)\|$, to avoid significantly changing the transfer function $G(s)$.

For quantitative design, Eqs. (C.27) and (C.28) raise an additional question: By what factor should $\|Z(j\omega)\|$ exceed (or be less than) $\|Z_N(j\omega)\|$ and $\|Z_D(j\omega)\|$, in order for the inequalities of Eq. (C.27) or (C.28) to be well satisfied? This question can be answered by plotting the magnitudes and phases of the correction factor terms, as a function of the magnitudes and phases of (Z/Z_N) and (Z/Z_D) .

Figure C.6 shows contours of constant $\|1 + Z/Z_N\|$, as a function of the magnitude and phase of Z/Z_N . Figure C.7 shows similar contours of constant $\angle(1 + Z/Z_N)$. It can be seen that, when $\|Z/Z_N\|$ is less than -20 dB, then the maximum deviation caused by the numerator $(1 + Z/Z_N)$ term is less than ± 1 dB in magnitude, and less than $\pm 7^\circ$ in phase. For $\|Z/Z_N\|$ less than -10 dB, the maximum deviation caused by the numerator $(1 + Z/Z_N)$ term is less than ± 3.5 dB in magnitude, and less than $\pm 20^\circ$ in phase.

Figures C.8 and C.9 contain contours of constant $\|1/(1 + Z/Z_D)\|$ and $\angle 1/(1 + Z/Z_D)$, respectively, as a function of the magnitude and phase of Z/Z_D . These plots contain minus signs because the terms appear in the denominator of the correction factor; otherwise, they are identical to Figs. C.6 and C.7. Again, for $\|Z/Z_D\|$ less than -20 dB, the maximum deviation caused by the denominator $(1 + Z/Z_D)$ term is less than ± 1 dB in magnitude, and less than $\pm 7^\circ$ in phase. For $\|Z/Z_D\|$ less than -10 dB, the maximum deviation caused by the denominator $(1 + Z/Z_D)$ term is less than ± 3.5 dB in magnitude, and less than $\pm 20^\circ$ in phase.

C.4 EXAMPLES

C.4.1 A Simple Transfer Function

The first example illustrates how the Extra Element Theorem can be used to find a transfer function essentially by inspection. We are given the circuit illustrated in Fig. C.10. It is desired to solve for the transfer function

$$G(s) = \frac{v_2(s)}{v_1(s)} \quad (C.29)$$

and to express this transfer function in factored pole-zero form. One way to do this is to employ the Extra Element Theorem, treating the capacitor C as an “extra” element. As illustrated in Fig. C.11, the electrical port is taken to be at the location of the capacitor, and the “original conditions” are taken to be the case when the capacitor impedance is infinite, i.e., an open circuit. Under these original conditions, the transfer function is given by the voltage divider composed of resistors R_1, R_3 , and R_4 . Hence, $G(s)$ can be expressed as

$$\frac{v_2(s)}{v_1(s)} = G(s) = \left(\frac{R_4}{R_1 + R_3 + R_4} \right) \frac{\left(1 + \frac{Z_N}{Z} \right)}{\left(1 + \frac{Z_D}{Z} \right)} \quad (C.30)$$

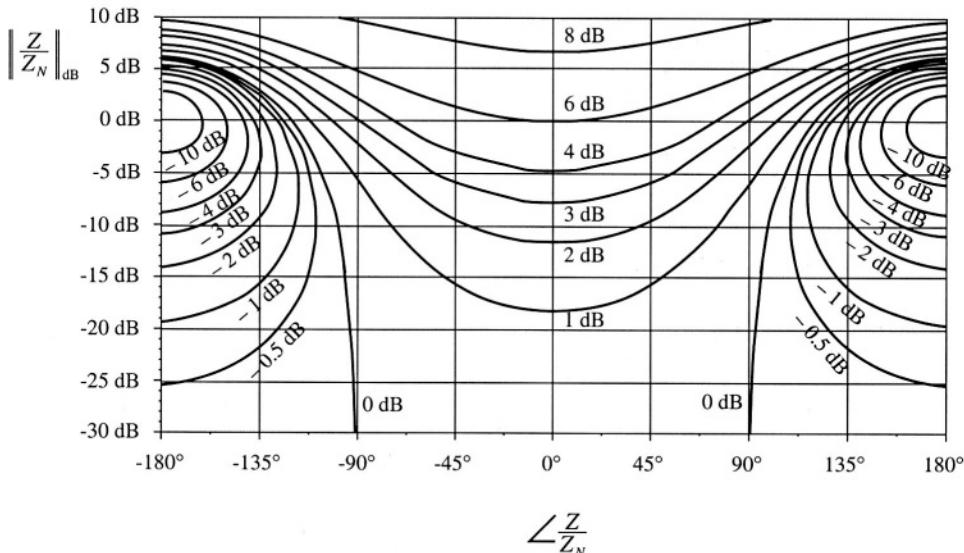


Fig. C.6 Contours of constant $\|1 + Z/Z_N\|$, as a function of the magnitude and phase of Z/Z_N .

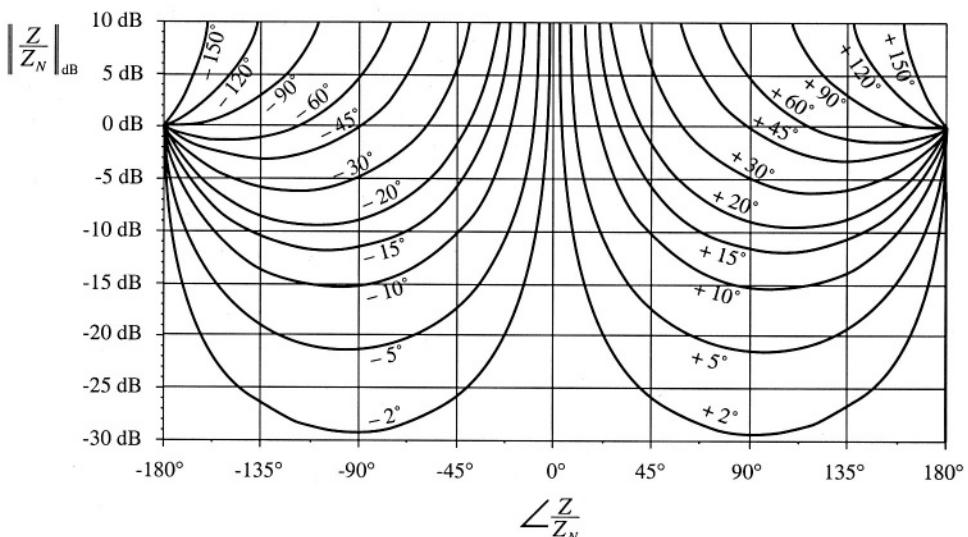


Fig. C.7 Contours of constant $\angle(1 + Z/Z_N)$, as a function of the magnitude and phase of Z/Z_N .

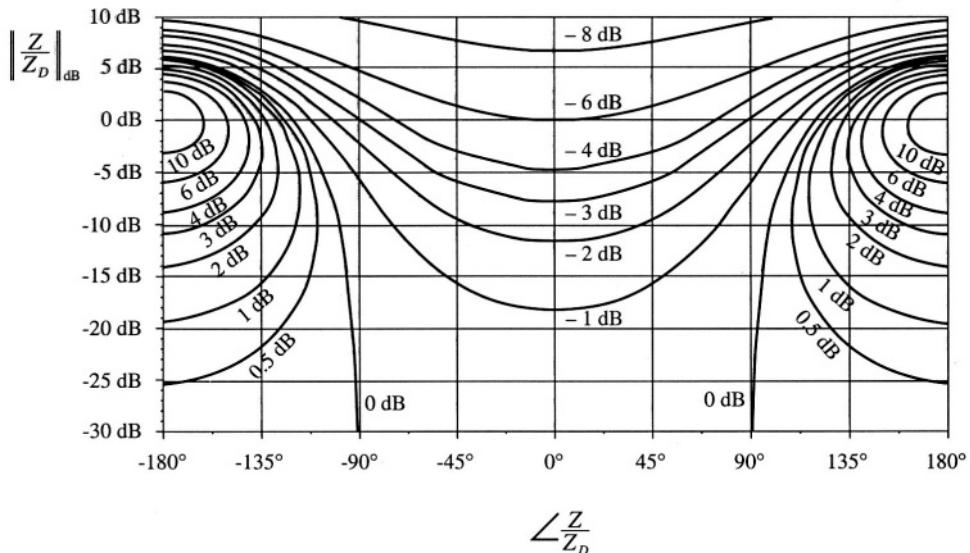


Fig. C.8 Contours of constant $\left\| 1/(1 + Z/Z_D) \right\|$, as a function of the magnitude and phase of Z/Z_D

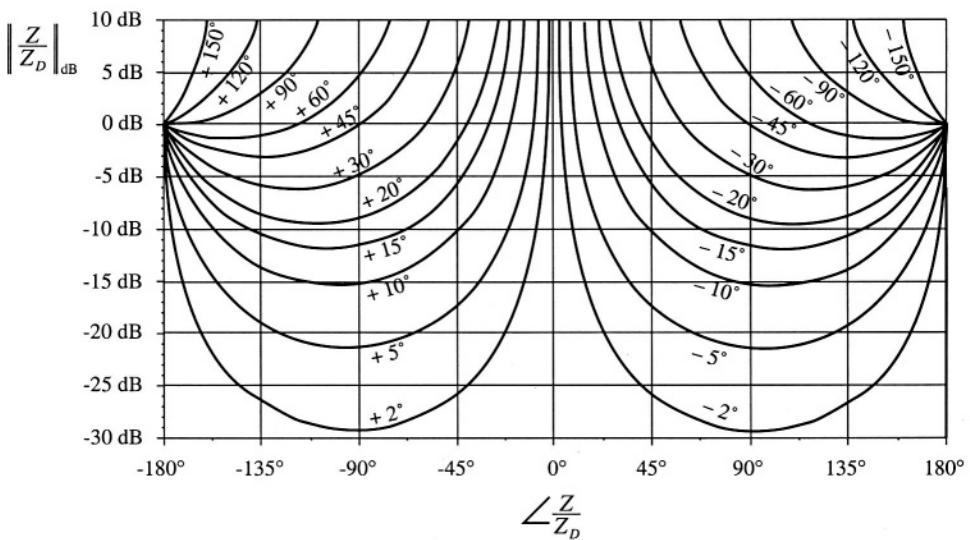


Fig. C.9 Contours of constant $\angle 1/(1 + Z/Z_D)$, as a function of the magnitude and phase of Z/Z_D

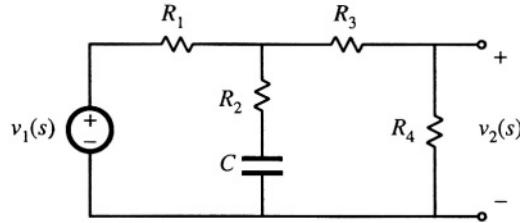


Fig. C.10 R-C circuit example of Section C.4.1.

where $Z(s)$ is the capacitor impedance $1/sC$.

The impedance $Z_D(s)$ is the Thevenin equivalent impedance seen at the port where the capacitor is connected. As illustrated in Fig. C.12(a), this impedance is found by setting the independent source $v_1(s)$ to zero, and then determining the impedance between the port terminals. The result is:

$$Z_D = R_2 + R_1 \parallel (R_3 + R_4) \quad (\text{C.31})$$

Figure C.12(b) illustrates determination of the impedance $Z_N(s)$. A current source $i(s)$ is connected to the port, in place of the capacitor. In the presence of the input $v_1(s)$, the current source $i(s)$ is adjusted so that the output $v_2(s)$ is nulled. Under these null conditions, the impedance $Z_N(s)$ is found as the ratio of $v(s)$ to $i(s)$.

It is easiest to find $Z_N(s)$ by first determining the effect of the null condition on the signals in the circuit. Since v_2 is nulled to zero, there is no current through the resistor R_4 . Since R_3 is connected in series with R_4 , there is also no current through R_3 , and hence no voltage across R_3 . Therefore, the voltage v_3 in Fig. C.12(b) is equal to v_2 , i.e.,

$$v_3 = v_2 \xrightarrow{\text{null}} 0 \quad (\text{C.32})$$

Therefore, the voltage v is given by iR_2 . The impedance Z_N is

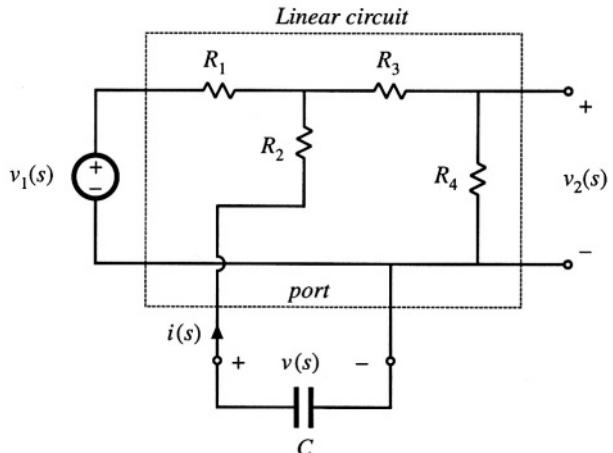


Fig. C.11 Manipulation of the circuit of Fig. C.10 into the form of Fig. C.1.

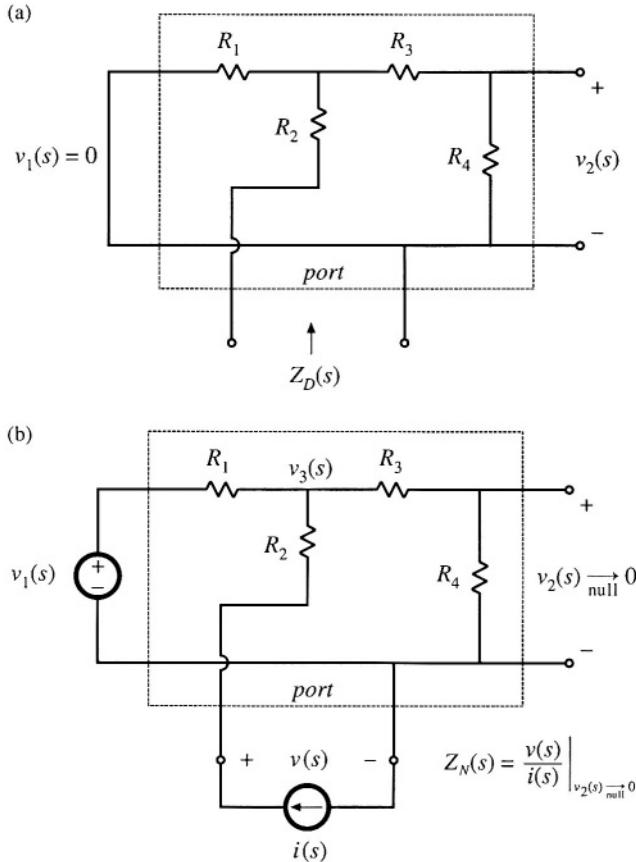


Fig. C.12 Measurement of the quantities $Z_N(s)$ and $Z_D(s)$: (a) determination of $Z_D(s)$, (b) determination of $Z_N(s)$

$$Z_N(s) = \frac{v(s)}{i(s)} \Big|_{v_2(s) \xrightarrow{=} 0} = R_2 \quad (C.33)$$

Note that, in general, the independent sources v_1 and i are nonzero during the Z_N measurement. For this example, the null condition implies that the current $i(s)$ flows entirely through the path composed of R_2 , R_1 , and v_1 .

The transfer function $G(s)$ is found by substitution of Eqs. (C.31) and (C.33) into Eq. (C.30):

$$G(s) = \left(\frac{R_4}{R_1 + R_3 + R_4} \right) \frac{(1 + sCR_2)}{\left(1 + sC \left[R_2 + R_1 \parallel (R_3 + R_4) \right] \right)} \quad (C.34)$$

For this example, the result is obtained in standard normalized pole-zero form, because the capacitor is the only dynamic element in the circuit, and because the “original conditions,” in which the capacitor impedance tends to an open circuit, coincide with dc conditions in the circuit. A similar procedure can be

applied to write the transfer function of a circuit, containing an arbitrary number of reactive elements, in normalized form via an extension of the Extra Element Theorem [3].

C.4.2 An Unmodeled Element

We are told that the transformer-isolated parallel resonant inverter of Fig. C.13 has been designed with the assumption that the transformer is ideal. The approximate sinusoidal analysis techniques of Chapter 19 were employed to model the inverter. It is now desired to specify a transformer; this requires that limits be specified on the minimum allowable transformer magnetizing inductance. One way to approach this problem is to view the transformer magnetizing inductance as an extra element, and to derive conditions that guarantee that the presence of the transformer magnetizing inductance does not significantly change the tank network transfer function $G(s)$.

Figure C.14 illustrates the equivalent circuit model of the inverter, derived using the approximate sinusoidal analysis technique of Section 19.1. The switch network output voltage $v_s(t)$ is modeled by its fundamental component $v_{s1}(t)$, a sinusoid. The tank transfer function $G(s)$ is given by:

$$G(s) = \frac{v_o(s)}{v_{s1}(s)} \quad (\text{C.35})$$

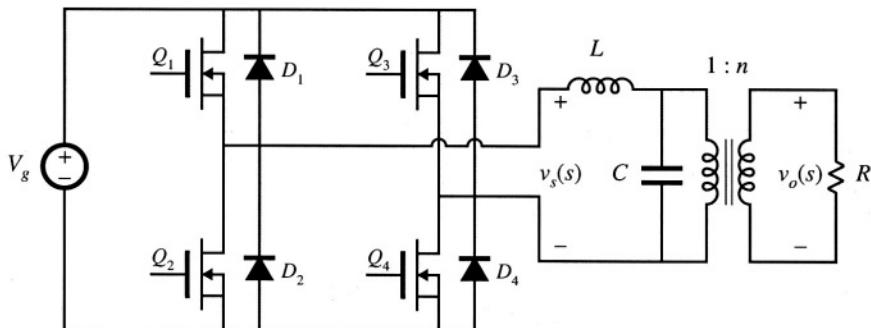


Fig. C.13 Parallel resonant inverter example.

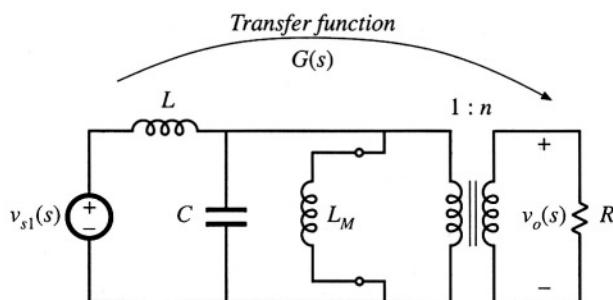


Fig. C.14 Equivalent circuit model of the tank network, based on the approximate sinusoidal analysis technique.

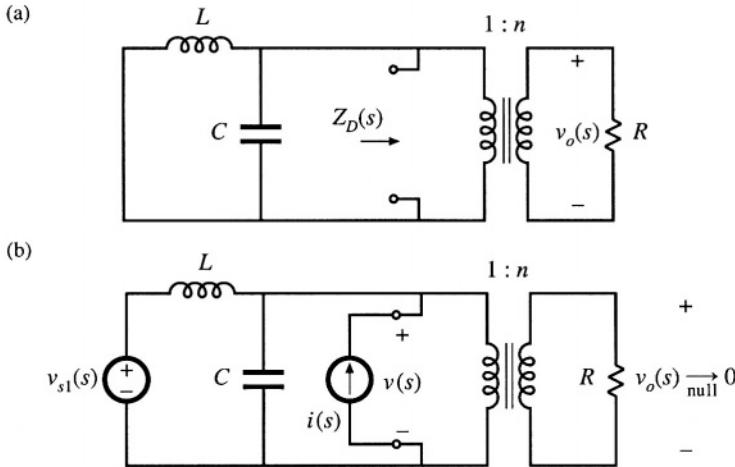


Fig. C.15 Measurement of $Z_N(s)$ and $Z_D(s)$: (a) determination of $Z_D(s)$, (b) determination of $Z_N(s)$.

Under the conditions that the transformer is ideal (i.e., the transformer magnetizing inductance L_M is open circuited), then the transfer function is given by:

$$G(s)\Big|_{L_M \rightarrow \infty} = \frac{n}{1 + s \frac{n^2 L}{R} + s^2 LC} \quad (\text{C.36})$$

We can therefore employ the extra element theorem to determine how finite magnetizing inductance changes $G(s)$. With reference to Fig. C.1, the system input is $v_{s1}(s)$, the output is the voltage $v_o(s)$, and the “port” is the primary winding of the transformer, where the magnetizing inductance is connected. In the presence of the magnetizing inductance, the transfer function becomes

$$G(s) = \left(G(s)\Big|_{L_M \rightarrow \infty} \right) \frac{\left(1 + \frac{Z_N(s)}{Z(s)} \right)}{\left(1 + \frac{Z_D(s)}{Z(s)} \right)} \quad (\text{C.37})$$

where $Z(s)$ is the impedance of the magnetizing inductance referred to the primary winding, sL_M .

Figure C.15(a) illustrates determination of $Z_D(s)$. The input source $v_{s1}(s)$ is set to zero, and the impedance between the terminals of the port is found. It can be seen that the impedance $Z_D(s)$ is the parallel combination of the impedances of the tank inductor, tank capacitor, and the reflected load resistance:

$$Z_D(s) = \frac{R}{n^2} \parallel sL \parallel \frac{1}{sC} \quad (\text{C.38})$$

Figure C.15(b) illustrates determination of $Z_N(s)$. In the presence of the input source $v_{s1}(s)$, a current $i(s)$ is injected at the port as shown. This current is adjusted such that the output $v_o(s)$ is nulled. Under these conditions, the quantity $Z_N(s)$ is given by $v(s)/i(s)$. It can be seen that nulling $v_o(s)$ also nulls the voltage $v(s)$. Therefore,

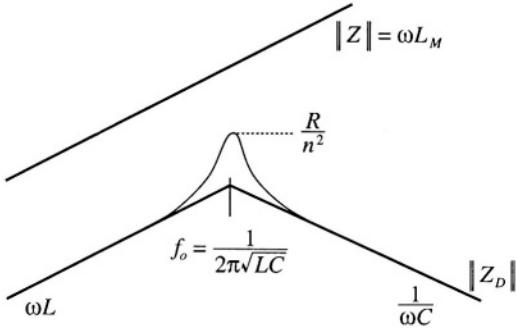


Fig. C.16 To avoid significantly changing the transfer function $G(s)$, the transformer should be designed such that $\| Z \| \gg \| Z_D \|$.

$$Z_N(s) = \frac{v(s)}{i(s)} \Big|_{v_o(s) \rightarrow 0} = 0 \quad (C.39)$$

Note that, in general, $i(s)$ will not be equal to zero during the $Z_N(s)$ measurement. The null condition is achieved by setting the source $i(s)$ equal to the value $-v_{s1}(s)/sL$. Thus, in the presence of finite magnetizing inductance, the transfer function $G(s)$ can be expressed as follows:

$$G(s) = \left(G(s) \Big|_{L_M \rightarrow \infty} \right) \frac{\left(1 + \frac{0}{Z(s)} \right)}{\left(1 + \frac{Z_D(s)}{Z(s)} \right)} = \frac{\left(G(s) \Big|_{L_M \rightarrow \infty} \right)}{\left(1 + \frac{Z_D(s)}{Z(s)} \right)} \quad (C.40)$$

We can now plot the impedance inequalities (C.27) that guarantee that the magnetizing inductance does not substantially modify $G(s)$. The $Z_D(s)$ given in Eq. (C.38) is the impedance of a parallel resonant circuit. Construction of the magnitude of this impedance is described in Section 8.3.4, with results illustrated in Fig. C.16. To avoid affecting the transfer function $G(s)$, the impedance of the magnetizing inductance must be much greater than $\| Z_D(j\omega) \|$ over the range of expected operating frequencies. It can be seen that this will indeed be the case provided that the impedance of the magnetizing inductance is greater than the impedances of both the tank inductance and the reflected load impedance:

$$\begin{aligned} L_M &\gg L, \text{ and} \\ \omega_0 L_M &\gg \frac{R}{n^2} \end{aligned} \quad (C.41)$$

where $\omega_0 = 1/(\sqrt{LC})$. These conditions can be further reduced to

$$\begin{aligned} L_M &\gg L, \text{ and} \\ L_M &\gg \frac{R}{n^2} \sqrt{LC} \end{aligned} \quad (C.42)$$

C.4.3 Addition of an Input Filter to a Converter

As discussed in Chapter 10, the addition of an input filter to a switching regulator can significantly alter its loop gain $T(s)$. Hence, it is desirable to design the input filter so that it does not substantially change

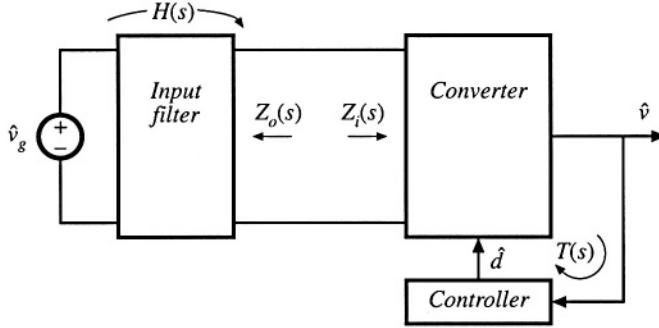


Fig. C.17 Addition of an input filter to a switching voltage regulator system.

the converter control-to-output transfer function $G_{vd}(s)$. The Extra Element Theorem can provide design criteria that show how to design such an input filter.

Figure C.17 illustrates the addition of an input filter to a switching voltage regulator system. The control-to-output transfer function of the converter power stage is given by:

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} \Big|_{\hat{v}_g(s)=0} \quad (\text{C.43})$$

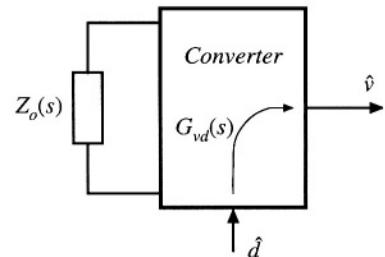
The quantity $Z_o(s)$ is the Thevenin equivalent output impedance of the input filter. Upon setting $\hat{v}_g(s)$ to zero in Fig. C.17, the system of Fig. C.18 is obtained. It can be recognized that this system is of the same form as Fig. C.2, in which the "extra element" is the output impedance $Z_o(s)$ of the added input filter. With no input filter [$Z_o(s) = 0$], the "original" transfer function $G_{vd}(s)|_{Z_o(s)=0}$ is obtained. In the presence of the input filter, $G_{vd}(s)$ is expressed according to Eq. (C.3):

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s) \rightarrow 0} \right) \left(\frac{1 + \frac{Z(s)}{Z_N(s)}}{1 + \frac{Z(s)}{Z_D(s)}} \right) \quad (\text{C.44})$$

where

$$Z_D(s) = Z_i(s) \Big|_{\hat{d}(s)=0} \quad (\text{C.45})$$

Fig. C.18 Determination of the control-to-output transfer function $G_{vd}(s)$ for the system of Fig. C.17.



is the impedance seen looking into the power input port of the converter when \hat{d} is set to zero, and

$$Z_N(s) = Z_i(s) \Big|_{\dot{v}(t) \xrightarrow{\text{null}} 0} \quad (\text{C.46})$$

is the impedance seen looking into the power input port of the converter when the converter output \hat{v} is nulled. The null condition is achieved by injecting a test current source \dot{i}_{test} at the converter input port, in the presence of \hat{d} variations, and adjusting \dot{i}_{test} such that \hat{v} is nulled. Derivation of expressions for $Z_N(s)$ and $Z_D(s)$ for a buck converter example is described in Section 10.3.1.

According to Eq. (C.28), the input filter does not significantly affect $G_{vd}(s)$ provided that

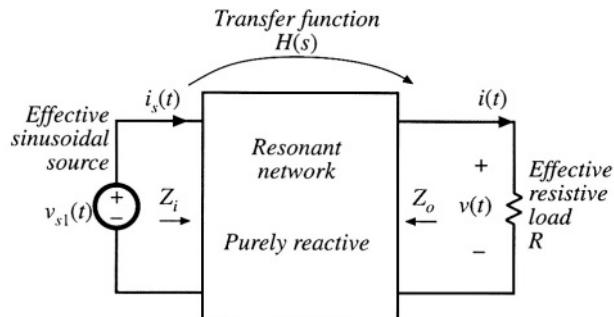
$$\begin{aligned} \|Z_o(j\omega)\| &\ll \|Z_N(j\omega)\| \\ \|Z_o(j\omega)\| &\ll \|Z_D(j\omega)\| \end{aligned} \quad (\text{C.47})$$

These inequalities can provide an effective set of criteria for designing the input filter. Bode plots of $\|Z_N(j\omega)\|$ and $\|Z_D(j\omega)\|$ are constructed, and then the filter element values are chosen to satisfy (C.47). Several examples of this procedure are explained in Chapter 10.

C.4.4 Dependence of Transistor Current on Load in a Resonant Inverter

The conduction loss caused by circulating tank currents is a major problem in resonant converter design. These currents are independent of, or only weakly dependent on, the load current, and lead to poor efficiency at light load. The origin of this problem is the weak dependence of the tank network input impedance on the load resistance. For example, Fig. C.19 illustrates the model of the ac portion of a resonant inverter, derived using the sinusoidal approximation of Section 19.1. The resonant network contains the tank inductors and capacitors of the converter, and the load is the resistance R . The current $i_s(t)$ flowing in the effective sinusoidal source is equal to the switch current. This model predicts that the switch current $i_s(s)$ is equal to $v_{s1}(s)/Z_i(s)$, where $Z_i(s)$ is the input impedance of the resonant tank network. If we want the switch current to track the load current, then at the switching frequency $\|Z_i\|$ should be dominated by, or at least strongly influenced by, the load resistance R . Unfortunately, this is often not consistent with other requirements, in which Z_i is dominated by the impedances of the tank elements. To design a resonant converter that exhibits good properties, the engineer must develop physical insight into how the load resistance R affects the tank input impedance and output voltage.

Fig. C.19 Resonant inverter model.



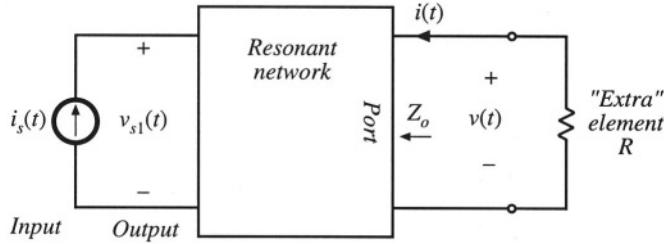


Fig. C.20 Application of the Extra Element Theorem to the system of Fig. C.19, to expose the dependence of $Z_i(s)$ on R .

To expose the dependence of $Z_i(s)$ on the load resistance R , we can treat R as the “extra” element as in Fig. C.20. The input impedance $Z_i(s)$ is viewed as the transfer function from the current i_s to the voltage v_{s1} ; in this sense, i_s is the “input” and v_{s1} is the “output.” Equations (C.2) and (C.3) then imply that $Z_i(s)$ can be expressed as follows:

$$Z_i(s) = \frac{v_{s1}(s)}{i_s(s)} = Z_{i0}(s) \frac{\left(1 + \frac{R}{Z_N(s)}\right)}{\left(1 + \frac{R}{Z_D(s)}\right)} = Z_{i\infty}(s) \frac{\left(1 + \frac{Z_N(s)}{R}\right)}{\left(1 + \frac{Z_D(s)}{R}\right)} \quad (\text{C.48})$$

Here, the impedance $Z_{i0}(s)$ is

$$Z_{i0}(s) = Z_i(s) \Big|_{R \rightarrow 0} \quad (\text{C.49})$$

i.e., the input impedance $Z_i(s)$ when the load terminals are shorted. Likewise, the impedance $Z_{i\infty}(s)$ is

$$Z_{i\infty}(s) = Z_i(s) \Big|_{R \rightarrow \infty} \quad (\text{C.50})$$

which is the input impedance $Z_i(s)$ when the load is disconnected (open circuited).

Determination of $Z_N(s)$ and $Z_D(s)$ is illustrated in Fig. C.21. The quantity $Z_N(s)$ is found by nulling the “output” v_{s1} to zero, and then solving for $v(s)/i(s)$. The quantity $Z_N(s)$ coincides with the conventional output impedance $Z_o(s)$ illustrated in Fig. C.19. In Fig. C.21(a), the act of nulling v_{s1} is equivalent to shorting the source v_{s1} of Fig. C.19. In Section 19.4, the quantity $Z_N(s)$ is denoted $Z_{o0}(s)$, because it coincides with the converter output impedance with the switch network shorted.

The quantity $Z_D(s)$ is found by setting the “input” i_s to zero, and then solving for $v(s)/i(s)$. The quantity $Z_D(s)$ coincides with the output impedance $Z_o(s)$ illustrated in Fig. C.19, under the conditions that the source v_{s1} is open-circuited. In Section 19.4, the quantity $Z_D(s)$ is denoted $Z_{o\infty}(s)$, because it coincides with the converter output impedance with the switch network open-circuited.

The reciprocity relationship, Eq. (C.4), becomes

$$\frac{Z_{i\infty}(s)}{Z_{i0}(s)} = \frac{Z_{o\infty}(s)}{Z_{o0}(s)} \quad (\text{C.51})$$

The above results are used in Section 19.4 to expose how conduction losses and the zero-voltage switching boundary depend on the loading of a resonant converter.

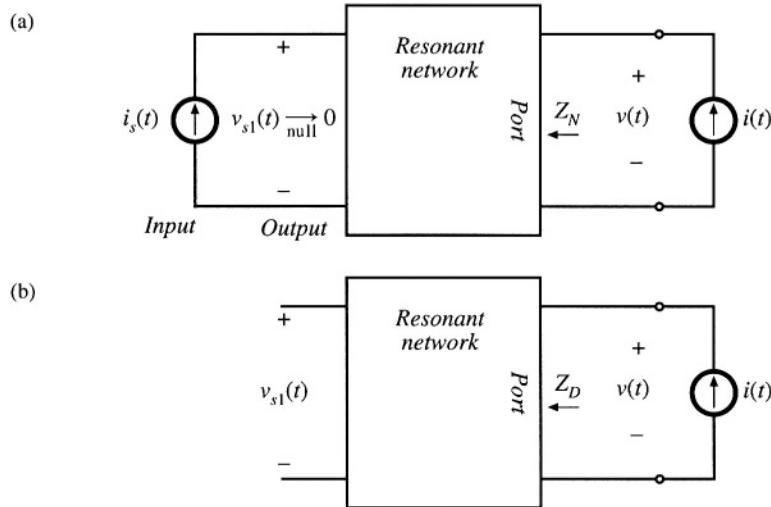


Fig. C.21 Determination of the quantities $Z_N(s)$ and $Z_D(s)$ for the network of Fig. C.20: (a) finding $Z_N(s)$, (b) finding $Z_D(s)$.

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Appendix D

Magnetics Design Tables

Geometrical data for several standard ferrite core shapes are listed here. The geometrical constant K_g is a measure of core size, useful for designing inductors and transformers that attain a given copper loss [1]. The K_g method for inductor design is described in Chapter 14. K_g is defined as

$$K_g = \frac{A_c^2 W_A}{MLT} \quad (D.1)$$

where A_c is the core cross-sectional area, W_A is the window area, and MLT is the winding mean-length-per-turn. The geometrical constant K_{gfe} is a similar measure of core size, which is useful for designing ac inductors and transformers when the total copper plus core loss is constrained. The K_{gfe} method for magnetics design is described in Chapter 15. K_{gfe} is defined as

$$K_{gfe} = \frac{W_A A_c^{2(1 - 1/\beta)}}{MLT \ell_m^{2\beta}} u(\beta) \quad (D.2)$$

where ℓ_m is the core mean magnetic path length, and β is the core loss exponent:

$$P_{fe} = K_{fe} B_{max}^\beta \quad (D.3)$$

For modern ferrite materials, β typically lies in the range 2.6 to 2.8. The quantity $u(\beta)$ is defined as

$$u(\beta) = \left| \left(\frac{\beta}{2} \right)^{-\left(\frac{\beta}{\beta+2} \right)} + \left(\frac{\beta}{2} \right)^{\left(\frac{2}{\beta+2} \right)} \right|^{-\left(\frac{\beta+2}{\beta} \right)} \quad (D.4)$$

$u(\beta)$ is equal to 0.305 for $\beta = 2.7$. This quantity varies by roughly 5% over the range $2.6 \leq \beta \leq 2.8$. Values of K_{gfe} are tabulated for $\beta = 2.7$; variation of K_{gfe} over the range $2.6 \leq \beta \leq 2.8$ is typically quite small.

Thermal resistances are listed in those cases where published manufacturer's data are available. The thermal resistances listed are the approximate temperature rise from the center leg of the core to ambient, per watt of total power loss. Different temperature rises may be observed under conditions of forced air cooling, unusual power loss distributions, etc. Listed window areas; are the winding areas for conventional single-section bobbins.

An American Wire Gauge table is included at the end of this appendix.

D.1 POT CORE DATA

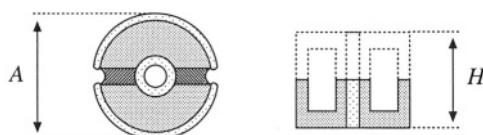


Fig. D.1

Core type (AH) (mm)	Geometrical constant K_g cm ⁵	Geometrical constant K_{gfe} cm ^x	Cross-sectional area A_c (cm ²)	Bobbin winding area W_A (cm ²)	Mean length per turn MLT (cm)	Magnetic path length ℓ_m (cm)	Thermal resistance R_{th} (°C/W)	Core weight (g)
704	$0.738 \cdot 10^{-6}$	$1.61 \cdot 10^{-6}$	0.070	$0.22 \cdot 10^{-3}$	1.46	1.0		0.5
905	$0.183 \cdot 10^{-3}$	$256 \cdot 10^{-6}$	0.101	0.034	1.90	1.26		1.0
1107	$0.667 \cdot 10^{-3}$	$554 \cdot 10^{-6}$	0.167	0.055	2.30	1.55		1.8
1408	$2.107 \cdot 10^{-3}$	$1.1 \cdot 10^{-3}$	0.251	0.097	2.90	2.00	100	3.2
1811	$9.45 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$	0.433	0.187	3.71	2.60	60	7.3
2213	$27.1 \cdot 10^{-3}$	$4.9 \cdot 10^{-3}$	0.635	0.297	4.42	3.15	38	13
2616	$69.1 \cdot 10^{-3}$	$8.2 \cdot 10^{-3}$	0.948	0.406	5.28	3.75	30	20
3019	0.180	$14.2 \cdot 10^{-3}$	1.38	0.587	6.20	4.50	23	34
3622	0.411	$21.7 \cdot 10^{-3}$	2.02	0.748	7.42	5.30	19	57
4229	1.15	$41.1 \cdot 10^{-3}$	2.66	1.40	8.60	6.81	13.5	104

D.2 EE CORE DATA

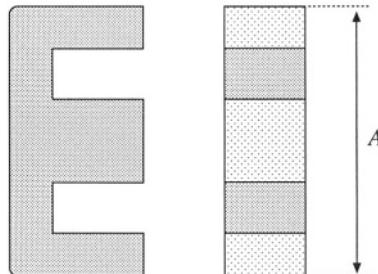


Fig. D.2

Core type (A) (mm)	Geometrical constant K_g (cm ⁵)	Geometrical constant K_{gfe} (cm ⁵)	Cross-sectional area A_c (cm ²)	Bobbin winding area W_A (cm ²)	Mean length per turn MLT (cm)	Magnetic path length ℓ_m (cm)	Core weight (g)
EE12	$0.731 \cdot 10^{-3}$	$0.458 \cdot 10^{-3}$	0.14	0.085	2.28	2.7	2.34
EE16	$2.02 \cdot 10^{-3}$	$0.842 \cdot 10^{-3}$	0.19	0.190	3.40	3.45	3.29
EE19	$4.07 \cdot 10^{-3}$	$1.3 \cdot 10^{-3}$	0.23	0.284	3.69	3.94	4.83
EE22	$8.26 \cdot 10^{-3}$	$1.8 \cdot 10^{-3}$	0.41	0.196	3.99	3.96	8.81
EE30	$85.7 \cdot 10^{-3}$	$6.7 \cdot 10^{-3}$	1.09	0.476	6.60	5.77	32.4
EE40	0.209	$11.8 \cdot 10^{-3}$	1.27	1.10	8.50	7.70	50.3
EE50	0.909	$28.4 \cdot 10^{-3}$	2.26	1.78	10.0	9.58	116
EE60	1.38	$36.4 \cdot 10^{-3}$	2.47	2.89	12.8	11.0	135
EE70/68/19	5.06	$75.9 \cdot 10^{-3}$	3.24	6.75	14.0	18.0	280

D.3 EC CORE DATA

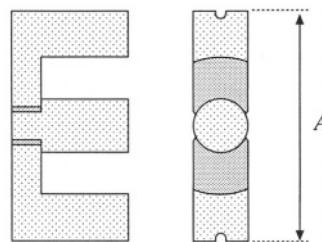


Fig. D.3

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(A) (mm)	K_g (cm ⁵)	K_{gfe} (cm ⁴)	A_c (cm ²)	W_A (cm ²)	MLT (cm)	ℓ_m (cm)	R_{th} (°C/W)	(g)
EC35	0.131	$9.9 \cdot 10^{-3}$	0.843	0.975	5.30	7.74	18.5	35.5
EC41	0.374	$19.5 \cdot 10^{-3}$	1.21	1.35	5.30	8.93	16.5	57.0
EC52	0.914	$31.7 \cdot 10^{-3}$	1.80	2.12	7.50	10.5	11.0	111
EC70	2.84	$56.2 \cdot 10^{-3}$	2.79	4.71	12.9	14.4	7.5	256

D.4 ETD CORE DATA

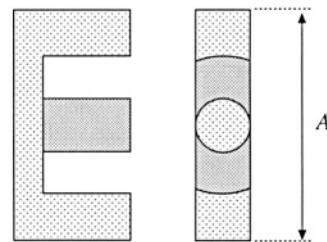


Fig. D.4

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(A) (mm)	K_g (cm ⁵)	K_{gfe} (cm ⁴)	A_c (cm ²)	W_A (cm ²)	MLT (cm)	ℓ_m (cm)	R_{th} (°C/W)	(g)
ETD29	0.0978	$8.5 \cdot 10^{-3}$	0.76	0.903	5.33	7.20	30	
ETD34	0.193	$13.1 \cdot 10^{-3}$	0.97	1.23	6.00	7.86	19	40
ETD39	0.397	$19.8 \cdot 10^{-3}$	1.25	1.74	6.86	9.21	15	60
ETD44	0.846	$30.4 \cdot 10^{-3}$	1.74	2.13	7.62	10.3	12	94
ETD49	1.42	$41.0 \cdot 10^{-3}$	2.11	2.71	8.51	11.4	11	124

D.5 PQ CORE DATA

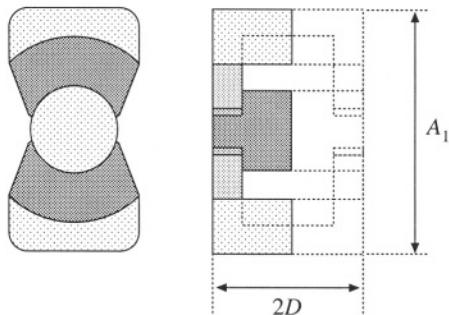


Fig. D.5

Core type	Geometrical constant $(A_1/2D)$ (mm)	Geometrical constant K_g (cm^5)	Geometrical constant K_{gfe} (cm^x)	Cross-sectional area A_c (cm^2)	Bobbin winding area W_A (cm^2)	Mean length per turn MLT (cm)	Magnetic path length ℓ_m (cm)	Core weight (g)
PQ 20/16	$22.4 \cdot 10^{-3}$	$3.7 \cdot 10^{-3}$	0.62	0.256	4.4	3.74	13	
PQ 20/20	$33.6 \cdot 10^{-3}$	$4.8 \cdot 10^{-3}$	0.62	0.384	4.4	4.54	15	
PQ 26/20	$83.9 \cdot 10^{-3}$	$7.2 \cdot 10^{-3}$	1.19	0.333	5.62	4.63	31	
PQ 26/25	0.125	$9.4 \cdot 10^{-3}$	1.18	0.503	5.62	5.55	36	
PQ 32/20	0.203	$11.7 \cdot 10^{-3}$	1.70	0.471	6.71	5.55	42	
PQ 32/30	0.384	$18.6 \cdot 10^{-3}$	1.61	0.995	6.71	7.46	55	
PQ 35/35	0.820	$30.4 \cdot 10^{-3}$	1.96	1.61	7.52	8.79	73	
PQ 40/40	1.20	$39.1 \cdot 10^{-3}$	2.01	2.50	8.39	10.2	95	

D.6 AMERICAN WIRE GAUGE DATA

AWG#	Bare area, 10^{-3} cm^2	Resistance, $10^{-6} \Omega/\text{cm}$	Diameter, cm
0000	1072.3	1.608	1.168
000	850.3	2.027	1.040
00	674.2	2.557	0.927
0	534.8	3.224	0.825
1	424.1	4.065	0.735
2	336.3	5.128	0.654
3	266.7	6.463	0.583
4	211.5	8.153	0.519
5	167.7	10.28	0.462
6	133.0	13.0	0.411
7	105.5	16.3	0.366
8	83.67	20.6	0.326
9	66.32	26.0	0.291
10	52.41	32.9	0.267
11	41.60	41.37	0.238
12	33.08	52.09	0.213
13	26.26	69.64	0.190
14	20.02	82.80	0.171
15	16.51	104.3	0.153
16	13.07	131.8	0.137
17	10.39	165.8	0.122
18	8.228	209.5	0.109
19	6.531	263.9	0.0948
20	5.188	332.3	0.0874
21	4.116	418.9	0.0785
22	3.243	531.4	0.0701
23	2.508	666.0	0.0632
24	2.047	842.1	0.0566
25	1.623	1062.0	0.0505
26	1.280	1345.0	0.0452
27	1.021	1687.6	0.0409
28	0.8046	2142.7	0.0366
29	0.6470	2664.3	0.0330

Continued

AWG#	Bare area, 10^{-3} cm^2	Resistance, $10^{-6} \Omega/\text{cm}$	Diameter, cm
30	0.5067	3402.2	0.0294
31	0.4013	4294.6	0.0267
32	0.3242	5314.9	0.0241
33	0.2554	6748.6	0.0236
34	0.2011	8572.8	0.0191
35	0.1589	10849	0.0170
36	0.1266	13608	0.0152
37	0.1026	16801	0.0140
38	0.08107	21266	0.0124
39	0.06207	27775	0.0109
40	0.04869	35400	0.0096
41	0.03972	43405	0.00863
42	0.03166	54429	0.00762
43	0.02452	70308	0.00685
44	0.0202	85072	0.00635

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