MULTILEVEL INVERTER TECHNOLOGY FOR HIGH POWER SUPPLY

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Abstract

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control.

Using the same number of power devices as a standard nine-level inverter, the proposed inverter operates as a high-power digital-to-analog converter.

Power inverter modules fed with separate d.c. voltage sources of voltage ratio 15V / 30V / 60V / 120V are connected to form a cascade multilevel inverter.

The proposal has the potential for uninterruptible power supply, audio amplifier systems and flexible a.c. transmission applications.

1. Introduction

Multilevel inverter include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

The most attractive features of multilevel inverters are as follows:

1) They can generate output voltages with extremely low distortion and lower $\frac{dv}{dt}$.

2) They draw input current with very low distortion.

3) They generate smaller common-mode (CM) voltages, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, common-mode voltages can be eliminated.

4) They can operate with a lower switching frequency.

In this paper, we examine an improved cascade multilevel inverter using separate d.c. voltage sources.

The functions of using multilevel power inverters are twofold.

Firstly, the series connection of power converter modules reduces the voltage stress of each converter module (or increases the voltage capability of the overall converter structure), making the multilevel inverters suitable for high-voltage applications.

Secondly, the resolution of the a.c. voltage waveforms (i.e., the quality of the generated voltage) increases with the number of voltage levels available in the multilevel inverters. As a result of the improved resolution in the voltage harmonic content, filtering efforts can be reduced.

The proposed inverter has the following advantages:

1) It offers much higher voltage resolution than a traditional cascade inverter by providing a high resolution of 31 voltage levels with minimum device count.

2) The increase in voltage resolution leads to huge improvement in power quality and great reduction in filtering efforts.

3) It combines the advantageous features of a cascade inverter with separate d.c. voltage sources and static phase shifter.

4) Electrolytic capacitors used for providing the d.c. voltage sources will never be connected in opposite polarity in all cases.

2. Nine-level inverter and 31-level inverter

Fig. 1. shows the circuit structure of an inverter leg of a nine-level cascade inverter. Four identical inverter modules are connected in series (cascade) to form a single-phase nine-level inverter. All modules are fed by d.c. voltage sources of the same magnitude. The output voltage has nine voltage levels: -4E, -3E, -2E, -E, 0, +E, +2E, +3E, +4E.

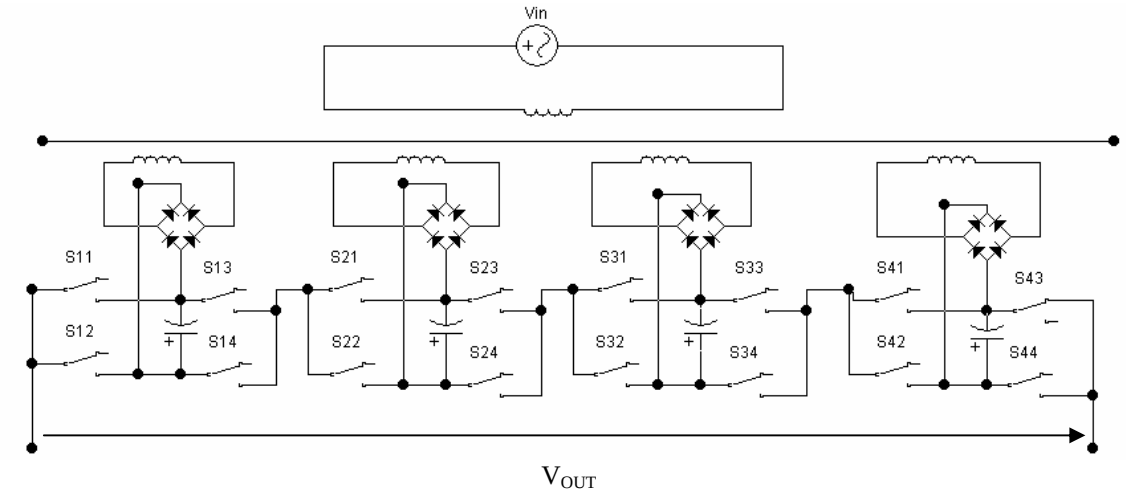

Fig. 1 Schematic of a single-phase cascaded nine-level inverter

By using d.c. voltage sources with a magnitude ratio of 15V/30V/60V/120V the traditional nine-level inverter can be turned into a 31-level inverter. Fig. 2. shows the schematic of the new proposed 31-level inverter for a single-phase system.

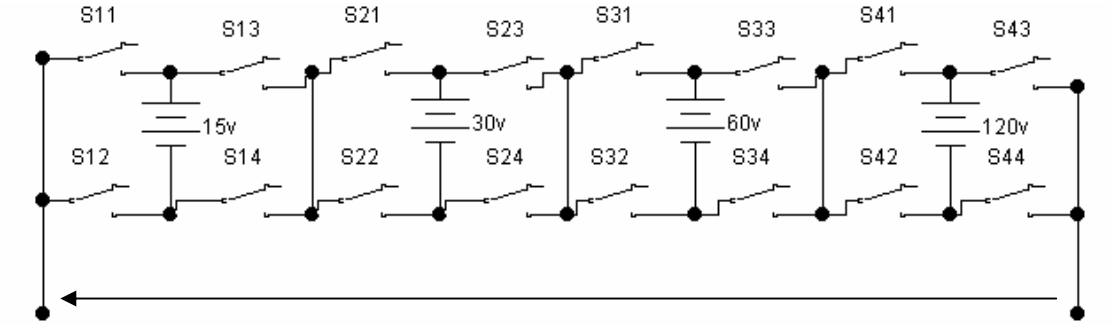

Fig.2 Schematic of the new proposed 31-level inverter

This circuit topology is identical to that of a traditional nine-level inverter except that unequal separate voltages are employed. For positive (negative) voltage generation, switches S_{N2} and S_{N3} (S_{N1} and S_{N4}) are turned on in each inverter module, where subscript N denotes the Nth inverter module.

Table 1. illustrates the switching patterns of all 31 discrete levels.

TABLE 1. Switching patterns for the 31 voltage levels

Switching patterns	Voltage	Switching patterns	Voltage
0	0	0	0
1	15	-1	-15
2	30	-2	-30
3	45=15+30	-3	-45=-15-30
4	60	-4	-60
5	75=15+60	-5	-75=-15-60
6	90=30+60	-6	-90=-30-60
7	105=15+30+60	-7	-105=-15-30-60
8	120	-8	-120
9	135=15+120	-9	-135=-15-120
10	150=30+120	-10	-150=-30-120
11	165=15+30+120	-11	-165=-15-30-120
12	180=60+120	-12	-180=-60-120
13	195=15+60+120	-13	-195=-15-60-120
14	210=30+60+120	-14	-210=-30-60-120
15	225=15+30+60+120	-15	-225=-15-30-60-120

Because the separate d.c. voltage sources are usually provided by voltages across large electrolytic capacitors, the switching patterns show an important point that all electrolytic capacitors are always connected in the same polarity in all cases. This avoids the possibility of having electrolytic capacitors connected in opposite polarity.

In order to further increased the voltage quality, the inverter module can be pulsewidth modulated (PWM) within the discrete level of 15V, so that the effective voltage can overcome the limit of the 31 discrete voltage levels. In the proposed circuit, only the inverter module supplied by the 15V voltage source needs to be PWM controlled. Other inverter modules fed by higher voltage sources (i.e. 30V, 60V and 120V) do not need PWM control, thus minimizing the switching loss.

3. Control Strategy

The switching pattern is determined by comparing a reference sinusoidal reference at a specific sampling rate and then choosing the switching pattern near to the sampled value according to table I. The sampling frequency was first set at about 2 khz and the output frequency is set at 50 hz. In order to observe the basic non-PWM operation of the 31-level inverter, the inverter module fed by the d.c. voltage source of 15V is not PWM controlled initially.

The sampling frequency is usually determined by:

1) the minimum ON / OFF time of the switching device;

2) the number of output levers required.

The minimum ON/OFF time is an important parameter in high-power applications. The typical value of minimum ON/OFF time of a gate-turn-off thyristor (GTO) is approximately 200 μs. In order to maintain a 31-level output voltage, the sampling frequency of the system should be higher than the rate of change of the output frequency.

For example, with a 50 Hz output signal, the minimum sampling frequency to obtain 31-level output will be approximately 100 the desired output frequency.

For uninterruptible power supply (UPS) applications, higher switching frequency is possible due to the use of faster power devices. It can be observed that the 31-level PWM voltage waveform is near sinusoidal and has very good harmonic context.

4. Conclusions

A 31-level inverter with high resolution with minimum device count has been proposed. It combines the advantages of the cascade inverter and static phase-shifter concepts.

The choice of the voltage ratio 15V/30V/60V/120V ensures that all electrolytic capacitors used in the multilevel inverter will not be connected in the reverse polarity, therefore guaranteeing the reliability of the separate d.c. voltage sources. Using the same number of switches of a traditional nine-level inverter, the proposed inverter offers 31 levels.

5. References

[1] Viorel Popescu–"*Electronica de putere*" - Editura de Vest, Timisoara, 1998.

[2] Robert W. Erickson–"*Fundamentals of power electronics*" - ISBN: 0–412–08541–0.