Space Vector Modulated Three-Phase Current Source Converter for DC Motor Drive

Milan S. Adzic *, Evgenije M. Adzic†, Vladimir A. Katic†
* Subotica Tech – College of Applied Sciences, Subotica, Serbia, e-mail: *adzicm@vts.su.ac.rs*
† Faculty of Technical Sciences, Novi Sad, Serbia, e-mail: *evgenije@uns.ac.rs*, *katav@uns.ac.rs*

***Abstract*—The main disadvantage of applying a standard network driven thyristor rectifiers for a DC motor speed control is the fact that such drives loads the network with reactive power and due to its nonlinear structure network current is nonsinusoidal with a higher harmonics content. Modern development of electronic power components, primarily IGBT and MOSFET switches, allows the replacement of a thyristor three-phase rectifiers with an active converter with a six fully-controlled switches that provides usage of switching frequencies significantly above the network frequency. By suitable control algorithm PWM converter can provide sinusoidal input current waveform, which significantly contributes to the reduction of higher harmonics content in the network. The paper presents the results obtained by simulation and experiment for the case of application of an active PWM converter driven DC motor for speed control. Results analysis clearly shows the benefits of the active PWM converter application.**

***Keywords*— Current Source Inverter (CSI), DC machine, Vector control, Modulation strategy.**

I. INTRODUCION

Three-phase current source pulse-width modulated (PWM) converters have attracted attention in recent years, due to feasibility to achieve sinusoidal input currents and unity power factor [1-3]. The possible application of PWM current source converter (CSC) is a DC motor drive, as shown in Fig. 1 [4-5]. In standard three-phase thyristor controlled DC motor drives, input currents deviates from desirable sinusoidal waveform and displacement power factor deviates from desirable unity value, as control firing angle changes during operation. So, tighter power grid code regulations in recent years, make justified replacement of standard DC motor drives with current source PWM converters.

Most of the research papers on CSC have been done with sinusoidal PWM with triangular carrier waveform which is suitable for control units implemented in analog technology [6-7]. Modern digital control units as digital signal processors (DSP) enabled use of space vector theory also for this type of application [8-9]. In this paper, the current space vector PWM modulation (SVPWM) principle is proposed, which directly takes α- and β-input current component references suitable for CSC vector control.

Proposed current SVPWM method includes overmodulation mode of operation, which would be always active during transient periods and enable use of constant predefined limits of the current controller.

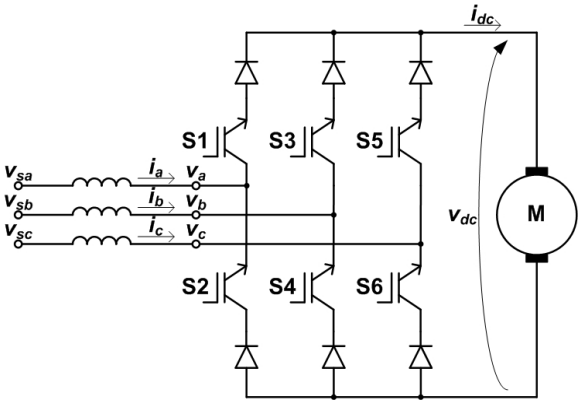

Fig. 1. DC motor one quadrant drive with current source PWM converter.

After establishing current SVPWM method, speed control strategy for DC motor connected at the CSC dc link side is given. This control method is based on the fact that in grid voltage oriented vector control of grid-connected converter, active and reactive power flow through the converter could be controlled independently by input current components in synchronous reference frame.

II. SPACE VECTOR MODULATION FOR CSC

With a three-phase current source PWM converter there are nine possible operating states. In other words, there are nine on/off combinations of six converter switches, with two switches always turned on and remaining four switches turned off. For instance, if switches S1 and S6 are turned on (1), and the remaining switches are turned off (0), converter input line currents (i_a, i_b, i_c) are equal to (i_{dc}, 0, -i_{dc}), respectively. All possible CSC states are given in Table 1.

TABLE I.
AVAILABLE CURRENT SOURCE CONVERRTER STATES

State	S1	S2	S3	S4	S5	S6	i_a	i_b	i_c
1	1	0	0	0	0	1	i_{dc}	0	-i_{dc}
2	0	0	1	0	0	1	0	i_{dc}	-i_{dc}
3	0	1	1	0	0	0	-i_{dc}	i_{dc}	0
4	0	1	0	0	1	0	-i_{dc}	0	i_{dc}
5	0	0	0	1	1	0	0	-i_{dc}	i_{dc}
6	1	0	0	1	0	0	i_{dc}	-i_{dc}	0
7	1	1	0	0	0	0	0	0	0
8	0	0	1	1	0	0	0	0	0
9	0	0	0	0	1	1	0	0	0

Using a Clarke transformation, all nine available input line currents combinations could be transferred in stationary $\alpha\beta$ reference frame:

$$i_\alpha = \frac{2}{3}\left(i_a - \frac{1}{2}i_b - \frac{1}{2}i_c\right) \; i_\beta = \frac{2}{3}\left(\frac{\sqrt{3}}{2}i_b - \frac{\sqrt{3}}{2}i_c\right) \qquad (1\text{-}2)$$

In order to keep the same amplitude of α- and β-currents as the amplitude of original line currents, the transformation with 2/3 is used. Each converter state is represented with pair of $\alpha\beta$ components, which uniquely defines current space vector. All the current space vectors listed in Table 2, are given relatively to the dc link current idc. One can note there are six active space vectors and three zero current vectors. Possible six active space vectors create a hexagon in $\alpha\beta$ reference frame, and divide it in six sectors, which is shown in the Fig. 2. All the possible reference $\alpha\beta$ current combinations must result with the current vector within the given hexagon.

TABLE II.
AVAILABLE CSC'S SPACE VECTOR STATES STATES

State	i_a	i_b	i_c	i_α	i_β	Vector
1	*1*	*0*	*-1*	*1*	*1/√3*	$\underline{I}_1=2/\sqrt{3}e^{j\pi/6}$
2	*0*	*1*	*-1*	*0*	*2/√3*	$\underline{I}_2=2/\sqrt{3}e^{j3\pi/6}$
3	*-1*	*1*	*0*	*-1*	*1/√3*	$\underline{I}_3=2/\sqrt{3}e^{j5\pi/6}$
4	*-1*	*0*	*1*	*-1*	*-1/√3*	$\underline{I}_4=2/\sqrt{3}e^{j7\pi/6}$
5	*0*	*-1*	*1*	*0*	*-2/√3*	$\underline{I}_5=2/\sqrt{3}e^{j9\pi/6}$
6	*1*	*-1*	*0*	*1*	*-1/√3*	$\underline{I}_6=2/\sqrt{3}e^{j11\pi/6}$
7	*0*	*0*	*0*	*0*	*0*	$\underline{I}_7=0$
8	*0*	*0*	*0*	*0*	*0*	$\underline{I}_8=0$
9	*0*	*0*	*0*	*0*	*0*	$\underline{I}_9=0$

All nine CSC states can be represented by the following space vectors:

$$\vec{I}_k = \frac{2}{\sqrt{3}} i_{dc} \cdot e^{j\cdot(2k-1)\frac{\pi}{6}} \qquad k = 1,\ldots,6 \qquad (3)$$

$$\vec{I}_k = 0 \qquad k = 7,8,9 \qquad (4)$$

All other combinations of input line currents must be created using the combination of these available converter states. The space vector modulation technique is based on the fact that every current vector Iref inside the hexagon can be expressed as a weighted average combination of the two adjacent active space vectors and the zero vector. Therefore, in each PWM cycle imposing the desired reference current vector may be achieved by switching between these three converter states. In order to obtain minimum switching frequency for each of the power devices, the state sequence must be arranged such that transition from one state to the next is performed by switching only one converter leg. This condition determines which zero vector would be used in given sector, and it can be found in Table 3. Result is that in every sector there is a switch always turned on during reference vector passing through it.

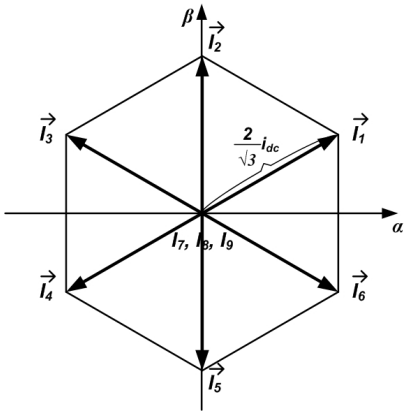

Fig. 2. Hexagon with current space vector states.

TABLE III.
YERO VECTOR THROUGHT THE SECTORS

Sector	1st active vector	2nd active vector	Zero vector
1	$\underline{I}_6$ (**1**,0,0,1,0,0)	$\underline{I}_1$ (**1**,0,0,0,0,1)	$\underline{I}_7$ (**1**,1,0,0,0,0)
2	$\underline{I}_1$ (1,0,0,0,0,**1**)	$\underline{I}_2$ (0,0,1,0,0,**1**)	$\underline{I}_9$ (0,0,0,0,1,**1**)
3	$\underline{I}_2$ (0,0,**1**,0,0,1)	$\underline{I}_3$ (0,1,**1**,0,0,0)	$\underline{I}_8$ (0,0,**1**,1,0,0)
4	$\underline{I}_3$ (0,**1**,1,0,0,0)	$\underline{I}_4$ (0,**1**,0,0,1,0)	$\underline{I}_7$ (1,**1**,0,0,0,0)
5	$\underline{I}_4$ (0,1,0,0,**1**,0)	$\underline{I}_5$ (0,0,0,1,**1**,0)	$\underline{I}_9$ (0,0,0,0,**1**,1)
6	$\underline{I}_5$ (0,0,0,**1**,1,0)	$\underline{I}_6$ (1,0,0,**1**,0,0)	$\underline{I}_8$ (0,0,1,**1**,0,0)

The central part of the SVPWM strategy is the computation of both the active and zero state times for each modulation cycle, T_s. These could be calculated by equalizing the applied average voltage to the desired reference value. Looking at Fig. 3 one can find that, assuming $\boldsymbol{I_{ref}}$ to be laying in sector k, the adjacent active vectors are $\boldsymbol{I_{k-1}}$ and $\boldsymbol{I_k}$. In the following, T_{k-1} denotes on time of vector $\boldsymbol{I_{k-1}}$, T_k denotes on-time of vector $\boldsymbol{I_k}$, and T_0 is the zero state time. Taking into account that $\boldsymbol{I_7}=\boldsymbol{I_8}=\boldsymbol{I_9}=0$, that T_s is sufficiently small, so $\boldsymbol{I_{ref}}$ can be considered approximately constant during this interval, and the fact that $\boldsymbol{I_{k-1}}$ and $\boldsymbol{I_k}$ are constant vectors during interval T_s, the vector on-times can be evaluated by:

$$\vec{i}_{REF} \cdot T_s = \vec{I}_{k-1} \cdot T_{k-1} + \vec{I}_k \cdot T_k \qquad T_{k-1} + T_k + T_0 = T_s \qquad (5\text{-}6)$$

The space vector module can create the PWM switching pattern using directly the reference α- and β-current components, i_α^{REF} and i_β^{REF}. On such a way it is particularly suitable for digital vector current control, giving to the regulators full control over the converter input line current d- and q-components. These d- and q-current components, defined on the regulators outputs, are transferred to the stationary $\alpha\beta$ reference frame and passed through to the space vector modulator. The main task of the space vector modulator is to calculate the needed

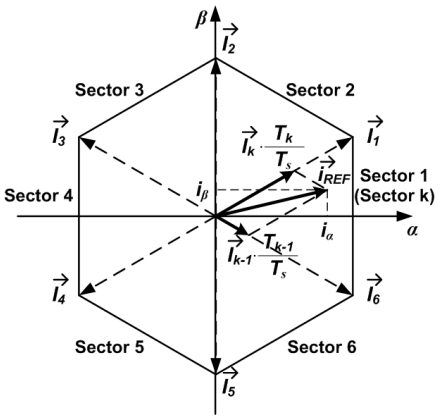

Fig. 3. Average $\boldsymbol{I_{ref}}$ in sector k, created using $\boldsymbol{I_{k-1}}$, $\boldsymbol{I_{k-1}}$ and zero vector.

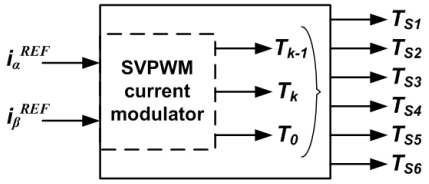

Fig. 4. Current SVM using directly i_α^{REF} and i_β^{REF}.

vector on-times directly from i_α^{REF} and i_β^{REF}, and to distribute them to the corresponding switches depending on the current sector (Fig. 4). General relation between the i_α^{REF} and i_β^{REF} and needed space vector on-times that is valid for all the sectors can be derived from Eqs. (5) and (3). It follows that:

$$\begin{bmatrix} T_{k-1} \\ T_k \end{bmatrix} = \frac{T_s}{i_{dc}} \begin{bmatrix} \sin\left[(2k-1)\frac{\pi}{6}\right] & -\cos\left[(2k-1)\frac{\pi}{6}\right] \\ -\sin\left[(2k-3)\frac{\pi}{6}\right] & \cos\left[(2k-3)\frac{\pi}{6}\right] \end{bmatrix} \begin{bmatrix} i_\alpha^{REF} \\ i_\beta^{REF} \end{bmatrix}$$

$$T_0 = T_s - T_{k-1} - T_k \tag{7-8}$$

For implementation, table with predefined solutions of sine/cosine values in Eq. (7) for each sector can be used. From Eq. (7) one can note that in vector on-time calculation process there is dividing by actual value of dc link current, i_{dc}. Due to this here can happened that calculated T_{k-1} and T_k values are above maximum T_s. If this is the case, modulator is living linear mode of operation and entering in overmodulation. For example, that would be the case in transient periods when reference values are much greater than actual dc link current. But, one must note that available dc link current actually defines the maximum input line current amplitude. For proper operation of space vector modulator for CSC, it must deal with this problem. The best way to detect overmodulation is to monitor the calculated zero vector on-time. If there is not enough time for both active vectors needed to represent the reference vector, then the available zero vector on-time would be negative:

$$if\,(T_0 = T_s - T_{k-1} - T_k < 0) \Rightarrow over\,\mathrm{mod}ulation \tag{9}$$

If overmodulation is detected, active vector on-times need to be recalculated in that way to share maximum PWM time available:

$$T_{k-1} = T_s \frac{T_{k-1}}{T_{k-1} + T_k} \quad T_k = T_s \frac{T_k}{T_{k-1} + T_k} \tag{10-11}$$

Based on above analysis Table 4 could be created that gives us connection between the on-time (duty cycle) of each converter switch and the calculated on-times of active and zero vectors, for each sector.

TABLE IV.
DISTRIBUTION OF VECTOR ON-TIMES TO SWITCHES THROUG HOUT ALL THE SECTORS

Switch ontime	Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
T_{S1}	T_S	T_{k-1}	0	T_0	0	T_k
T_{S2}	T_0	0	T_k	T_S	T_{k-1}	0
T_{S3}	0	T_k	T_S	T_{k-1}	0	T_0
T_{S4}	T_{k-1}	0	T_0	0	T_k	T_S
T_{S5}	0	T_0	0	T_k	T_S	T_{k-1}
T_{S6}	T_k	T_S	T_{k-1}	0	T_0	0

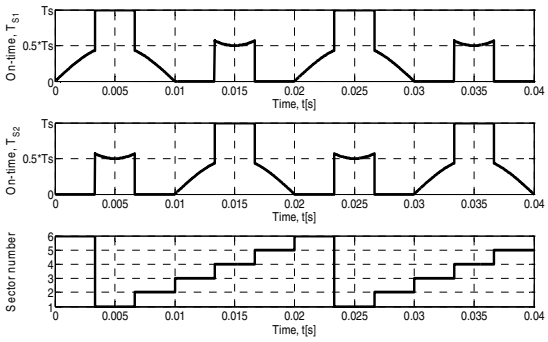

Fig. 5. One-leg switches on-times-linear mode.

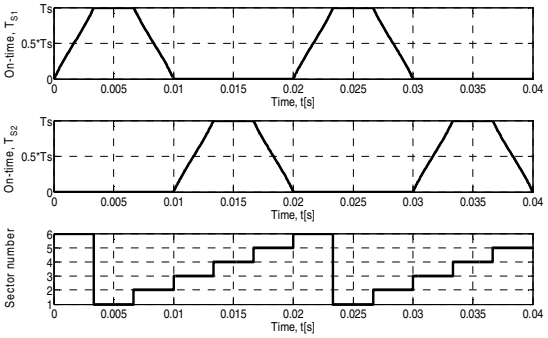

Fig. 6. One-leg switches on-times-overmodulation.

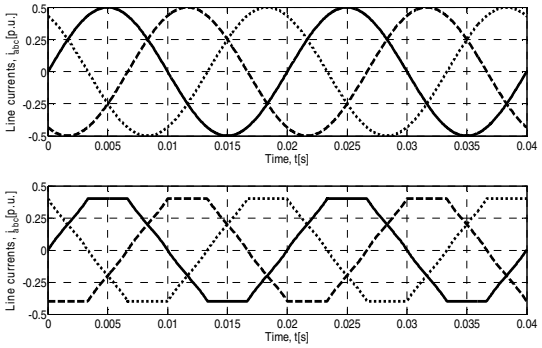

Fig. 7. Converter input line currents, i_{abc}, in linear and overmodulation mode of SVPWM operation.

Characteristic waveform of current source converter switches on-times in the PWM cycle interval, during reference vector rotating throughout all the sectors are shown in Figs. 5 and 6. In both cases amplitude of reference vector is *0.5 [p.u.]* rotating at the frequency of *50 [Hz]*. In Fig. 5 linear mode of operation is shown, where dc link current i_{dc} was equal to *1 [p.u.]*, and in Fig. 6 overmodulation appears because in this case i_{dc} was put to be equal to *0.4 [p.u.]*.

Average converter line currents in the PWM interval can be calculated as:

$$i_a = (T_{S1} - T_{S2}) i_{dc} \; i_b = (T_{S3} - T_{S4}) i_{dc} \; i_c = (T_{S5} - T_{S6}) i_{dc} \tag{12-14}$$

Using Eqs. (12-14) it can be shown that in linear operation mode converter line currents would have

sinusoidal waveform for given switches on-times and that in overmodulation these have trapezoidal waveform, which is shown in Fig 7. This verifies and proves operation of presented current space vector modulation method.

PWM pattern and needed interrupt signals for presented SVPWM for current source converter, which can achieve the specified Table 4, is given in the Fig. 9. Because of the complexity of the switching pattern, it is not possible to simply use standard PWM peripherals of standard DSPs as in case of the SVPWM for voltage source converter. Therefore, in this case is a convenient asymmetrical PWM signal with three interrupt signals as shown in the Fig. 8. At the begin of PWM period, first interrupt signal is generated when it is necessary to turn-on switch with allocated on-time T_{k-1} and also the switch which is constantly involved in the current sector (with assigned on-time T_s). Then, it must turn-off switches whose allocated on-times are 0. After time T_{k-1} regard to PWM begin, second interrupt signal is generated when it is necessary to turn-on switch with allocated on-time T_k and then turn-off switch with assigned on-time T_{k-1}. Finally, after time T_k measured from the second interrupt, third interrupt signal is generated when it is necessary to turn-on switch with allocated on-time T_0 and turn-off switch with assigned on-time T_k. Implementation of presented PWM pattern must ensure that current circuit is never interrupted during converter operation. This means that each time during transition between states, certain switches must be first turned on and then others turned off.

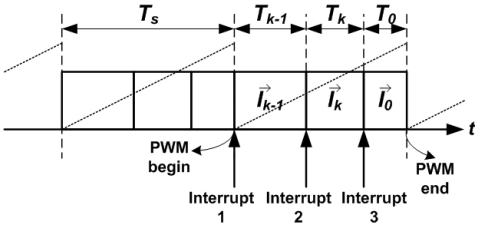

Fig. 8. PWM switching pattern for modulator.

III. SPEED CONTROL OF DC MOTOR DRIVEN BY CSC

As presented in Fig. 1 the current source converter can supply the dc motor directly. If converter switching frequency is limited to relatively small value which cannot ensure constant dc link current during switching period, there can be additional inductance in series with the motor. Shown converter is one-quadrant drive because it cannot provide dc link current in both directions.

The block diagram of the control system for current source converter supplied dc motor is shown in the Fig. 9. Control system consists of two cascaded control loops, outer speed control loop and inner dc motor or converter dc link current loop. This control method is based on the fact that in grid voltage oriented vector control of grid-connected converter, active and reactive power flow through the converter could be controlled independently by input current components in synchronous reference frame. So, speed control is achieved by actually controlling active power flow through the converter, and input displacement power factor control is achieved controlling current component in other axis i.e. controlling

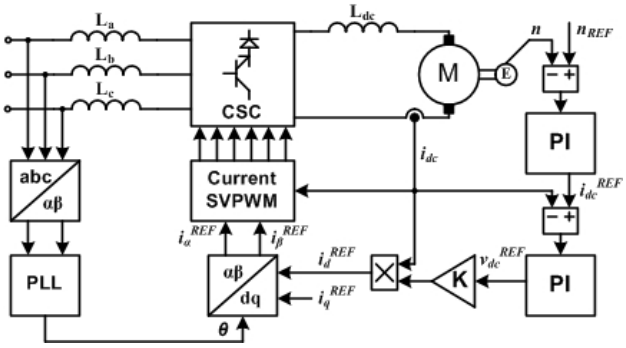

Fig. 9. Speed control scheme for DC motor.

reactive power flow through converter.

If synchronous rotating frame is oriented towards the grid voltage, i.e. if v_q=0, then active and reactive power through the converter can be expressed as:

$$p = \frac{3}{2}\left(v_d i_d + v_q i_q\right) = \frac{3}{2} v_d i_d \tag{15}$$

$$q = \frac{3}{2}\left(v_q i_d - v_d i_q\right) = -\frac{3}{2} v_d i_q \tag{16}$$

From Eqs. (15) and (16) one can note that in such oriented synchronous reference frame one current component, i_d, directly determines converter active power, and other, i_q, determines reactive power. If converter power losses are neglected input three-phase power is equal to the output dc power, so:

$$p = \frac{3}{2} v_d i_d = v_{dc} i_{dc} \tag{17}$$

from which *d*-current component reference could be calculated as:

$$i_d^{REF} = \frac{2}{3 v_d} v_{dc}^{REF} i_{dc}^{REF} = K v_{dc}^{REF} i_{dc}^{REF} \tag{18}$$

DC motor speed is regulated by controlling the voltage at its terminals (for permanent magnet motors or in base speed range of separately excited motors), i.e. dc link voltage.

So, the speed controller is giving dc link current reference i_{dc}^{REF} for inner current loop, and current loop is giving dc link voltage reference in order to get reference *d*-input current component for SVPWM modulated current converter. *q*-current component may be used for reactive power control, and if unity power factor is needed then it have to be set to zero.

IV. SIMULATION RESULTS

Detailed model of the system presented in Fig. 9 has been developed in Matlab/Simulink software package. A permanent magnet dc motor is simulated. Parameters used in simulation were corresponding to parameters in developed experimental setup, given in Table V.

Two usual set of tests have been performed in the simulation model: analysis of motor speed response on speed reference change during constant load and analysis of motor speed response on load change during constant speed. Objective was to verify and prove motor speed control scheme represented in Fig. 9 before work on

experimental setup, and also to obtain proper controllers gains in order to have responses according to desired set requirements.

Fig. 10 demonstrates motor speed response for speed reference change and for constant motor load. Motor load was set to *0.084 p.u.* for which steady-state dc-current was *0.26 p.u.* due to the same values having later in experiment. At begin *t=0 s*, reference speed *0.2 p.u.* was set, then at *t=0.6 s* it was reduced to *0.1 s* and at *t=1.2 s* zero speed was commanded. In each case speed response is almost aperiodic, with small overshoot of *3%* and settling time of *0.21 s* which is about three times faster then mechanical time constant of considered dc-drive. Set control requirements were according to criterion of obtaining critical aperiodic response [11]. Fig. 11 shows dc-link current, i.e. motor current response during such manipulation. Steady-state values were equal (*0.258 p.u.*) for different motor speeds indicating constant motor load. For every speed reference drop, there is appropriate motor current reference drop due to the required motor torque reduce. From speed and current regulator outputs, i_{dc_ref} and v_{dc_ref} respectively, input line current *dq*-components are calculated, and for this case shown in Fig. 12. It could be noted that referenced *dq*-current components were obtained due to the matching of actual and referenced values. Fig. 13 isolates time interval around *0.6 s*, when speed reference was reduced from *0.2 p.u.* to *0.1 p.u.* in order to analyze input line currents. It could be noticed that sinusoidal input currents in phase with corresponding input grid voltages were achieved, both in steady-state and in transient period, due to the commanded zero reactive power transfer between converter and the grid.

Fig. 14 demonstrates motor speed response for motor load change and constant reference speed. Because the same controllers parameters used as in previous case, motor speed response have large drop and overshoot of *30%* upon sudden motor loading and unloading, respectively. Parameters were calculated according to appropriate criterion for reference change. For dc-drive with load profile comprehends of abrupt changes, controllers gains must be several times higher as simulation approved. However, constant speed in steady-state was achieved. Fig. 15 shows motor load profile used in this case, and speed controller output and motor current response. Motor current changes fully correspond to load torque changes, as expected. Figs. 16 and 17 illustrates input line currents response in *dq* and original *abc* domain. Due to the small input coupling inductances with the grid actual and referenced *dq*-currents look equal in shown time scale which include whole transition period. Again, actual line currents are sinusoidal and in phase with input grid voltages, even in transient periods, due to the referenced zero reactive power.

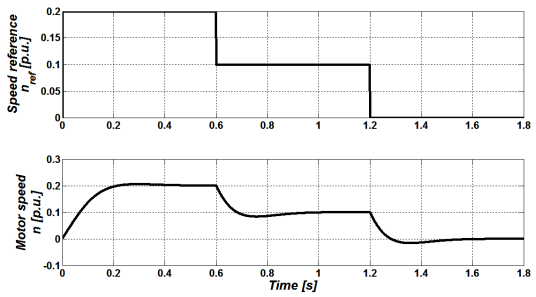

Fig. 10. Motor speed response for speed reference change.

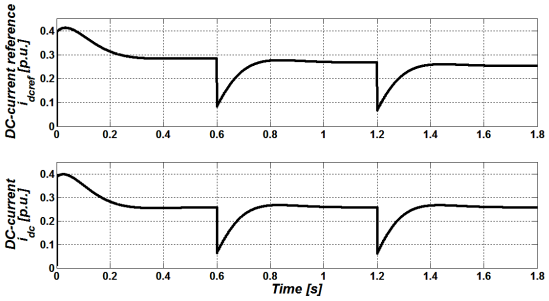

Fig. 11. dc-link current response for speed reference change.

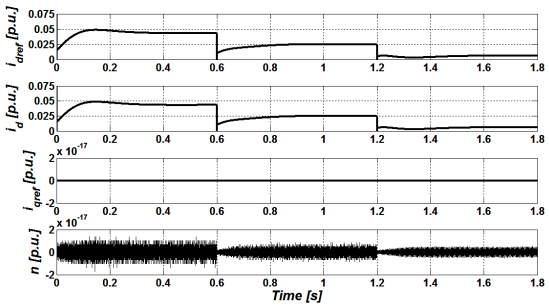

Fig. 12. dq-current components response for speed reference change.

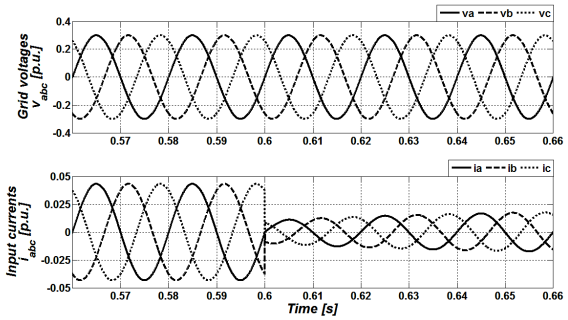

Fig. 13. Input line currents response for speed reference change.

TABLE V.

PARAMETERS USED IN EXPERIMENT

Nominal voltage, U_n	15 [V]
Nominal current, I_n	4 [A]
Nominal speed, n_n	7365 [ob/min]
Nominal flux linkage, ψ_n	19.4 [mWb]
Motor terminal resistance, R_a	0.334 [Ω]
Motor terminal inductance, L_a	0.09 [mH]
Input line inductances, L_a, L_b, L_c	0.22 [mH]
Dc link inductance, L_{dc}	7.2 [mH]
Base voltage, U_{base}	50 [V]
Base current, I_{base}	6 [A]
Base speed, n_{base}	8000 [rpm]

Analyze of the system response to the reactive power reference was also performed. Fig. 18 demonstrates that reactive power reference determines *q*-current component and does not influence on *d*-current component and motor speed. Fig. 19 shows input line currents for reactive power reference change at *t=0.3 s*. It could be noted that amplitude and phase shift of currents were changed according to the set reference.

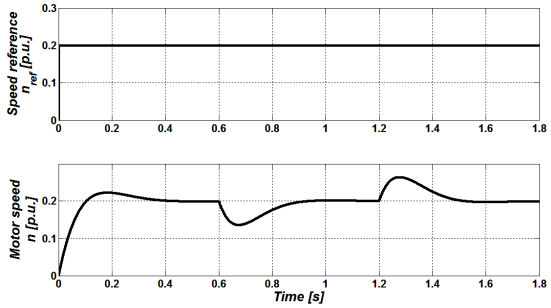

Fig. 14. Motor speed response for load change.

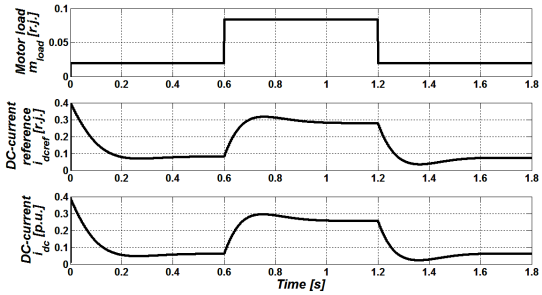

Fig. 15. dc-link current response for load change.

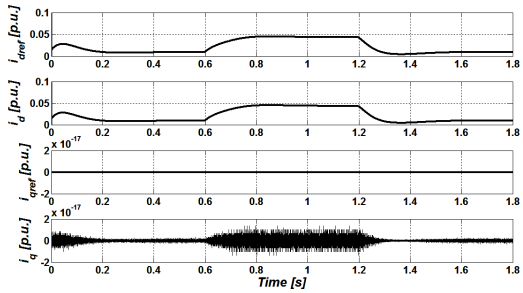

Fig. 16. dq-current components response for load change.

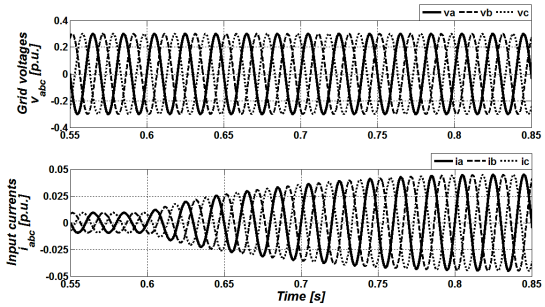

Fig. 17. Input line currents response for load change.

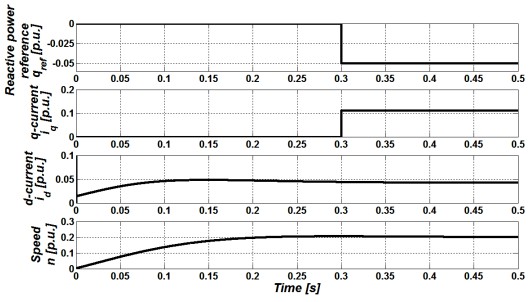

Fig. 18. Reactive power reference does not affect motor speed.

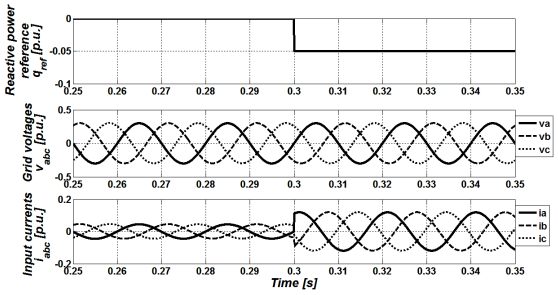

Fig. 19. Input line current response for reactive power reference set.

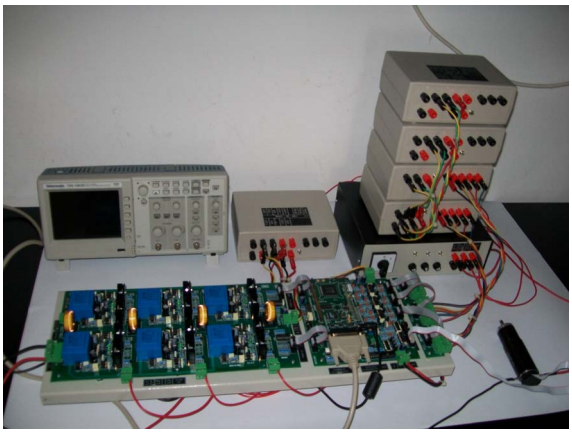

Fig. 20. Developed experimental setup with four-quadrant PWM rectifier for DC-motor drive.

V. EXPERIMENTAL RESULTS

Experimental setup for low-voltage application, shown in Fig. 20, has been developed in order to verify proposed control algorithm and simulation model in Fig. 9. All measured and control signals are adapted for development platform based on fixed-point digital signal processor TMS320F2812, which was used for control algorithm implementation.

Figs. 21 and 22 shows grid voltages at the point of converter connection, in original (*abc* domain) and stationary reference frame ($\alpha\beta$ domain), respectively. Amplitude of working grid voltage was *15 V*, which is *0.3* in per unit (*p.u.*) values. This is due to the low-voltage small power DC motor (90 W) used in experiment. It could be noticed that grid voltages are not pure sinusoidal waveforms and they are distorted particularly in the region of maximum values, where they are flattened as a consequence of a nonlinear loads in the grid, especially rectifiers. As a consequence, after transformation to the stationary reference frame, α-component has almost the same waveform as original voltage and β-component has triangular waveform in the region of maximum values.

Fig. 23 shows the determined grid voltage angle, which is synchronization angle and it is used in Parke transformations (rotating transformation) in the control algorithm. Conventional PLL was used, which is feedback system that consists of a comparator, low-pass filter and integrator, and generates grid angle θ, so that q-component of grid voltage equals to zero [10].

In order to test operation of the developed SVPWM current modulator and speed control algorithm, reference speed is set to *0.2 p.u.* Motor load torque was such that dc-current was equal to 0.*26 p.u.* which could be seen in

recorded Fig. 24. Upper diagram shows actual measured dc-link current and below is its filtered value which goes as input for current modulator. Input line converter currents from the grid, for this case, could be seen in Fig. 25. Obtained current waveform is close to sinusoidal and distortion yields from several reasons: distortion of input grid phase voltages (5^{th} and 7^{th} harmonic components, mostly), not enough robust PLL used when weak grid voltage is more distort in drive run phase, and unsolved dead-time compensation issue in complete (current zero-crossing instants).

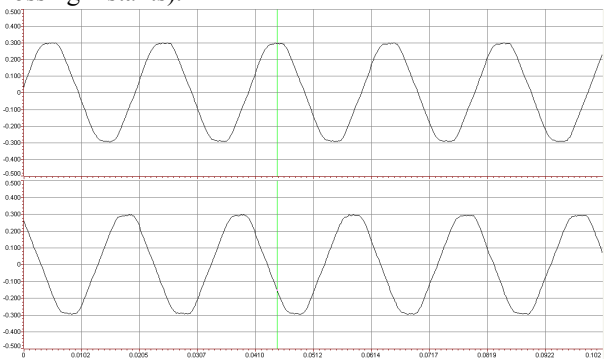

Fig. 21. Grid voltages in phases *a* and *b*.

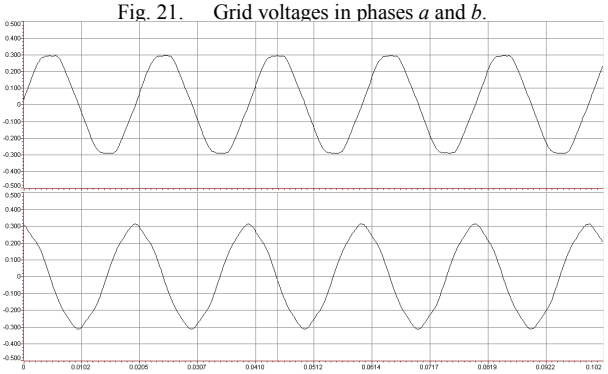

Fig. 22. Grid voltages in *alpha* and *beta* axis.

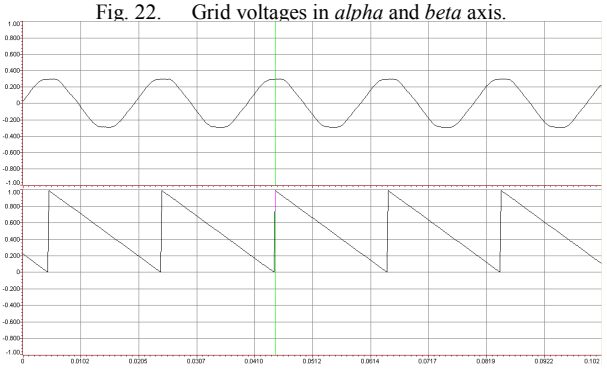

Fig. 23. *Alpha* voltage component and synchronization angle.

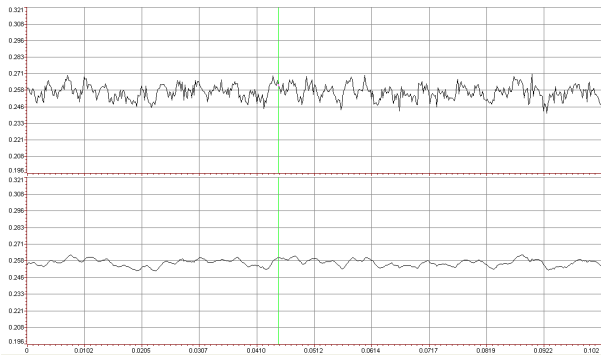

Fig. 24. dc-link current and its filtered value for given motor load.

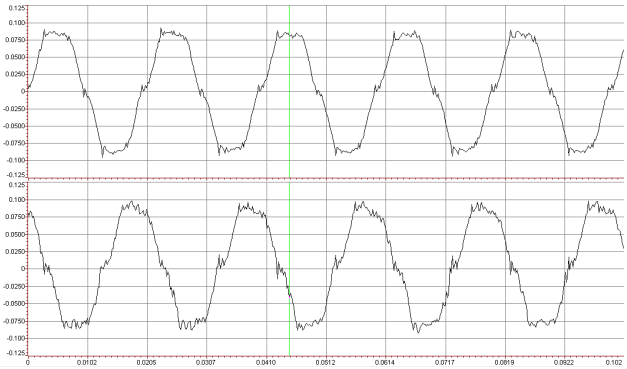

Fig. 25. Converters two input phase currents (*a* and *b*).

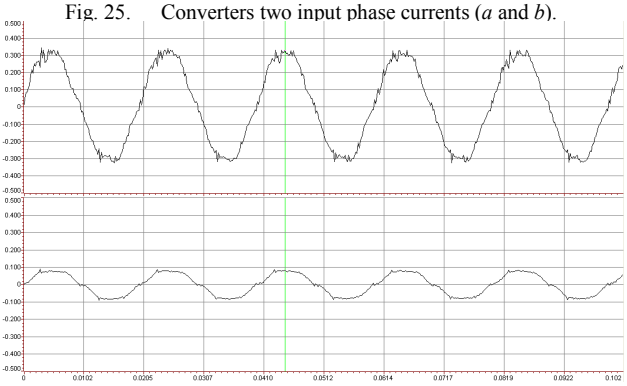

Fig. 26. Converter input phase voltage and current.

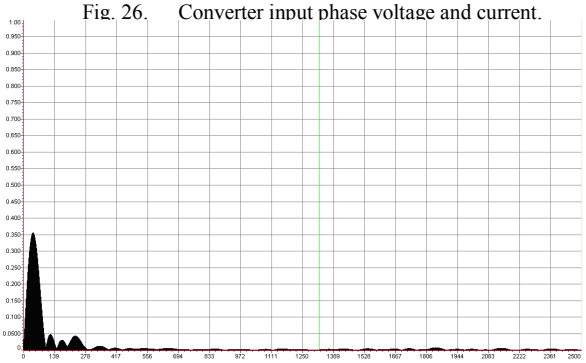

Fig. 27. FFT of the converter input phase current.

However, obtained converter line currents were in phase with corresponding phase voltages, due to the referenced zero *q*-current component. Fig. 26 shows comparative view of input voltage and current for the same phase. Phase shift is equal to zero. Amplitude of realized currents is around 0.075 which is more then simulated in Figs. 13 and 17, due to neglected converter losses in algorithm, but which must be covered from the grid. Accordingly, *d*-current have bigger value compare to referenced value. Distortion in phase voltages upon drive loading is also noticeable, which influence on the control algorithm that does not include these conditions. Fig. 27, shows spectral content of the converter input line current for the observed case. There is harmonic content of 2^{th}, 3^{th}, 5^{th} and 7^{th} components. 2^{th} harmonic is consequence of unbalanced input phase voltages and *3th*, 5^{th} and 7^{th} harmonics are due to characteristic distortion of distribution grid phase voltages. Presented control algorithm does not suppose these issues, and it could be solved in some future work.

Finally, Fig. 28 shows motor speed response on speed reference change for shown constant load. At the time *t=0.035s* speed reference is set to *0.2 p.u*. The speed is settled without overshoot after approximately *0.18 s*. After

that at *t=0.25 s* reference speed is reduced to *0.1 p.u.* and at the *t=0.38 s* to zero value. It could be noted that motor follows the reference speed with high dynamic, because setlling time is about mechanical time constant of the considered drive. When zero command is set, implemented algorithm suddenly set zero $\alpha\beta$ current references to current modulator. Due to this motor speed is reduced very fast.

Fig. 29 shows motor speed response to the motor load change. At the *t=0.05 s* reference speed is set to *0.2 p.u.* and the motor is not loaded. At instant *t=0.13 s* motor is suddenly loaded with shown load in Fig. 24. It can be seen that motor speed drops slightly for short period of approximately *0.12 s*. At instant *t=0.3 s* motor is suddenly unloaded, motor speed grows and it is settled back to the reference after *0.12 s*.

Experimental results fully correspond to obtained simulation results for the same system parameters, and prove proposed speed control algorithm for SVPWM current converter driven DC motor.

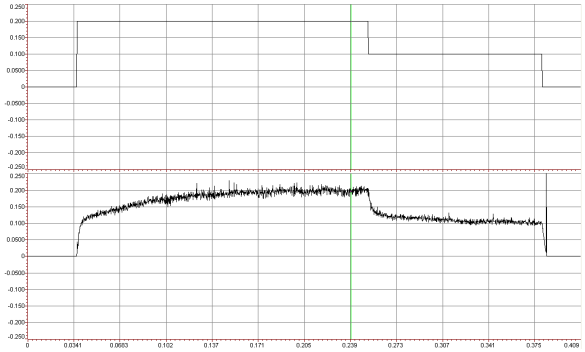

Fig. 28. Speed response on reference change.

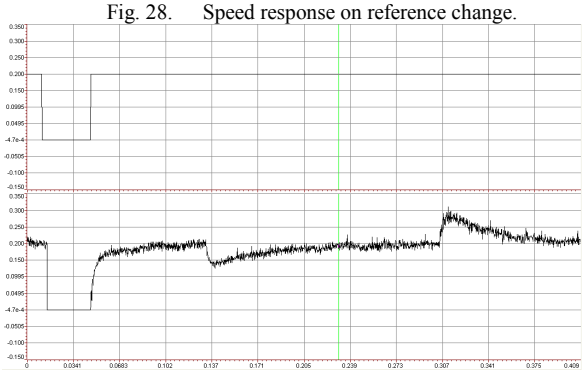

Fig. 29. Speed response on load change.

VI. CONCLUSION

In this paper space vector modulation for current source converter which directly takes stationary α- and β-current components references is introduced. It is specially suitable for vector control of the converter. The overmodulation mode of modulator which is mostly not encountered for in the literature is introduced. It ensures proper converter operation during transient periods, providing the possibility to use constant limit values for current controller. Space vector modulated current source converter is used as a DC motor drive. Motor speed control strategy is proposed, simulated and proved by experiment. Compare to the conventional network driven thyristor rectifier or dc chopper supplied with diode rectifier proposed topology and control algorithm achieve sinusoidal input currents with almost unit power factor and fast dynamic speed control.

REFERENCES

[1] M. Salo, H. Tuusa, "A vector controlled current-source PWM rectifier with a novel current damping-method", *IEEE Trans. Pow. Electron.,* vol. 15, pp. 464–470, May 2000.

[2] B.H. Kwon, B. Min, "A fully software-controlled PWM rectifier with current link", *IEEE Trans. Ind. Electron.,* vol. 40, pp. 355–363, June 1993.

[3] B. W. Pontt, J. Rodriguez, S. Bernet, S. Kouro, "Current-Source Converter and Cycloconverter Topologies for Industrial Medium-Voltage Drives", *IEEE Trans. on Ind. Electron..*, vol. 55, pp.2786-2797, July 2008.

[4] M. Jussila, M. Salo, L. Kahkonen, H. Tuusa, "A Vector Modulated Three-Phase Four-Quadrant Rectifier – Application to a Dc Motor Drive", *Institute of Power Electronics,* Tampere University of Technology, http://www.elkraft.ntnu.no/norpie/10956873/Final%20Papers/010%20-%20Paper_010pdf.pdf .

[5] H.F. Bilgin, K.N. Köse, G. Zenginobuz, M. Ermis, E. Nalcaci, I. Cadirci, H. Köse, "A unity-power-factor buck-type PWM rectifier for medium/high-power DC motor drive applications", *IEEE Trans. on Ind. App.,* vol. 38, pp. 1412–1425, Sep./Oct. 2002.

[6] K. Limori, K. Shinohara, M. Muroya, Y. Matsushita, "Zero-switching-loss PWM rectifier of converter without DC link components for induction motor drive", *IEEE-PCC 2002, Osaka, Japan*, vol. 2, pp.409-414, 2002.

[7] M L. Huber, and D. Borojević, "Space vector modulated three-phase to three-phase matrix converter with input power factor correction", *IEEE Trans. Ind. App.,* vol. 31, pp. 1234–1246, November/December 1995.

[8] M. Jussila, M. Salo, H. Tuusa, " Realization of a three-phase indirect matrix converter with an indirect vector modulation method", *IEEE-PESC 2003*, Vol. 2, pp. 689–694.

[9] A. M. Qiu, Y. W. Li, N. Zargari, Y. Liu, "High Performance Current Source Inverter Fed Induction Motor Drive with Minimal Harmonic Distortion", IEEE-PESC 2007, vol. , pp. 79-85, June 2007.

[10] F. Blaabjerg, R. Teodorescu, M. Liserre, A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems", *IEEE Trans. on Ind. Ele.,* vol. 53, pp. 1398-1409, October 2006.

[11] S. N. Vukosavic, "Digitalno upravljanje elektricnim pogonima", Akademska misao, Belgrade, 2003.