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Bodo´s Power®

Electronics in Motion and Conversion

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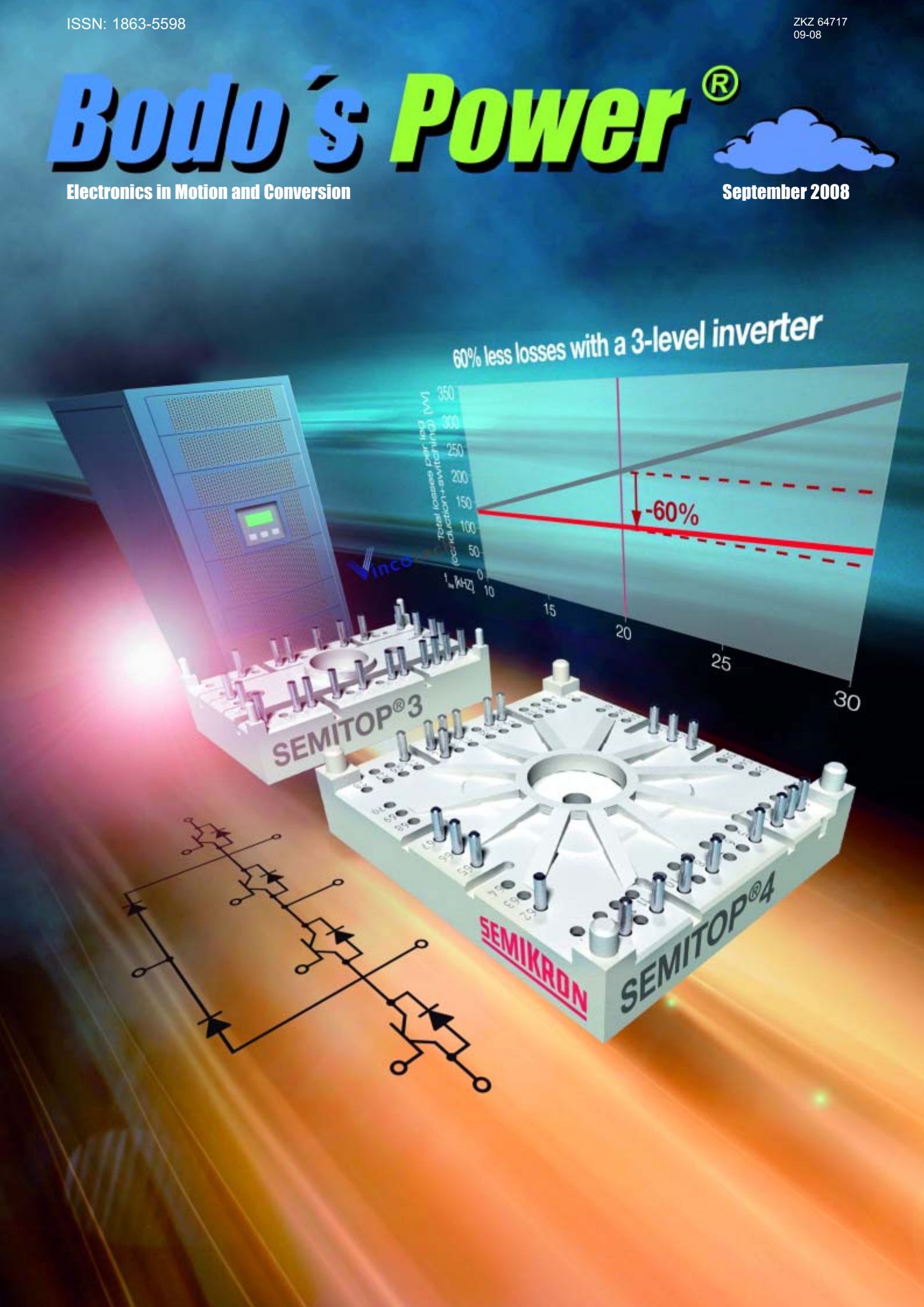

IGBTs for 3-level inverters

Improved efficiency in DC/AC conversion

Electrical energy is an extremely valuable commodity and many market studies demonstrate that the demand for electrical energy is continually increasing exponentially. In the period from 2001 to 2006, energy consumption increased by 16.1% increase (Source: BP Statistical Review of World Energy, June 2007). Owing to the limited availability of electrical energy and ever increasing oil prices, however, a new technical age has begun – an age in which the goal is to reduce electrical energy consumption and promote research into alternative sources of energy. As a result, continuous improvements are urgently needed on the efficiency front in all industrial and consumer applications.

By Marco Di Lella and Riccardo Ramin, Product Manager SEMIKRON Italy

When we speak of efficiency, we are referring mainly to electrical efficiency. This usage, however, is a restriction of the meaning of the word efficiency itself. In power electronic applications the main goal pursued by engineers in the development of a new product is to maximize different types of efficiency such as electrical and thermal efficiency, as well as optimize harmonic distortion and overall dimensions.
The above-mentioned goals have to be fulfilled in line with other increasingly tighter goals: the achievement of economic efficiency and development times. One question that arises in this context is whether more powerful modules with better efficiency rates can meet the all-important efficiency goals.

SEMITOP® power modules boast excellent thermal performance and integrate the latest silicon technologies and highly innovative circuit topologies, resulting in maximum efficiency and cost effectiveness. The isolated power modules are for PCB soldering. The use of a single mounting screw and the copper baseplate-free design ensure excellent thermal performance, resulting in unbeatable reliability in application. Reliability is also validated in an extensive qualification programme based on 17 different tests performed for more than 10,000 hours.

The SEMITOP® product range has been expanded, adding a new module specifically developed for 3-level inverter applications.

Three-level inverter topology is being used increasingly often in UPS applications, including those with medium-low power ratings (5-40 kVA).

Multilevel inverter technology is based on a rather simple concept: IGBT modules are connected in series, allowing for voltage ratings far higher than the IGBT reverse blocking voltages. This concept was first introduced for high-voltage and high-power converter applications in order to allow for the use of standard IGBTs in applications with voltage ratings in the tens of thousands range.
The use of multilevel inverters is a simple way of improving efficiency in DC/AC conversion. The converter produces an output waveform very close to a sinusoidal wave with extremely low harmonic distortion levels. This boasts two advantages: The switching frequency can be lower than that of a typical two-level application, allowing for reduced silicon losses; and a reduced output filter results in a reduction in overall dimensions and costs.

A typical three-phase inverter designed in half-bridge topology (Figure 1) allows for an output voltage waveform that can switch between two voltage levels only. The topology in Figure 1b, by contrast, allows for an output voltage waveform that switches through three voltage levels, which is why this topology is also known as three-level inverter topology.

We will now analyse the principle behind a three-level inverter in order to ascertain the differences between it and a conventional 2-level inverter [1]. For a three-phase three-level inverter a structure similar to that used with 12 electronic devices (IGBT) is needed (see Fig 2). Each phase will switch across three voltage levels ($+V_{dc}/2$, 0, $-V_{dc}/2$). In a

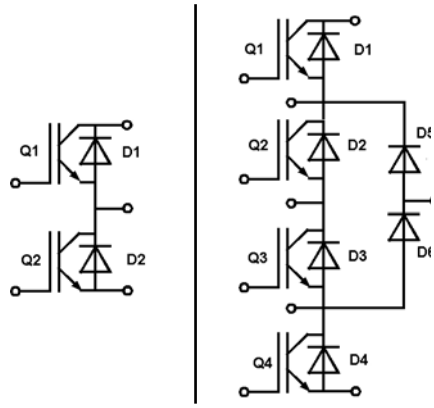

Figure 1 – Typical leg of a 2-level inverter (2L) and a 3-level inverter (3L)

structure such as this the maximum voltage across the IGBT is limited to half the maximum DC link voltage ($V_{dc}/2$). This is down to the fact that the IGBTs are connected to the neutral point (MP) by two fast diodes called neutral clamp diodes.

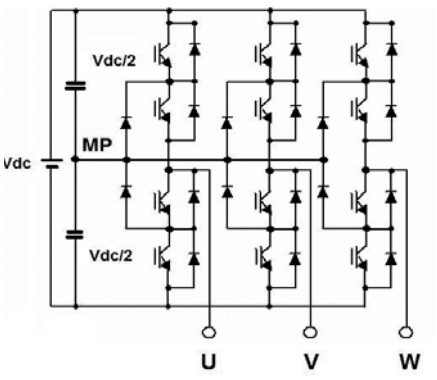

Figure 2 – Three-phase three-level inverter topology

Three-phase two-level inverter Pulse Width Modulation generation algorithms [2] can also be applied to multilevel inverters. The algorithms with a triangular carrier waveform produce the best benefits in terms of harmonic distortion reduction, i.e. a three-level inverter needs both a carrier and a reference.
In this case the number of triangular carriers is equal to L-1, L being the number of voltage levels. For a three-phase three-level inverter this means that two triangular carriers and one sinusoidal reference are needed.

Three alternative PWM strategies with differing phase relationships can be used for a three-level inverter:

- Alternative phase opposition disposition (APOD), where carriers in adjacent bands are phase shifted by 180°
- Phase opposition disposition (POD), where the carriers above the reference zero point are 180°out of phase with those below zero
- Phase disposition (PD), where all carriers are in phase across all bands

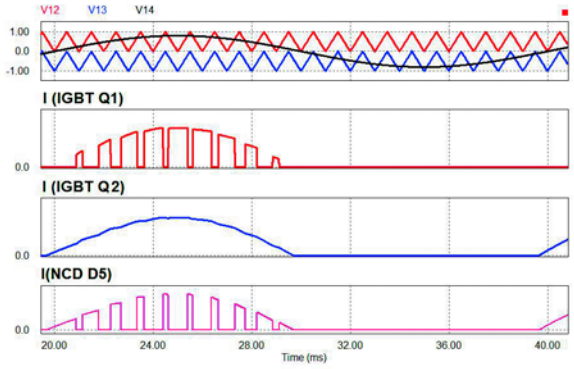

Figure 3 – Principle behind a three-level inverter

PD strategy is used most frequently because it produces minimum harmonic distortion for the line-to-line output voltage. Triangular carriers and sinusoidal reference profiles, as well as IGBT and NCD current profiles are shown in Figure 3.

A three-level inverter appears to comprise highly complex circuitry compared with a two-level inverter. The resulting technical and economic advantages, however, are the reasons why the use of three-level inverters is strongly recommended.

Here, two standard modules will be compared in the same application with identical boundary conditions, as described in Table 1 ([3],[4]). The IGBT and diode conducting and switching losses are calculated using the formulae given in Table 2 [5],[6].

A three-level inverter features an IGBT with a lower reverse blocking voltage - 600V instead of 1200V. 600V chips are normally faster and thinner than 1200V chips. The silicon in a three-level inverter therefore has lower switching losses and a lower forward voltage drop.

S = 20 kVA	cos (φ) = 0,85	f_{sw} = 20 kHz
M = 1	$V_{ll,rms}$ = 400V	$I_{out,rms}$ = 29 A
i_{pk} = 40,8 A	T_s = 80°C	

	IGBT Blocking Voltage	Ic @ Ts=80°C	Vce,sat typ @ 50A chip level	Eon+Eoff @ Ic=50A,Rg=33Ω	IGBT Rthj,s
SK 30 MLI 066	600V	31A	1,65 V	4,2mJ @ Vcc=300V, Tj= 150°C	1,8 [K/W]
SK 60 GB 128	1200V	44A	1,9 V	12,5mJ @Vcc=600V, Tj=125°C	0,6 [K/W]

Table 1 – Conditions of simulation and main IGBT parameters

As shown in Table 3, the total losses per single arm of the three-level inverter are 60% lower than those of the two-level inverter. Q2 and Q3 switching losses are negligible.

D1 and D4 diodes carry a very low current value since the current of Q1 commutes to D5; the current of Q4 commutes to D6, while the current of Q2 commutes to Q3. Clamp diodes carry the full load current.

3 Levels Inverter (3L)	
Conduction losses IGBT Q1/Q4	$P_{con} = U_o \cdot I_{avg} + r_f \cdot I_{rms}^2$ $I_{avg} = \frac{\hat{M} \cdot \hat{I}}{4\pi} \cdot \left[\sin\lvert\varphi\rvert + (\pi - \lvert\varphi\rvert)\cos\varphi\right]$ $I_{rms}^2 = \frac{\hat{M} \cdot \hat{I}^2}{4\pi}\left[1 + \frac{4}{3}\cos\varphi + \frac{1}{3}\cos(2\varphi)\right]$
Conduction losses IGBT Q2/Q3	$P_{con} = U_o \cdot I_{avg} + r_f \cdot I_{rms}^2$ $I_{avg} = \frac{\hat{I}^2}{\pi} - \frac{\hat{M} \cdot \hat{I}}{4\pi} \cdot \left[\sin\lvert\varphi\rvert - \lvert\varphi\rvert)\cos\varphi\right]$ $I_{rms}^2 = \frac{\hat{I}^2}{4} - \frac{\hat{M} \cdot \hat{I}^2}{4\pi}\left[1 - \frac{4}{3}\cos\varphi + \frac{1}{3}\cos(2\varphi)\right]$
Switching losses IGBT Q1/Q4	$P_{sw} = \frac{1}{\pi} \cdot (E_{on} + E_{off}) \cdot f_{sw}$

2 Levels Inverter (2L)	
Conduction losses Q1/Q2	$P_{on} = \frac{1}{2} \cdot \left(\frac{V_{CE_o}}{\pi} \cdot \hat{i} + \frac{r_{CE}}{4} \cdot \hat{i}^2\right) + m \cdot \cos\phi \cdot \left(\frac{V_{CE_o}}{8} \cdot \hat{i} + \frac{r_{CE}}{3 \cdot \pi} \cdot \hat{i}^2\right)$
Switching losses IGBT Q1/Q2	$P_{sw} = f_{sw} \cdot E_{sw} \cdot \frac{\sqrt{2}}{\pi} \cdot \frac{I_1}{I_{ref}} \cdot \left(\frac{V_{cc}}{V_{ref}}\right)^{K_v}$

Table 2 – Formulae used to calculate switching and conducting losses for a 3L inverter [5] and a 2L inverter [6]

SK 30 MLI 066	
IGBT: total losses per arm	118 W
Neutral clamp diode total losses (D5/D6)	28 W
Total losses per arm	146 W

SK 60 GB 128	
IGBT: total losses per arm	176,1 W
Diodes total losses	53 W
Total losses per arm	229 W

Table 3 – Analysis of losses: 3L inverter vs. 2L inverter

Figure 4 shows the overall losses as a function of the switching frequency for a single inverter leg (3L vs. 2L). In order to reduce noise pollution, UPS applications in the 20KVA range work with switching frequencies above the audible human hearing range. In this switching

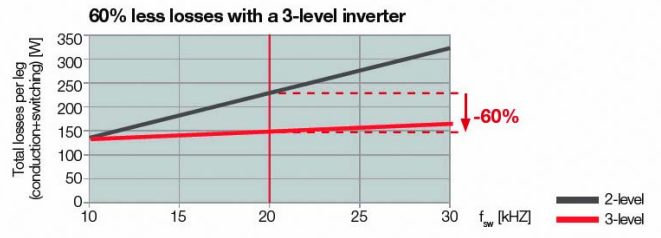

Figure 4 – Comparison between total losses per arm and frequency

frequency range, the total leg losses for a 3L inverter are significantly lower than those of a 2L inverter.

Moreover, in a 3L inverter, the output voltage waveform is very similar to a sinusoidal wave, which is why the 3L inverter needs very small output filters. Stresses acting on the 3L IGBTs and diodes are therefore reduced, thus increasing the long-term reliability and the overall application efficiency.

From an economic perspective, in this specific analysis, a 3L inverter leg based on 600V silicon is 25% cheaper than a 2L inverter leg with 1200V silicon.

The real benefit of a 3L inverter is the reduced stresses on the power switches owing to the lower losses as well as the fact that the output voltage switches through three voltage levels. The resultant output voltage waveform is almost sinusoidal with a reduced harmonic distortion, leading to the use of smaller output filters. Reduced overall losses also mean that a smaller heat sink can be used. A smaller heat sink and smaller output filter allow for reduced overall dimensions in the UPS application, which in turn reduces the overall application costs.

For the aforementioned reasons, the use of a standard SEMITOP® module in 3L inverters for UPS applications can maximize electrical and thermal efficiency, reduce the time to market and, more importantly, reduces the overall costs for the UPS application.

SEMITOP at a glance

Features of SEMITOP® modules:

- DCB in direct contact with heat sink: no baseplate needed
- A ceramic layer for insulation
- Pins for PCB soldering
- One mounting screw for easy mounting
- Current rating
  - up to 200A for 600V IGBT
  - up to 100A for 1200V IGBT
  - up to 300A for Mosfet

SEMITOP® modules allow for:

- Reduced assembly costs
- Optimum thermal resistance
  - up to -30% compared with isolated TO
  - up to -18% compared with IMS
- The combination of a wide range of topologies with a wide range of chip technologies: input bridges, inverters, AC switches, half-bridges, converter-inverter-brake, brake chopper
- Compact design with cost and space savings
- The use of pins with extremely low series resistance: up to 14% lower conducting losses than competitor technology

All modules are RoHS compliant

References:

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