Voltage-Source Active Power Filter Based on Multilevel Converter and Ultracapacitor DC Link

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***Abstract*—A new topology for active power filters (APF) using an 81-level converter is analyzed. Each phase of the converter is composed of four three-state converters, all of them connected to the same capacitor dc link voltage and their output connected in series through output transformers. The main advantages of this kind of converter are the negligible harmonic distortion obtained and the very low switching frequency operation. The single-phase equivalent circuit is analyzed and their governing equations derived. The dc link voltage control, based on manipulating the converter's voltage phase, is analyzed together with the circuit's characteristics that determine the capability to draw or deliver active and reactive current. Simulation results for this application are compared with conventional pulsewidth-modulated (PWM) converters, showing that this filter can compensate load current harmonics, keeping better-quality sinusoidal currents from the source. The simulated configuration uses a 1-F ultracapacitor in the dc link, making it possible to store energy and deliver it during short voltage dips. This is achieved by applying a modulation control to maintain a stable ac voltage during dc voltage drops. A prototype of the filter was implemented and tested, and the obtained current waveforms showed to be as good as expected.**

***Index Terms*—Active filters, multilevel systems.**

I. Introduction

MODERN power electronics have contributed a great deal to the development of new powerful applications and industrial solutions; but at the same time, these advances have increased the harmonic contamination present in line currents, which ends up distorting the voltage waveforms. Some power electronics applications, such as diode power rectifiers, thyristor converters, and static VAr compensators (SVCs), are clear examples. This has encouraged the development of passive and active filters, which are intended to block all nonfundamental current components. Passive filters have many disadvantages, such as weight, volume, frequency tuning, and cost, making their implementation sometimes unpractical. On the other hand, different configurations of pulsewidth-modulated (PWM) inverters have been implemented as active power filters (APF) to compensate harmonic currents. Nevertheless, these devices have shown to produce a series of problems in related equipment when operated at high frequencies [1], such as circulating currents, dielectric stress, overvoltage, and corona discharge. All these reasons have created many research works on the topic of PWM modulation [2]–[5].

Multilevel inverters [6]–[8] can work as amplitude modulation and PWM, and this fact makes the outputs of the converter very much cleaner. This way of operation allows having almost perfect currents, and very good voltage waveforms, eliminating most of the undesirable harmonics. The series connection of several bridges allows to work with much higher voltages [1], [9], [10], and the stepped voltage waveforms eliminate the voltage stress in associated equipment, such as transformers. Moreover, the bridges of each converter work at a very low switching frequency, which allows working with low speed semiconductors, and low switching frequency losses [11].

The objective of this paper is to show the performance advantages of a multilevel converter used as an APF. The filter is used to compensate a contaminating load with small power factor and to feed the load during voltage dips. The results are compared with conventional PWM modulators working at a switching frequency of 10 kHz.

II. Multilevel Topology Analysis

A multilevel inverter consists basically of an array of power semiconductors and converters, which produce an output voltage of stepped shape by connecting its output terminals to more than one different voltage source. The result is a voltage waveform with lower distortion and less voltage stress across the power semiconductors. Since the first multilevel inverter was patented in 1975, many different multilevel inverter topologies have been introduced and analyzed by different authors. An interesting survey of this kind of device is presented in [12].

For this particular application, a cascaded H-bridge multilevel inverter has been chosen due to special advantages, such as greater number of levels with the same number of semiconductors and lower voltage stress across some of its semiconductor terminals for the same number of output levels [12], among others.

The circuits in Fig. 1 show one phase of two alternative configurations of this type of multilevel voltage-source inverter. Both configurations are based on the series connection of more than one H bridge, whose output voltages are scaled in power of three, maximizing the number of levels obtainable (3^N levels of voltage, where N is the number of bridges in the cascade). Then, with only four converters ($N = 4$), 81 different levels of voltage are obtained: 40 levels of positive values, 40 levels of negative values, and zero [8]. The semiconductors commutate at very low switching frequency, achieving a modulated voltage waveform that can be adjusted by changing the commutation

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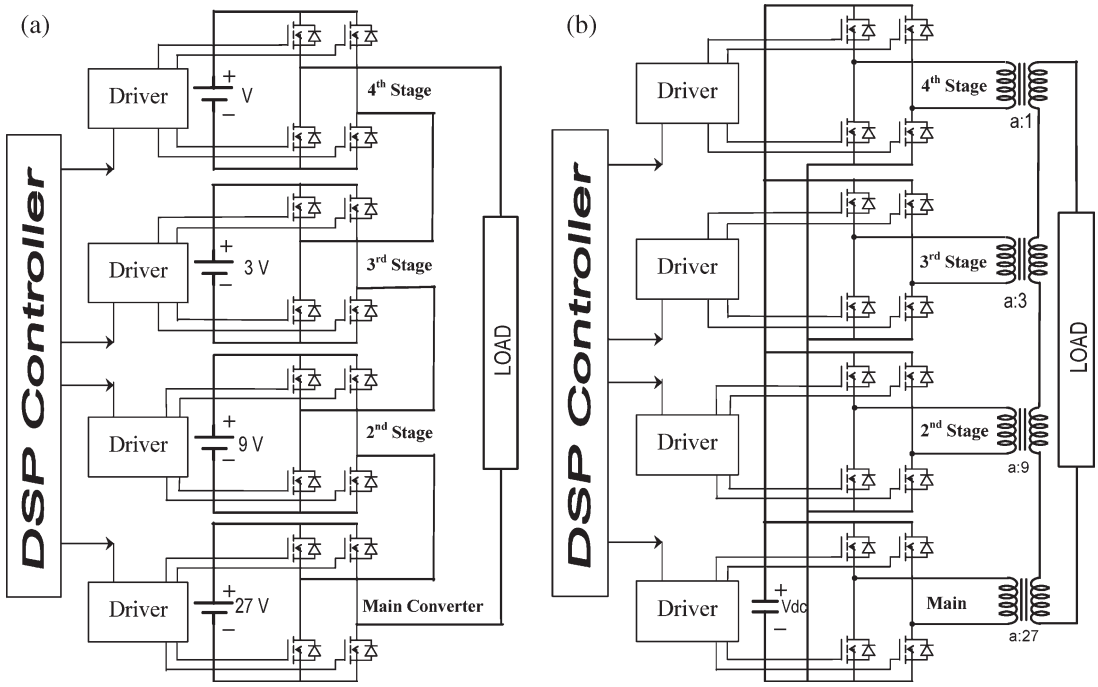

Fig. 1. Main components of a four-stage 81-level multiconverter. (a) Individual voltage sources for each module. (b) One single voltage source for all modules, and series connection via output transformers.

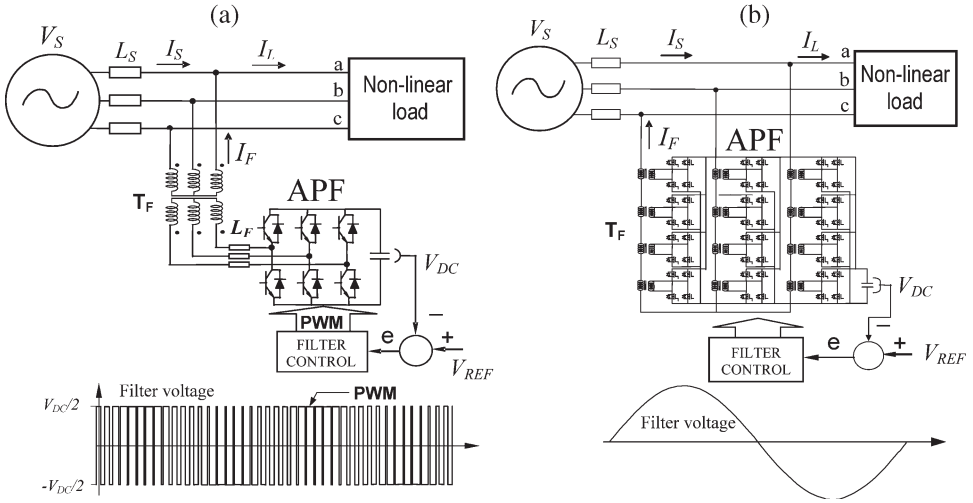

Fig. 2. (a) Shunt APF using PWM techniques. (b) Shunt APF using a multilevel inverter.

angles and/or the dc voltage. Each H bridge can produce three different voltage levels: +Vdc, −Vdc, and zero. Topology 1) consists of separated dc sources for each module and direct series connection at the ac side; topology 2) uses a single dc source for all modules and the series ac connection is interfaced by scaling transformers. While working as an active filter, although the converter's steady state active power is zero, the active power of each individual module may be different from zero. Therefore, the topology 2) was used because it avoids the need for isolated energy-balancing devices if capacitors are used as individual dc storage devices. In this case, a single capacitor for all the three phases is used at the dc link for temporary energy storage instead of four floating capacitors for each phase, which represents a great simplification in the design of the APF. Besides, all the power transistors operate at the same voltage rating. For scaling the output voltage at the ac side, the transformers' turn ratios are scaled in power of 3, and the one located at the bottom in Fig. 1(b) has the highest voltage ratio (a:27) and works at the lowest switching frequency (equal to the main frequency). The converter connected to this transformer is called the Main Converter because it manages most of the reactive power. The ratings of the transformers are from bottom (Main Converter) to top: 0.675, 0.225, 0.075, and 0.025 pu.

III. APF Configuration

Fig. 2(a) shows a typical configuration for a shunt APF using PWM strategy. The source is feeding a contaminating load, such as a power rectifier. The APF, connected in parallel, injects the harmonic currents to the load and the power system sees a

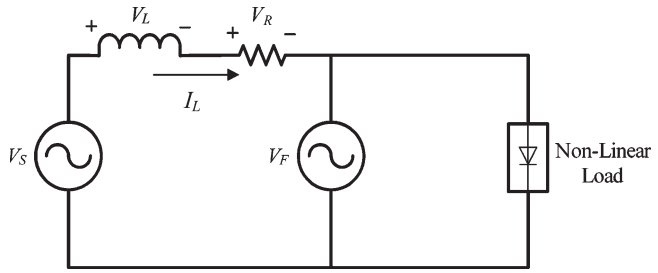

Fig. 3. Single-phase equivalent circuit.

cleaner sinusoidal current waveform. Nevertheless, the PWM filter produces significant switching looses and electromagnetic noise, and its output voltage [also shown in Fig. 2(a)], as well as its current, has high frequency noise content. Fig. 2(b) shows the proposed topology for a shunt APF using the multilevel converter described before. It can be seen that the voltage generated by this filter is quite similar to a sinusoidal waveform. The small steps of each level are almost negligible. The contrast between these two technologies is evident.

One of the advantages of the proposed configuration is that better current signals are achieved with very low commutation frequencies. The multilevel inverter is connected in parallel with the contaminating load and is operated as a voltage-source inverter, modulating a sinusoidal voltage at its terminals. If the inverter's output impedance is significantly lower than the line's impedance, then the filter should supply the load's harmonic currents almost completely. Three four-stage multiconverters, like the one shown in Fig. 1(b), are connected to the same capacitor at the dc side and in Y configuration at the ac side. Capacitor voltage is simply controlled by manipulating the voltage phase angle between the filter and the source, thus controlling the amount of active power flowing to and from the filter. The output voltage is practically sinusoidal as shown in Fig. 2(b). Therefore, the filter feeds practically all harmonic currents consumed by the load.

Assuming the filter's behavior is practically equivalent (in steady state) to that of a sinusoidal voltage source, the power analysis can be done considering the multilevel inverter as a sinusoidal voltage source in parallel with the load. Nevertheless, the fact that this voltage source cannot deliver active power in the long term has to be taken into account for control analysis. Fig. 3 shows a single-phase equivalent of the circuit formed by the source, the line, the filter, and the contaminating load.

Fig. 4 shows phase diagrams of the source voltage, filter voltage, and line current for different angles and amplitudes of the filter's voltage. The line impedance is considered to have a predominant inductive component (compared to the resistive component), as a general assumption. This characteristic will determine the filter's ability to draw active power from the source. The line parameters, as it will be shown later, have a great influence on the filter's behavior, a fact that has to be taken into account in the design of the control system.

The interaction between two voltage sources, interfaced by the line impedance (under steady state), is governed by the geometrical relations between their voltage amplitudes and the angle between them. This is expressed graphically in Fig. 4(a) and (b). When both voltages are in phase, and the filter's voltage amplitude is manipulated, reactive power can be controlled but no active power control is achieved, as shown in Fig. 4(a). On the other hand, when both amplitudes are fixed and the angle is manipulated within small values, then mostly active power flow is controlled, as shown in Fig. 4(b). These relations will govern the active power flow behavior and therefore the dc capacitor charge will be controlled by this means. The error between the measured voltage of the dc link capacitor and a voltage reference feeds a PI controller, which manipulates the phase angle between the filter voltage and the source voltage.

In order to characterize precisely this interaction, the equations that represent these geometrical relations are derived. Using the $d-q$ frame shown in Fig. 4(c), we obtain

$$V_F^d - V_S^d = -RI^d + XI^q \tag{1}$$
$$V_F^q - V_S^q = -RI^q - XI^d \tag{2}$$

where

$$V_F^d = V_F\sqrt{3} \tag{3}$$
$$V_F^q = 0 \tag{4}$$
$$V_S^d = V_S\sqrt{3}\cos(\alpha) \tag{5}$$
$$V_S^q = -V_S\sqrt{3}\sin(\alpha). \tag{6}$$

The $d-q$ frame used is fixed to V_F because in this way the active and reactive current expressions (I^d and I^q) are referred to the load node. The angle α is referred to V_S and therefore the angle shown in Fig. 4(c) is negative. Combining (1)–(6), expressions for I^d and I^q [in steady state] can be derived

$$I^d = \frac{-RV_F\sqrt{3} + RV_S\sqrt{3}\cos(\alpha) - XV_S\sqrt{3}\sin(\alpha)}{(R^2+X^2)} \tag{7}$$

$$I^q = \frac{XV_F\sqrt{3} - XV_S\sqrt{3}\cos(\alpha) + \frac{X^2}{R}V_S\sqrt{3}\sin(\alpha)}{(R^2+X^2)} - \frac{V_S\sqrt{3}\sin(\alpha)}{R}. \tag{8}$$

These equations can be plotted in terms of the relation X/R to explore the filter's capability to draw active power from the source. Fig. 5 shows plots of I^d and I^q for different X/R ratios.

The plot for I^d shows that the more inductive the line, the greater the active current that can be drawn from the source by the filter to be delivered to the load. It should also be observed that for every line impedance ratio (X/R) there is an angle at which a maximum amount of active current can be drawn. Over this angle, the active current decreases, and this implies that some kind of adaptive control system has to be implemented in order to adjust the changes in the line. If the derivate of (7) equals to zero is solved, the angle at which maximum active power is transferred is obtained. This angle is such that $\tan\alpha = -X/R$. In addition, it can be noted that I^q is always positive when power is drawn from the source $(I_d > 0)$, meaning that the line current is always ahead of the filter's voltage and therefore $\cos(\phi)$ is positive in these cases. For these plots, the line impedance was maintained at 0.25 pu.

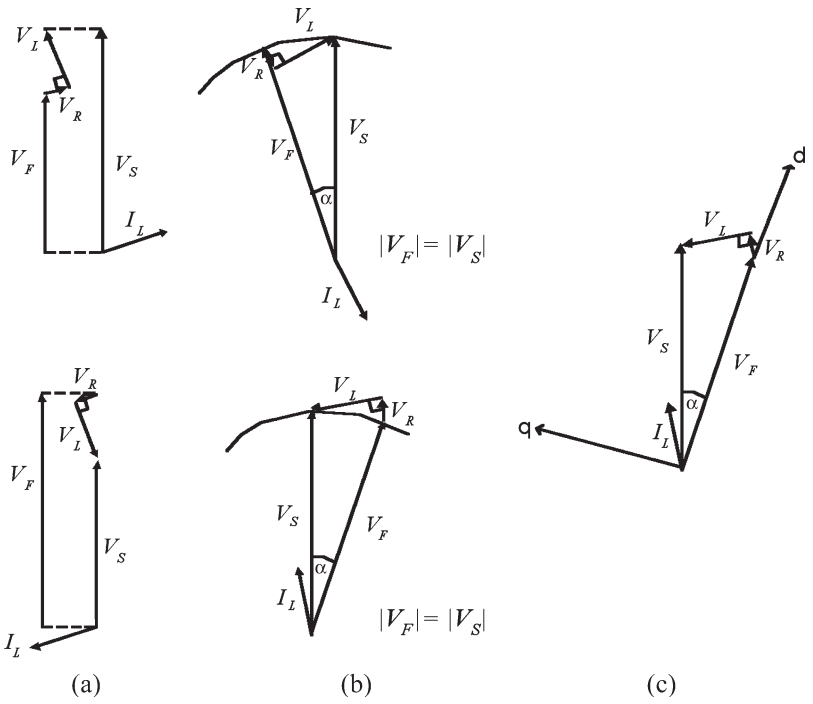

Fig. 4. Phase diagrams of voltages and currents, where $I_{\text{Line}} = I_L$. (a) Reactive power control. (b) Active power control. (c) General control.

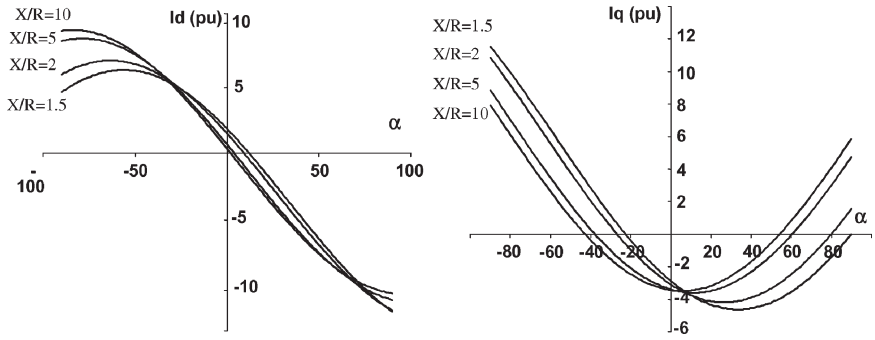

Fig. 5. Active (I_d) and reactive (I_q) currents supplied by the source at the filter node.

IV. Simulation Results

Fig. 6 compares the current quality obtained with (a) a shunt APF implemented with a PWM inverter working at 10-kHz switching frequency and (b) with the four-stage (81-level) converter described in this paper. Both figures show the load current (a three-phase diode rectifier), the source current, and the filter current. The parameters are the same for both systems: Vsource $= 120$ Vff, line impedance $Z_L = 0.01 + j0.314\ \Omega$, rectifier input impedance $Z_R = 0.1 + j0.157\ \Omega$, rectifier output dc load $R_D = 5\ \Omega$ plus a smoothing reactor $L_S = 20$ mH. The commutation frequencies for the semiconductors in the multilevel inverter are considerably lower than in the PWM inverter. The Main Converter with a voltage ratio transformer of a:27 [where "a" represents a voltage ratio used as a reference for all transformers, as described in Fig. 1(b)] commutates at fundamental 50 Hz, and the modules with voltage ratios of a:9, a:3, and a:1 commutate at 250, 850, and 2650 Hz, respectively.

Another point of comparison is the cost. As stated in Section II, lower-order modules take a very small portion of the total reactive power and hence do not contribute to drastically increase the cost of this method (the ratings of the transformers are from bottom to top in Fig. 1(b): 0.675, 0.225, 0.075, and 0.025 pu). In fact, it is possible that the cost could result lower than with conventional PWM techniques, because this system uses components that are cheaper for their lower frequency ratings and simplicity (smaller single-phase units) compared with the one required in Fig. 2(a) for PWM–APF.

Another capability of this system is to work as a voltage dip proof source. To implement this capability, a capacitor of very high capacity (ultracapacitor) has to be used, and the modulation index (m) is manipulated to maintain a nominal voltage at the output. When a voltage dip appears, m is manipulated to maintain a nominal voltage at the inverter terminals. In this case, an automatic isolating device would have to be implemented between the source and the load in order to feed the load from the filter without feeding the rest of the system.

An example of the aforementioned filter was simulated using the software PSIM [13]. The parameters of the system are $V_S(\text{source}) = 380$ Vff, line impedance $Z_L = 0.1 + j0.569\ \Omega$, diode rectifier input impedance $Z_R = 0.1 + j0.157\ \Omega$, rectifier output dc voltage $V_D = 500$ V, load $R_D = 5\ \Omega$ plus a

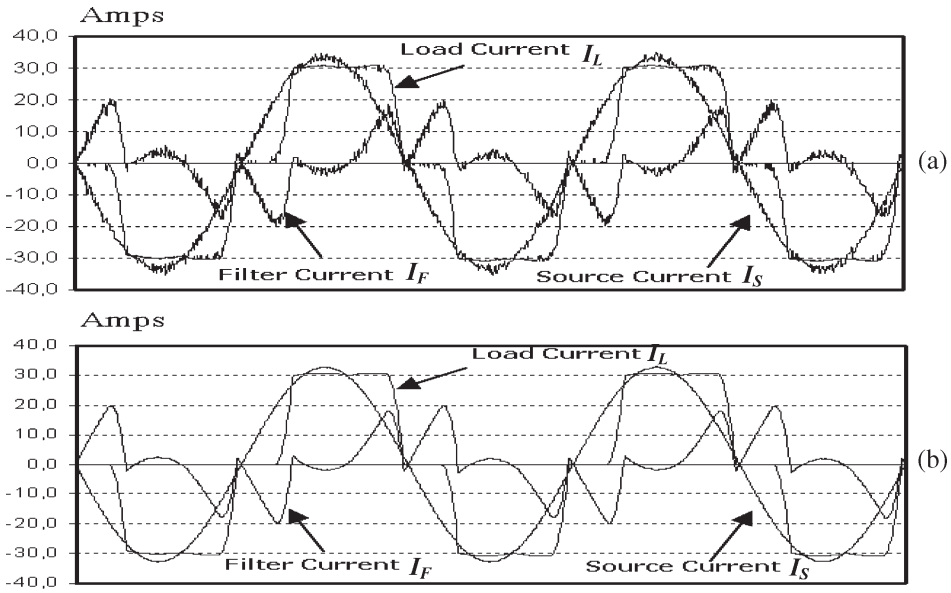

Fig. 6. APF waveforms. (a) PWM technique. (b) Proposed technique.

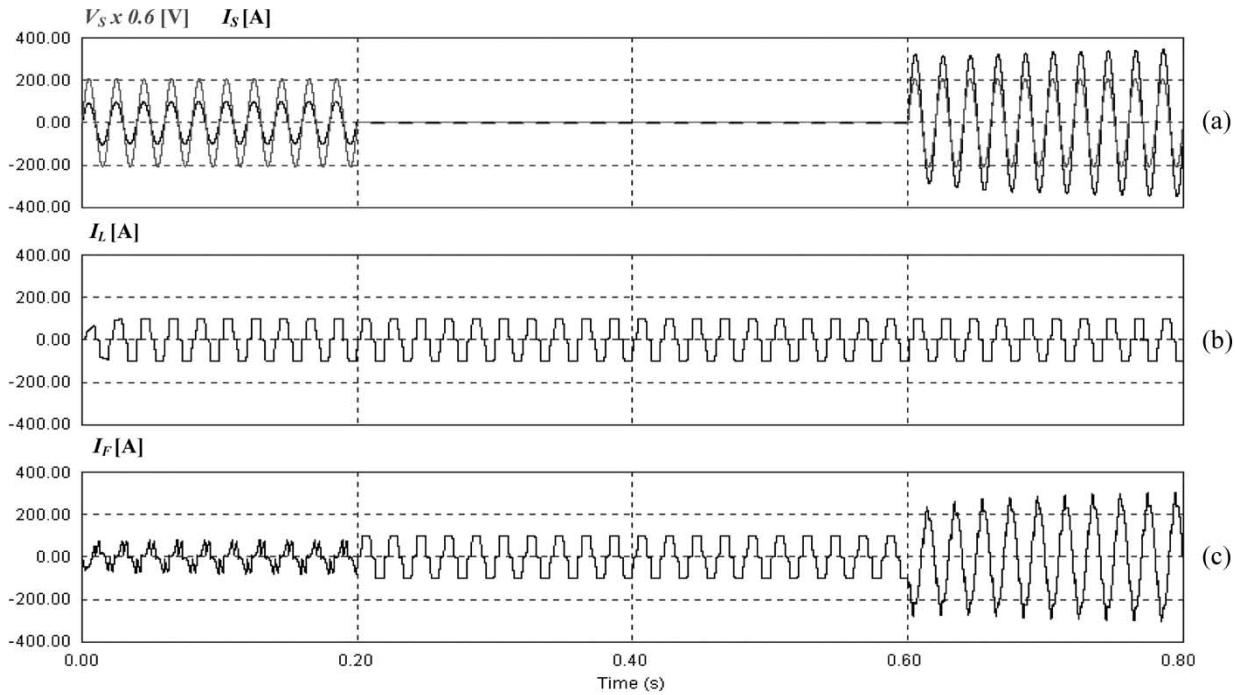

Fig. 7. Currents waveforms from simulation. (a) Source current and scaled voltage. (b) Load current. (c) Filter current.

smoothing reactor $L_S = 40$ mH. This represents a dc load of approximately 50 kW.

A voltage dip is simulated at $T = 0.2$ s, with a duration of 0.4 s. During this period, the load was fed from the filter's capacitor and a sinusoidal voltage of nominal amplitude is maintained at the filter's output.

Fig. 7 shows a plot of the (a) source voltage (V_S) and current (I_S), (b) load current (I_L), and (c) filter current (I_F) during the simulation. The source voltage (scaled) allows appreciating the power factor from the source. During the voltage dip (between $T = 0.2$ s and $T = 0.6$ s), there is no current flowing from the mains for obvious reasons.

As can be seen in Fig. 7, the source currents are perfectly sinusoidal and with unity power factor. In addition, the load currents are completely fed by the filter during the voltage dip. This demonstrates that this kind of multiconverter works perfectly as a voltage dip proof filter, delivering near-sinusoidal voltages.

Fig. 8 shows details of voltages and currents during the experiment. When the source goes offline, the filter starts delivering all the current consumed by the load.

Fig. 9 shows the (a) source voltage, (b) dc link capacitor voltage, and (c) capacitor current. It is clear that when the source goes offline, the capacitor starts delivering all the active power, depressing its voltage. The ultracapacitor voltage drop

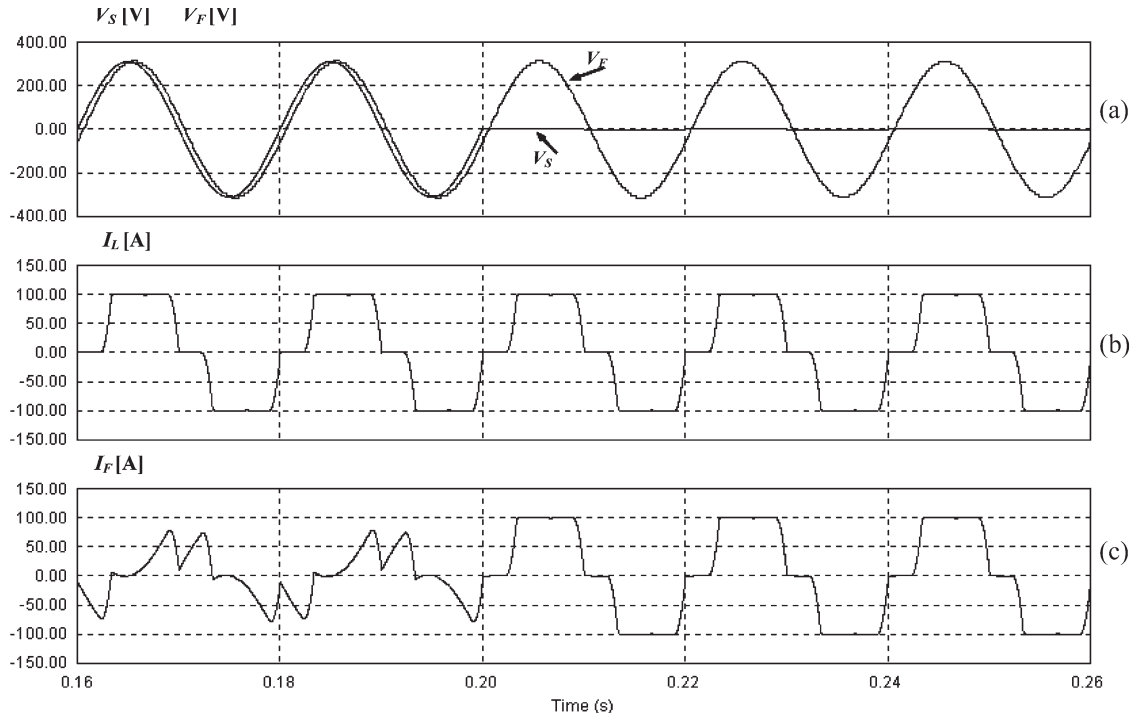

Fig. 8. Detail of (a) voltages, (b) load currents, and (c) filter current when the fault occurs.

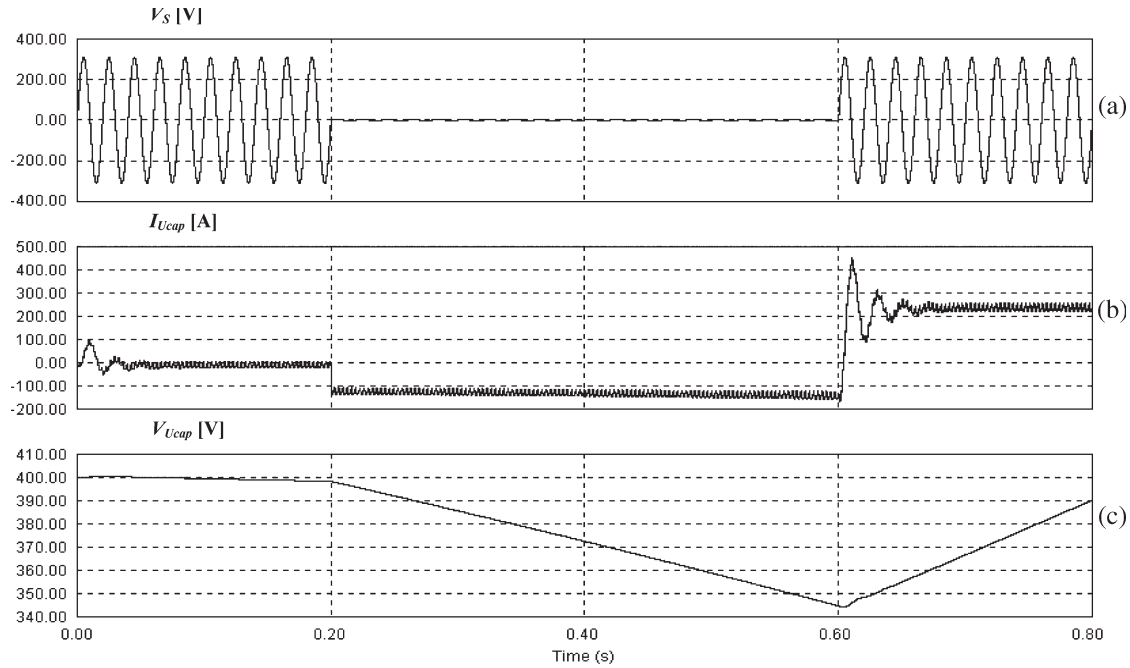

Fig. 9. Detail of (a) source voltage, (b) capacitor current, and (c) capacitor voltage.

represents the energy supplied by the capacitor during the voltage dip. After the voltage from the source is reestablished, the control modifies the filter's voltage angle to inject active power to the filter and recover the capacitor's voltage level.

V. Experimental Results

Fig. 10 shows an experimental inverter like the one in Fig. 1(b), which was implemented for testing. The transformer ratios are scaled in power of 3, yielding a total of 81 different voltage levels at the inverter terminals. The source voltage is 110 V fn, and the dc capacitor voltage reference at the APF is set to 146 V to achieve a nominal voltage at the inverter terminals under steady state. The line impedance is $Z_L = 1.43 + j4.4\ \Omega$, and rectifier (nonlinear load) output dc load $R_D = 27\ \Omega$ plus a smoothing reactor $L_S = 65$ mH. The equivalent power load is 2.5 kW.

Fig. 11 shows a detail of the (a) source voltage V_S, (b) source current I_S, (c) filter current I_F, and (d) load current I_L. It is easy to see that the source current waveform has almost no

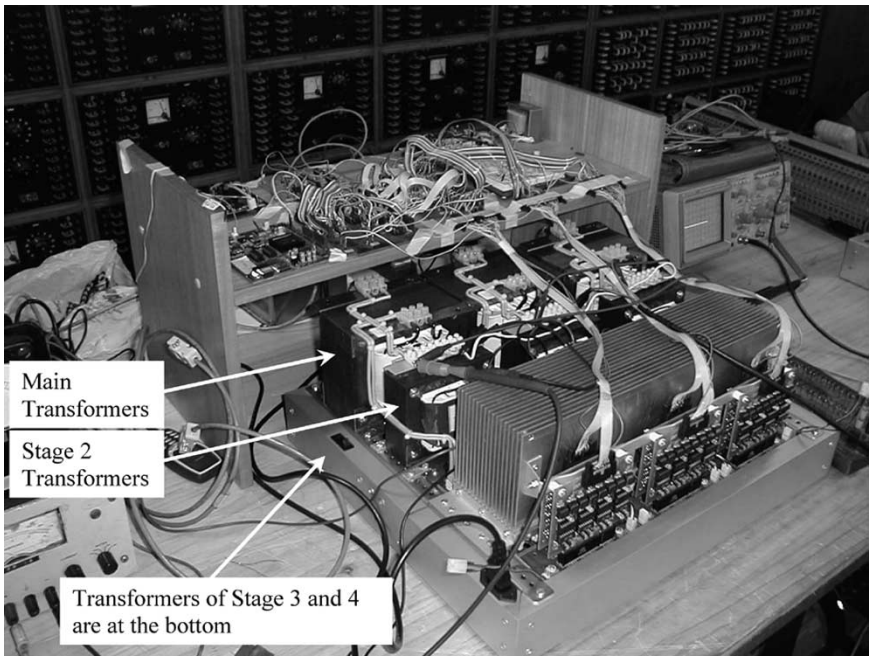

Fig. 10. Experimental 2.5 kW 81-level prototype.

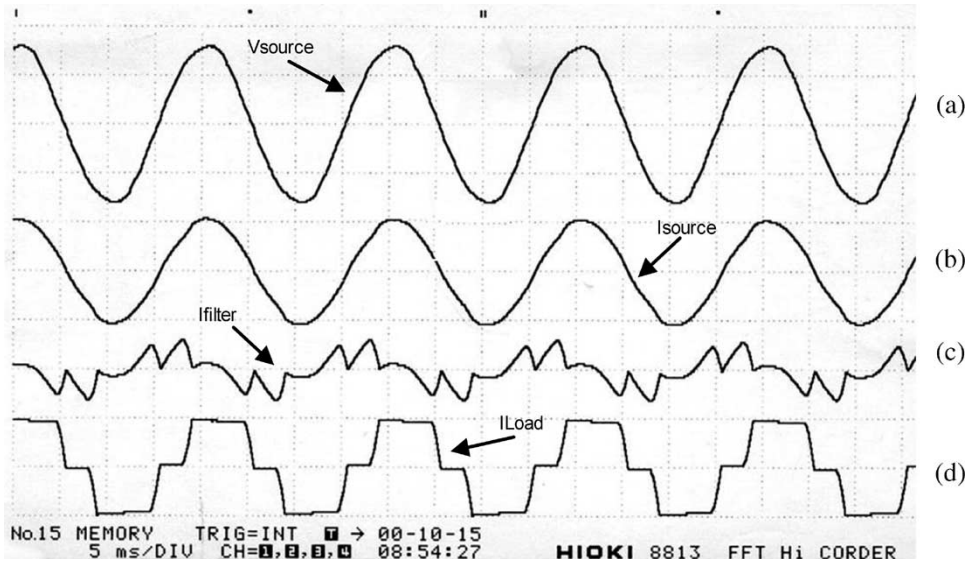

Fig. 11. Detail of source, filter, and load current (10 A/div), and source voltage (100 V/div).

harmonic content and is practically in phase with the source voltage while the filter delivers all of the harmonic content.

The waveforms in Fig. 12 present the transient behavior of the filter. During the connection of a load, the control takes a couple of cycles to reach steady state. In case of disconnection, the time is a little longer because of the arc of the switch being used to extinguish.

Although this is a voltage-source inverter, small parasitic inductors are unavoidably present in series to the inverter terminals because of the transformer's leakage inductances. Anyway, this is not at all bad, because it helps filtering the dv/dt of the small voltage steps of the converter, avoiding current peaks if the load has a voltage-source characteristic (i.e., capacitors). The drawback of these inductances is that a voltage distortion is generated when the filter has to compensate harmonic currents of high di/dt. Therefore, transformers of low leakage inductance should be used. This distortion and the lagging angle of the filter's voltage are shown in Fig. 13.

VI. Conclusion

A four-stage 81-level inverter using three-state "H" converters was analyzed, simulated, and tested for use as an APF. It has been shown that some of the advantages of this kind of converter compared with conventional PWM converters are lower commutation frequency and better quality of voltage and current waveforms. Some of the drawbacks are higher semiconductor count and extra transformers needed.

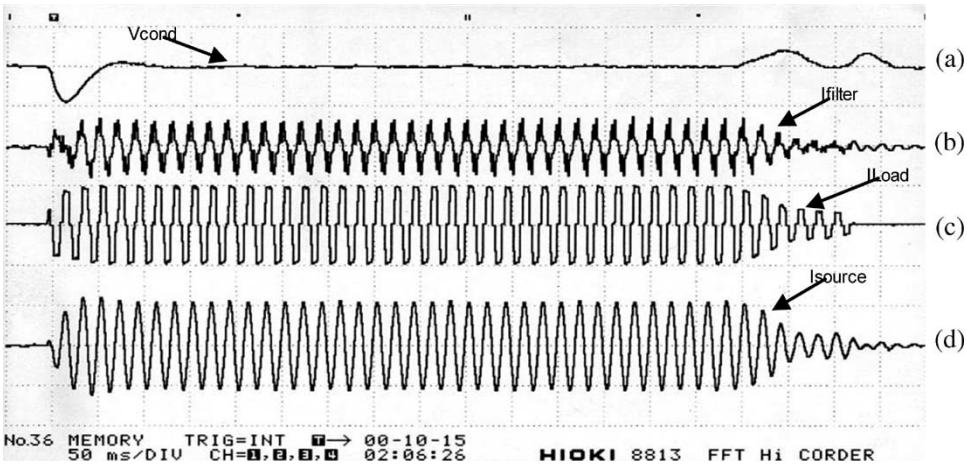

Fig. 12. Transient response. Capacitor voltage (20 V/div); filter, load, and source currents (10 A/div).

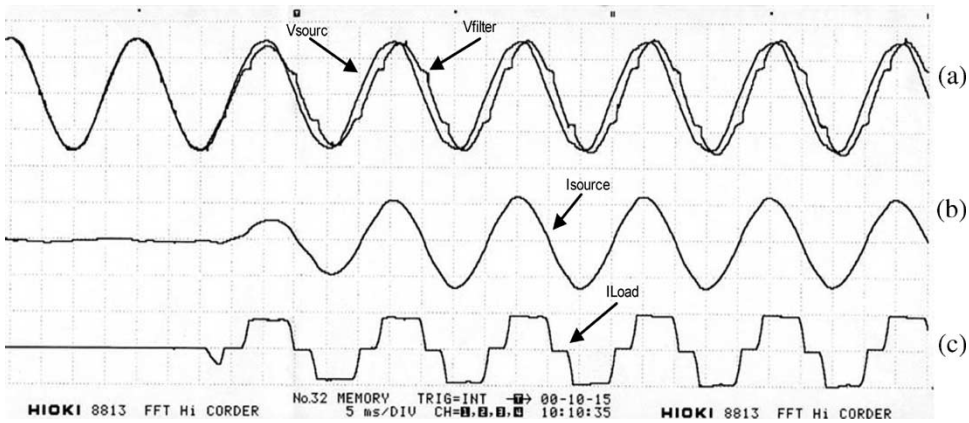

Fig. 13. Filter voltage distortion detail. Source and filter voltages (100 V/div); source and load currents (10 A/div).

A simple control scheme has been used, which consists of modifying the filter's voltage angle while maintaining nominal voltage amplitude. This control scheme allows to easily modify the amount of active power transferred to or from the filter and thus control the dc capacitor voltage. Nevertheless, a control system for this kind of filter would have to incorporate adaptive features to adapt to changes in the line parameters.

The proposed filter, compensating a contaminating load, was simulated, including a voltage dip during the experiment. Simulation waveforms showed that source currents were always sinusoidal and with high power factor, while the voltage at the load terminals were sinusoidal at all times.

A prototype of the proposed inverter was constructed and operated as an APF. The experiment showed that this kind of equipment behaves perfectly if operated within its capabilities, delivering all current harmonics consumed by the load, responding and stabilizing quickly to transient changes in the load. Moreover, the experiments showed remarkably good quality current and voltage waveforms, without the usual high frequency content present in PWM inverters. It was also shown that the transformer's characteristics could distort the voltage signals if the leakage inductances are significative.

The proposed APF can work perfectly as a voltage dip protection if a relatively high capacitance device, like an ultracapacitor, is used. Even a UPS capability could be implemented if devices of higher energy storage capacity (such as batteries) are used at the dc link terminals. In such a case, a current sensor and some changes to the control system would have to be implemented.

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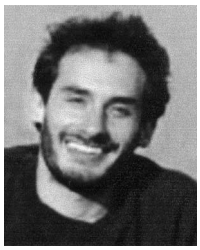

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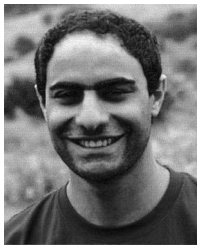

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