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A comparative analysis of different pulse width modulation methods for low cost induction motor drives

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ABSTRACT

Many pulse width modulation (PWM) methods for low cost induction motor (IM) drives have been proposed to design high performance industrial motor drives. However most of them have unbalance three phase output currents due to the dynamic unbalance between the two capacitors. Three different PWM methods, namely; hysteresis current control, sinusoidal pulse width modulation (SPWM) and a novel four switch low cost IM drives are discussed in this paper. The second one, namely SPWM, is based on the generalization of existing methods, and the third one is the proposed method, which is an improvement over the two other methods. Although all three schemes can provide three output currents with 120° phase shift for IM drive, the proposed technique is superior to others in achieving more precise current control with minimum distortion and harmonic noise, and at the same time, negligible unbalance in output currents. Simulation and experimental results of hysteresis current control, SPWM method and new proposed method is presented in order to confirm the effectiveness of proposed method in providing balanced three phase output currents and voltages.

1. Introduction

PWM voltage source inverters (VSI) are used in a wide variety of industrial applications, such as uninterruptible power supplies (UPS), static frequency changers, and variable-speed motor drives [1]. Industrial applications require variable-speed motor drives. AC synchronous and induction machines are rugged and economical, and thus are excellent choices for industrial applications [2]. Historically, AC motors have been used mainly for constant-speed applications. Recent progresses in power electronic devices such as isolated gate bipolar junction transistor (IGBT), and microelectronics such as fast digital signal processor (DSP) based microcontrollers, have made them suitable and efficient for variable-speed motor drives [1,2]. In many applications, especially in low power range, a further cost reduction in the converter is an important aspect. Development of low cost motor drive systems is a relevant topic, particularly when the power demanded by the target application is within the low power range [3,4]. For this reason, the three phase component-minimized voltage source inverter has been proposed and its performance compared to the conventional three phase inverter for driving an induction motor. Several articles report on Four Switch Three Phase voltage source Inverter (FSTPI) structure regarding inverter performance and switch control [3–5]. The FSTPI generates four active vectors in the plane, instead of six, as generated by the Six Switch Three Phase voltage source Inverter (SSTPI) topology [6]. In [3] four switch (B4) inverter employing four switches and four diodes is suggested as a practical alternative to the six switch (B6) inverter with six switches and six diodes. Meanwhile in B4 inverters, since one of the motor phase windings is connected directly to the neutral point of the dc-link capacitors, the single phase current flowing into the dc-bus will directly charge one of the capacitors and discharge the other. This can cause significant fluctuations of the dc-bus voltage and subsequently unbalance three phase currents at the inverter output, thus, requires much larger dc-link capacitors [4]. Van der Broeck and Skudelny in [5] discussed the harmonic effects of a two phase PWM inverter reducing the number of switching devices at the output stage from six to four and the method of generating three phase waveforms with two dc-link voltages. The modulation strategy suggested can produce three phase balanced sinusoidal waveforms at a reduced output voltage of 0.866 compared with the conventional six switch inverter. The analysis of harmonic losses and torque pulsation produced by the B4 inverter was carried out assuming that the switching frequency is much higher than the fundamental frequency. In that case, one can provide that the fundamental voltage and current values are approximately constant during a switching period. High switching frequency, however, may actually cause a reduction of efficiency, as switching losses in such a system account for a considerable amount of the total losses. A general PWM method so called scalar space vector

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modulation method has been applied for compensation of dc-link voltage fluctuations for four switch three phase inverter in Ref. [7]. With compensation of dc-link voltage ripples three balanced voltages and currents will be provided at the output of four switches inverter without need to extra circuitry in uncontrolled rectifier side. Various carrier-modulated PWM techniques are presented in [8,9], where SPWM is one of these methods implemented in B4 inverters to compensate the dc-bus voltage fluctuations [8,9]. In these papers, a dual ac drive system is suggested to minimize the single phase current flowing through the dc-link capacitors and to eliminate the dc-bus voltage fluctuations. This topology had the capability of delivering sinusoidal input currents with unity power factor and bi-directional power flow. However, the proposed system requires complex control strategies and additional hardware to control converter/inverter at the same time. In another scheme proposed in Ref. [10], the standard diode bridge rectifier is replaced by a single phase current controlled rectifier employing two switches and two capacitors enabling input current and input power factor control. This structure, with six power switches has the capability of bi-directional power flow with balanced three phase output voltages for ac motor drives. Authors of Ref. [11] proposed a new strategy that utilizes front end rectifier, which enables unity input power factor and an improved dc-link voltage fluctuations that provides three balanced currents in the output of inverter. Direct torque control technique has been applied for four switch IM dive [12]. Even though simulation results demonstrated balanced three phase output currents of four switch inverter but no experimental waveforms of such voltages and currents available for comparison and validation of the proposed method in practice. An adaptive space vector modulation (SVM) approach to compensate the dc-link voltage ripple in a B4 inverter has been proposed in Ref. [13]. Simulation and experimental results clearly confirm the significant improvement of three phase currents in inverter output. Ref. [14], proposed hysteresis current controller technique for B4 inverter. Inherently, this scheme has fast dynamic response and it is suitable for IM drives with SSTPI, but in FSTPI structure, the hysteresis band limitation increases the output current distortion. Meanwhile, in this scheme the switching frequency is variable that makes the output filter design difficult. Experimental results demonstrate high distortion and unbalanced three phase output currents with high THD. The current controlled PWM method, instead of the voltage controlled PWM, which called "*direct current controlled PWM*." has been applied for four switch three phase brush less dc motor (BLDC) drive [15]. Even though the output currents have acceptable waveforms with 120° phase shift but, they contain more current ripple than with the six switch inverter, that it can be reduced by controlling the hysteresis band size. Reducing the hysteresis band size will cause significant switching losses and consequently will reduce efficiency of overall control system. The utilization of three different configurations of induction motor drives such as; a standard three phase machine; a three phase machine with two windings and a standard two phase machine for the implementation of low cost systems for low-power applications, has been investigated in Ref. [16]. However, the utilized strategies are well-known and have been already introduced by other researchers. The output voltage integral control technique has been applied for compensating non-ideal dc-link bus in six switches voltage source inverters [17]. The technique is based on integrating the output voltage at a constant frequency on a pulse-by-pulse basis to ensure a sinusoidal volt–sec (v/s) distribution, irrespective of the non-ideal input dc-bus. The hysteresis band controlled four switch inverter fed interior permanent magnet synchronous motor (IPMSM) has been investigated in Ref. [18]. The system shows good dynamic performance but, the experimental results demonstrated high THD for inverter's output currents.

In this paper, a novel cost effective four switch three phase inverter fed IM drive is developed and simulated. A performance comparison of the proposed FSTP inverter with SPWM and conventional hysteresis methods is also made. The hysteresis current controller is a conventional scheme that has been employed in low cost four switch inverters by many researchers [14,18]. The SPWM strategy has been applied in FSTP inverters for compensation of dc-bus voltage fluctuations in controlled rectifier [8,9], but, unfortunately, only the simulation and experimental current and voltage results of the controlled rectifier have been demonstrated and no simulation and experimental results of IM currents and voltages are available for inverter performance evaluation. In present paper the performance of SPWM method in providing the slightly balanced output currents and voltages in FSTP inverters will be investigated. The new proposed method utilizes inherently the dc-bus ripple and voltage imbalances and generates gating signals required to produce high-quality sinusoidal output currents and voltages. The technique is based on integrating the output voltage at a constant frequency on a pulse-by-pulse basis to ensure a sinusoidal volt–sec distribution, irrespective of the input dc-bus fluctuations [17]. This scheme by considering B4 inverter asymmetric voltage vectors and dc-link capacitors voltage imbalance, will propose a simple modulation strategy based on output voltage integral control. The proposed modulation technique is based on the cycle-by-cycle control of the output voltage, thus providing a higher quality output waveform. This modulation technique either in simplicity of the equations or hardware and software implementations, is preferred to the previous modulation methods.

In order to have an online performance comparison between the SPWM method with hysteresis current control a prototype 2.2 kW induction motor drive test-bed with the Intel 80C196KD microcontroller [19] is built to provide the experimental results. The validity and effectiveness of the proposed method will be verified only by simulation and will be compared with the simulation and experimental results of proposed SPWM and conventional hysteresis current control schemes.

The main contributions of this paper in relation to previous works are:

- introducing a novel method namely: "the output voltage integral control modulation for low cost three phase IM drives";
- a detailed study of the SPWM strategy in four switch three phase inverter;
- an overall comparison of conventional hysteresis method with SPWM and novel proposed schemes;

This paper is organized as follows; after the Introduction in Section 1, Section 2 gives the extended mathematical model, theoretical background, and a brief description of the B4 inverter. Next, Section 3 describes the development of proposed algorithms, followed by Section 4 presenting simulation results of the proposed approach. The performance of the SPWM method and hysteresis current controller is tested by simulations and experimentations presented in Section 5 and finally, Conclusions are presented in Section 6.

2. Comparison between inverter topologies

A circuit diagram of the B4 inverter is illustrated in Fig. 1. The topology employs four switches and four diodes to generate two line–line voltages, V_{13} and V_{23}, whereas V_{12} is generated according to Kirchhoff's voltage law [20] from a split-capacitor bank in the dc-link. Due to the circuit configuration, the maximum obtainable peak value of the line–line voltage equals $V_{dc/2}$. In comparison with

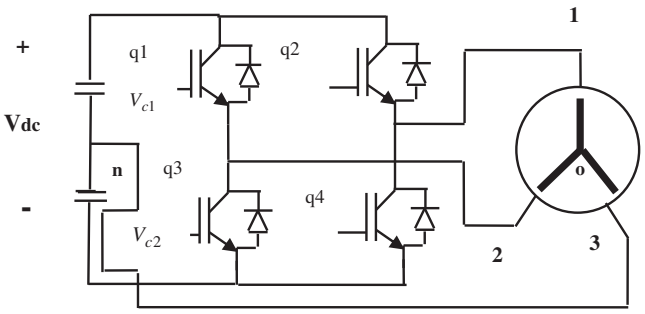

Fig. 1. B4 inverter configuration.

a B6 inverter, a number of attractive features can be noticed, where it is assumed the same load for the two inverters, such as:

- a semiconductor reduction of 1/3 is obtained and two IGBT drive circuits can be omitted because only two inverter legs are used;
- the conduction losses can be reduced with 1/3 because only two inverter legs will conduct compared with a B6 inverter, where three inverter legs will conduct;
- potential for reduced price because of the reduction in the number of switches.

Despite these advantages, the main shortcomings of this topology are;

- decreased voltage gain and thereby increased current rating for the devices at the same output power;
- increased voltage stress on both power devices and induction machine if the same output voltage should be kept [21];
- large variations and unbalances of the voltage across the two dc-link capacitors caused by one phase circulating current [21].

Different comparisons are more detailed in [3,4].

With respect to the circuit shown in Fig. 1 it is assumed that the conduction states of the power switches are associated with binary variables q_1 to q_4. Therefore, a binary "1" will indicate a closed switch, while "0" will indicate the open state. Pairs q_1–q_3 and q_2–q_4 are complementary and, as a consequence, $q_3 = 1 - q_1$ and $q_4 = 1 - q_2$. Also it will be assumed that a stiff voltage is available across the two dc-link capacitors, and $V_{c1} = V_{c2} = V_{dc/2}$, where V_{dc} corresponds to a stiff dc-link voltage. Pole voltages V_1, V_2, V_3 (line to "n" the center point of split capacitors, voltages) depend on the states of the power switches. They can be expressed in terms of the binary variables q_1 and q_2, and the dc-link voltage as follows:

$$V_1 = (2q_1 - 1)V_{dc/2} \quad (1)$$

$$V_2 = (2q_2 - 1)V_{dc/2} \quad (2)$$

$$V_3 = 0 \quad (3)$$

In the four switch configuration, there are four switching status as shown in Figs. 1 and 2 such as (0, 0), (0, 1), (1, 0), and (1, 1), in which the motor load is replaced by a resistive load [15]. In the case of the six switch converter, switching status (0, 0) and (1, 1) are regarded as zero-vectors, which cannot supply the dc-link voltage to the load, so that current cannot flow through the load. However, in the four switch converter, one phase of the motor is always connected to the midpoint of the dc-link capacitors, so that current is flowing even at the zero-vectors, as shown in Fig. 2a and c [15]. Moreover, in the case of (0, 1) and (1, 0), the phase which is connected to the midpoint of dc-link capacitors is uncontrolled and only the resultant current of the other two phases flow through this phase. If the load is ideally symmetric and capacitors voltage are equal, there is no current in uncontrolled phase in the (0, 1) and (1, 0) vectors. Large variations of the voltage across the two dc-link capacitors caused by one phase current circulating through the capacitive bank, will cause significant ripples, distortions, and unbalances in inverter output currents [3,4]. Two of the inverter switching states (1, 1), (0, 0) cause unequal loading of the split dc-link capacitors. This causes one half of the link to discharge at a faster rate than the other, resulting in the generation of a voltage

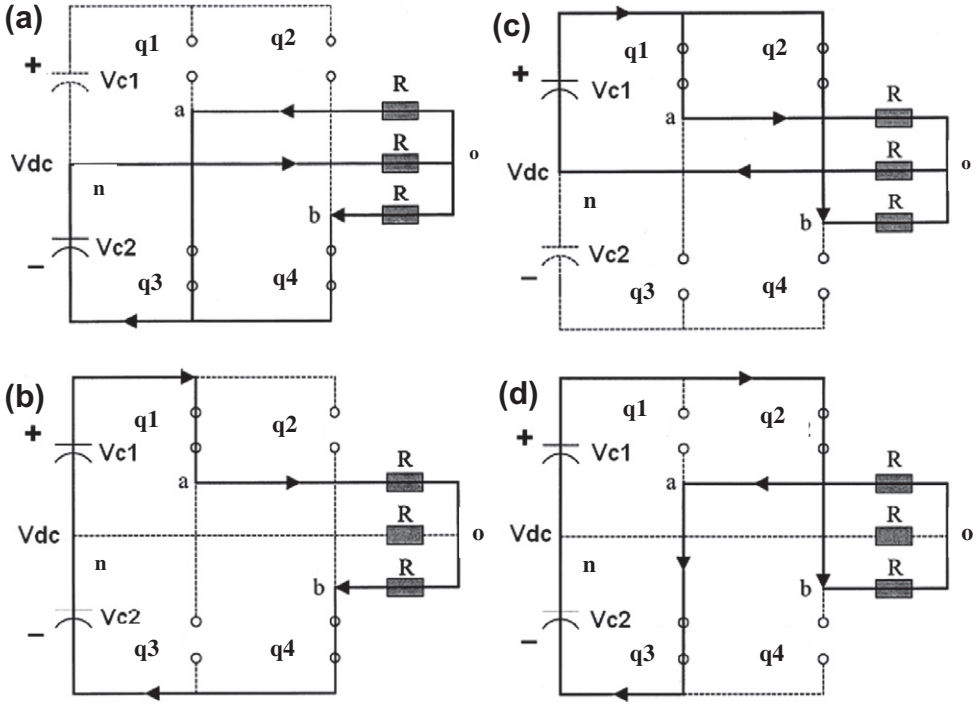

Fig. 2. Inverter switching states and their respective dc-link loading patterns.

imbalance. At low output frequencies considerable periods of time can be spent predominantly in one of the unbalanced states, leading to an imbalance that has a noticeable effect on inverter output waveform quality [11]. So, any imbalance in capacitors voltage will lead to more current ripple than with the six switch inverter.

The possible values of pole voltages V_1 and V_2, depend on the state of the switches q_1 and q_2. As can be seen from Figs. 1 and 2, and Eqs. (1)–(3) there are four switching states with the following pole voltages

- $V_1 = V_2 = -V_{dc/2}$, when $q_1 = q_2 = 0$;
- $V_1 = V_{dc/2}$, $V_2 = -V_{dc/2}$, when $q_1 = 1$ $q_2 = 0$;
- $V_1 = V_2 = V_{dc/2}$, when $q_1 = q_2 = 1$;
- $V_1 = -V_{dc/2}$, $V_2 = V_{dc/2}$, when $q_1 = q_2 = 1$;

the phase to neutral voltages can be defined as follows:

$$V_{o1} = V_1 - V_{no} \quad (4)$$

$$V_{o2} = V_2 - V_{no} \quad (5)$$

$$V_{o3} = V_3 - V_{no} \quad \text{and } V_3 = 0 \quad (6)$$

where "n" is the center point of split capacitors, "o" is the neutral point of IM windings and V_{no} is the voltage between the center point of split capacitors and the neutral point of IM windings. These phase voltages can be expressed in terms of the binary variables q_1 and q_2, and the dc-link voltage, V_{dc}, as follows [18]:

$$V_{o1} = \frac{V_{dc}}{6}[4q_1 - 2q_2 - 1] \quad (7)$$

$$V_{o2} = \frac{V_{dc}}{6}[4q_2 - 2q_1 - 1] \quad (8)$$

$$V_{o3} = \frac{V_{dc}}{6}[-2q_1 - 2q_2 + 2] \quad (9)$$

Using all the possible combinations of q_1 and q_2 the line to neutral (IM phase) voltages get the values given in Table 1 From this table it is noted that voltage V_{o3} is a three - level PWM swinging between $V_{dc/3}$, 0, and $-V_{dc/3}$. On the other hand, the voltages V_{o1} ,V_{o2}, are the four-level type swinging between $V_{dc/6}$, $V_{dc/2}$ and $-V_{dc/6}$,$-V_{dc/2}$. Further, the fundamental content is the same in the three phase output voltages.

For better realization, the three phase quantities are transformed into $\alpha\beta$ quantities [7].

$$v_{\alpha\beta} = A v_{123} \quad (10)$$

$$A = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (11)$$

where $V_{\alpha\beta} = [V_\alpha, V_\beta]^T$, and $V_{123} = [V_{o1}, V_{o2}, V_{o3}]^T$.

The IM is assumed to be symmetric, with its neutral wire disconnected. The α, β voltage components are given by [7]:

$$V_\alpha = \sqrt{\frac{2}{3}}\left(q_1 V_{dc} - \frac{q_2}{2}V_{dc} - \frac{V_{dc}}{4}\right) \quad (12)$$

$$V_\beta = \sqrt{\frac{2}{3}}\left(\frac{\sqrt{3}}{2}q_2 V_{dc} - \frac{\sqrt{3}}{4}V_{dc}\right) \quad (13)$$

Table 1
Switching functions and the output voltages from B4 inverter.

Switching function		Switch on		Output voltage vector		
q_1	q_2	$T_1 = q_1$, $T_3 = q_2$, T_4 T_2		V_{o1}	V_{o2}	V_{o3}
0	0	T_2	T_4	$-V_{dc/6}$	$-V_{dc/6}$	$V_{dc/3}$
0	1	T_2	T_3	$-V_{dc/2}$	$V_{dc/2}$	0
1	0	T_1	T_4	$V_{dc/2}$	$-V_{dc/2}$	0
1	1	T_1	T_3	$V_{dc/6}$	$V_{dc/6}$	$-V_{dc/3}$

Table 2
Combinations of the switch states.

q_1	q_2	$V = v_\alpha + jv_\beta$
0	0	$V_1 = (V_{dc}/\sqrt{6})e^{-j2\pi/3}$
1	0	$V_2 = (V_{dc}/\sqrt{2})e^{-j\pi/6}$
1	1	$V_3 = (V_{dc}/\sqrt{6})e^{j\pi/3}$
0	1	$V_4 = (V_{dc}/\sqrt{2})e^{j5\pi/6}$

Table 2 shows the combinations of the switch states. So as shown in Fig. 3 four different vectors in the $\alpha\beta$ plane, two small and two large voltage vectors per PWM period will be available [7]. In case of voltage control the output line-to-line voltage can be defined as:

$$V_{13} = V_{o1} - V_{o3} \quad (14)$$

$$V_{23} = V_{o2} - V_{o3} \quad (15)$$

The output voltage of the phase 1 with the reference of the center point of the split capacitors can be defined by controlling q_1 and q_3 in a PWM fashion. In order to generate balanced three phase output voltage the voltage V_{23} should be shifted by +60° or −60° according to output phase sequence. Although in B4 inverter, two phases can be controlled by q_1–q_4 switches, the basic problem is, how one can control the third phase to maintain the three phases in balance at inverter's output. q_1–q_4 should be controlled using existing modulation schemes, such that the fundamental frequency component of the B4 inverter output voltages has a 60° phase difference [8,9]. In this way, the fundamental components of the three phase voltages are a balanced set with 120° of phase difference as shown in Fig. 4.

3. Structure of the proposed pattern generator

The proposed pattern generator as shown in Fig. 5, has a closed-loop structure based on the sensing of the instantaneous value of

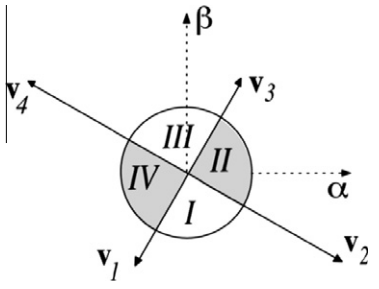

Fig. 3. Four different vectors in the $\alpha\beta$ plane.

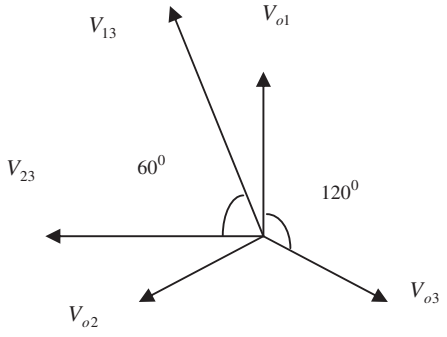

Fig. 4. Three phase voltage with 120° phase shift.

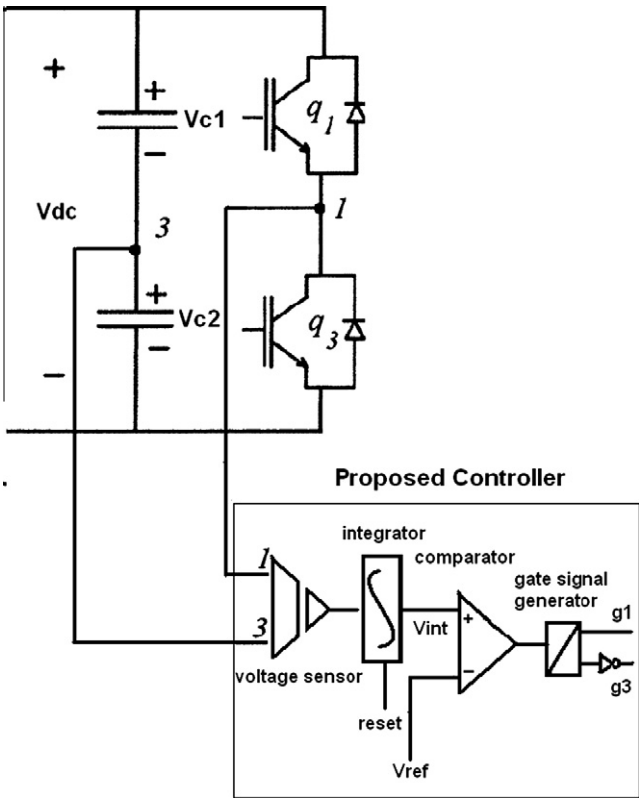

Fig. 5. PWM pattern generator of proposed method.

the B4 inverter line voltages (V_{23}, V_{13}). This voltage contains the information regarding the dc-bus ripple of upper and underneath dc-link capacitors voltage. Thus, by controlling the line voltages, one can regulate the output voltage on a per-phase basis and compensate the effect of the ripple and dc-link voltage imbalances. The waveforms in Fig. 6 show the operation of the system in positive half cycle. The line voltage, V_{13}, is fed to a reset-able integrator. The output of the integrator is compared with a reference sinusoidal signal with a dc bias. As the integrator output reaches the reference signal, the comparator output reaches the desired value, and switch is turned off. At the same time, the integrator output is reset to zero. The integrator output is clamped to zero until the end of the switching period (T_{sw}).

3.1. Compensation of dc-bus variations

The B4 inverter line voltage of Figs. 1 and 5 is determined by

$$\begin{cases} V_{13} = V_{dc/2} & \text{when top switch is on} \\ V_{13} = -V_{dc/2} & \text{when bottom switch is on} \end{cases}$$

The slope of integration is proportional to the instantaneous value of the dc-bus voltage that will fluctuate due to the presence of the ripples. When the dc-bus voltage is higher, the rate of integration is faster and, hence, the integration value reaches the reference faster, generating a narrower pulse width. On the other hand, the lower the dc-bus voltage, the wider the generated pulse. As mentioned before, in positive half cycle, integrator should be fed by upper capacitor voltage which its output value is positive and can reach the reference input. Otherwise, the integrator output will not reach the reference value in positive half cycle. Also, this problem exists in negative half cycle. So, the integrator must be fed by the bottom capacitor voltage value. The PWM pattern generated by this online real-time integration is a function of the non-ideal dc-bus, and the pulse width generated by virtue of comparison with a sinusoidal reference voltage ensures a sinusoidal v/s distribution in the output voltage [17]. Thus, the proposed modulator can inherently compensate for the ripple in the dc-bus. This improves the performance of the B4 inverter without resorting to complex control circuitry. The proposed PWM pattern generator is implemented in a B4 inverter. It consists of two independent modulators of Fig. 5 placed across the midpoint of each inverter leg and midpoint of the dc-link voltage with control references phase-shifted by 60° with respect to each other.

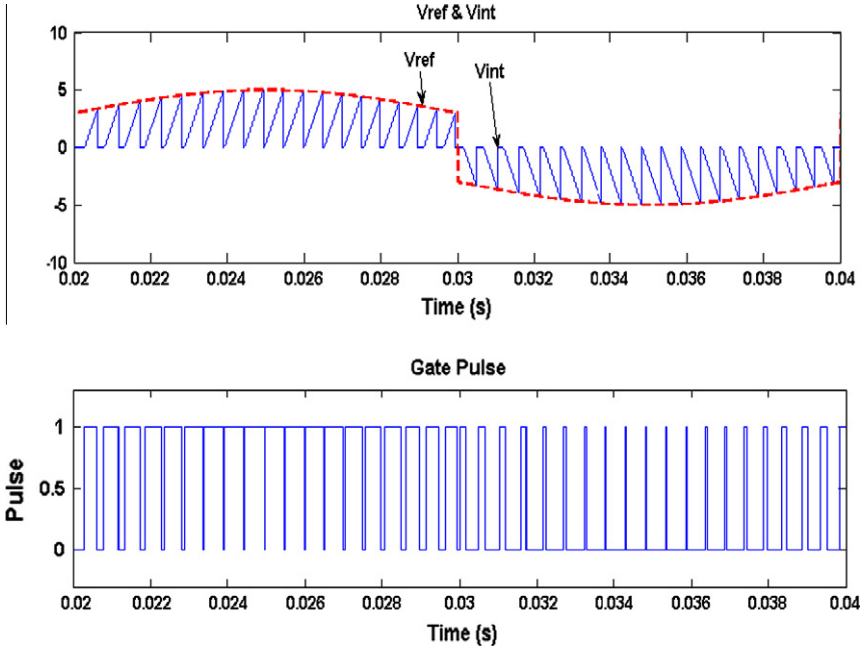

Fig. 6. Upper trace: reference sinusoidal waveform, integrator output, lower trace: PWM pulses for q_1.

Table 3
IM parameters.

IM rated power	2.2 kW
Rated current	5 A
Rated voltage	220 V
Rated frequency	50 Hz
Pole numbers, P	4
Stator resistance	0.92 Ω
Rotor resistance	0.66 Ω
Stator leakage inductance	0.0035 H
Rotor leakage inductance	0.0035 H
Mutual inductance	0.0016 H
dc-Link capacitance	C1 = C2 = 500 μF

3.2. Proposed modulation method highlights

As one can recognize from Figs. 5 and 6 without positive dc bias in positive half cycle of sinusoidal reference signal and negative dc bias in negative half cycle of the same signal the generated pulses width will be very narrow, and therefore the switching frequency will be higher than the rating frequency of IGBT switches. Thus the reference signals in positive and negative half cycles are defined as [17]:

$$\begin{cases} V_{ref} = V_{\text{bias}} + V_m \cdot \sin(2\pi f_0 t) \text{positive half cycle} \\ V_{ref} = -V_{\text{bias}} + V_m \cdot \sin(2\pi f_0 t) \text{negative half cycle} \end{cases}$$

where f_0 is the inverter fundamental output frequency.

The modulation index is defined as:

$$M = \frac{|V_m|}{|V_{\text{bias}}|} \tag{16}$$

Let f_{sw} be the switching frequency of the inverter and K_s the gain of the voltage sensor; the instantaneous integrator output is given as:

$$V_{\text{int}} = \frac{K_s \cdot V_{\text{dc}}}{\tau} t \tag{17}$$

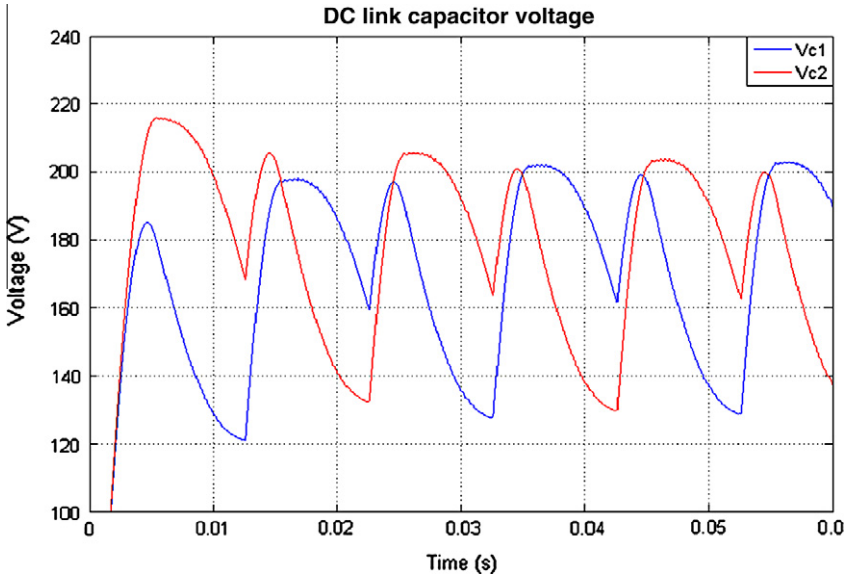

Fig. 7. dc-Link capacitors voltage.

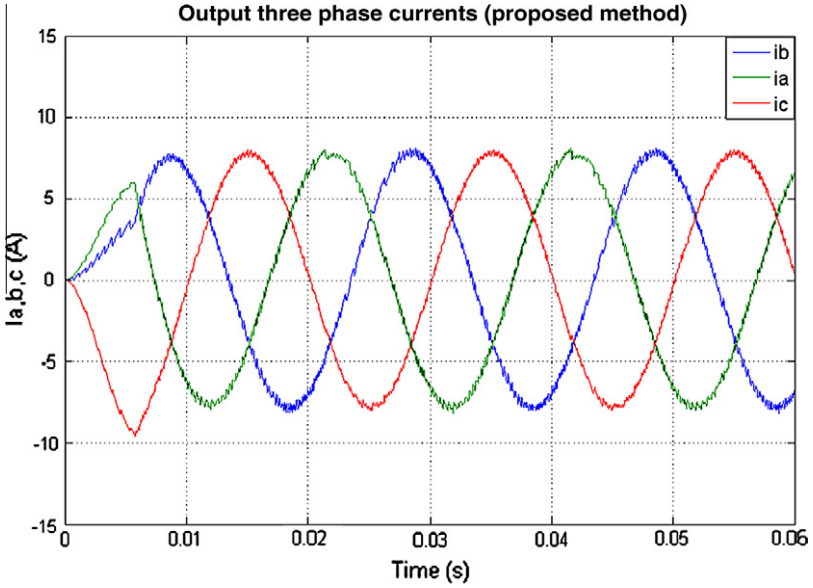

Fig. 8. Three phase currents in the proposed method.

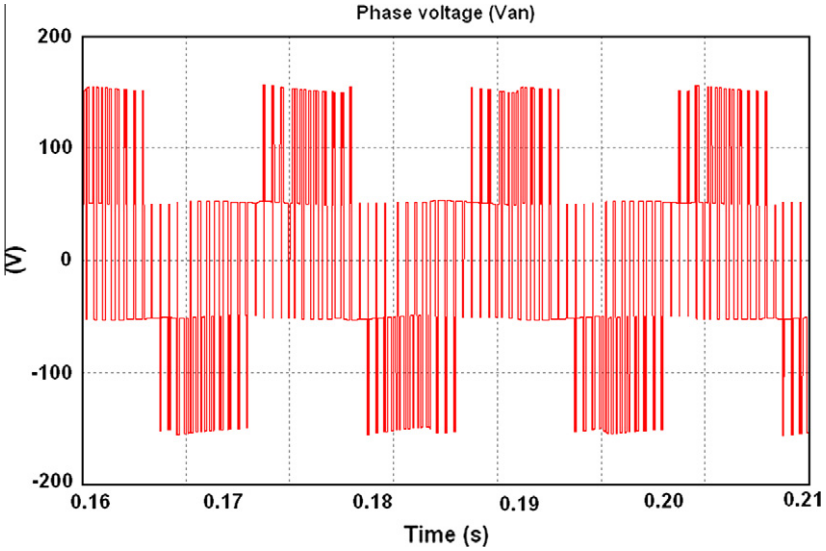

Fig. 9. The phase voltage (V_{o1}) in the proposed method.

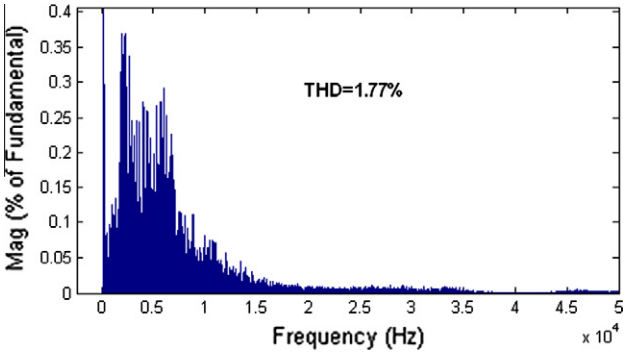

Fig. 10. The harmonic spectra of phase current (*ia*).

The integration time constant should be selected such that the integrator output always reaches the reference signal. If the time constant is too large, the integrator output will not reach the reference signal and the constant frequency operation will be lost. The largest integration ramp occurs when the reference voltage is at its maximum, i.e., $V_m + V_{\text{bias}}$. Therefore, the required condition for time constant selection is:

$$\frac{K_s \cdot V_{\text{dc}} \cdot T_{sw}}{\tau} > V_m + V_{\text{bias}}$$

Rearranging the above equation and setting $M = 1$ (i.e., $V_m = V_{\text{bias}}$), we obtain the integrator time constant as:

$$\tau < \frac{K_s \cdot V_{\text{dc}} \cdot T_{sw}}{2 \cdot V_{\text{bias}}}$$

4. Simulation results of proposed scheme

In order to verify the effectiveness of the proposed inverter configuration and its control strategy, a digital computer simulation model has been developed in MATLAB/SIMULINK platform according to Figs. 1 and 5 [22]. For simplification, the B4 inverter switches will be modeled as ideal elements without any switching losses in

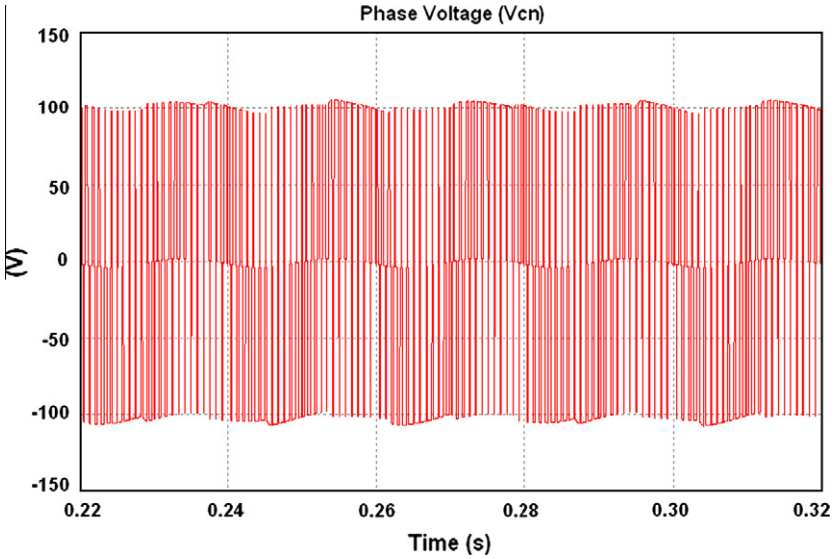

Fig. 11. The phase to neutral voltage (V_{o3}) in the proposed scheme.

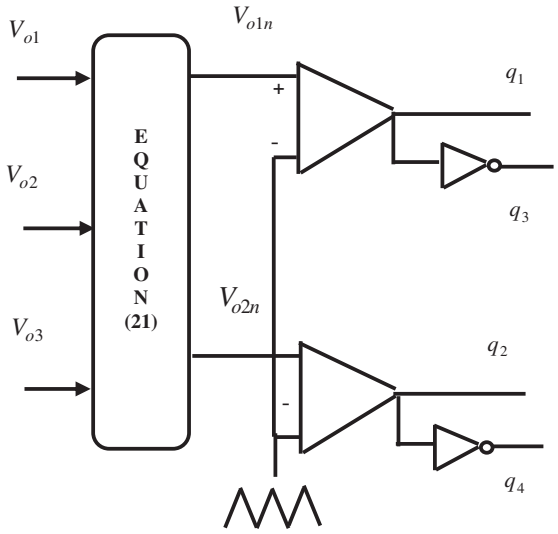

Fig. 12. Sine triangle PWM for FSTPI control.

developed simulation model. The sampling frequency for all simulations was chosen 15 kHz. The IM parameters and inverter characteristic are summarized in Table 3. Extensive simulations have been done based on proposed strategy. Fig. 7 shows the dc-link capacitors imbalance voltages, caused by one phase current circulating through the capacitive bank. The balanced three phase currents will be obtained by the proposed modulation even with the unbalance dc-link voltages. The output three phase currents are shown in Fig. 8. The steady-state three phase IM currents shown in this figure indicate balance operation of the four switch, three phase inverter controlled by proposed modulation scheme. Figs. 9 and 10 illustrate the phase voltage (V_{o1}) and the harmonic spectrum of the line current for the proposed technique, respectively. Fig. 9 clearly shows that V_{o1} is the four-level type swinging between $V_{dc/6}$, $V_{dc/2}$, $-V_{dc/6}$, and $-V_{dc/2}$. The uncontrolled phase to neutral voltage (V_{o3}) is a three level swinging between $V_{dc/3}$, 0, $-V_{dc/3}$ and is shown in Fig. 11. The calculated voltage levels of V_{o1}, and V_{o3} by Eqs. (7)–(9) in Table 1 confirm by simulation results of Figs. 9 and 11. The total harmonic distortion of the line current for the proposed PWM is found 1.77% that is much less than the standard value of 5%.

5. SPWM and hysteresis current control schemes

5.1. Simulation and experimental results of SPWM scheme

Given a desired set of three phase voltages for the inverter's output [8,9]:

$$v_{o1} = V_o \sin(\omega_o t) \tag{18}$$

$$v_{o2} = V_o \sin\left(\omega_o t - \frac{2\pi}{3}\right) \tag{19}$$

$$v_{o3} = V_o \sin\left(\omega_o t + \frac{2\pi}{3}\right) \tag{20}$$

where V_o is the magnitude of the output voltages. Two sinusoidal reference signals V_{o1n} and V_{o2n} with 60° phase-shifted is compared with a carrier signal to determine the PWM switching instants as shown in Fig. 12:

$$\begin{aligned} v_{o1n} &= v_{o1} - v_{o3} = \sqrt{3} V_o \sin\left(\omega_o t - \tfrac{\pi}{6}\right) \\ v_{o2n} &= v_{o2} - v_{o3} = \sqrt{3} V_o \sin\left(\omega_o t - \tfrac{\pi}{2}\right) \end{aligned} \tag{21}$$

The four switches of B4 inverter should be controlled using sinusoidal modulation scheme, such that the fundamental frequency component of the output voltages of the B4 inverter has a 60° phase difference. In this way, the fundamental components of the three phase voltages of the motor windings are a balanced set with 120° of phase difference [8,9]. Numerous simulation and experimental results are obtained for a prototype 2.2 kW squirrel cage IM using SPWM method. Fig. 13 shows the simulation results of IM currents. The steady-state three phase IM currents shown in this figure indicate unbalance operation of the four switch, three phase inverter. This imbalance in B4 three phase output currents caused by the dc-link capacitors voltage fluctuations. The harmonic spectrum of phase current (*ia*) is shown in Fig. 14 whereas the total harmonic distortion of *ia* is found 5.54%. One can recognize that the THD of *ia* in Fig. 14 is much higher than the THD of the same phase in proposed method of Fig. 10. Fig. 15 shows the experimental setup of FSTPI induction motor drive. The prototype IGBT inverter includes a power circuit, an interfacing and sensing modules, a fixed

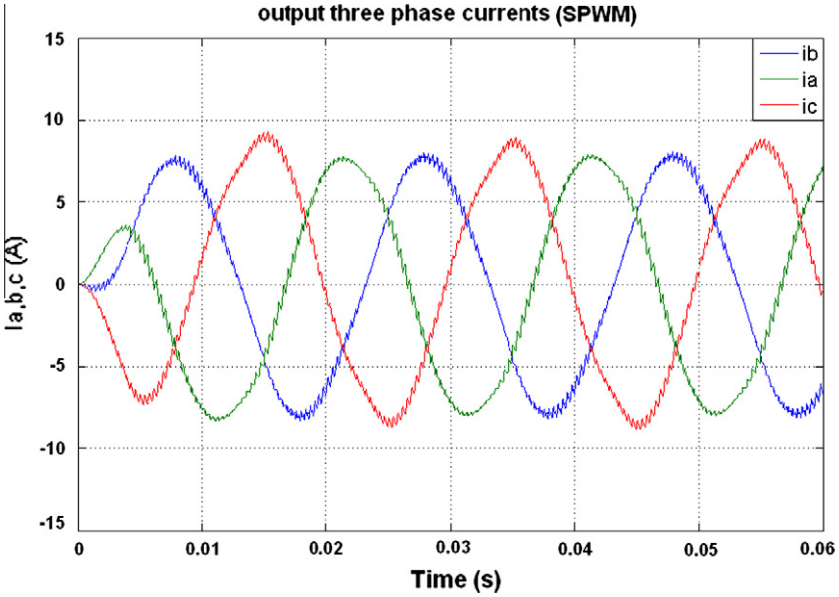

Fig. 13. Simulation three phase currents in SPWM scheme.

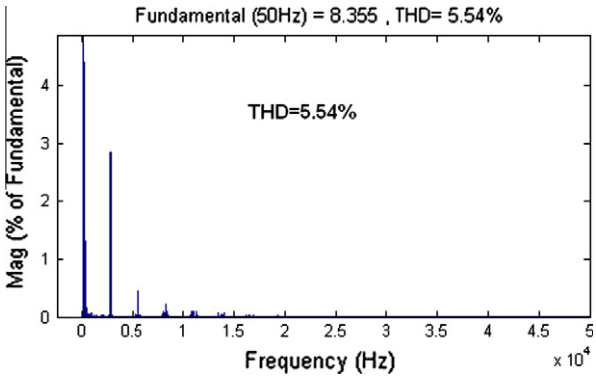

Fig. 14. The harmonic spectra of (*ia*) in SPWM scheme.

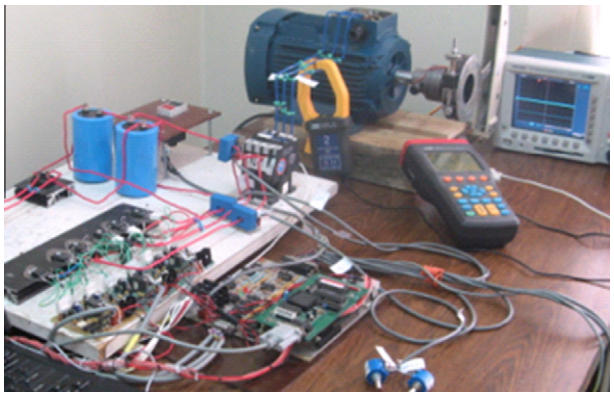

Fig. 15. Experimental setup of FSTPI IM drive.

point 16 bit Intel 80C196KD-based control module [19], and two IGBT driver modules. The inverter is equipped with software and hardware protections, including over-current, over-voltage and over-temperature protections. Two phase currents *ia* and *ib* are sensed by current transducers (CT). These currents beside V_{dc}, and heat-sink temperature are fed to the microcontroller through interfacing board. The sampling frequency for experimental implementation was chosen 10 kHz. Fig. 16 shows the experimental steady-state three phase currents. These experimental results verify that without compensation in dc-link voltages there is slight unbalance in the phase currents which cause relatively higher speed vibrations as compared to conventional six switch inverter fed drive. Because of relatively high dc-link capacitors, 1500 μF, the steady-state output currents shown in Fig. 16 almost have the same magnitude. So with bigger capacitor in dc-link and high switching frequency, the three phase output currents will have lower THD. Fig. 17 demonstrates the experimental IM phase to neutral voltage, V_{o1}. The controlled phase voltage is four-level swinging between $V_{dc/6}$, $V_{dc/2}$, $-V_{dc/6}$, and $-V_{dc/2}$. The uncontrolled phase to neutral voltage (V_{o3}) is three level swinging between $V_{dc/3}$, 0, $-V_{dc/3}$ and is shown in Fig. 18. Simulation results of Figs. 9 and 11 from proposed method and experimental results of Figs. 17 and 18 from SPWM scheme indicate good agreement between simulation and experimentation.

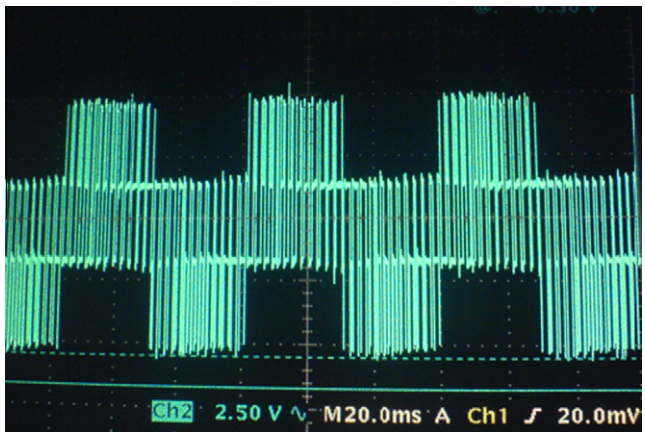

Fig. 17. The phase voltage (V_{o1}) in SPWM scheme, experimental.

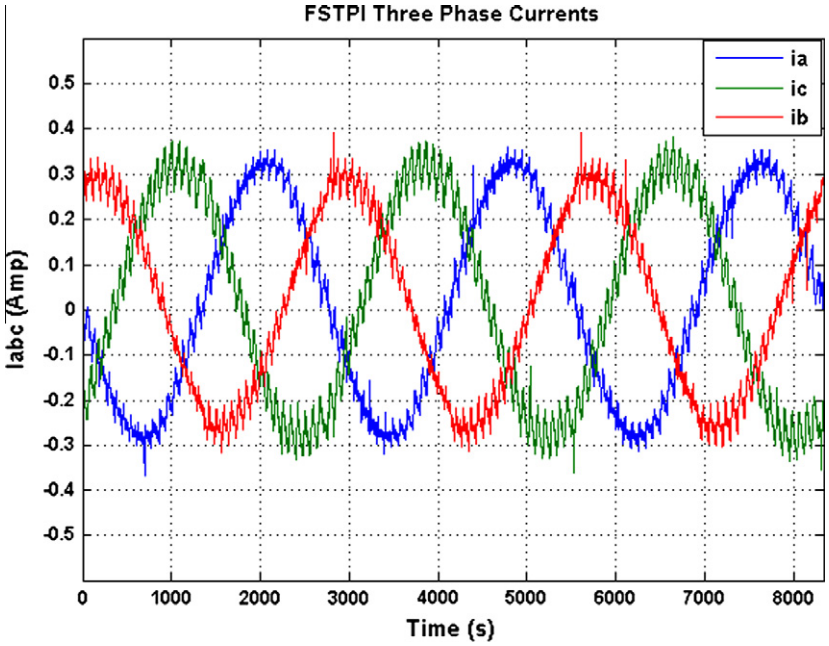

Fig. 16. Experimental three phase currents in SPWM scheme.

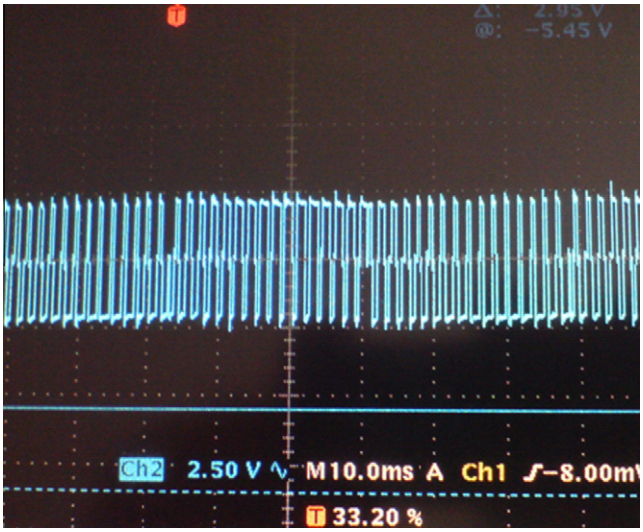

Fig. 18. The phase voltage (V_{o3}) in SPWM scheme, experimental.

5.2. Simulation and experimental results of hysteresis scheme

Hysteresis current controller, presented in [14,18], utilizes hysteresis in comparing load currents to current references. Hysteresis current controllers have the advantage of simplicity and robustness and high speed dynamics, but converters' switching frequency largely depends on the load parameters and consequently the load current harmonics ripple is not optimal. Improved hysteresis control strategies were proposed, including those of Bose in [23] and Yao and Holmes in [24] which presented the variable – hysteresis - band current control technique. This control method, where the band is modulated with the system parameters, maintains a nearly constant switching frequency. However its current ripple is still not optimal. The same experimental setup of SPWM scheme for FSTPI induction motor drive in Fig. 15 was used for hysteresis method implementation. The simulation results of steady-state three phase IM currents fed from four switch inverter and the harmonic spectrum of the line current are shown in Fig. 19. The total harmonic distortion of the line current for the hysteresis scheme is found 8.09% that is much higher than the same value of proposed method and SPWM scheme. The steady-state three phase IM

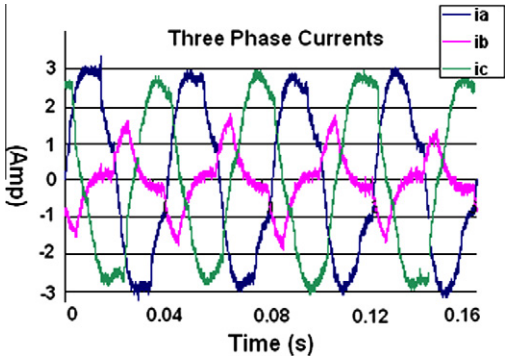

Fig. 20. Experimental three phase currents in hysteresis scheme.

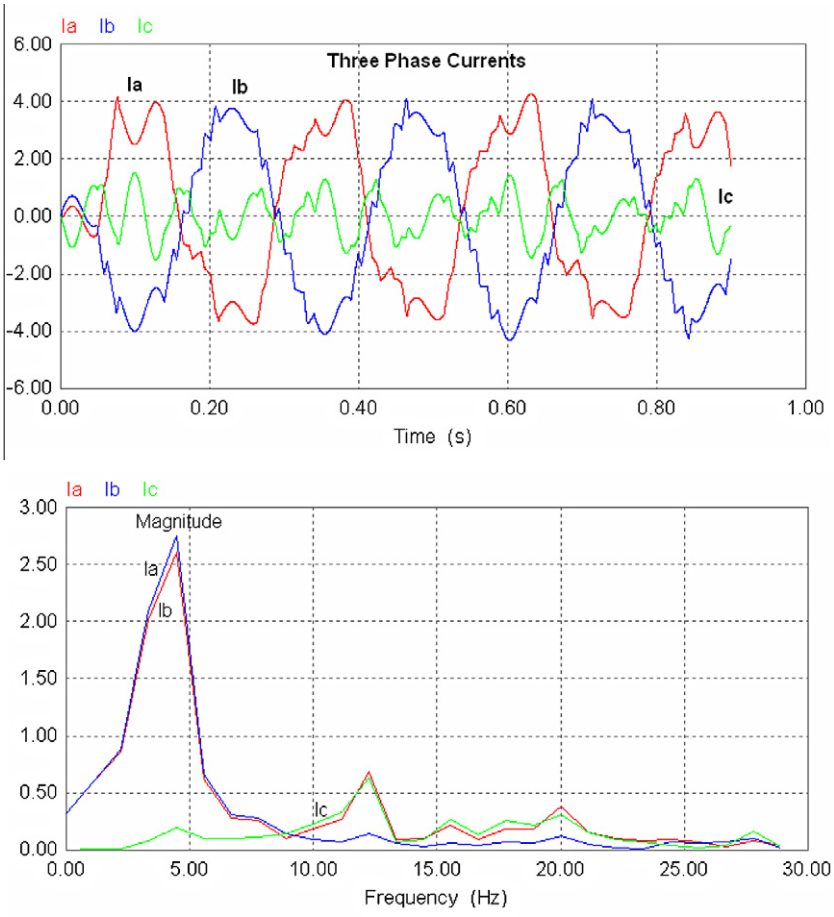

Fig. 19. Upper trace: three phase currents in hysteresis scheme; Lower trace: harmonic spectrum.

currents shown in this figure indicate unbalance operation of the four switch, three phase inverter controlled by hysteresis scheme. Fig. 20 shows the experimental results of IM currents. The steady-state three phase IM currents shown in this figure indicate that the hysteresis scheme has unbalance behavior in four switch, three phase inverters. The harmonics contents of three output currents are unacceptable for online implementation of B4 inverter by hysteresis strategy.

By comparing Figs. 13,14,16,19, 20 from SPWM and hysteresis methods with Figs. 8 and 10 from proposed method one can recognize that the proposed method provides better three phase output currents with less THD and negligible unbalances.

6. Conclusion

A cost effective B4 inverter fed IM drive has been simulated. This scheme employs only four IGBT switches instead of six, as utilized in conventional motor drives. This reduces the cost of the inverter, the switching losses, and the complexity of the control algorithm and interface circuits to generate six PWM signals. The proposed method utilizes the dc-bus ripple and voltage imbalances and generates gating signals required to produce high-quality sinusoidal output currents and voltages. A performance comparison of proposed method with SPWM and conventional hysteresis current control schemes is also made in terms of total harmonic distortion of stator currents. Simulation and experimental results from SPWM and hysteresis schemes confirm the superiority of proposed method in providing more precise current control with minimum distortion and harmonic noises (THD), and at the same time, less unbalance in output currents. Simulation results from proposed method confirm that this scheme can be applied in real-time control of IM drive.

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