

TIMING DIAGRAM

- Timing Diagram is a graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states.

Instruction Cycle:

- The time required to execute an instruction is called instruction cycle.

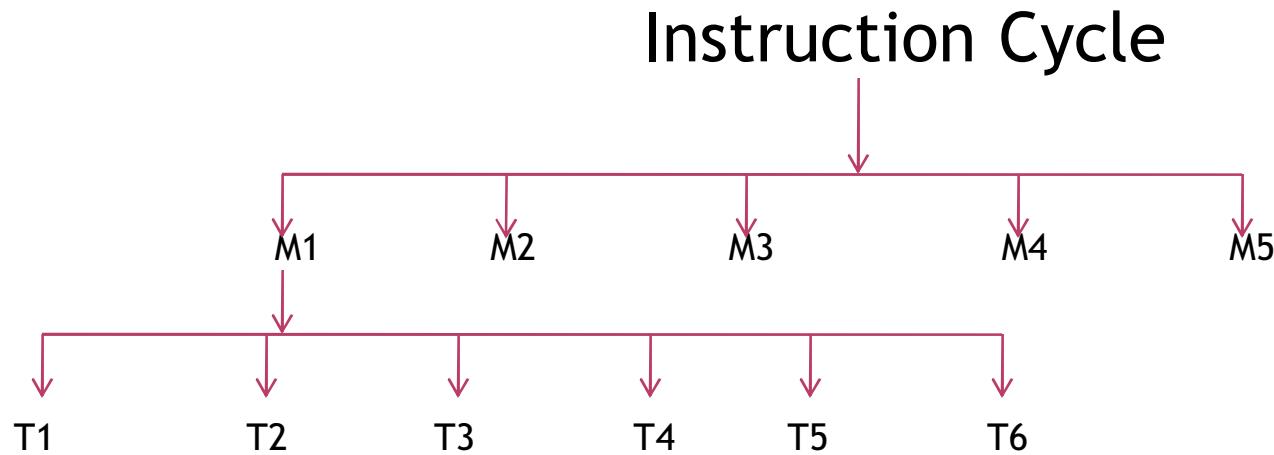
Machine Cycle:

- The time required to access the memory or input/output devices is called machine cycle.

T-State:

- The machine cycle and instruction cycle takes multiple clock periods.
- A portion of an operation carried out in one system clock period is called as T-state.

INSTRUCTION CYCLE



M_n –Machine Cycle

T_n –T State

MACHINE CYCLES OF 8085

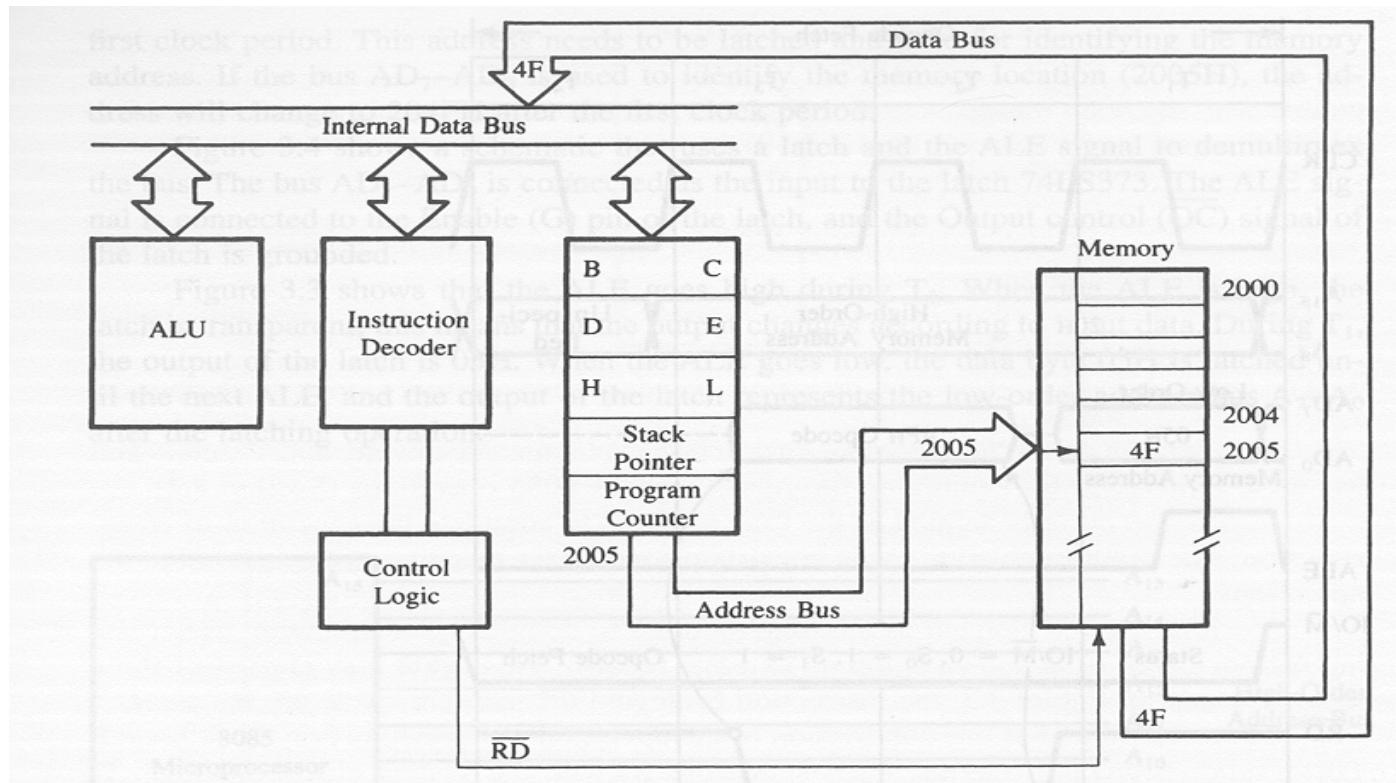
The 8085 microprocessor has 5 (seven) basic machine cycles. They are

- Opcode fetch cycle (4T)
- Operand fetch Cycle(3T)
- Memory read cycle (3 T)
- Memory write cycle (3 T)
- I/O read cycle (3 T)
- I/O write cycle (3 T)
- Interrupt acknowledge cycle
- Idle machine cycle

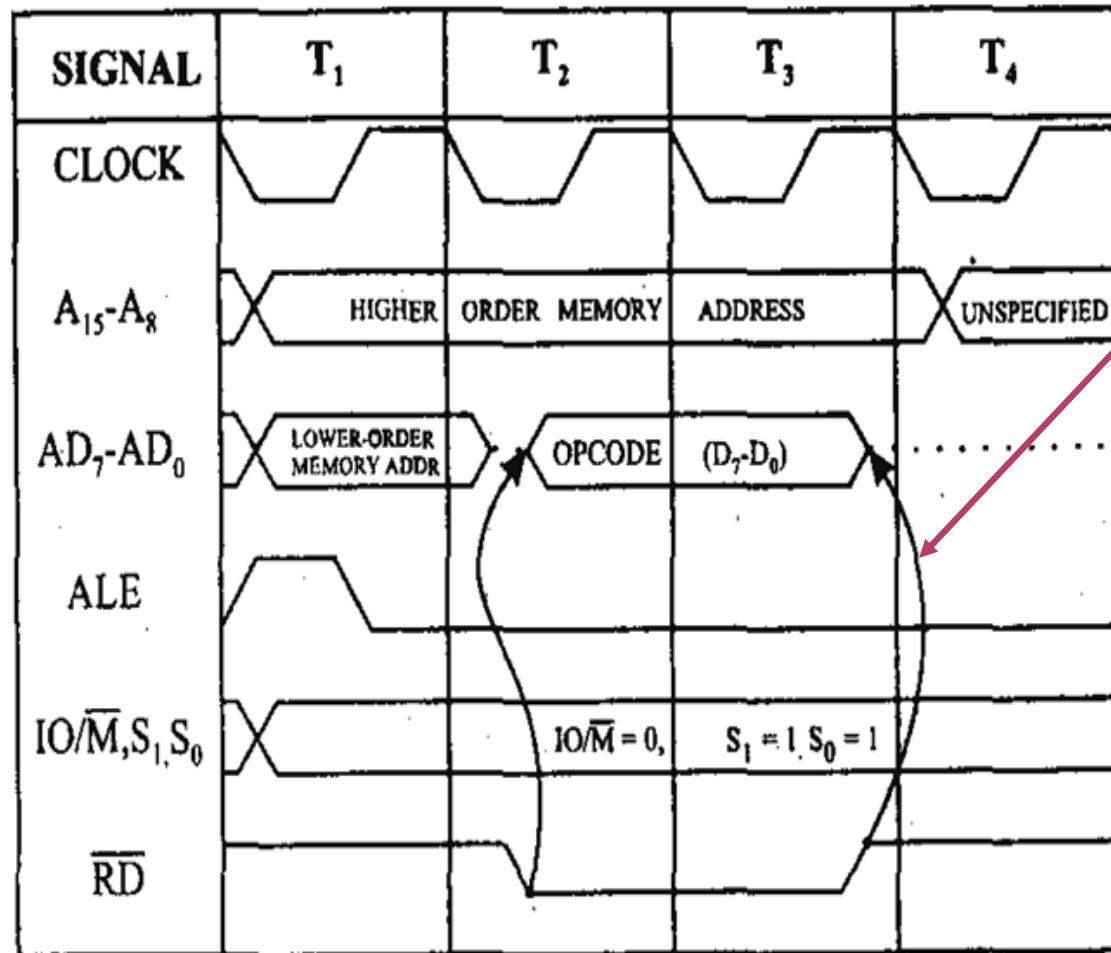
OPCODE FETCH MACHINE CYCLE OF 8085

- Each instruction of the processor has one byte opcode.
- The opcodes are stored in memory. So, the processor executes the opcode fetch machine cycle to fetch the opcode from memory.
- Hence, every instruction starts with opcode fetch machine cycle.
- The time taken by the processor to execute the opcode fetch cycle is $4T$.
- In this time, the first, 3 T-states are used for fetching the opcode from memory and the remaining T-states are used for internal operations by the processor.

EXAMPLE: INSTRUCTION FETCH OPERATION



OPCODE FETCH MACHINE CYCLE OF 8085



Instruction (opcode) reaches the instruction decoder now !

It takes four clock cycles to get one instruction into the CPU.

STATUS SIGNAL

Machine Cycle	IO / M	S ₁	S ₂
Opcade fetch	0	1	1
Memory read	0	1	0
Memory write	0	0	1
I/O read	1	1	0
I/O write	1	0	1
Interrupt Acknowledge	1	1	1
Bus Ideal	0	0	0

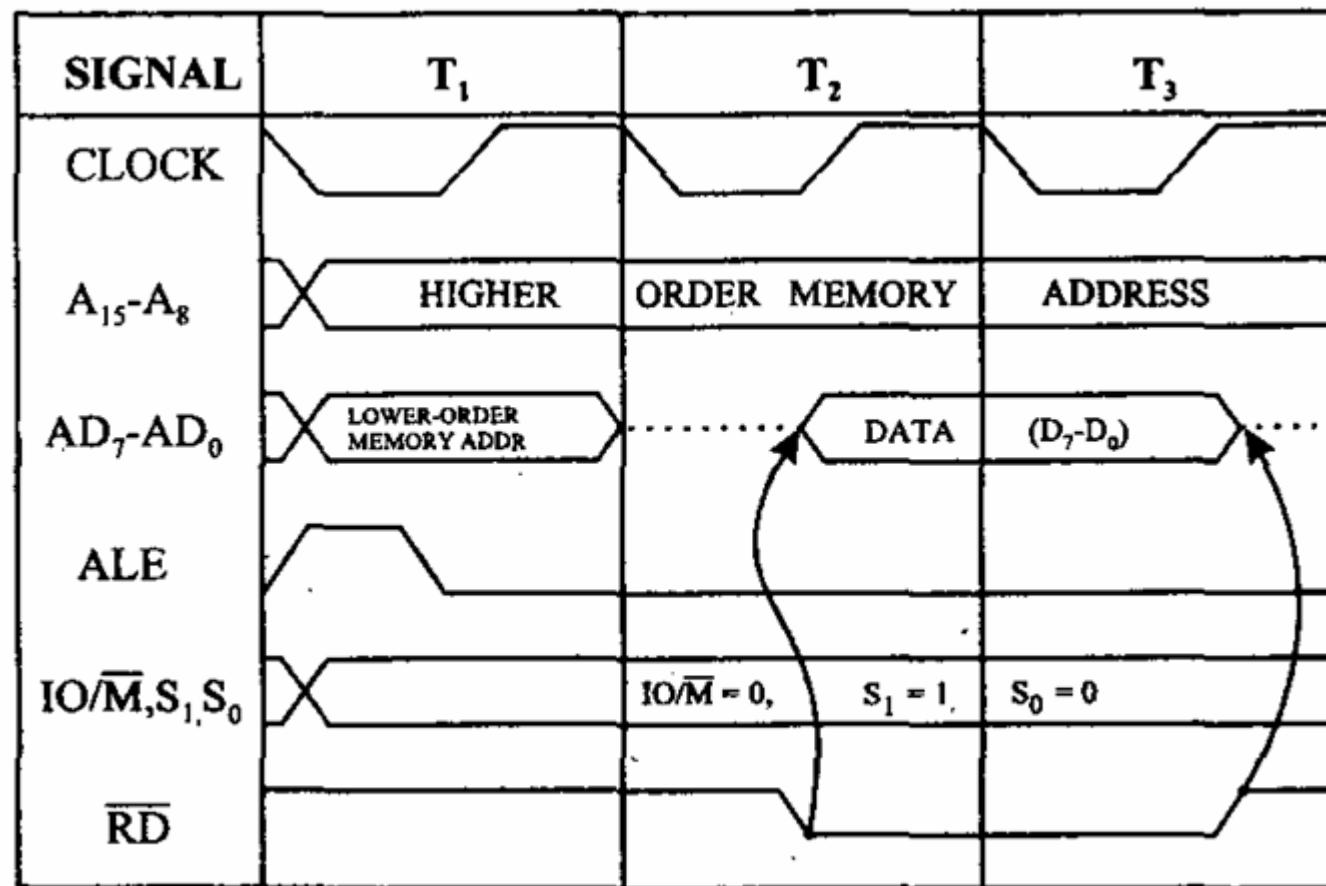
INSTRUCTIONS THAT REQUIRE T5 , T6 STATE

Instruction	Operation performed
CALL	Stack pointer is decremented by 1
CALL conditional PUSH R _P	Stack pointer is decremented by 1
DCX R _P	Register pair decremented by 1
INX R _P	Register pair incremented by 1
PCHL	HL pair transferred to PC
SPHL	HL pair transferred to SP
RET conditional	The condition of flags checked

MEMORY READ MACHINE CYCLE OF 8085

- The memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to execute this cycle.
- The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle.

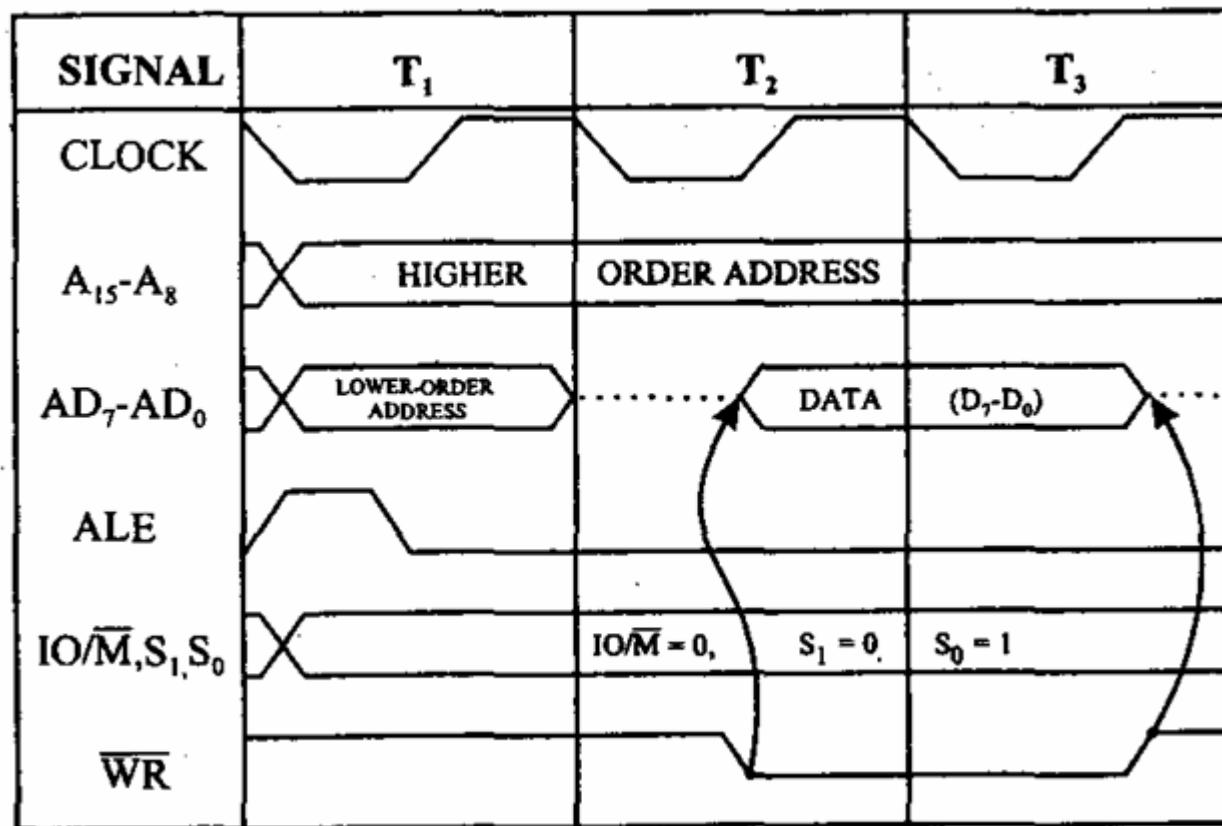
MEMORY READ/OPERAND FETCH MACHINE CYCLE OF 8085



MEMORY WRITE MACHINE CYCLE OF 8085

- The memory write machine cycle is executed by the processor to write a data byte in a memory location.
- The processor takes, 3T states to execute this machine cycle.

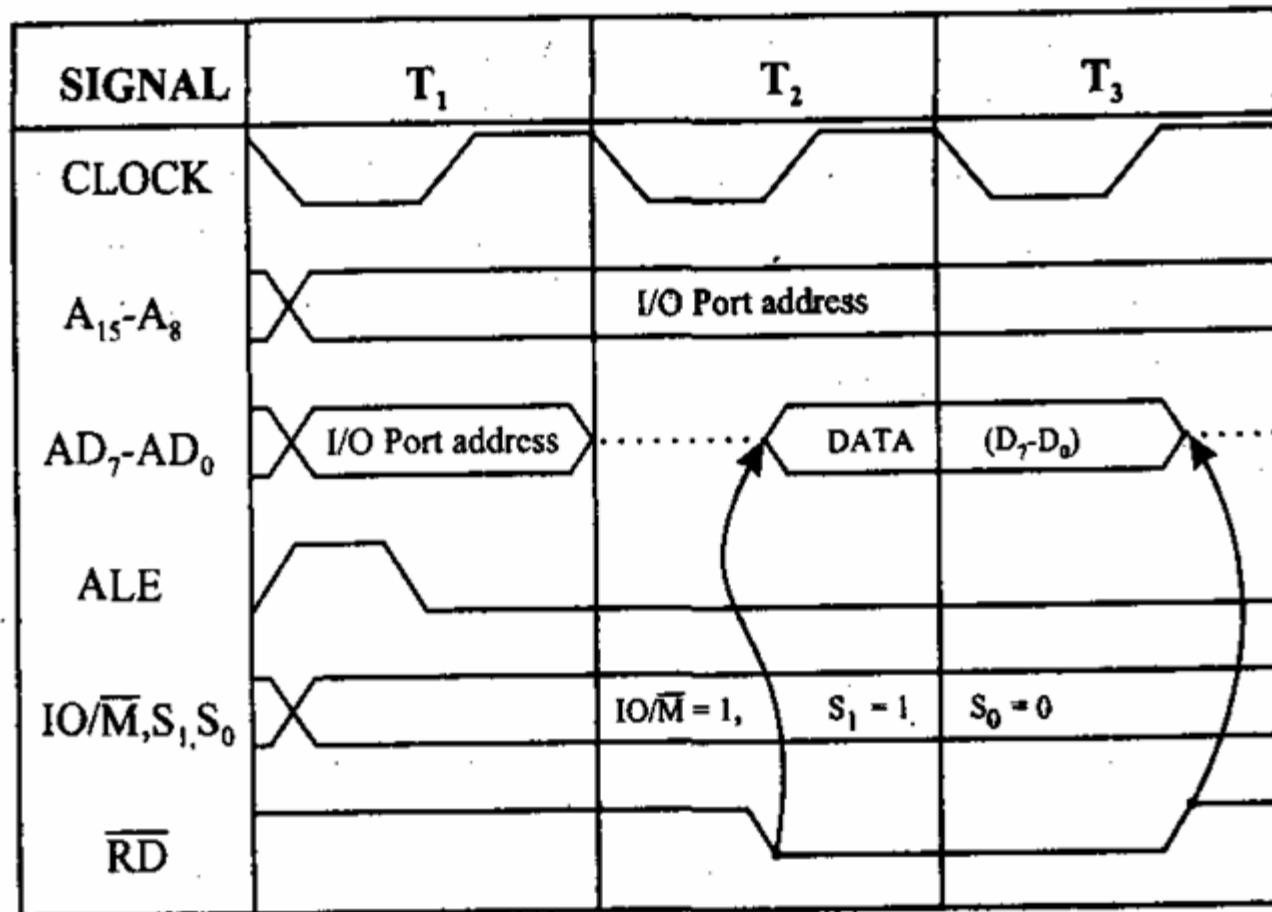
MEMORY WRITE MACHINE CYCLE OF 8085



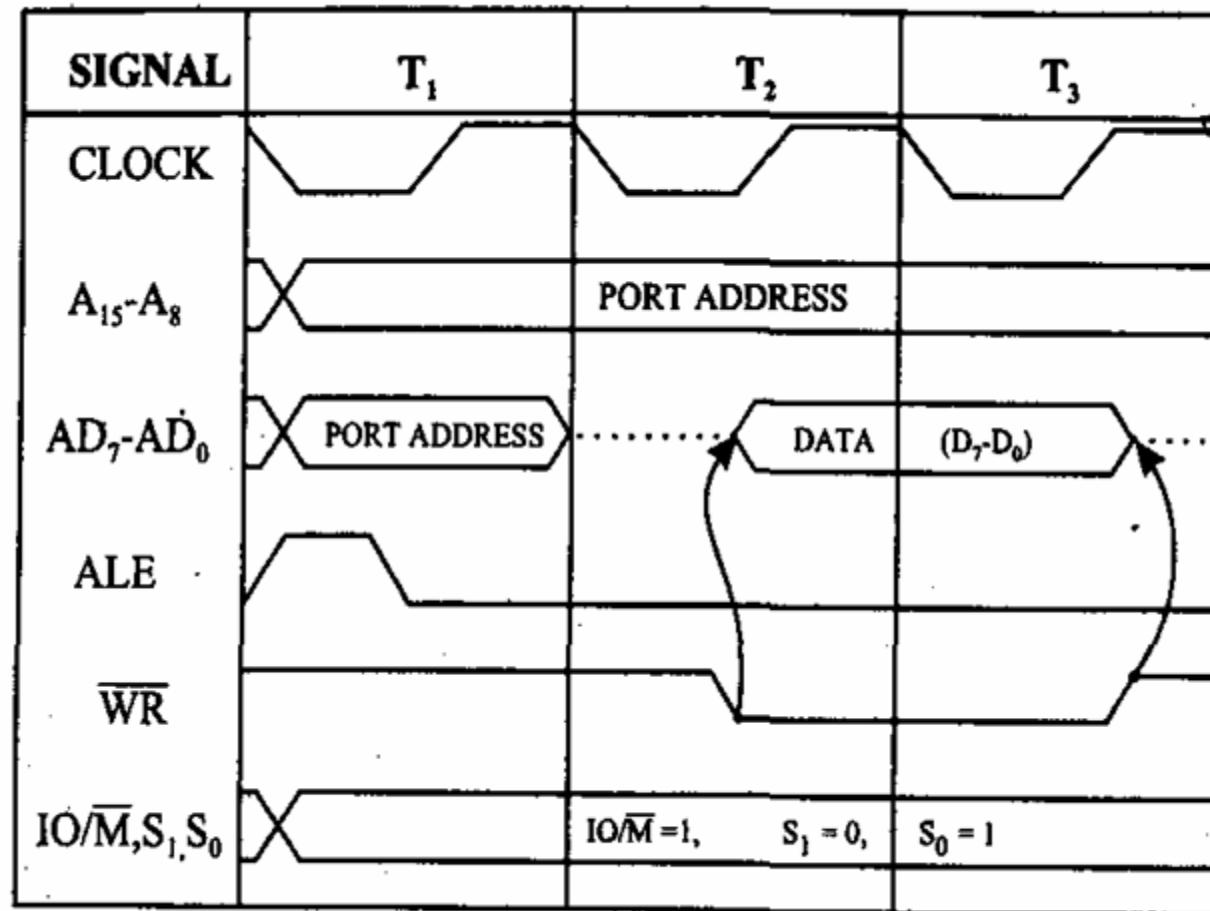
I/O READ CYCLE OF 8085

- The I/O Read cycle is executed by the processor to read a data byte from I/O port or from the peripheral, which is I/O, mapped in the system.
- The processor takes 3T states to execute this machine cycle.
- The IN instruction uses this machine cycle during the execution.

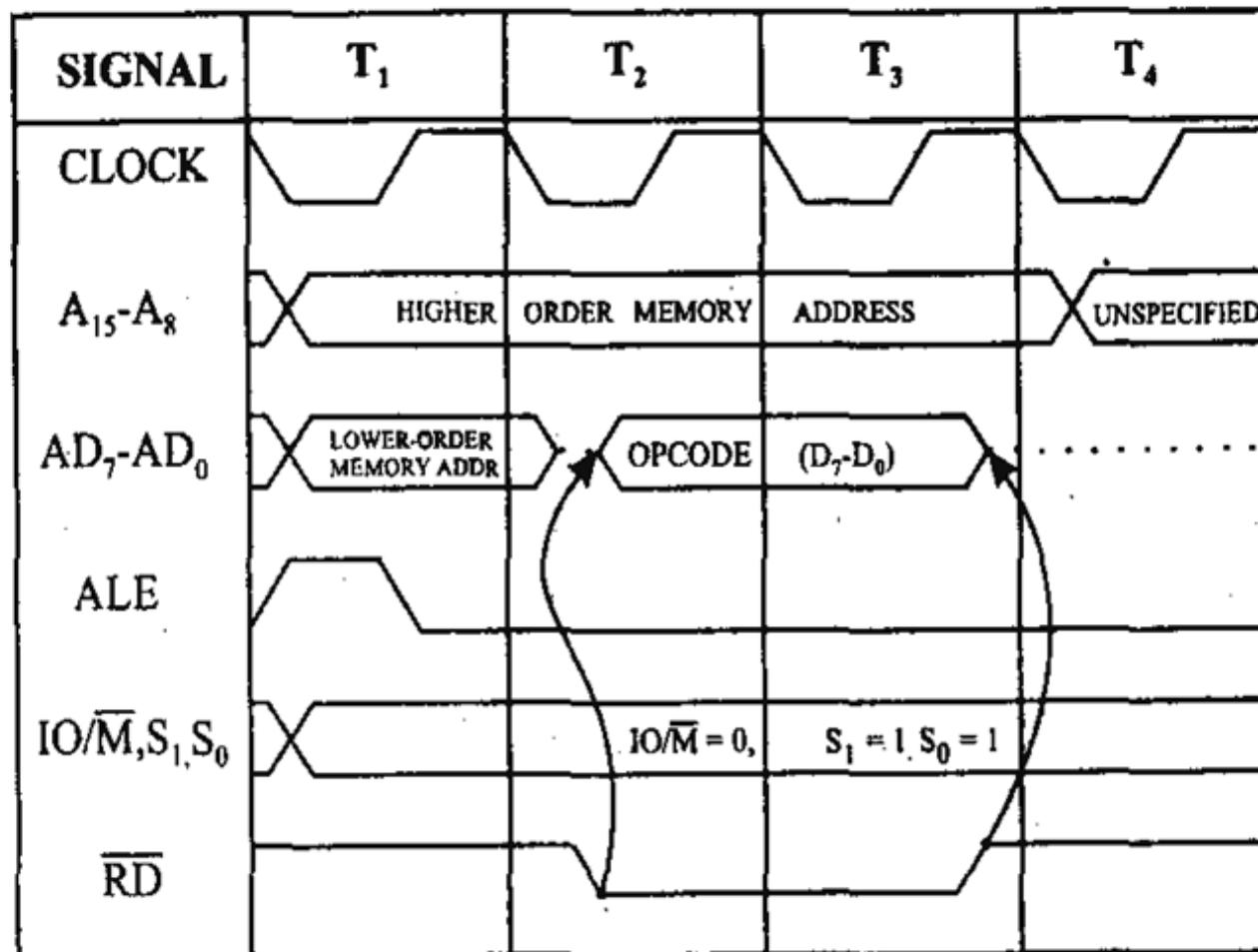
I/O READ CYCLE OF 8085



I/O WRITE CYCLE OF 8085



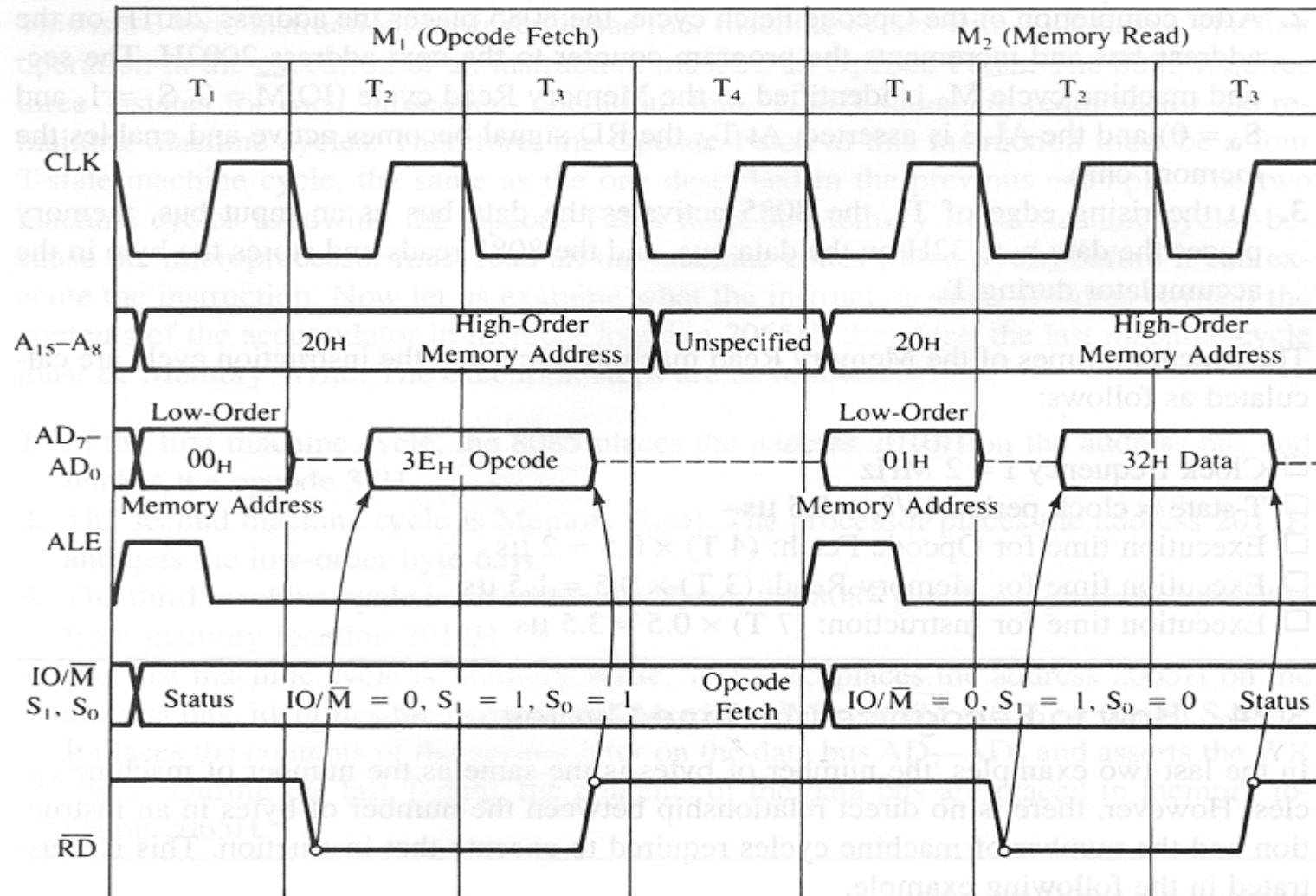
TIMING DIAGRAM OF MOV R₁,R₂



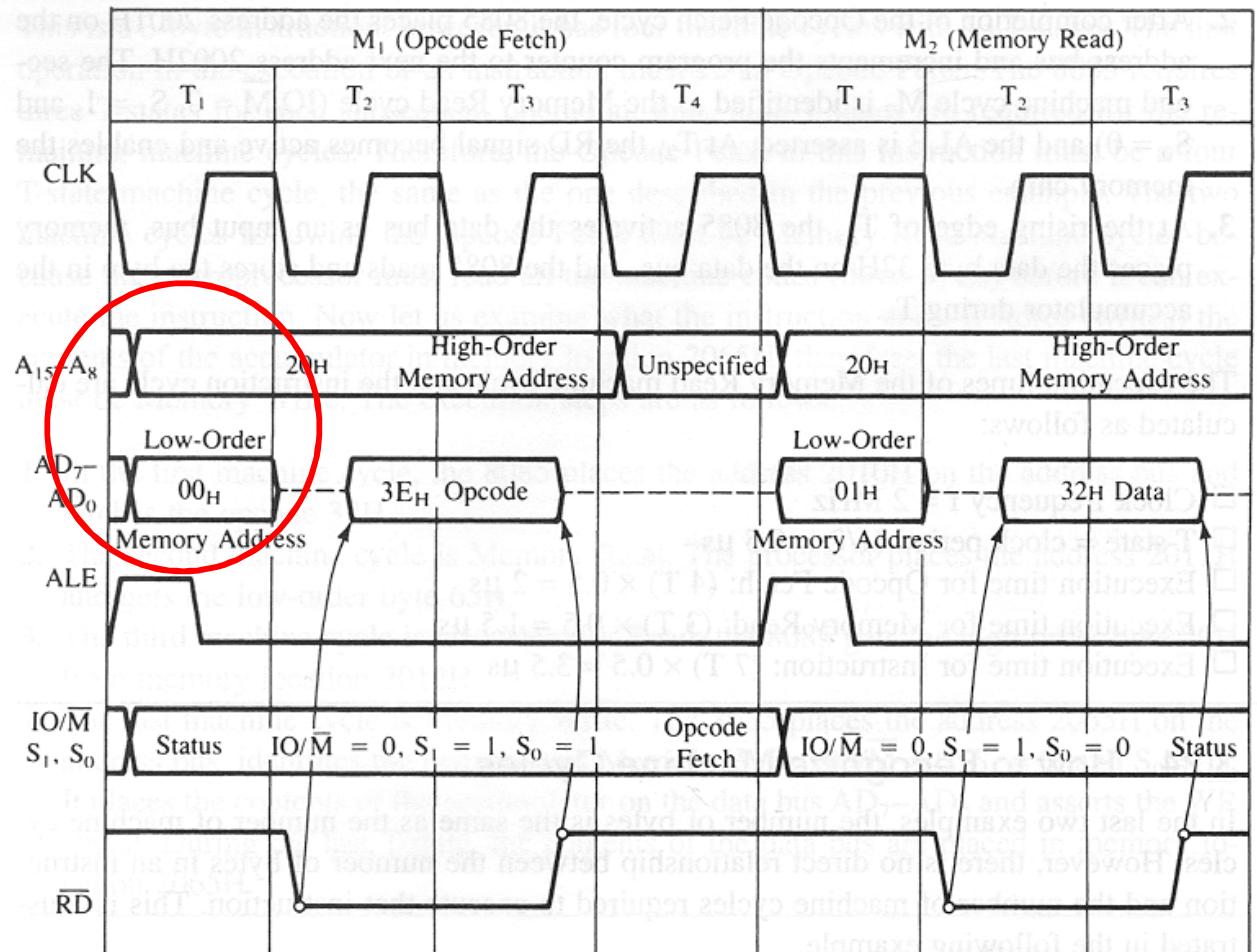
INSTRUCTIONS HAVING SIMILAR TIMING DIAGRAM

ALL MOV R1,R2	ALL ADD R
ALL ADC R	CMA,CMC,STC
ALL CMP R	ALL INR R
ALL DCR R	ALL ORA R,ANA R,XRA R
ALL ROTATE INSTRUCTIONS	ALL SUB R
ALL SBB R	RIM,SIM
DAA	EI,DI
NOP	XCHG

TIMING DIAGRAM OF MVI A,32 H

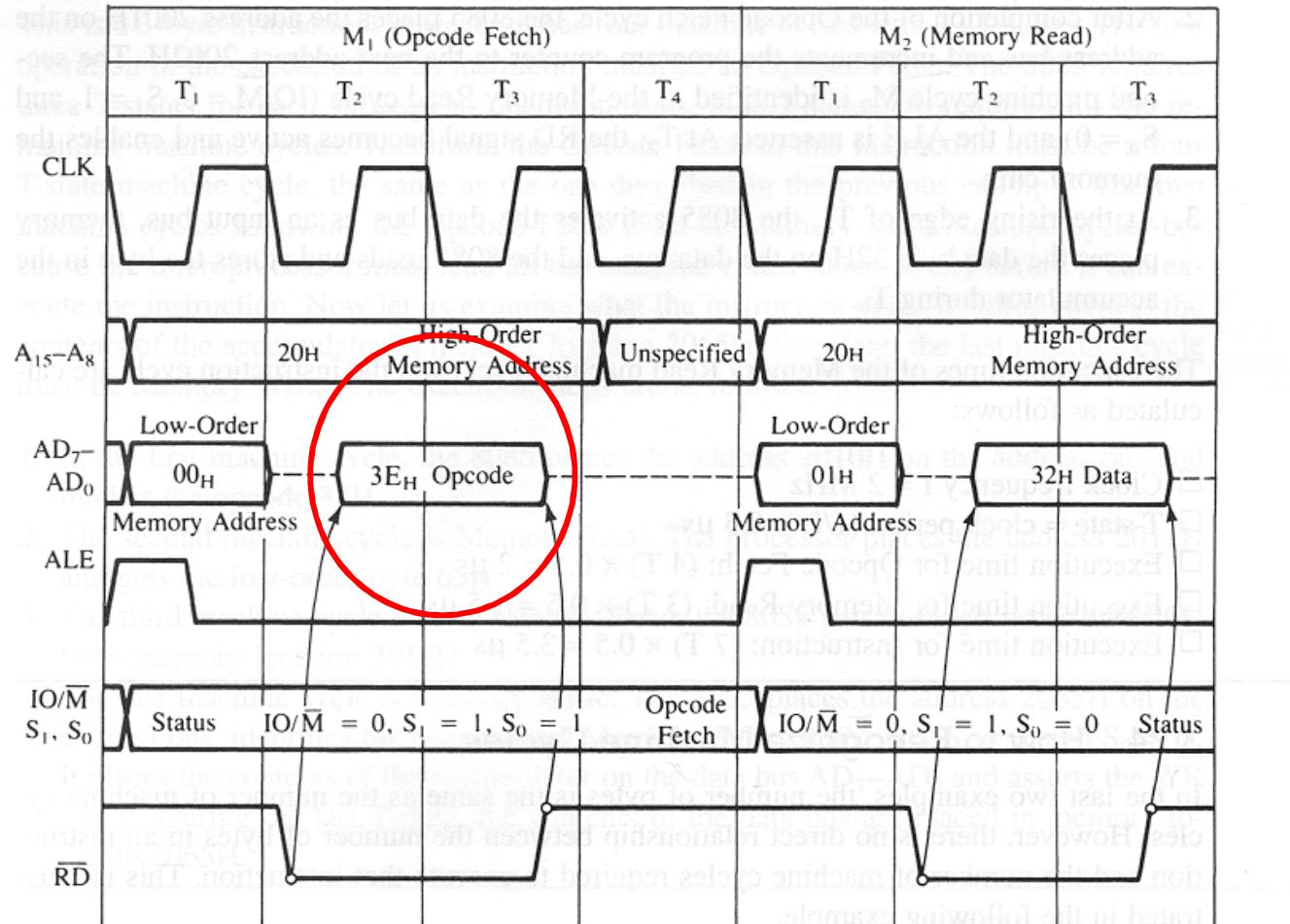


Execution of an Instruction

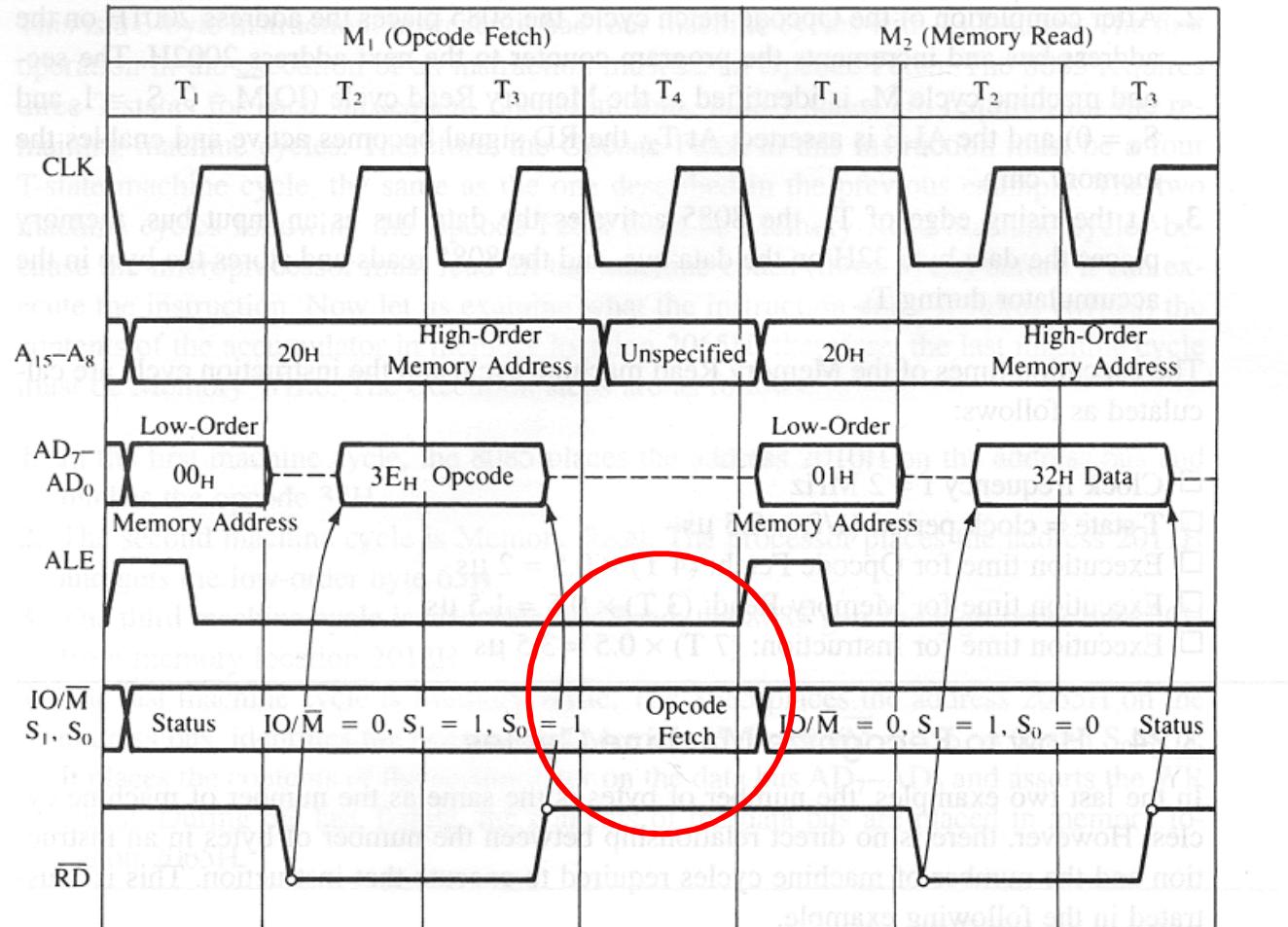


Put the first
memory
location on the
address bus
(2000 h)

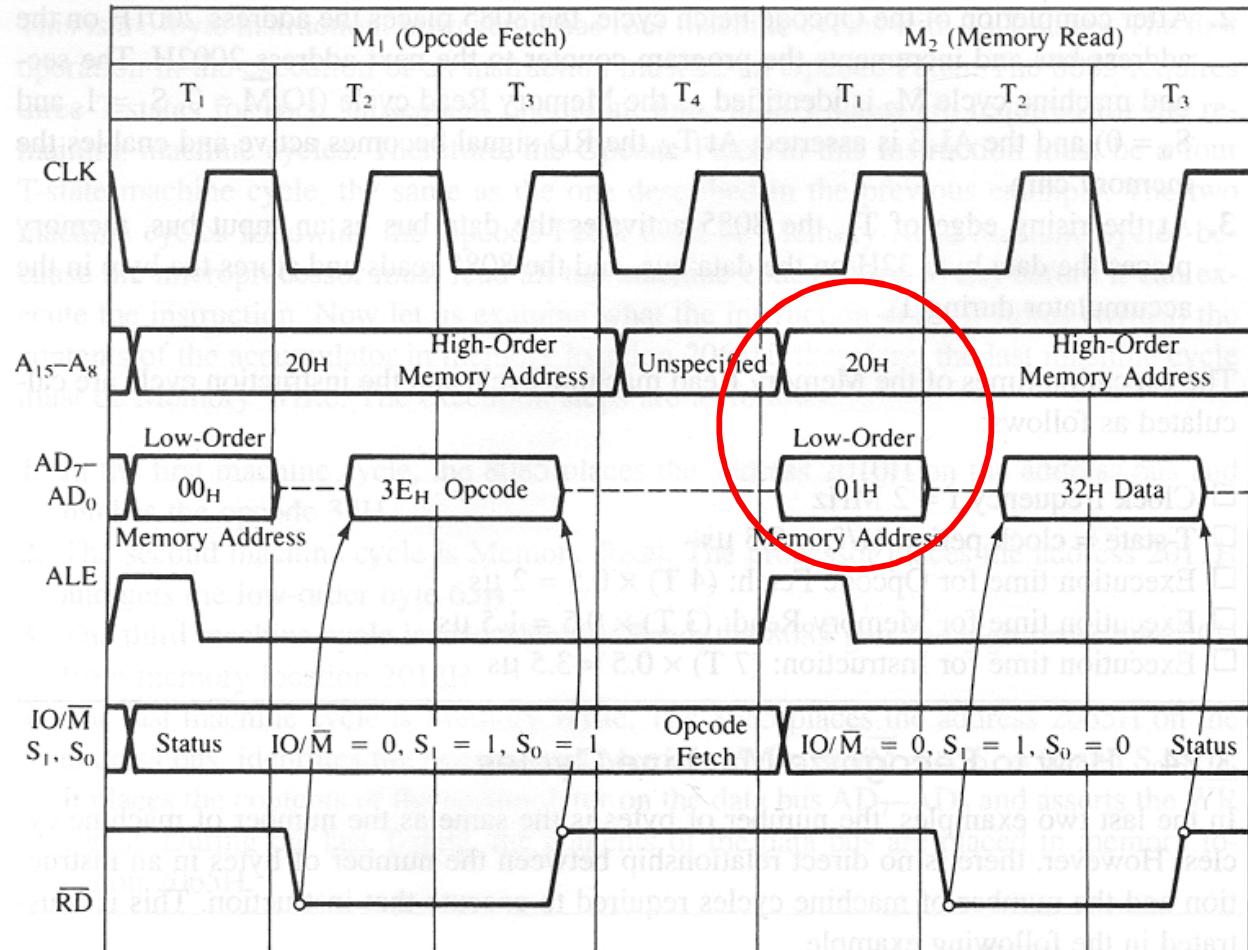
Execution of an Instruction



Execution of an Instruction

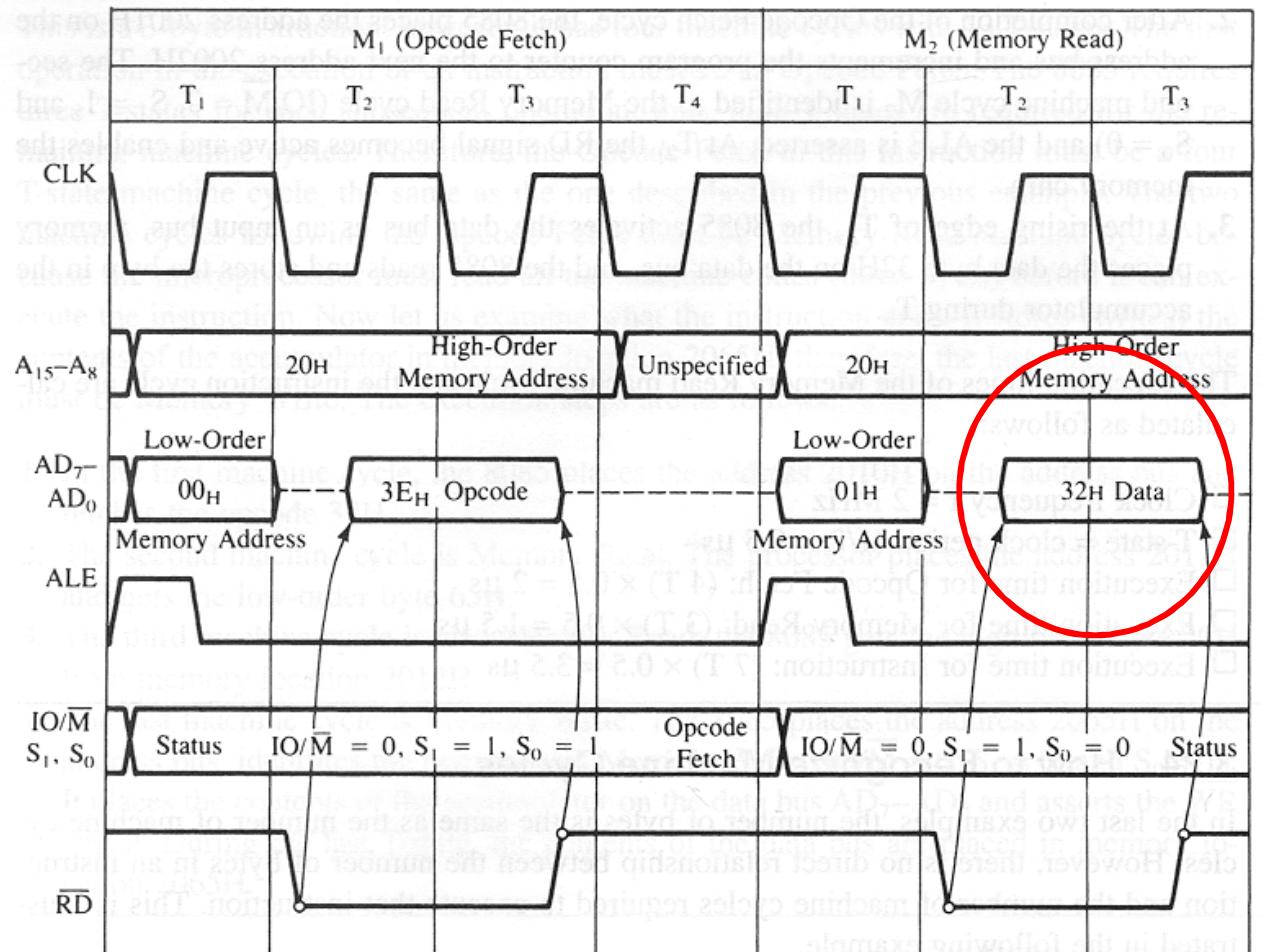


Execution of an Instruction



Put the next
memory
location on the
address bus
(2001 h)

Execution of an Instruction



Execution of an Instruction

How long does it take to execute this two-byte instruction (op-code) ?

- Clock frequency $f = 2 \text{ MHz}$
- T-state = clock period $(1/f) = 0.5 \mu\text{s}$
- Execution time for Opcode Fetch: $(4 \text{ T}) \times 0.5 = 2 \mu\text{s}$
- Execution time for Memory Read: $(3 \text{ T}) \times 0.5 = 1.5 \mu\text{s}$
- Execution time for Instruction: $(7 \text{ T}) \times 0.5 = 3.5 \mu\text{s}$

It is quite possible to accurately predict the time that is required to run each instruction, and to run the entire program !

INSTRUCTIONS HAVING SIMILAR TIMING DIAGRAM

ADI DATA	ANI DATA
ACI DATA	ORI DATA
SUI DATA	XRI DATA
SBI DATA	MVI R,DATA