HIGH-POWER-FACTOR ADJUSTABLE SPEED DRIVE USING DIODE CLAMPED MULTILEVEL INVERTER

G. A. Dhomane* and H. M. Suryawanshi**

*Assistant Prof., Electrical Engg. Dept., Govt. Engineering College, Chandrapur

**Professor, Electrical Engg. Dept., Visvesvaraya National Institute of Technology, Nagpur

ABSTRACT

This paper presents a new approach to alleviate the harmonics and to enhance the power factor of the adjustable speed drive (ASD). A conventional ASD with 2-level PWM inverters generate high dv/dt and high frequency common mode voltages which are harmful for the drive applications. It reduces the motor bearings life and conducted EMI deteriorates the insulation. In this paper a diode clamped multilevel (3-level) inverter is used to perform dual task. It generates high frequency (HF) current to be injected at the input of the three-phase front-end rectifier thereby improving the harmonic spectra and the power factor. It also drives the induction motor. The salient feature of this paper is that it does not require separate converters for improving power factor and to drive induction motor. Furthermore, inverter switches operate with zero voltage switching (ZVS), thus reducing the switching losses substantially. The voltage stress of the switches also has been reduced to half of the conventional 2-level converter. The inverter is operated with sinusoidal pulse width modulation (SPWM) technique. The simulation results for a prototype of 2.2 kW are presented.

INDEX TERMS

Adjustable speed drive, high frequency current injection, multilevel inverter, and zero voltage switching.

INTRODUCTION

According to the estimate of Electric Power Research Institute (EPRI) of USA, around 65% of greed energy in USA is consumed in electrical machine drives, and 75% of these are pump-, fan-, and compressor–type drives. It is reported that currently around 97% of medium to high power drives used for industrial applications operate at fixed speed [1], where flow is controlled by mechanical methods, such as throttling control, dampers, resulting in a substantial amount of power loss. It is seen that by using adjustable speed drive (ASD), with fully open throttle can improve the efficiency up to 30% at light load [2].The ASDs are used to save electric energy and increase productivity in variable-output work processes of all new and well-established industries such as: digital information gadgets, digital home appliances, automotive and robotics, electric actuators, pump compressors, other vehicles, industrial processes, and distributed and renewable energy system etc. The ASDs, generally require rectifier inverter arrangements. Three-phase diode rectifiers are extensively used as the front end rectifiers as they are cheap and simple. However, for three-phase rectifier not only the power factor is penalized but also a current with high harmonic content is drawn from the utility [3].The total harmonic distortion (THD) of such system increases to 80% [4]. With the increasing use of ASDs, as different PWM techniques are used, the major concern is of harmonic reduction in the system. The basic harmonic reduction techniques such as passive filters, active filters, multipulse rectifiers and harmonic current injection methods have their own merits and demerits. The passive filters are bulky and prone to resonance. The accurate current templates are required in most of the active filters, which are difficult to generate and adjust. Different three-phase topologies have been proposed to obtain a low harmonic content and to improve the power factor [5]-[22]; the current shaping has been extensively used as good choice in three-phase systems [12]-[20]. An integrated single switch approach is provided in [12]. This scheme is simple and easy to implement, but requires transformers and the line current THD is also higher. A passive net construction circuit is proposed in [13]. The resistances present in the scheme cause additional power loss in the passive net. The scheme in [14] shows significant reduction in line current harmonic, but requires interconnection of a Wye-delta zigzag transformer with access to the neutral to circulate the third harmonic current. Above schemes with transformers become uneconomical for low and medium power capacity. Several new techniques have been proposed [15] and [16], for improving the performance of three-phase rectifiers. The neutral connection is

eliminated in [17]-[19] and show reduction in THD. These utilize inductors with significant size as they operate on the line frequency. Moreover, the split capacitors and three bidirectional switches, each switch requiring one active switch and four diodes are used. The high-power-factor, front-end rectifier is proposed in [20]. In this scheme, the switches are hard-switched. The high-power factor converters using high-frequency current injection are presented in [21]-[22]. THD is low and offers high power factor however, switches experience high voltage stresses in restricting its application to medium voltage drives. The several configurations of the dc-voltage link multilevel converters were proposed in [23].

This paper presents a single-stage, soft-switched converter for medium to high voltage high-power-factor ASD with multilevel inverter. No separate switches or converter is needed for line current shaping and for driving the motor unlike conventional schemes. The high frequency current is injected from diode clamped multilevel inverter (DCMLI) to the three-phase rectifier thereby, producing a high-frequency modulation of the rectifier input voltages. This results in inherent high-power-factor operation due to the continuous conduction mode (CCM) of operation of input source inductors. Thus, the need of active front-end rectifier (with IGBTs) is eliminated. The topology is characterized by low THD, low EMI conduction and low switching loss owing to soft switching. The major advantages of the proposed schemes are; it does not require additional active components for current injection and the switching stresses are reduced to half of the conventional methods and that makes it suitable for high-voltage drive applications.

TOPOLOGY DISCRIPTION AND OPERATION

The proposed three-phase HF current injection topology is depicted in Fig.1. It consists of line source inductors (L_{SR}-L_{SB}), a three-phase diode bridge rectifier (D_1-D_6) and HF current injection circuit. The HF current injection circuit comprises of three-phase diode clamped multilevel inverter (DCMLI), dc blocking capacitors (C_1-C_3) and high-frequency inductors (L_1-L_3). These inductors are connected to the input side of the three-phase rectifier. The output dc voltage, V_{dc} of the rectifier acts as the input to the inverter through two split capacitors (C_{dc1}-C_{dc2}) with 0 as the midpoint. Each leg of the DCMLI (Fig. 2a) consists of four active switches (S_{11}-S_{14}) and two clamping diodes (D_{11}-D_{12}). One phase-leg of a three-level DCMLI consists of four IGBTs and two clamping diodes. The other two phase-legs would be connected across the same dc bus and the clamping diodes connected to the same midpoint 0 of the dc capacitor. The phase and line voltages of DCMLI can be seen in Fig. 2b. Each phase-leg of the converter has two pairs (S_{11}, S_{12} and S_{13}, S_{14}) of switching devices in series. It seems like doubling the number of devices from two (a conventional two-level converter) to four per phase-leg in addition to providing two extra diodes. However, doubling the number of devices with the same voltage ratings would double the dc voltage and hence the voltage and power capacity of the converter also. Thus, only the addition of clamping diodes per phase-leg adds to the converter cost. If the converter were a high voltage converter with devices in series then the number of devices would be about the same. A diode clamp at the midpoint also helps to ensure a more decisive voltage sharing between the pair of devices. Despite the higher conduction losses (two devices in current path) three-level topology features lower total semiconductor losses than conventional and fast IGBTs in a two-level topology as the switching frequency increases. The multi-level topology has the following additional advantages as compared to the two-level topology.

- superior harmonic spectrum for a given switching frequency
- lower voltage stress on switches, cables and transformer/motor windings and
- substantially lower switching losses.

If the ac voltage pulse width is of duration σ per half-cycle, then the fundamental rms voltage is given by

$$V_1 = \frac{2\sqrt{2}}{\pi}\left(\frac{V_{dc}}{2}\right)\sin\frac{\sigma}{2} = \frac{2\sqrt{2}}{\pi}\left(\frac{V_{dc}}{2}\right)\cos\alpha \qquad (1)$$

where, $\sigma = \pi - 2\alpha$ and V_{dc} = dc link voltage

In the converter, feed back capacitors (C_1-C_3) and inductances (L_1-L_3) are designed for high frequency operation. Therefore, feedback capacitor offers very high impedance to supply voltage. Hence, the voltage across the capacitor C_1, (v_{C1}) has modulation of supply frequency of 50 Hz. Therefore, at any instant the voltage across the C_1 is equal to the supply voltage, v_R. As the capacitor carries high frequency current, the v_{C1} has HF voltage ripples superimposed on power frequency component. This capacitor also serves the dc blocking to the injected current. The principle of operation of the proposed converter is best understood by a single-phase-leg equivalent circuit as depicted in Fig. 2(a). The devices are switched at high frequency, f_S. During a particular

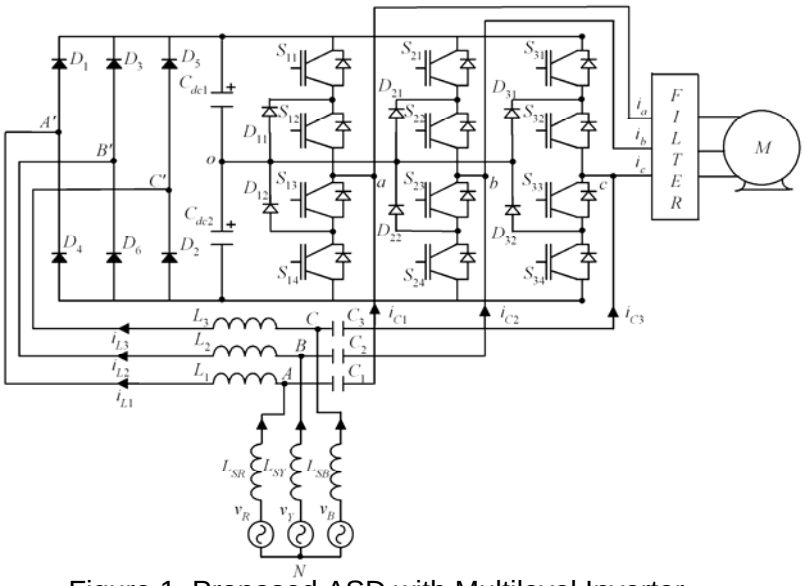
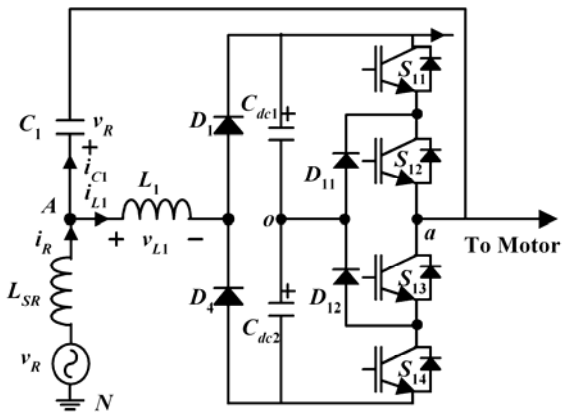


Figure 1. Proposed ASD with Multilevel Inverter



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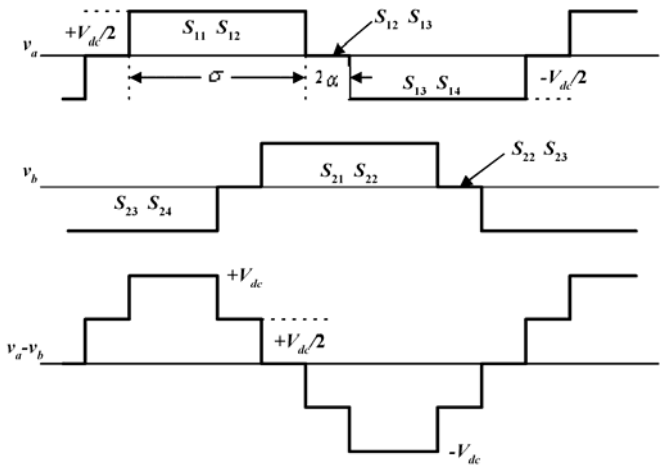


(b)

Figure 2. (a) Single-phase-leg equivalent circuit. (b) Output pole voltage and line voltage DCMLI.

switching interval, k, when upper switches S_{11} and S_{12} are on and lower switches S_{13} and S_{14} are off, the voltage across L_1, (v_{L1}), during this interval is same as input phase voltage v_R. The current i_{L1}, through L_1 increases linearly from 0 to its peak value I_{L1p} (Fig. 3a) at the rate proportional to the instantaneous value of the supply phase voltage v_R. The other inductors current also increase at the rate proportional to the instantaneous values of their respective phase voltages. At the same time the capacitor current, i_{C1} decreases from its positive peak $+I_{C1p}$ to negative peak - I_{C1p} through 0. Due to high-frequency switching, the supply current i_R is the sum of average values of i_{L1} and i_{C1}. Hence input supply current is given by

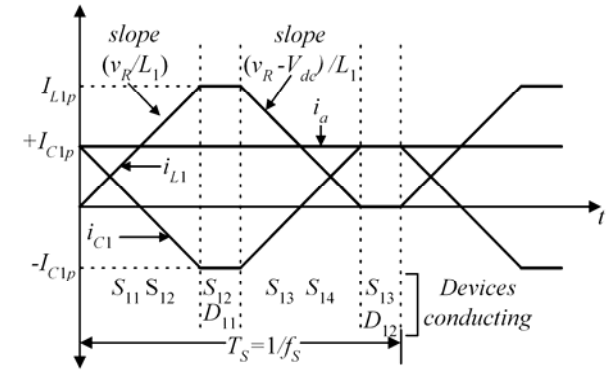
$$i_R = I_{L1avg} + I_{C1avg} \quad (2)$$

where, I_{L1avg} and I_{C1avg} are average values of inductor and capacitor currents. During the interval when upper switches (S_{11} and S_{12}) are on,

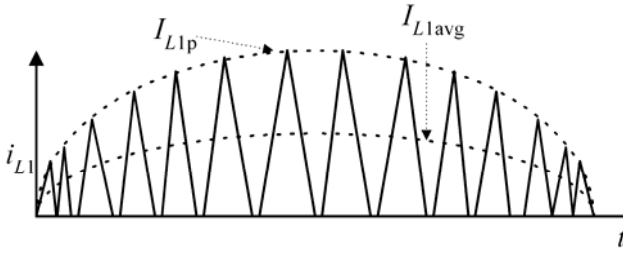
$$I_{L1avg} = \left(\frac{I_{L1p}}{2}\right), I_{C1avg} = 0 \quad (3)$$

When switches, S_{12} and S_{13} are on (S_{11} and S_{14} off), the voltage across L_1 is (V_{dc}/2)-v_R. The current i_{L1} remains constant at I_{L1p} and capacitor current is $-I_{C1p}$. During this interval, as clamping diode D_{11} conducts and i_{L1} remains constant, the voltage across L_1, is zero.

When lower switches, S_{13} and S_{14} are on, the voltage across L_1 is (v_R-V_{dc}). The i_{L1} decreases from its peak value I_{L1p} to zero and remains zero till the next cycle begins. The i_{C1} ramps up to its peak value $+I_{C1p}$ from $-I_{C1p}$ and remains at $+I_{C1p}$ till the next cycle begins.



(a)



(b)

Figure 3. (a) Idealized inductor, capacitor and supply currents . (b) Inductor current envelop

The peak current value, I_{L1p}, in a particular switching cycle, varies with the value of input voltage in that cycle. The values of input voltage, during different switching cycles, vary sinusoidally. Therefore, the peak values, I_{L1p} also varies sinusoidally in the envelope defined by the supply phase voltage as depicted in Fig. 3(b). The supply current, i_R is the sum of average values of i_{L1} and i_{C1}. Moreover, the average value of i_{C1} over a switching cycle is zero. Therefore, i_R is equal to the I_{L1avg}. Since, each time inductor current pulses begin at zero (discontinuous conduction), the I_{L1avg} and i_R also vary sinusoidally in phase with the supply voltage. The similar action takes place in other phases and in negative half-cycle also. Therefore, the overall power factor is very close to unity. The HF switching of inductor forces diodes of the three-phase rectifier to turn on and off at the switching frequency during the complete cycle of the supply voltage. When none of the diodes is conducting, the supply current flows through the capacitor C_1, the switch S_{13} and the clamping diode D_{12}. Thus, maintains the continuous current through the source inductor L_{SR}. Hence, the discontinuity in the supply current, which is mainly responsible for deteriorating the quality of the supply current, is removed which results in continuous conduction mode (CCM) operation of source inductor. Therefore, the operation of source inductors in CCM leads to inherent active wave shaping of input current and improvement in input power factor.

ANALYSIS

In order to simplify the analysis following assumptions are made

1) Input three-phase supply is balanced and purely sinusoidal.
2) The switching frequency is far greater than the power line frequency ($f_S >> f$).
3) The resistance of the inductors is adequately small to be neglected.
4) All the switches are ideal.

The three-phase voltages are given by

$$v_R = V_p \sin(\omega t)\ ,\ v_Y = V_p \sin(\omega t - \frac{2\pi}{3})\ ,$$

$$v_B = V_p \sin(\omega t + \frac{2\pi}{3}) \qquad (4)$$

A. Input supply current, i_R

Since the switching frequency is very high, the ac line current in a switching period, as stated earlier, is the sum of average values of i_{L1} and i_{C1}. Therefore,

$$i_R = i_{L1(avg)} + i_{C1(avg)} \qquad (5)$$

$$i_{L1(avg)} = \frac{1}{T_S}\left[\int_0^{\sigma}\left(\frac{I_{L1p}}{\sigma}t\right)dt + \int_{\sigma}^{\sigma+2\alpha} I_{L1p}\,dt + \int_{\sigma+2\alpha}^{2\sigma+2\alpha}\frac{I_{L1p}}{\sigma}\left(-t+2\sigma+2\alpha\right)dt + \int_{2\sigma+2\alpha}^{2\sigma+4\alpha} I_{L1p}\,dt\right]$$

$$= \frac{I_{L1p}}{2} \qquad (6)$$

From (6), the average current is given by

$$i_{L1(avg)} = \frac{v_R}{2L_1}\left(\frac{\sigma}{\omega_s}\right) \qquad (7)$$

If T_s is the switching period of the DCMLI and V_p is the peak value of the supply phase voltage, then (7) can be given as

$$i_{L1(avg)} = \frac{\sigma T_s}{4\pi L_1} V_p \sin\omega t \qquad (8)$$

The average value of the current through the capacitor, i_{C1} is zero.

Therefore (2) and (8) lead to supply current as

$$i_R = \frac{\sigma T_s}{4\pi L_1} V_p \sin\omega t = K V_p \sin\omega t \qquad (9)$$

where, $K = \frac{\sigma T_s}{4\pi L_1}$

The equation (9) clearly indicates that, the input supply current i_R, is always in phase with the

supply voltage, v_R. Hence the proposed converter operates at unity power factor.

B. Input power and current

Input power is given by

$$P = 3\left[\frac{1}{\pi}\int_0^{\pi} v_R i_R d\omega t\right]$$

where, v_R and i_R are the supply phase voltage and current respectively.

From (4) and (9)

$$P = 3\frac{1}{\pi}\int_0^{\pi} v_p \sin\omega t \cdot \frac{\sigma T_S}{4\pi L_1} v_p \sin\omega t d\omega t = \frac{3{v_p}^2 \sigma T_S}{8\pi L_1} \quad (10)$$

Input rms current can be given as;

$$I_{Rrms} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\frac{\sigma T_S}{4\pi L_1} V_p\right)^2 \sin^2\omega t d\omega t} = \frac{\sigma T_S V_p}{4\sqrt{2}\pi L_1} \quad (11)$$

C. Design of inductor, L_1

Three-phase power is given by

$$P = 3V_{Rrms} I_{Rrms}$$

$$P = 3\frac{V_p}{\sqrt{2}}\frac{\sigma T_S V_p}{4\sqrt{2}\pi L_1} \quad (12)$$

From (31) the value of the inductor L_1

$$L_1 = \frac{3{V_p}^2 \sigma T_S}{8\pi P} \quad (13)$$

If η is efficiency and P_o is output power of the converter then

$$L_1 = \frac{3{V_p}^2 \sigma T_S \eta}{8\pi P_o} \quad (14)$$

D. Design of capacitor, C_1

The rms value of the current through the capacitor, C_1 is given as

$$I_{Crms} = \frac{I_p}{\sqrt{3}}\sqrt{\frac{3\pi - 2\sigma}{\pi}} \quad (15)$$

Energy stored in the capacitor is given by

$$\frac{1}{2}C_1 {V_{Rrms}}^2 = V_{Rrms} I_{Rrms} T_S$$

$$C_1 = \frac{2\left[\frac{I_p}{\sqrt{3}}\left(\sqrt{\frac{3\pi - 2\sigma}{\pi}}\right)\right]T_S}{V_{Rrms}}$$

$$C_1 = \frac{4\sqrt{2}P_o\left(\sqrt{\frac{3\pi - 2\sigma}{\pi}}\right)}{3{V_p}^2 f_s \eta} \quad (16)$$

where, f_S is switching frequency, P_o is the output power and η is the converter efficiency.

DESIGN PROBLEM

To validate the proposed scheme, a three-phase induction motor is used with the converter designed with the following specifications:

Specifications of the proposed scheme

a. Induction motor
   Input power = 3 hp (2.2 kW), three-phase
   voltage = 400 V, 50 Hz
   Speed = 1500 rpm.

b. Proposed converter
   Rated ac input voltage per phase, V_R = 230 V
   Input supply frequency, f = 50 Hz
   DC bus voltage, V_0 = 650 V
   Rated output of the converter, P_0 = 2.2 kW
   Switching frequency, f_S = 50 kHz

Calculations of inductor and capacitor

a. Feedback inductor (L_1-L_3)

Using equation (14) with output power, P_0 = 2.2 kW, σ = 150^0 and assumed efficiency of the converter as 92%, the value of the feedback inductor is estimated to

$$L_1 = \frac{3{V_p}^2 \sigma T_S \eta}{8\pi P_o} = 276.07 \ \mu\text{H}$$

b. Feedback Capacitor (C_1-C_3)

Feedback capacitor can be evaluated by using equation (16)

$$C_1 = \frac{4\sqrt{2}P_o\left(\sqrt{\frac{3\pi - 2\sigma}{\pi}}\right)}{3{V_p}^2 f_s \eta} = 1.038 \ \mu\text{F}$$

Hence, C_1 = C_2 = C_3 = 1 μF (polypropylene capacitor) is chosen.

C. Calculations of filter components

The output filter is connected between multilevel inverter and the induction motor. The maximum resonance frequency of the filter is selected to be the half of the switching frequency. The design is carried out as per [13]-[14].

$f_c = \frac{1}{2\pi\sqrt{LC}}$, where, f_c is the cutoff frequency

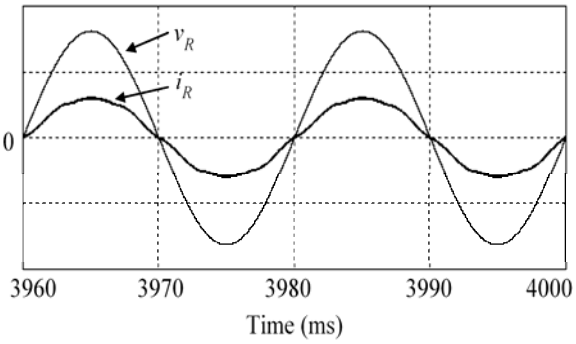
f_c = 25 kHz. The filter L and C components found to be

L = 1mH and C = 40 nF

Due to high frequency switching the filter component size and cost are greatly reduced.

RESULTS

A detailed analysis of the ASD with DCMLI is carried out and based on the design, The following values of components are selected for the simulations.



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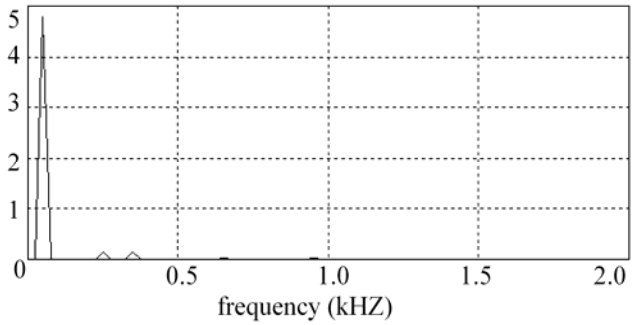

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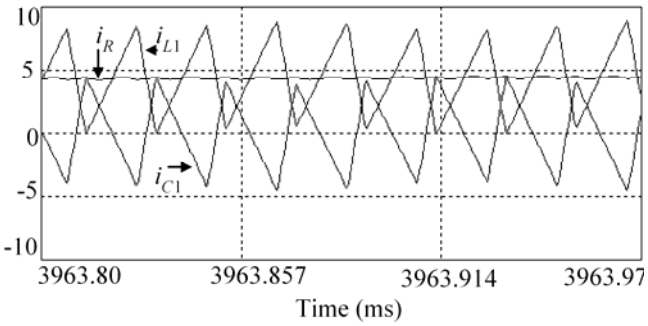
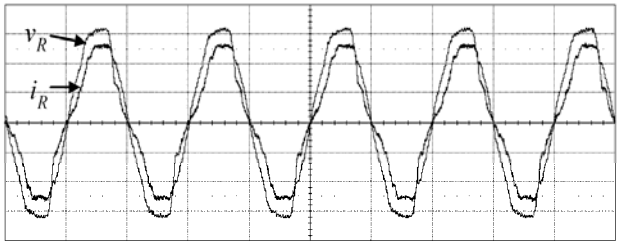


(c)

Figure 4. Simulation results: (a) Supply phase voltage (200 V/div.) and current (10 A/div.). (b) FFT of supply current. (1 A/div.) (c) Supply, inductor and capacitor currents (5 A/div.)

L_{SR}=L_{SR}=L_{SB} = 0.5 mH, C_1=C_2=C_3 = 1 μF, L_1=L_2=L_3 = 275 μH, C_{dc1}=C_{dc2}= 470 μF.

The simulation (using PSIM) of the proposed converter is carried out and the simulation results are depicted in Fig 4. Fig. 4a shows the supply phase voltage and phase current indicating the unity power factor of the converter. Fig. 4b shows the *FFT* of the supply current, whereas, Fig. 4c shows supply current, inductor current and capacitor current. The experimental results are shown in Fig. 5. The supply phase voltage and current are shown in Fig. 5a. These waveforms confirm the high-power-factor operation of the



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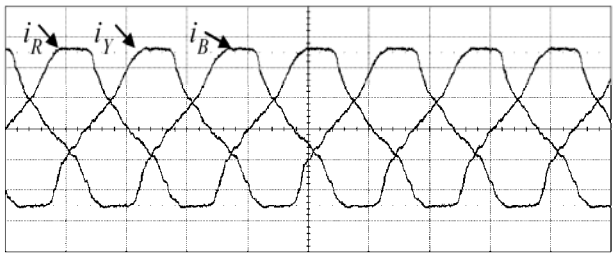

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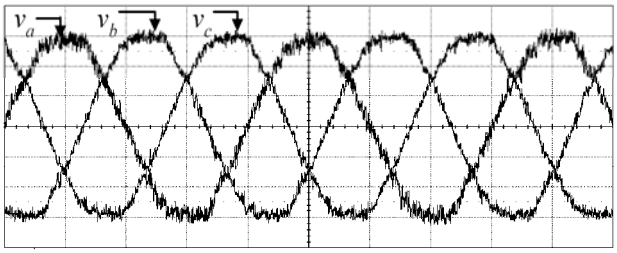

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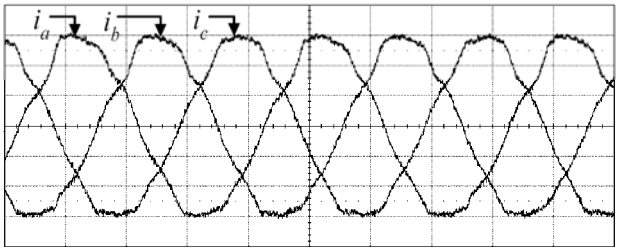

(d)

Figure 5. Experimental results: (a) Supply phase voltage (100V/div.) and current (2 A/div.). (b) Three-phase supply currents.(2 A/div.). (c)Three-phase motor terminal voltage (100 V/div.). (d) Three-phase motor current (2 A/div).

converter. Fig. 5b shows the three-phase supply current waveforms. The THD of the input current at full load is found to be 3.2 %. The experimental waveforms of supply current, inductor current and capacitor current are depicted in Fig. 5c. The experimental switch voltage and current waveforms are given in Fig. 5d. These waveforms

indicate the zero voltage switching (ZVS) of the switches. This eliminates the turn-on losses associated with the power switches. In addition, the soft-switching reduces the switch stress and improves the device utilization. The full load efficiency of the converter is found to be 92% The experimental results comply with the theoretical analysis and simulation. The experimental performance of the converter is summarized in Table 1.

Table 1: Performance of the converter under different loads

Parameter	Full load	50% load	25% load
Input PF	0.998	0.987	0.980
%THD, line current	3.2	4.8	6.4

CONCLUSIONS

Analysis, design and simulation of a three-phase proposed converter are carried out. The proposed three-phase convert offers many advantages such as unity power factor operation, high THD, low EMI and low switch stresses. The soft-switching of the devices decreases the switching losses therby increasing the efficiency. Switch voltage stresses are reduced and voltage capability is increased due to multilevel structure. The topology is suitable for medium to high voltage high power ASD applications.

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Biography

Gunwant A. Dhomane was born in Wardha, India on 1963. He received B. E. degree in Electrical Engineering from Walchand College of Engineering, Sangli, Kolhapur University and M. E. from Government College of Engineering, Amravati University, Amravati and Ph. D from VNIT, Nagpur in 1986, 1995 and 2010 respectively. He is an Assistant Professor in Electrical Engineering Department at Government College of Engineering, Chandrapur. His research interest includes ac-dc and ac-ac converters, UPS, soft-switching techniques, digital controllers and power-factor-correction circuits

Hiralal M. Suryawanshi was born in Nagpur, India, on January 1, 1963. He received the B.E. degree from Walchand College of Engineering, Sangli, India, in 1988, the M.E. degree from the Indian Institute of Science, Bangalore, India, in 1994, and the Ph.D. degree from Nagpur University, Nagpur, in 1998, all in electrical engineering. He is currently Professor with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, and Nagpur. His research interests include power electronics, emphasizing the developmental work in the areas of resonant converters, power factor correctors, active power filters, FACTs devices, multilevel converters, and electric drives. Dr. Suryawanshi is a member of the Institution of Electrical Engineers, U.K., and the Institution of Engineers (India).