COMPARISON OF DIFFERENT TOPOLOGIES OF MULTILEVEL CURRENT SOURCE CONVERTER

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Abstract - **This paper a new topology for multilevel current source converter. The main agenda in choosing the platform of multilevel current source converters is for the current applications. The new converter uses parallel connections of full-bridge cells. The IGBT (switches) in these cells are designed using matrix converter. Four different methods have been presented for obtaining multi level outputs. In method 1 all DC current sources are equal to Idc which is known as symmetrical multilevel current source converters where the number of level of overall output current is given by S=1+(2N). In method 2, the number of power devices required depends on the output current level needed. To provide a large number of output levels without increasing the number of converters, the asymmetrical multilevel current source converters are used in which at least one of the DC sources is different from the other sources. The number of levels of the output current is given by S=1-2^(N+1).In method 3, the levels of DC current sources in the asymmetrical multilevel current source converters is given by** $S = 1 + 2\sum_{k=1}^{N} Idc, k$ **.In method 4, the number of levels of overall output current is given by S=3^N. These methods provide more flexibility and can generate large number of levels (odd and even), and also the number of output current levels can be easily adjusted. Using higher levels, the multilevel current converter generates approximately sinusoidal output current with very low harmonic distortion. The proposed current source converter will simulated using the SIMULINK tool box available in MATLAB platform and the results will be compared with traditional method to check whether the harmonic content is very low. If so, the new multilevel current source converter topology can form the core for the current applications, such as statcom, shunt active filters, active power line conditioners etc. All these methods are compared based on the THD levels.**

I. INTRODUCTION

Recently multilevel power conversion technology has been a very rapidly growing area of power electronics with good potential for further developments. The most attractive applications of this technology are in the medium to high-voltage range[1]. Multilevel converters work more like amplitude modulation rather than pulse modulation, and as a result:

- Each device in a multilevel converter has a much lower dv=dt
- The outputs of the converter have almost perfect currents with very good voltage waveforms because the undesirable harmonics can be removed easily
- The bridges of each converter work at a very low switching frequency and low speed semiconductors can be used and

- Switching losses are very low [2].

The general function of the multilevel converter is to synthesize a desired output voltage from several levels of DC voltages as inputs. The DC voltage sources are available from batteries, capacitors, or fuel cells. There are three types of multilevel converters:

- Diode-Clamped Multilevel Converter
- Flying-Capacitor Multilevel Converter
- Cascaded-Converters with Separated DC Sources

The first practical multilevel topology is the diode-clamped multilevel converter topology [3]. The converter uses capacitors in series to divide the DC bus voltage into a set of voltage levels. To produce *N* levels of the phase voltage, an *N*-1level diode-clamp converter needs *N*-1 capacitors on the DC bus. The flying capacitor multilevel converter [4], [5] uses a ladder structure of the DC side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate *N*-1level staircase output voltage, *N*-1 capacitors in the DC bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the out put waveform. The last structure introduced in this paper is a multilevel converter, which uses cascade converters with separate DC sources and first used for plasma stabilization [6] it was then extended for three-phase applications [7]. The multilevel converter using cascaded-converter with separate DC sources synthesizes a desired voltage from several independent sources of DC voltage. A primary advantage of this topology is that it provides the flexibility to increase the number of levels without introducing complexity into the power stage. Also, this topology requires the same number of primary switches as the diode-clamped topology, but does not require the clamping diode. However, this configuration uses multiple dedicated DC-busses and often a complicated and expensive line transformer, which makes this a rather expensive solution. In addition, bidirectional operation is somewhat difficult to achieve [8]. Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitor. The number of output voltage levels can be adjusted by adding or removing the full-bridge cells.

The converters that were focused upon were voltage source converters, with multilevel voltage waveforms. These converters divide the total input voltage among a number of switches and allow a reduction of voltage harmonics. As mentioned, these are the most commonly used and best-understood multilevel converters.

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The most multilevel converters discussed in the literature are multilevel voltage source converters [9]. However, in many current applications, such as shunt active filters, active power line conditioners, VAR compensations etc., we need to use multilevel current converters. This paper presents a new multilevel current converter, and introduces four different algorithms for obtaining the levels of current sources in each bridges of the multilevel current source. Then the proposed multilevel current source converter is the core for the current applications, such as statcom , shunt active filters, active power line conditioners etc. **,** which is obtained based on this converter. The proposed new multilevel current converter consists of a set of parallel single-phase full-bridge converter units. The AC current output of each levels full-bridge converter is connected in parallel such that the synthesized current waveform is the sum of the converter outputs. In other words, for high current applications, many switches can be placed in parallel, with their current summed by inductors.

II. DEFINITIONS

In this section, a definition of elements that are required for constituting the multilevel is presented. Any power electronic converter can be viewed as a matrix of switches, which connects its input nodes to its output nodes. These nodes may be either DC or AC, and either inductive or capacitive; and the power flow may be in either direction. Some basic laws of electricity enforce two obvious restrictions:

*If one set of nodes (input or output) is inductive, the other set must be capacitive, so as not to create a cut set of voltage or current sources when the switches are closed.

*The combination of open and closed switches should never open circuit an inductor, or short circuit a capacitor.

The term converters are generally broken into a number of subsets. The term rectifier is used when the power flow is predominately from the AC port to the DC port and the term inverter is used when power flow is predominately from the DC port to the AC port. The term converter is used either when there is no predominant direction of power flow or as a general term to encompass both rectifiers and inverters. In a voltage source converter, the DC port is the capacitive port and voltage stiff (i.e. a large DC bus capacitor). The voltages in such a converter are well defined by this port and are generally considered independent of the converters operation. The value of the AC side inductance is comparatively small and modulation of the converter controls the AC side inductor currents. The voltage source converter should be responsible for the control of the DC bus capacitor voltage, and then the voltage is indirectly controlled by controlling the net current flow in the capacitor. The switches in such a converter must block a unidirectional voltage, but be able to conduct current in either direction if bidirectional power flow is desired as shown in (Fig.1).
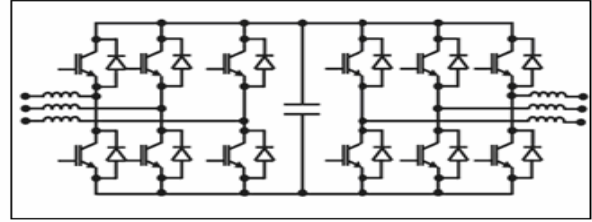

Fig.1: A Voltage Source Rectifier-Inverter Cascade

In a current source converter, the DC port is inductive and current stiff. The current in this port is well defined and slow to change. The voltage (particularly at the AC port) is considered the variable directly controlled by the converter modulation. Since the AC port usually has significant line or load inductance, line to line capacitors must be placed on the AC port. The switches must block either voltage polarity, but are only required to conduct current in one direction as shown in (Fig. 2).
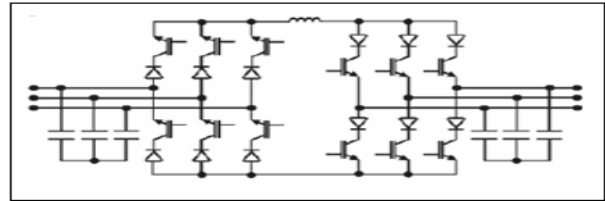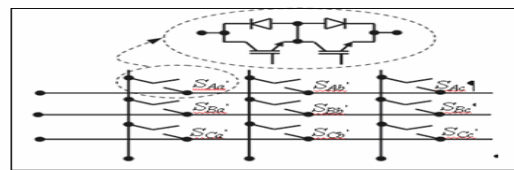

Fig 2: A current source rectifier-inverter cascade

Some converters do not easily fall, or cannot be placed into either category. The matrix or Venturini converter [10] is one example as shown in (Fig. 3). Both input and output ports are AC, and the definition of voltage stiff or current stiff (and hence voltage or current source) becomes somewhat arbitrary. Both input and output ports are AC, and neither port can be considered as a steady dc source, whether voltage or current. The next refinement is to define the meaning of multilevel. The following definition of a multilevel converter is offered [9]:

A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current.

The term two-level will be used where it is necessary to refer specifically to a converter, which is not multilevel. For example, the multi-phase matrix converter (Fig. 3) is, strictly speaking, a multilevel converter, according to this definition. Consider the three-phase to three-phase matrix converter, with voltage source inputs and an inductive load. Any single output can be switched to one of three different voltage levels (the voltages of the three input phases) and similarly, any input can be switched to one of four current levels(including

ero).

Fig 3: The matrix converter with one possible implementation of bidirectional switches

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In this example, both the input and the output nodes are AC periodic varying quantities and so these levels can only be considered stationary for an interval much shorter than their AC period. Both the voltage source and current source converters can be derived from the general matrix converter by setting one port to be either a two terminal DC voltage stiff or DC current stiff port. Note that now one of the ports has been made DC and voltage or current stiff, only one port will experience the multilevel stepped waveforms. The other will still have a continuous waveform similar to that of an equivalent two level converter. The traditional understanding of what constitutes a multilevel converter follows this more narrow definition. One of the ports has multiple (more than two) voltage or current stiff DC nodes or terminals, while the second port has a conventional single or three phase set of terminals which are switched to these multiple levels. Most multilevel converters discussed in the literature step between multiple voltage levels. This is usually the most useful configuration for a high power converter, as reducing conduction losses in both converter and machines will always favor increasing the voltage rating rather than the current rating of the converter. Also as power levels increase, the input and output voltage levels presented to the converter increase. The structure of these multilevel converters places the switches in series to share the duty of blocking these higher voltages. Equally, however, for high current applications, many switches can be placed in parallel, with their current summed by inductors. When switched separately, multilevel current waveforms result. It is also possible to create completely new converter topologies based on the concept of circuit duals. The capacitive port sees a multilevel current waveform. All switches experience and must withstand the total converter input voltage. If the capacitive port were an AC port and the inductive port current stiff and DC, then this would be classified as a current source, multilevel current converter. For example, the flying capacitor converter (a multilevel voltage converter) and its dual as a flying inductor converter (a multilevel current converter) are shown in Figs. 4 and 5, respectively.
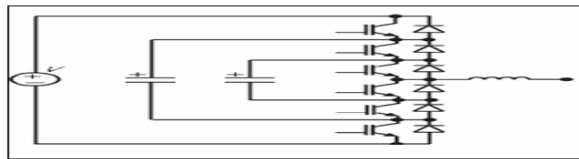

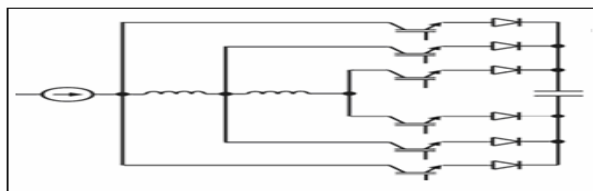Fig.4: The Flying Capacitor Converter- A Multilevel Voltage Converter

Fig.5: A Dual Derived from the Circuit in Fig. 4, the Flying Inductor Converter - A Multilevel Current Converter

As the following, the paper presents a new multilevel current converter.

III. THE PROPOSED MULTILEVEL CURRENT CONVERTER

A *The Proposed Topology*

The full-bridge topology is used to synthesize a three-level square-wave output current waveform. The full-bridge configuration of the single-phase current source converter is shown in Fig. 6.In a single-phase full-bridge configuration, four switches are needed. In full-bridge configuration, by

Fig.6: A Dual Derived from the Circuit in Fig. 4, the Flying Inductor Converter - A Multilevel Current Converter
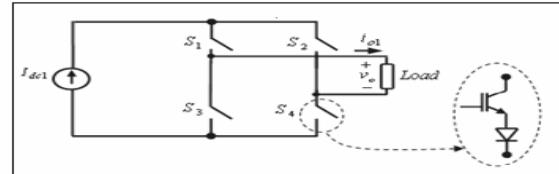
turning the switches $S1$ and $S4$ on and $S2$ and $S3$ of a current of Idc1 is available at output $io1$, while reversing the operation we get current of Idc1. To generate zero level of a full-bridge converter, the switches $S1$ and $S3$ are turned on while $S2$ and $S4$ are turned of or vice versa. The typical output waveform of full bridge of single-phase multilevel shown in Fig. 6, is shown in Fig. 7.

Fig.7: Typical Output Waveform of Three-LevelConfiguration
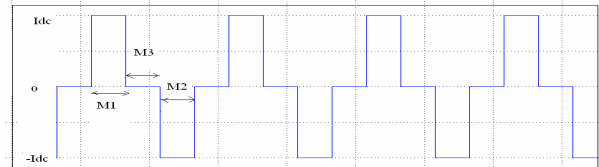
The three possible levels with respect to above discussion are shown in Table 1. Note that $S1$ and $S2$ should not be open at the same time, nor should $S3$ and $S4$. Otherwise, an open circuit would exist across the DC current source

Table 1: Output Current with Corresponding Conducting Switches

Modes	Conducting Switches	Output current (i_{o1})
1	S_1, S_4	$+I_{dc1}$
2	S_2, S_3	$-I_{dc1}$
1	S_1, S_3 or S_2, S_4	$+I_{dc1}$

Fig. 8 shows the equivalent circuits of the proposed topology at different modes. From Fig. 8, the instantaneous switches voltages of each module are given by:

$$Mode1 : \begin{cases} v_{S1} &= 0 \\ v_{S2} &= v_o(t) \\ v_{S3} &= v_o(t) \\ v_{S4} &= 0 \end{cases}$$

$$Mode2 : \begin{cases} v_{S1} &= -v_o(t) \\ v_{S2} &= 0 \\ v_{S3} &= 0 \\ v_{S4} &= -v_o(t) \end{cases}$$

$$Mode3 : \begin{cases} v_{S1} &= 0 \\ v_{S2} &= v_o(t) \\ v_{S3} &= 0 \\ v_{S4} &= -v_o(t) \end{cases}$$

Using parallel connections of many converters like the one shown in Fig. 6, we can synthesize multilevel current converter. The general function of this multilevel current

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source converter is to synthesize a desired current from several independent sources of DC currents. Fig. 9 shows a single-phase structure of a parallel converter with a separate DC current source. By different combinations of the four switches, $S1_¡S4$, each full-bridge converter can generate three different current outputs, +Idc1, -Idc1 and zero current. The AC outputs of each of the different level of full-bridge converters are connected in parallel such that the synthesized current waveform is the sum of the converter outputs.
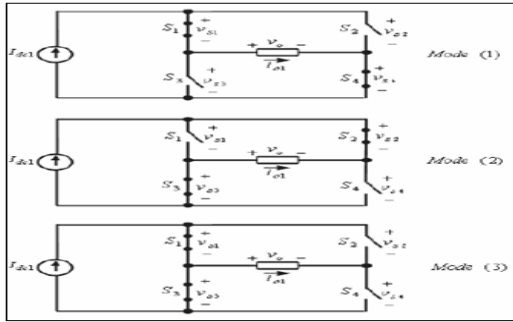

Fig.8: The Equivalent Circuits of the Proposed Topology at Different Modes

An output phase current waveform is obtained by summing the output currents of the converter bridges:

$$io(t) = io1(t) + io2(t) + \ldots + ioN(t)$$

where N is the number of parallel bridges.

1) *Method 1*

If all DC current sources in Fig. 9 are equal to Idc the converter is then known as symmetric multilevel current source converter. With having a number of full-bridge converter units, this technique results in an output current of the converter that is almost sinusoidal. The maximum output current of the N paralleled multilevel current source converter is $N *Idc$. In this topology, the number of levels of overall out-

put current (S) is given by:

$$S = 1 + 2N$$

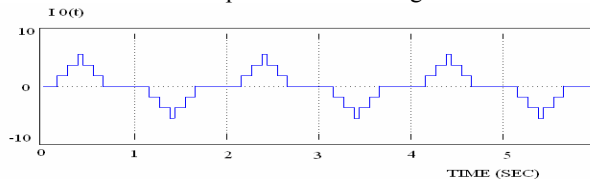The output of Fig 9 when using Method 1which yields an seven level current output as shown in Fig 10.

Fig.9: The 7-Level Converter Based on the First Proposed Method

The Total Harmonic Distortion {THD) level using this Method 1 is 14.61%

2) *Method 2*

In the proposed multilevel converter topology, the number of power devices required depends on the output

current level needed. However, increasing the number of power semiconductor switches increases the size of the converter circuit, cost and causes control complexity. To provide a large number of output levels without increasing the number of converters, asymmetric multilevel converters can be used. If at least one of the DC current sources is different from the other ones, the multilevel converter shown in Fig.9 can be called an asymmetric multilevel converter. Another method for choosing the levels of the DC current sources is in binary fashion, which gives an exponential increase in the number of the overall output levels. For N such paralleled converters, with DC current levels varying in binary fashion, the number of levels of overall output current (S) is calculated by:

$$S = (2^N+1) - 1$$

The maximum available output current is given by the following equation:

$$Maximum\ Output\ current = N (N + 1) / 2\ Idc$$

With only Three bridges (N=3), 15 levels of current are obtained: 7 levels of positive, 7 levels of negative values and zero. The method is also capable to producing odd and even levels. The output of Fig 9 when using Method 2 which yields and fifteen level current output as shown in Fig 11.
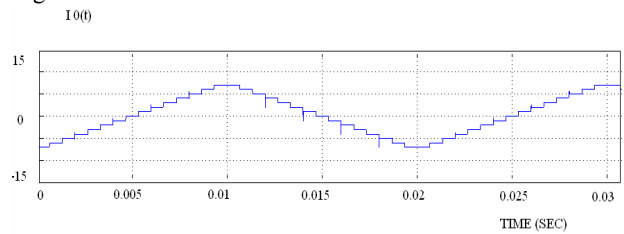

Fig.10: The 15-Level Converter Based on the Second Proposed Method

The Total Harmonic Distortion {THD) level using this Method 2 is 13.38%

3) *Method 3*

In this method, we choose the levels of DC current sources in the asymmetric multilevel current source as follows:

$$I_{dc,1} = I_{dc}$$
$$I_{dc,2} = 2I_{dc}$$
$$I_{dc,j} = I_{dc} + 2\sum_{k=1}^{j-1} I_{dc,k} \quad \forall j = 3, 4, \ldots, N$$

The number of levels of the overall output current waveform can be determined using the equation (9):

$$S = 1 + 2\sum_{k=1}^{N} Idc, k$$

and maximum available output current is given by:

$$Maximum\ Output\ current = \sum_{k=1}^{N} I_{dc,k}$$

With only Three bridges (N=3) and the per unit values Idc,1= 1, Idc,2=2, Idc,3=7, 21 levels of current are obtained: 10 levels of positive, 10 levels of negative values and zero. The method is also capable to producing odd and

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even levels. The output of Fig 9 when using Method 3 which yields and twenty one level current output as shown in Fig 12.
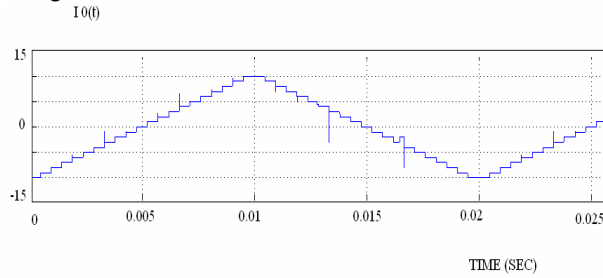

Fig.11: The 21-Level Converter Based on the Third Proposed Method

The Total Harmonic Distortion {THD) level using this Method 3 is 13.13%

4) *Method 4*

In this method the DC current sources levels are computed is as follows:

$$I_{dc,i} = 3^{i-1}I_{dc,1} \qquad i = 1, \ldots, N$$

For N such paralleled converters, the number of levels of overall output current (S) is calculated by:

S=3^N

and the maximum available output current is given by:

Maximum output current = $(3^N-1) I_{dc}/2$

With only Three bridges (N=3) and the per unit values $I_{dc,1}= 1$, $I_{dc,2}=3$, $I_{dc,3}=9$, 27 levels of current are obtained: 13 levels of positive, 13 levels of negative values and zero. The method is also capable to producing odd and even levels. The output of Fig 9 when using Method 4 which yields and twenty seven level current output as shown in Fig 13
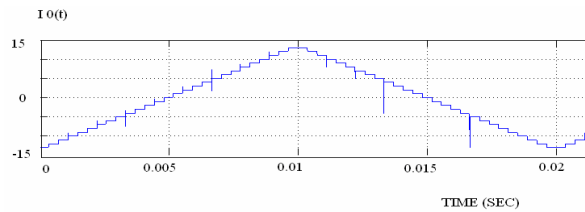

Fig.12: The 27-Level Converter Based on the Fourth Proposed Method

The Total Harmonic Distortion {THD) level using this Method 4 is 12.62%

Table 2: The Summarized Results of Different Methods

	Method 1	Method 2	Method 3	Method 4
No. of Switches	$4 \times N$	$4 \times N$	$4 \times N$	$4 \times N$
No. of DC sources	N	N	N	N
Maximum output current	$N \times I_{dc}$	$\frac{NN+1}{2}I_{dc}$	$\sum_{k=1}^{N} I_{dc,k}$	$\frac{3^N-1}{2}I_{dc}$
Levels of output current	$2 \times N + 1$	$2^{N+1} - 1$	$1 + 2\sum_{k=1}^{N} I_{dc,k}$	3^N

IV. CONCLUSION

In this paper, a new topology for multilevel current source converters has been presented. To determine the levels of DC current sources, four different methods have been suggested. The best method is chosen depending on THD values .The Method 4 with 12.62% THD will be the core of the current application such as STATCOM, shunt active filters, active power line conditioners etc .The switching techniques will also be verified using C language.

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HARMONIC ANALYSIS AND REDUCTION IN POWER ELECTRONIC CONVERTERS USING COMB FILTER

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Abstract:-The finite impulse response comb filters are used to overcome harmonic pollution. This paper proposes phasor and frequency estimation algorithm to avoid frequency deviation and to extract harmonics. The major components of this method are a frequency and phasor estimating algorithm, a finite-impulse-response comb filter, and a correction factor. The parallel implementation is simulated using MATLAB and the results are satisfactory.

Index Terms– Fast Fourier transform (FFT), finite-impulse-response (FIR) comb filter, harmonic analysis.

I.INTRODUCTION

There is a natural growth of harmonics in the electrical loads of a modern facility as it uses advanced electronics equipment such as communications, computers and servers. This equipment works on internal DC power supplies derived from the AC mains available. All these loads take non-linear currents from the supply and generate harmonics in the supply. The typical definition for a harmonic can be stated as follows "A sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency" [1].The process is shown in Fig.1. A "pure" power is defined as the one without any harmonics. But such clean waveforms typically only exist in a laboratory. Harmonics have been around for a long time and will continue to do so. Electrical generators try to produce electric power where the voltage waveform has only one frequency associated with it, (i.e.) the fundamental frequency. In India, this frequency is usually 50 Hz. This means that fifty times a second, the voltage waveform increases to a maximum positive value, then decreases to zero, further decreasing to a maximum negative value, and then back to zero. The rate at which these changes occur is as a trigonometric function of a sine wave. This harmonic

pollution does not mean that the equipment will not run properly. It depends on the stiffness of the power distribution system and the susceptibility of the equipment. The main sources of harmonic current are the phase angle controlled rectifiers and inverters. These are often called static power converters. Fluorescent lights can be the source of harmonics, as the ballasts are non-linear Inductors. [7] The third harmonic is predominating in this case. In adjustable speed drives, the speed variations give rise to harmonics. The speed variation which arises owing to inverter action contributes to harmonics in the windings of the machine. In addition, many ill effects (i.e., worse power quality for end users, more loss in transmission lines, overheating of machines, and malfunction of relays and breakers) are due to harmonic pollution. It goes without saying that harmonic analysis is a very important subject in power systems.

There are many algorithms developed to minimize the effect of harmonics. However available algorithm suffers from specific restriction such aliasing, leakage and picket fence effect. The new method proposed to overcome above effects has an accurate frequency and phasor estimation algorithm, an FIR comb filter to filter out specific signal components and a correction factors to eliminate the side effects of FIR comb filter. The evolved process of harmonic analysis is easy to implement and not affected by frequency deviation. [1]The proposed FIR comb filter still suffered from some side effects and to eliminate this window correction factors are used. The harmonic analysis involves two correction windows. Analysis involves a window correction for fundamental frequency, and harmonic content computation. In comb filters, pass-bands are adjusted to a discrete spectral structure of harmonic signals. It does not only enhance the periodicity of harmonics, but also reduce an additive noise by averaging over every point spacing at a signal interval. The performance of the comb filter is enhanced through smoothing hamming window. The parallel implementation is simulated using MATLAB and the results are satisfactory.
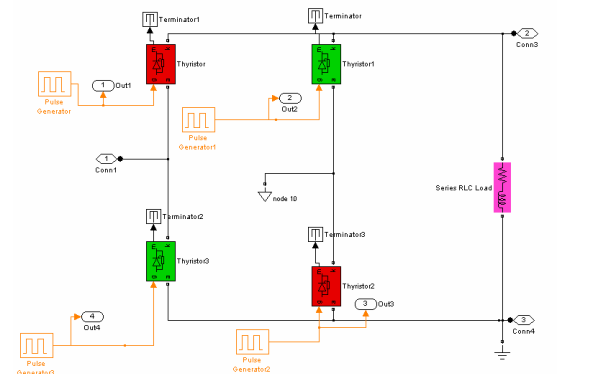

Fig1: Non-Linear Load

II. FREQUENCY AND PHASOR ESTIMATION ALGORITHM

This section presents the algorithm for estimating frequency and phasor from a power signal. Suppose the signal $x(t)$ is assumed to be of the form

$$x(t) = X \cos(2\pi f t + \phi) \tag{1}$$

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Since we know that

$$\cos\theta = \frac{e^{j\theta} + e^{-j\theta}}{2}.$$

Then, $x(k)$ can be expressed as

$$x(k) = \frac{X}{2}e^{j\phi}e^{j2\pi fk\Delta t} + \frac{X}{2}e^{-j\phi}e^{-j2\pi fk\Delta t}.$$

For further explorations, we use the following definitions:

$$a = e^{j2\pi f\Delta t}$$
$$A = \frac{X}{2}e^{j\phi}$$
$$z = \mathrm{Re}(a). \tag{2}$$

$$x(k) = Aa^k + A^*a^{-k}$$
$$\times a \qquad \times a^{-1}$$
$$x(k+1) = Aa^{k+1} + A^*a^{-k-1}$$

After some algebraic manipulations, we find

$$z = \frac{x(k) + x(k+2)}{2x(k+1)}. \tag{3}$$

The parameters of signal are computed as

$$f = \frac{\cos^{-1}(z)}{2\pi\Delta t}$$
$$A = \frac{x(k+1)a - x(k)}{(a^2 - 1)} \tag{4}$$

from above equation we prove that algorithm is undisturbed by frequency deviation,

$$x(k) - 2zx(k+1) + x(k+2) = 0. \tag{5}$$

III. DESIGN OF FIR COMB FILTER

As proposed in section II we will design comb filter and continue to develop with advance features. Consider the power equation,

$$x(t) = \sum_{i=1}^{m} X_i \cos(2\pi f_i t + \phi_i). \tag{6}$$

The network that simulates a single delay is called the FIR comb filter. [3] The input signal is delayed by a given time duration. [5]The effect will be audible only when the processed signal is combined (added) to the input signal. The process is shown in Fig.2.The network that simulates a single delay is called the FIR comb filter. The input signal is delayed by a given time duration.
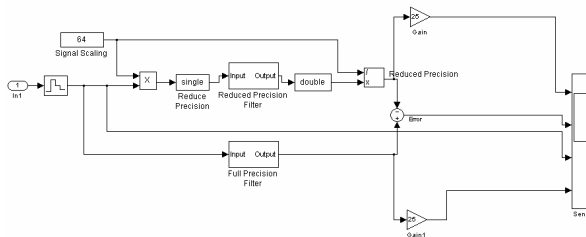

Fig 2: Comb-filter Circuit

processed signal is combined (added) to the input signal, which acts here as a reference [4]. The transfer function of such a filter shows a series of spikes and it looks like a

comb. The comb filter is designed in simulink as shown Fig2.
Some algebraic manipulations

$$\sum_{n=0}^{2m} C(n)x(k+n) = 0$$
$$C = \{\{1, -2z_1, 1\} * \{1, -2z_2, 1\} * \ldots * \{1, -2z_m, 1\}\} \tag{7}$$

We can arbitrarily filter the harmonic components in the signal (7), if we obtain the correct values of windows correction factor.

IV. WINDOW CORRECTION FACTOR

Although the proposed FIR comb filter can filter out the desired frequency components from the signal, it still has some side effects. It changes the amplitude and phase of the remaining components of the signal. To eliminate the side effect of the proposed filter, we provide window correction factor (WCF).

$$\tilde{x}(k) = \sum_{n=0}^{M-1} W(n)x(k+n). \tag{8}$$

The equation, (8) is rearranged as

$$\tilde{x}(k) = Aa^k \sum_{n=0}^{M-1} W(n)a^n + A^*a^{-k} \sum_{n=0}^{M-1} W(n)a^n \tag{9}$$

According to the rearranged equation given above, we can compute the parameters of the signal by the following equations

$$f = \frac{\cos^{-1}(z)}{2\pi\Delta t}$$
$$A = \frac{\tilde{x}(k+1)a - \tilde{x}(k)}{(a^2 - 1) \times WCF}. \tag{10}$$

Hence the proposed window correction for developed comb filter is
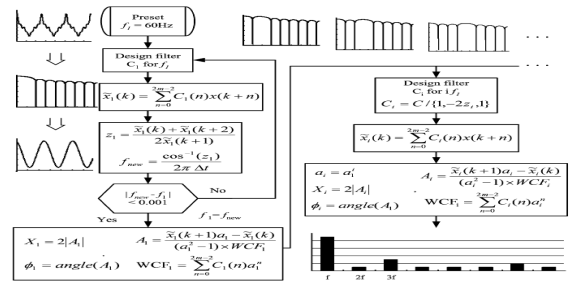
$$WCF = \sum_{n=0}^{M-1} W(n)a^n. \tag{11}$$

Fig3:HarmonicAnalysis

Therefore, knowing how to estimate fundamental frequency is the key point.[1] The procedure of our harmonic analysis is discussed: First, assume fundamental frequency is 60 Hz, and then use (7) to create a comb filter, which filters out every harmonic. After filtering, we find the new fundamental frequency.

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Then, we redesign the comb filter for the new fundamental frequency and repeat these steps until the fundamental frequency converges. Next, produce the combs filter to filter out every harmonic except the ith harmonic and compute the phasor of the ith harmonic. The process is shown in Fig3.

$$C_1 = \{\{1, -2z_2, 1\} * \ldots * \{1, -2z_m, 1\}\}. \tag{12}$$

To reduce computation time, we utilize deconvolution to Get C_i. After getting f_1, we also get C_1 at the same time. Then we get C by convolution,

$$C = C_1 * \{1, -2z_1, 1\}. \tag{13}$$

Although this method is not as fast as FFT, it is suitable for both online and offline applications.

Next, we get C_i by deconvolution (/)

$$C_i = \frac{C}{\{1, -2z_i, 1\}}.$$

We can get the $\tilde{x}_i(k)$ by the following equation:

$$\tilde{x}_i(k) = \sum_{n=0}^{2m-2} C_i(n)x(k+n).$$

Next, we only compute the phasor of each harmonic by

$$A_i = \frac{\tilde{x}_i(k+1)a_i - \tilde{x}_i(k)}{(a_i^2 - 1) \times WCF_i}. \tag{14}$$

Additionally, it is obvious that this method is more efficient in parallel than in serial computation. Since the accuracy of the fundamental frequency is the key point, we provide the LSE method to enhance the performance.

Then, z_1 can be obtained by

$$z_1 = (A'A)^{-1}A'B \tag{15}$$
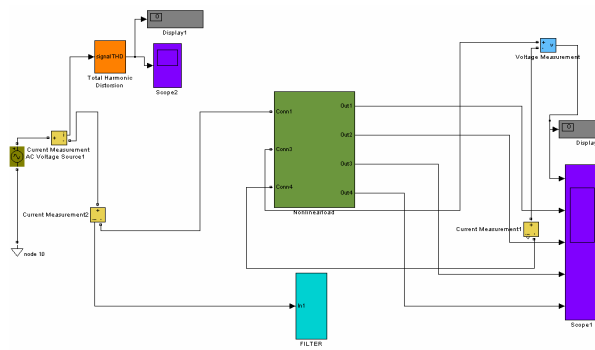
VI. HARMONIC REDUCTION MODEL

Fig.4. System Model

Above is harmonic reduction model developed using simulink in MATLAB. The model includes a comb filter which replaces the FFT blocks. With any simulink system, you can start the simulation by selecting "Start" from the "Simulation"menu.Once you have started; you can always terminate a simulation by selecting "stop" from the same menu.[5] Some simulations may reach their pre-set stop time and terminate automatically. You can set the simulation stop time, step size, and other simulation parameters by editing the "parameters" dialog box under the "Simulation" menu. You can select and move any block on a Simulink block diagram by clicking once and dragging. You can generally open a Simulink block by double-clicking on it. For example, demo systems will often have a box marked with a question mark (?).By double –clicking on this block, you can reveal an explanatory note contained inside it.

When you have finished with a Simulink system, you can close it by selecting "Close" from the "File" menu. Many ill-effects such as leakage effect, picket fence effect and aliasing effect are reduced using the above model. The sinusoidal input waveform x(t) applied to circuit yielding a third harmonic is filtered using comb filter and waveforms are shown below,
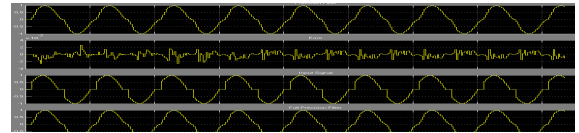
Fig.5. Simulation Waveforms

The waveform block includes input waveform, error signal, and filter outputs shown.

Total harmonics distortion (THD):

The total harmonic distortion, which is a measure of closeness in shape between a waveform and its fundamental component, is defined as [6],

$$THD = \frac{\sqrt{\sum_{k=2}^{\infty}(I_h)^2}}{I_1} \tag{16}$$

VII. SIMULATION RESULTS

Here, we present two simulation results comparing the method we proposed with the FFT. For convenience, the method we proposed is called a combined method (CM). In the first case, the fundamental frequency is 59.5 Hz, and the harmonic contents are shown in Table I. We add 0.5% white noise into the signal. The sampling frequency is 60*128=7680 because of the restriction of FFT. The computation results are also shown in Table I.

In this case, we use Matlab built-in function "FFT" to compute the results of FFT, and the window size of FFT is 128 samples. [2]There are two different window sizes of CM: one is for computing the fundamental frequency and another is for computing harmonic contents. The window size of the computing fundamental frequency is 265 samples (127 for the comb filter, 128 for DFT and ten for LSE). The window size of computing harmonic

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contents is changing with the order i of the harmonic (127 for comb filter, round (128/i) for DFT). From Table I, we can compare the performances of both methods. CM is better than FFT; this is because CM is not affected by frequency deviation. Moreover, if we want the performance of CM to be much better than FFT, we can add smoothing window like Hamming or Blackman window to filter out noise. In addition, the side effect of the smoothing window also can be eliminated by WCF. In the second case, we discuss the aliasing effect. Assume the fundamental frequency is 60.5 Hz and the sampling frequency is 60*128=7680. The harmonic contents and simulation results are shown in Table II. Since the fundamental frequency is 60.5 Hz, the frequency of the eighth harmonic is 484 Hz, which is above half of the sampling frequency. According to the Nyquist sampling theorem, this part of the signal cannot be recovered from samples. However, the influences of these harmonics still exist. The computation results of FFT are affected, which is called the aliasing effect. From Table II, we can find that CM gets the correct harmonic contents under no-noise condition, but it does not mean CM is out of the Nyquist sampling theorem. Table I&II are for reference. Table III is FFT analysis output is shown below

$$z_8 = \cos(2\pi 484\Delta t) = \cos(2\pi 476\Delta t). \quad (17)$$

TABLE I
SIMULATION SIGNAL AND RESULTS (F 1 = 59.5 Hz WITH 0.5% NOISE)

H	Amp.	FFT	CM	H	Amp.	FFT	CM
1	1	0.9931	0.9997	33	0	0.0031	0.0003
2	0.07	0.0737	0.0702	34	0	0.0034	0.0004
3	0.05	0.0526	0.0503	35	0	0.0033	0.0002
4	0	0.0016	0.0005	36	0	0.0032	0.0003
5	0.04	0.0411	0.0399	37	0	0.0033	0.0001

TABLE II
SIMULATION SIGNAL AND RESULTS (F 1 = 60.5 Hz)

f_1=60.5Hz		No Noise		0.5% Noise	
H	Amp.	FFT	CM	FFT	CM
1	1	1.0071	1.0000	1.0061	0.9998
2	0.07	0.0668	0.0700	0.0673	0.0704
3	0.05	0.0481	0.0500	0.0481	0.0500
4	0	0.0009	0.0000	0.0011	0.0006
5	0.04	0.0388	0.0400	0.0384	0.0402

Table III. FFT analysis comparison output

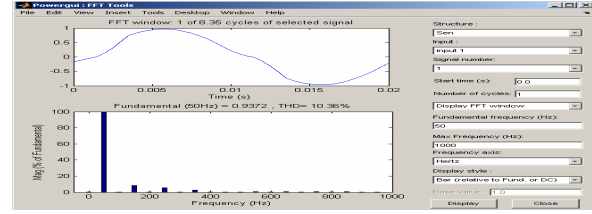| Filter Coefficients	THD	Fundamental 50 Hz	h3	h5	h7
-15	10.36	0.9372	8.23	5.5	2.5
-25	10.05%	0.9397	8.3	4.7	1.7
-35	10.68%	0.9423	8.5	4.0	1.1
-40	11.30%	0.9437	8.7	3.7	0.8
-55	14.02%	0.9479	9.5	3.3	1.3

Fig6. FFT comparison window

The signal components over half of the sampling frequency are reflected back and we cannot tell what these are. However, using the method we proposed will allow us to avoid an aliasing effect when the fundamental frequency is not exactly at 60 Hz. In this case, we add a Blackman window to enhance the preference while we add the noise into the signal.

VIII. CONCLUSION

In this paper, we provide a new measurement method for harmonic analysis. This method is easy to implement and very flexible. Users can change the window (smoothing window, DFT, or LSE) and window size to get better performance. Meanwhile, it does not seriously suffer the drawbacks like leakage effect, picket-fence effect, and sampling frequency have to be 2n multiple of the fundamental frequency. It is also more able to deal with the aliasing effect. This method really meets the need of offline applications and online applications. The parallel computation implemented allows meeting the needs of online applications. Implementation in case of parallel computation follows hamming window technique. Furthermore, if we can implement this method Blackman window to enhanced output for preferential additive noise into the signal. The parallel implementation is simulated using MATLAB and the results are satisfactory.

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DESIGN AND IMPLEMENTATION OF FLYING CAPACITOR MULTILVEL INVERTER

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Abstract - **Recent Research in Flying Capacitor Multilevel Inverter has shown that the number of voltage levels can be extended by changing the ratio of the capacitor voltages. For the three-cell FCMI, four levels of operation are expected if the traditional ratio of the capacitor voltages is 1:2:3. According to the previous research, the eight level case is referred to as maximally distended (or full binary combination schema) since it utilizes all possible transistor switching states. However, this case does not have enough per-phase redundancy to ensure capacitor voltage balancing under all phases is used along with per-phase redundancy to improve capacitor voltage balancing.**

1.INTRODUCTION

In Recent years, there has been considerable development in multilevel power conversion, especially for application to medium-voltage drives. The flying capacitor multilevel inverter topology is relatively new compared to the diode-clamped and series H-bridge inverters. FCMI have some some distinct advantages over the diode clamped topology including the absence of clemping diodes and the ability to regulate the flying capacitor voltage is greater than three. Unlike the series H-bridge inverter, isolated voltage sources are not required.

The reason that capacitor voltage balancing is not an issue in the FCMI is that there are several conduction paths within each phase that can produce the same voltage levels. This per-phase redundancy can be used to choose the path with the best balancing characteristics at any point in time. It is possible to change the ratio of capacitor voltages and sacrifice this redundancy in order to improve the power quality by increasing the number of voltage level. The loss in the capacitor voltage balancing control is compensated by using joint redundancy involving all phases.

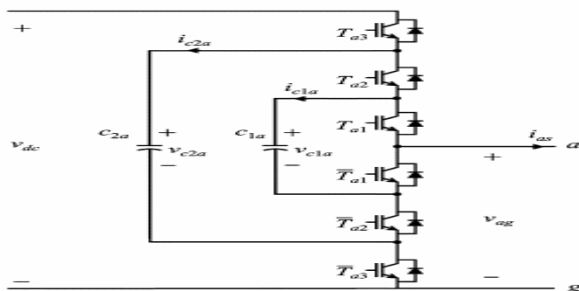## II FLYING CAPACITOR MULTILEVEL INVERTER

Fig. 1. Three-cell FCMI topology (a-phase)

Figure.1 shows three phase of the three-cell FCMI topology. For this inverter, each capacitor is changed to a different voltage and by changing the transistor switching states, the capacitor and V source are connected in different ways and produce various line-to-ground output voltages.

From the topology KVL and KCL equations can be expressed as

For the a-phase,

$$V_{ag}=(T_{a3})V_{dc}+(T_{a2}-T_{a3})V_{c2a}+(T_{a1}-T_{a2})V_{c1a}$$
$$i_{c1a}=(T_{a2}-T_{a1})i_{as}$$
$$i_{c2a}=(T_{a3}-T_{a2})i_{as}$$

Based on these fundamental equations the line-to-ground voltage and capacitor currents can be determined for all combinations of transistor signals as shown in Table I.

Table 1.Three-cel fcmi output voltages for a-phase

Ta1	Ta2	Ta3	Vag	ic1a	ic2a
0	0	0	0	0	0
0	0	1	Vdc-Vc2a	0	ias
0	1	0	Vc2a-Vc1a	ias	-ias
0	1	1	Vdc-Vc1a	ias	0
1	0	0	Vc1a	-ias	0
1	0	1	Vdc-Vc2a+Vc1a	-ias	ias
1	1	0	Vc2a	0	-ias
1	1	1	Vdc	0	0

From Table I, it can be seen that the line-to-ground voltage depends on the values of voltages for three phases.By changing the ratio of these voltages, it is possible to alter the number of voltage levels that the inverter can produce.This concepts was previously introduced for the FCMI topology as well as combinational "hybrid" topologies.As with other inverter topologies, the three- phase implementation involves three branches of the structure shown in figure.1 connected in parallel on the V side and typically connected to a Wye-configured load on the ac side.

The line-to-ground voltage can be expressed by

$$\begin{vmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{vmatrix} = \begin{vmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{vmatrix} \begin{vmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{vmatrix}$$

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The load's line-to-neutral voltages can also be determined directly from the line-to-ground voltages using

$$\begin{vmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{vmatrix} = \frac{1}{3} \begin{vmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{vmatrix} \begin{vmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{vmatrix}$$

III MULTILEVEL VOLTAGE-SOURCE MODULATION

Voltage-Source Modulation can be accomplished in a multi-level inverter system using the sine-triangle method.

A. DUTY CYCLES

The basics of the modulation method introduced herein is to define duty cycles for each phase, which will be based on commanded line-to-ground voltages. However, a supervisory control will typically output commanded phase voltages, which may be expressed,

$$V_{as} = \sqrt{2} \, Vs \cos(\theta_c)$$
$$V_{bs} = \sqrt{2} \, Vs \cos(\theta_c - 2\pi/3)$$
$$V_{cs} = \sqrt{2} \, Vs \cos(\theta_c + 2\pi/3)$$

Where Vs is the commanded magnitude and 0c is the electrical angle. Since the determinate of the matrix is zero, there are an infinite number of commanded line-to-ground voltage sets that yield the commanded phase voltages.

In the three phase system the zero-sequence components of V_{ag}, V_{bg} and V_{cg} are dc offsets and triplen harmonics of the fundamental frequency. The quantity and amplitude of triplen harmonics added to the commanded line-to-ground voltages may be selected in order to maximize converter output voltages reduce switching losses,or improve harmonic distortion. Herein, a third harmonic will be added in order to maximize the output voltaghe resulting in commanded line-to-ground voltage of

$$V_{ag}=V_{dc}/2 \, [1+m\cos(\theta_c)-m/6 \cos(3\theta_c)]$$
$$V_{bg}=V_{dc}/2 \, [1+m\cos(\theta_c-2\pi/3)-m/6 \cos(3\theta_c)]$$
$$V_{cg}=V_{dc}/2 \, [1+m\cos(\theta_c+2\pi/3)-m/6 \cos(3\theta_c)]$$

Where m is the modulation index, which has a range from 0 to 1.15, θ is the electrical angle which could be related to frequency.

$$\theta_c = \int 2\pi f * dt$$
$$V_{as} = mVdc/2 \cos(\theta_c)$$
$$V_{bs} = mVdc/2 \cos(\theta_c-2\pi/3)$$
$$V_{cs} = mVdc/2 \cos(\theta_c+2\pi/3)$$

The three duty cycles are compared to a set of triangle waveforms to produce commanded switching states for each phase.

$$d_a = \frac{1}{2}[1+m\cos(\theta_c)-m/6 \cos(3\theta_c)]$$
$$d_b = \frac{1}{2}[1+m\cos(\theta_c-2\pi/3)-m/6 \cos(3\theta_c)]$$
$$d_c = \frac{1}{2}[1+m\cos(\theta_c+2\pi/3)-m/6 \cos(3\theta_c)]$$

IV CAPACITOR VOLTAGE BALANCING METHOD

In order to obtain reasonable distinct multilevel output voltage results, the voltages on all six capacitors must be maintained at constant values. However, the load currents have different effects on the charging and discharging of the capacitor and will tend to unbalance the capacitor voltages. In this case, the redundant switching states becomes the key components for balancing the capacitor voltages. Since there are several conduction paths within each phase which can produce the same voltage levels while having different capacitor charging characteristics, per-phase redundancy can be used to choose the path with the best balancing performance. However, according to the table II, as the number of achieved voltage levels increases, the number of available per-phase redundant states decreases.In this case, incrementing or decrementing the switching states of all three phases Sa*,Sb* and Sc* can also be used to balance capacitor voltages since this results in change in the zero-sequence line-to-ground voltage, which doesnot have affects the load voltages. The concepts behind this joint-phase redundant state selection (JRSS) method is that the line-to-ground voltages (V_{ag}, V_{bg}, V_{cg}) of all phases may be changed simultaneously without affecting the load voltages since the terms that are common in all phases will cancel when looking at the line-to-neutral voltages(V_{as},V_{bs},V_{cs}) or line-to-voltages(V_{ab},V_{bc},V_{ca}).Because of the corresponding load voltages are the same for each of these cases,the selection of the appropriate joint state can improve the capacitor balancing situation.

A. On-Line Joint- Phase RSS.

For any desired three phase switching states Sa*,Sb* and Sc* all available redundant states, which can produce the same load voltages are evaluated and compared. These states include joint-phase redundant states and per-phase redundant states.The number of joint-phase redundant states N_{JRSS} can be expressed by

$$N_{JRSS} = n-[MAX(S_a*,S_b*,S_c*)-MIN(S_a*,S_b*,S_c*)]$$

Where n is the number of voltage levels.

The first joint-phase redundant states to be considered can be obtained from,

$$S_{Ja}* = S_a* -MIN(S_a*,S_b*,S_c*)$$
$$S_{Jb}* = S_b* -MIN(S_a*,S_b*,S_c*)$$
$$S_{Jc}* = S_c* -MIN(S_a*,S_b*,S_c*)$$

The number of per-phase redundant states N_{PRSSx} is related to ratio of the capacitor voltages.

Table II
Number of per-phase RSS in a five-level inverter(1:2:4)

S_a*	N_{PRSSa}	$T_{a1} \, T_{a2} \, T_{a3}$
0	1	(0 0 0)
1	2	(0 1 0),(1 0 0)
2	2	(0 0 1),(1 1 0)
3	2	(0 1 1),(1 0 1)
4	1	(1 1 1)

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The predicated capacitor voltage change during one window time can be calculated as

$\nabla Vcyx = i_{cyx}.t_{window}/C_y.$
x is the phase (a, b or c),
y is the capacitor(1or2),
t_{window} is the time for one window.
The predicated capacitor voltages for next window are determined as

$$\overline{V_{cyx}} = V_{cyx} + \Delta V_{cyx}$$

The square error for each potential state is evaluated by comparison to ideal voltage as

$$\varepsilon = \sqrt{\sum_{x=a}^{c} \sum_{y=1}^{2} (V_{cyx}{}^* - \overline{V_{cyx}})^2}$$

This algorithm minimizes the error between capacitor voltages and their ideal values, and thus gives the best possible choice to improve the overall balancing of voltages of the six capacitors.

V PROPOSED INVERTER PERFORMANCE

In this section, advantages and limitations of the proposed scheme are evaluated using detailed computer simulation.

A. switching losses

The traditional FCMI employs three cells to produce four output voltage levels. With more voltage levels, the system total harmonic distortion(THD) and output filter size can be greatly reduced, which results in
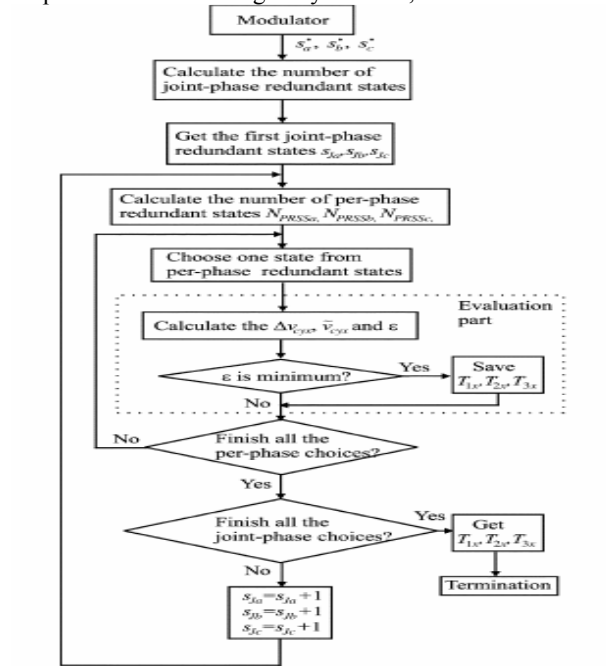

Fig 3 Flowchart of online joint phase RSS method

more compact system design and lower costs. The number of levels is extended by changing the ratio of voltage which means that the device voltage pairs will have different voltage ratings, the proposed control uses jPRSS instead as well as per-phase RSS. To compare the switching losses for the proposed control to the traditional method five-level inverter system was used in the base simulation. The inverter was simulated using 1200v,50A,IGBT/diode dual modules,
Properties:

> Vce,sat = 3.3v
> Vd,sat = 3v
> Err = 3.3mJ
> Eon = 6.94mJ
> Eoff = 8.72mJ
> For 600v ,50A ,IGBT/diode dual modules,

Properties:

> Vce,sat = 2.8v
> Vd,sat = 3v
> Err = 0.429mJ
> Eon = 1.36mJ
> Eoff = 3.14mJ
> dc output voltage = 1200v
> pwm clock frequency = 5kHz

An R-L load was placed on the inverter operating with 40KVA, 32KW and 60Hz. It can be seen that a small amount of switching losses are sacrificed in order to balance the flying capacitors. However , due to the absence of one pair of transistor, the 309w. Over all the efficiency of proposed method method is slightly higher that the efficiency of the traditional method.

B. Capacitor Size

The total voltage was set to 750µF. By selecting standard sizes, this method uses, 1000µF 150V, 470µF 300V, and 330µF 450V capacitors per phase in order to ensure each capacitor has a voltage ripple of less than 2%.The proposed method requires a 1000µF 150V and 1500µF 300V capacitor in each phase to ensure the same voltage ripple.

VI. COMPUTER SIMULATION RESULTS

A. Steady-State Study

A computer simulation has been created to verify the proposed method. In this simulation, a three-phase induction motor with parameters showed in Table IV is connected to the inverter as a load. The dc voltage is set to 200 V. The capacitance values of the capacitors are 3300 µF and the commanded fundamental frequency is 60 Hz. For the first study, the ratio of capacitor voltages is set to 1:2:4 to obtain five level steady-state operation. The modulation index is near maximum value 1.14. The

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motor runs with commanded rotor speed of 186.6 rad/s and a load torque of 8Nm . Fig. 5 shows the capacitor voltage deviations, capacitor voltages Vc1a , Vc2a, a-phase line-to-ground voltage V_{ag} , line-to-line voltage V_{ab}, and motor current ias , As can be seen, capacitor voltages are maintained at a fairly constant level with Vc1a =50 V and Vc2a=100 V, which satisfies the ratio requirement. The capacitor voltage deviations jump around 0 V, the voltage ripple for each capacitor is around 2%. The capacitor voltage balance can also be seen in that the line-to-ground voltage has five distinct levels. The effect of JRSS is seen in the bus clamping of the line-to-ground voltage to the highest and lowest levels. However, since the line-to-ground voltages of the other phases are also changed at the same time, the line-to-line voltages are not affected. From the line-to-line voltages, the effective nine level waveform can be seen (four positive levels, four negative levels, and one zero-level). Also, the resulting sinusoidal current lags the output voltage by 41° making the power factor 0.75. The last traces in Fig. 5 are the common-mode (line to dc link midpoint) voltages for the extend FCMI and a traditional FCMI operating under the same conditions. By comparison, it can be seen that the extended FCMI has the same common-mode voltage level steps, but at a higher frequency due to JRSS capacitor voltage balancing. This is a drawback of the proposed method since higher frequency common-mode voltages could lead to higher frequency common-mode currents.
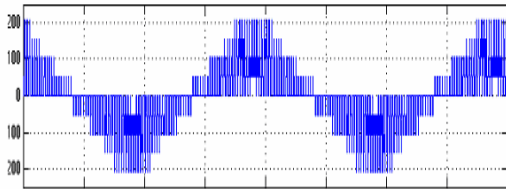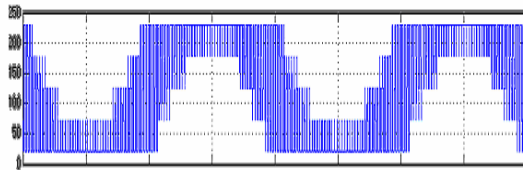

Fig.5. Line-line voltage Vab

Fig.6.Line to ground voltage Vag

VII. CONCLUSION

This paper has presented the extending operation of a three-cell flying capacitor multilevel inverter. Redundant switching states, vital to capacitor voltage balancing, are sacrificed to achieve a higher number of output voltage levels. Two joint-phase redundant state selection algorithms were proposed to keep the capacitor voltages constant. Simulation results demonstrate the effectiveness of each algorithm. One algorithm was validated inverter which typically operates in the four-level mode was extended to five-level operation. It was

also demonstrated through simulation that the three-cell inverter can achieve eight-level operation for applications involving reactive power compensation.

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ANALYSIS OF CHOPPER FED DC DRIVE SYSTEM WITH PULSE WIDTH MODULATION CONTROLS

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Abstract - **In this paper, the chopper fed dc drive system analyzed with different pulse width modulation (PWM) techniques namely Uniform PWM (UPWM), Sinusoidal PWM (SPWM) and Trapezoidal PWM (TPWM) techniques. In drives requiring a wide range of speed control, armature voltage control is combined with field control. Armature voltage control has the advantage of retaining the maximum torque capability of motor at all speeds. The field control is used only for getting speeds which cannot be obtained by armature control. Thus by combining the armature and field control method, speeds above and below base speeds can be obtained. The armature voltage control is done by combined operation of the phase controlled rectifier and class C chopper, the field flux control is done using class A chopper. The drive system is operated in forward motoring mode and the performance parameters of the system are analyzed. The modulation index of the different PWM is varied and the various performance parameters are obtained. The performance parameter analyzed here are Input Power factor (PF), Harmonic Factor of the line current (HF), Distortion Factor of the input current (DTF), Displacement Factor (DPF), load current Ripple Factor (RF), and speed (N). The chopper fed dc drive system is analyzed and best control technique is chosen from the various PWM control techniques. The above proposed circuit is simulated by using MATLAB/SIMULINK and program for best control technique is written by using C language.**

I. INTRODUCTION

Today's industries are increasingly demanding process automation in all sectors. Automation results into better quality, increase production and reduced cost. The variable speed drives, which steplessly control speed of a.c-d.c motors are indispensable controlling elements in automation systems. Depending on the application, some of them are fixed speed and some of them variable speed. Variable speed drives, till a couple of decades back, had various limitations, such as poor efficiencies, larger space, lower speed etc. However, the advent of power electronics transformed the scene completely and today we have variable drive systems which are not only smaller in size but also very efficient, highly reliable and meeting all the

stringent demands of the various industries of modern era. Direct current dc motors have been used in variable speed drives for a long time. The versatile control characteristics of dc motors have contributed to their extensive use in industry. dc motors can provide high starting torques which is basic requirement for traction drives. Control

over a large speed range, both below and above the rated speed can be easily achieved.

These methods of speed control are simpler and less expensive than those of alternating current motors.

Control of a dc motor's speed by a chopper is required where the supply is dc (as from a battery) or an ac voltage that has already been rectified to a dc voltage. The most important applications of choppers are in the speed control of dc motors used in industrial or traction drives. Choppers are used for the control of dc motors because of a number of advantages, such as high efficiency, flexibility in control, light weight, small size, quick response and regeneration down to very low speeds. Chopper controlled dc drives have also applications in servos on battery operated vehicles such as forklift truck, trolleys and so on. The choppers offer a number of advantages over controlled rectifiers for a dc motor control in open loop and closed loop configurations. Because of the higher frequency of the output voltage-ripple, the ripple in the motor armature current is less and the region of discontinuous conduction in the speed-torque plane is smaller. A reduction in the armature current ripple reduces the machine losses and its derating. A reduction or elimination of discontinuous conduction region improves speed regulation and transient response of a drive.

In this paper, the performance parameter of the chopper fed dc drive system with three PWM controls are analyzed and best PWM control are chosen from three PWM controls.

II. MODULATION TECHNIQUES FOR CHOPPER

For chopper various number of PWM technique are used, In this paper three PWM controls are used that are A) Uniform PWM, B) Sinusoidal PWM, C) Trapezoidal PWM.

A. Uniform PWM Technique

The principle of this control strategy is shown in Fig.1. The carrier triangular wave has a fixed maximum amplitude V_c and varies at a frequency fc defined as the chopping frequency. This signal should be synchronized with any of the line voltages in order to obtain the required symmetry of the output waveforms. The carrier wave is compared with a variable time-independent dc control voltage V_m to generate the drive signal of the

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chopping transistor [1]. The control signal varies in the range ($0 \leq V_m \leq V_c$), with the ratio of V_m to V_c is defined as the modulation index α (i.e., α= V_m / V_c). Since the modulation is uniform, the modulation index varies from zero up to maximum amplitude of one (i.e., $0 \leq α \leq 1$).
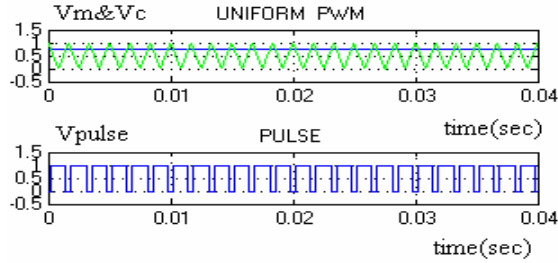

Fig. 1. Uniform pulse width modulation technique

B. Sinusoidal PWM Technique

The principle of this control strategy is shown in Fig.2.The widths of the drive signals depend upon the ratio of V_m, the peak amplitude of the modulating wave, and V_c, the peak amplitude of the carrier wave. This ratio is defined as the modulation index α, given as α= V_m / V_c. Control of the average output voltage is practically accomplished by the variation of α, which, in turn, can be achieved by the variation of V_m. It should be pointed out that sinusoidal pulse width modulation is maintained regular if α varies in the range $0 \leq α \leq 1$. If the system is allowed to operate with α>1, the modulation process ceases to be sinusoidal [4]. However, for α=1 (the limit for regular SPWM), the output average voltage is substantially lower than its possible maximum value. This paper reports regular sinusoidal PWM such that the modulation index is allowed to vary within the limit $0 \leq α \leq 1$ only.
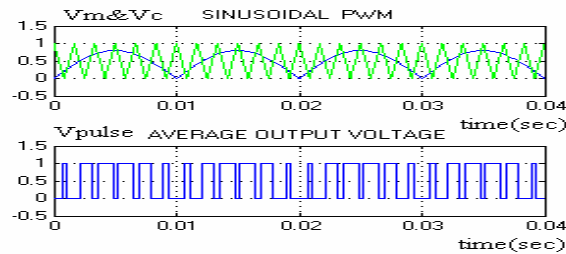

Fig. 2 .Sinusoidal pulse width modulation technique

C. Trapezoidal PWM Technique

The principle of this control strategy is shown in Fig. 3. The gating signals are generated by comparing a triangular carrier V_c wave with a modulating trapezoidal V_m wave [3]. The trapezoidal wave can be obtained from a triangular wave by limiting its magnitude to ± V_m, which is related to the peak value V_m(max) by V_m = β V_m(max). Where β is called triangular factor, because the waveform become a triangular wave when β=1. The modulation index α= V_m / V_c = β V_m(max)/V_c for $0 \leq α \leq 1$. the angle of flat portion of the trapezoidal wave is given

by 2ό=(1- β)π, for fixed value of V_m(max) and V_c, α that varies with the output voltage can be varied by changing the triangular factor β.
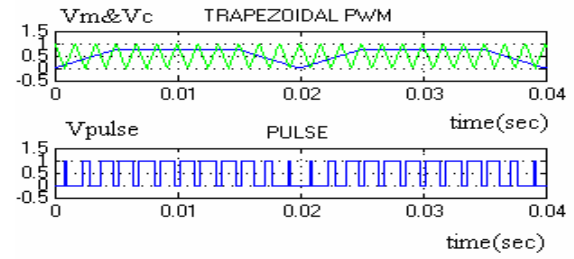

Fig. 3. Trapezoidal pulse width modulation technique

III. SYSTEM DESCRIPTION AND PRINCIPLE OF OPERATION

A. System Description

The power circuit configuration of the chopper fed dc drive system under consideration is shown in Fig.4. The circuit comprises two stages in armature side and single stage in field side. In the armature side the first stage, a six-pulse controlled bridge rectifier is employed to unify the direction of the load voltage and current, in the second stage consist of CLASS C chopper, operating in the chopping mode, is used to vary the amplitude of the average output voltage. The field is fed from CLASS A chopper, operating in the chopping mode, is to vary the field flux or field current.

B. Principle Of Operation

Over each switching period, there exist two patterns of conduction Pattern I and Pattern II, corresponding, respectively, to the on and off states of the power switch as follows.
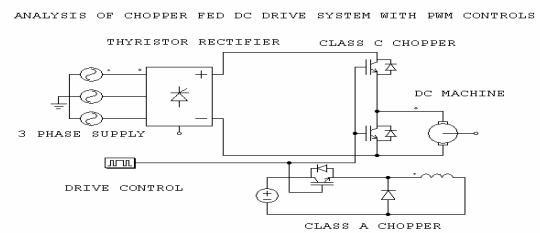

Fig. 4. Chopper fed dc drive system

1) Forced Current Transition (Pattern I)

This pattern corresponds to the on-state periods of the chopping switch, where the rectified supply voltage appears across the terminals of the load (armature) circuit, forcing the current to flow from the supply into the armature circuit.

2) Current Freewheeling (Pattern II)

This pattern corresponds to the off-state periods of the chopping switch, where the load circuit is isolated from the supply and the armature is short-circuited through the

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freewheeling diode. Therefore, the load terminal voltage is zero, and the armature current decays through the freewheeling diode.

Depending upon the loading conditions, the system may operate in one of the following two conduction modes:

I) Continuous Conduction Mode (CCM): In CCM, the load current comprises Patterns I and II in a repetitive sequence.

II) Discontinuous Conduction Mode (DCM): Under light loading conditions, the modulation process may not be maintained regular over the period of output symmetry. When this is the case, the load (armature) current is discontinuous. Over the imposed zero-current gap, the armature circuit is open-circuited, with the back EMF, a speed-dependent parameter, appears across the motor terminals.

IV. PERFORMANCE PARAMETER OF THE SYSTEM

In this paper, five performance parameters are analyzed A) Power Factor, B) Displacement Factor, C) Distortion Factor, D) Harmonic Factor, E) Ripple Factor.

A. Power Factor

In an AC circuit, not all of the apparent power (the RMS voltage times the RMS current and measured in VA), is real power or average power (measured in Watts) that actually performs work. Power factor is the ratio between these two power, Power Factor (P.F.) = Real Power (watts) /Apparent Power (VA) Or Real Power = Apparent Power x Power Factor [2]. It can be seen that if all the apparent power is real, the power factor is 1 and if there is no real power, the power factor is 0. All other power conditions fall between these two values. The cause of this difference between the real and apparent power is depending on the type of load

B. Displacement Factor

Assuming all the power factor is due to displacement factor, then Real Power = Apparent Power x Displacement factor The cosine of the angle of the phase difference, $(\pi/6+\psi)$, where ψ is displacement angle of the line current, whether leading as in a capacitive load or lagging as in a inductive load, defines this ratio of resistive current to reactive current and also is the definition of power factor for linear loads [2]. Real Power = Apparent Power x *cos* $(\pi/6+\psi)$ Therefore, Displacement Factor = *cos* $(\pi/6+\psi)$.

C. Distortion Factor

The portion of the power factor is caused by the shape of the current wave and how much it differs from a pure sine wave, it is referred to as the distortion factor.

Assuming all the power factor is due to distortion factor, then Real Power = Apparent Power x Distortion Factor, If the distortion is measured as a ratio of the fundamental current to the total current, then, Real Power = Apparent Power x (Fundamental Current/Total Current) Therefore, Distortion Factor = Fundamental Current /Total Current [2].

D. Harmonic Factor

The input current, being non sinusoidal, contains currents of harmonic frequencies. The harmonic factor defined as the ratio of the rms value of net harmonic current to the rms value of nth harmonic current, $HF=I_h/I_n$, where, I_h =rms value of net harmonic current, I_n =rms value of nth harmonic current [3]. The harmonic factor indicates the harmonic content in the input supply current and thus measure the distortion of the input current.

E. Ripple Factor

In power conversion circuits, the actual output waveform of any converter constructed from the input sources will in general be different from the input. This tells us that the output must contain unwanted components along with the wanted components. These unwanted components are unfortunately unavoidable and they can be described as the Fourier components. The complete collection of unwanted components defines distortion. The terms harmonic distortion or simply harmonics refer to this unwanted behavior. Particularly in dc application such as that of chopper circuits, the collected unwanted components are typically referred to by the term ripple [3]. A more specific definition is ripple factor which is a tool to measure how much deviation the converter output parameter has from its nominal designed value. Due to the fact that ripple is closely related to distortion of the output waveform. The ripple factor=I_{ac}/I_{dc}, where, I_{ac}=rms value of output current, I_{dc}= average value of output current.

V. SYSTEM SIMULATION

A. System Simulation With UPWM

The nature of the rectification stage, the output voltage and current waveforms are repetitive at a frequency f_o equals six times the supply frequency f_s, with an output period of symmetry equals to $\Pi/3$. Typical waveforms of the load voltage and load current of the system under consideration are shown in Fig. 5. A chopping frequency of 600 Hz (two pulses per output period of symmetry) is employed for demonstration purposes [1]. The number of pulses per output period of symmetry is given by, $N=f_c/6f_s$.Since N is desired to be an integer in order to obtain symmetry in the output waveforms, the control circuitry should be designed such that M is a multiple of six. This implies that for a 50-Hz system, where

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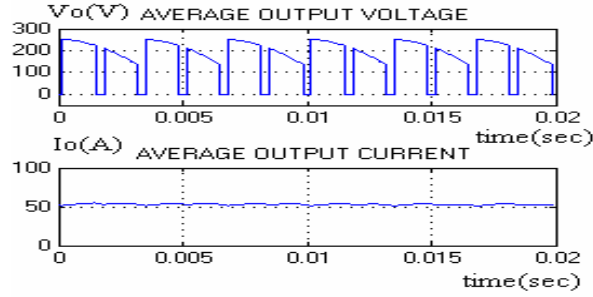$N=f_c/300$, the chopping frequency should be a multiple of 300.

Fig. 5. Simulation result of the system with UPWM

B. System Simulation With SPWM

Typical load current and voltage waveforms are shown in Fig.6.These waveforms are repetitive at a frequency f_o equal to twice that of the supply voltage, f_s, (i.e., $f_o=2f_s$) [5]. Assuming that the modulating to supply frequency ratio is given by M (i.e. $M=f_c/f_s$) and providing that M is a positive even integer, each cycle of the supply voltage contains N chopping cycles, where N is an integer given by $N=f_c/3f_o$.
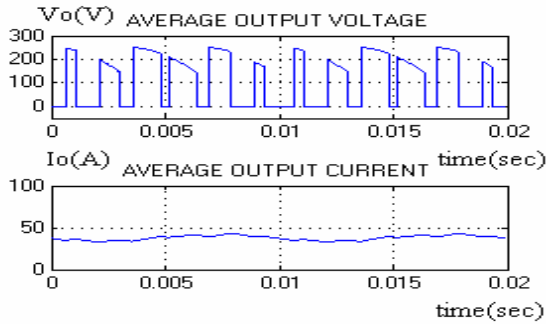

Fig. 6. Simulation result of the system with SPWM

C. System Simulation With TPWM

The output voltage and current waveforms are repetitive at a frequency f_o equals six times the supply frequency f_s, with an output period of symmetry equals to $\Pi/3$ [3]. Typical waveforms of the load voltage and load current of the system under consideration are shown in Fig.7. The number of pulses per output period of symmetry is given by, $N=f_c/6f_o$.Since N is desired to be an integer in order to obtain symmetry in the output waveforms. The chopping frequency should be a multiple of 300.
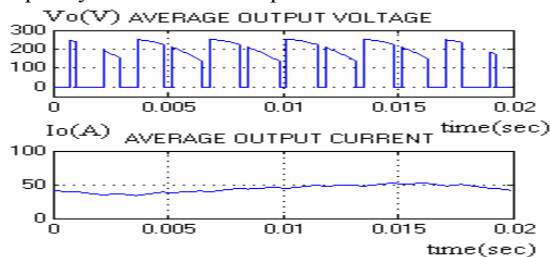

Fig. 7. Simulation result of the system with TPWM

VI. PERFORMANCE EVALUATION

In this section, the performance parameters of the system under consideration will be evaluated and thoroughly investigated for given loading conditions. The popular generator-type load characteristic, where the load torque is proportional to the proportional to the running speed, is considered. A 5hp, 240-V, 16-A, 1200-RPM separately excited dc motor is employed. The measured values of the armature resistance and inductance are 2.581Ω and 28 mH, respectively, implying a relatively low design armature time-constant of 10ms.The computed value of the design-excitation constant is 0.34 $V*sec/rad$. The rms amplitude of the line voltage is chosen such that when the modulation index is maximum (i.e.α=1), the average value of the terminal voltage V_{av}, equals the rated voltage of the dc motor V_r. The maximum input supply voltage is given by $V_{max}= (V_{dc*}\pi)/(3*3^{1/2})$.for given motor V_{max} =146-V.

A. Input Power Factor

Input power factor is combination of the real power and apparent power of the supply system [2]. The power factor curve is shown in Fig.8. In three PWM control power factor decreases with increases in modulation index.
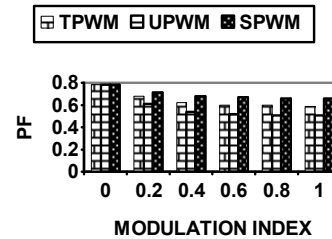

Fig. 8. Power factor curve

B. Displacement Factor

The displacement factor defines this ratio of resistive current to reactive current [2], therefore displacement factor= cos $(\pi/6+\psi)$. The displacement factor curve is shown in Fig.9. In three PWM control displacement factor increases with modulation index increases.
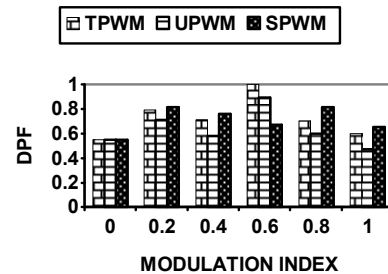

Fig. 9. Displacement factor curve

C. Distortion Factor of the Input Current

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The distortion factor is the ratio of the rms value of fundamental current to the rms value of total current [2]. The distortion factor curve is shown in Fig .10. In three PWM control distortion factor decreases with modulation index are varying from 0 to 0.5, distortion factor increase with modulation index is varying from0.5 to 1.
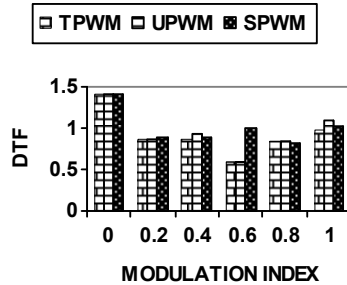

Fig. 10. Distortion factor curve

D. Harmonic Factor Of The Line Current

The harmonic factor is the ratio of the rms value of net harmonic current to rms value of nth harmonic current [3]. The harmonic factor curve is shown in Fig.11.in three PWM control harmonic factor increases with modulation index is varying from 0 to 0.6, harmonic factor is decrease with modulation index is varying from 0.6 to 1
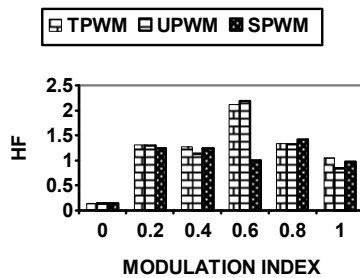

Fig. 11. Harmonic factor curve

E. Ripple Factor Of The Load Current

The ripple factor curve is shown in Fig.12. The ripple factor of UPWM control decreases with modulation index increases. In other control ripple factor constant with modulation index increases.
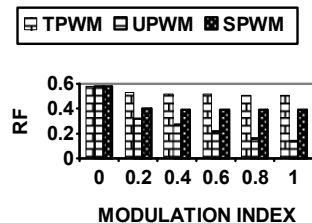

Fig. 12. Ripple factor curve

F. Speed Of The Motor

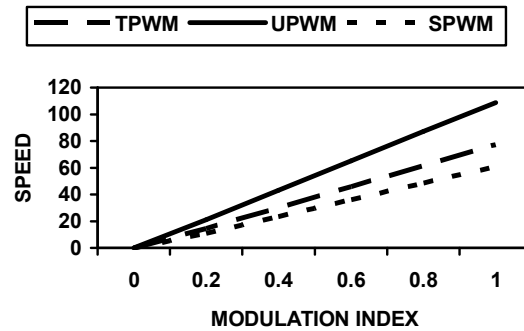The speed curve is shown in Fig.13. In three PWM controls speed increases with modulation index increases.

Fig. 13. Speed curve

VII. CONCLUSION

In this paper, different PWM techniques for chopper fed dc drive system are discussed and performance parameters of the system are analyzed using MATLAB/SIMULINK. The Sinusoidal PWM technique is found to be the best of all available techniques for performance analysis. This control technique is verified in C programming language.

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A NEW THREE LEVEL ZVS CONVERTER

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Abstract- **This paper deals with the design issues relevant to achieve ZVS for three level converters. It shows the method of designing a three level converter and to achieve ZVS in the wide range of load current and input voltage by employing coupled inductor. This converter overcomes the drawbacks presented by the conventional zero-voltage switching (ZVS) three-level converter, such as high circulating energy, severe parasitic ringing on the rectifier diodes, loss of duty cycle, high conduction loss and limited ZVS load range for the primary switches. This converter employs a coupled inductor to achieve zero-voltage switching of the primary switches in the entire line and load range is described. Because the coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output rectifiers.**

I. INTRODUCTION

IN RECENT years, multilevel power converters have received a lot of attention due to their suitability for applications with high input voltages[1]. Specifically, multilevel inverters and dc–dc converters can be implemented with semiconductor switches rated at a fraction of the input voltage, which are typically less expensive and more efficient than their high-voltage-rated counterparts. Because the implementation complexity of multilevel converters is increased dramatically by the number of levels, which diminishes the benefits of multilevel conversion, the majority of development efforts in dc–dc multilevel conversion have been focused on three-level converters.

Generally, three-level dc–dc converters feature power conversion with semiconductor switches rated at one-half of the input voltage. The major deficiencies of the ZVS implementations described in [2]–[4] are brought about by an increased inductance in the primary circuit that is required to achieve a complete ZVS of all primary switches down to light loads. This inductance, which is obtained by intentionally increasing leakage inductance of the transformer and /or by adding an external inductance in the transformer and /or by adding an external inductance in series with the primary of the transformer, has a detrimental effect on the performance. It introduces a circulating current on the primary side, causes a secondary – side loss of duty cycle, and produces severe parasitic ringing on the secondary side of the transformer as it resonates with the rectifier's junction capacitance.

The circulating current caused by excessive energy stored in the inductance employed to extend the ZVS range down to light loads increases the current stress of the primary switches and the primary-side conduction losses at heavy load. The primary side conduction losses are further increased due to the secondary side duty cycle loss which must be compensated by reducing the turn's ratio of the transformer. Furthermore, a smaller turn's ratio of the transformer also increases the voltage stress on the secondary-side rectifiers so that rectifiers with a higher voltage rating that typically exhibit a higher Conduction loss may be required. Finally, to control the ringing voltage across the output rectifiers, a lossy snubber circuit is required on the secondary side which also reduces the conversion efficiency.

The proposed three-level ZVS converter employs a coupled inductor on the primary side to achieve ZVS in the entire line and load range. Since this coupled inductor does not appear as a series inductance in the load current path, it does not cause loss of duty cycle or severe voltage ringing across the output diode. As a result, the proposed circuit exhibits increased conversion efficiency.

II. THREE-LEVEL ZVS CONVERTER WITH COUPLED INDUCTOR

It shows a circuit diagram of the proposed three-level soft-switched dc-dc converter that employs a coupled inductor on the primary side to extend the ZVS range of the primary switches with a minimum circulation energy and conduction loss. The three-level converter consists of a series connection of four primary switches Q_1 through Q_4, rail-splitting capacitors C_{IN1} and C_{IN2}, "flying capacitors" C_{S1} and C_{S2}, isolation transformer TR, and coupled inductor L_C. In this circuit, the load is coupled to the converter through a full-wave rectifier connected to the center-tapped secondary of the transformer. In addition, clamping diodes D_{C1} and D_{C2} are used to clamp the voltage of outer switches Q_1 and Q_4, respectively, to $V_{IN}/2$ after the switches are turned off. Finally, blocking capacitor C_B is employed to prevent transformer saturation.
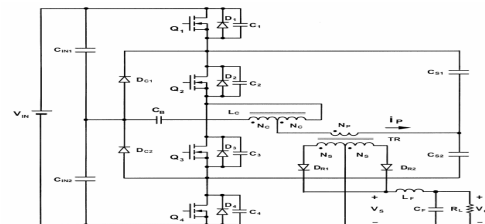

Fig. 1. Proposed three-level ZVS converter with coupled inductor.

III. PRINCIPLE OF OPERATION

In the simplified circuit, it is assumed that inductance of output filter L_F is large enough so that

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during a switching cycle the output filter can be modeled as a constant current source with the magnitude equal to output current i_o. Also, it is assumed that the capacitances of capacitors C_{IN1} and C_{IN2}, which form a capacitive divider that splits the input voltage in half, are large so that capacitors C_{IN1} and C_{IN2} can be modeled by voltage sources $V_1=V_{IN}/2$ and $V_2=V_{IN}/2$, respectively. Similarly, it is assumed that the capacitances of capacitors C_{S1} and C_{S2} are large enough so that the capacitors can be modeled as constant voltage sources V_{CS1} and V_{CS2}, respectively.

The average voltages of the coupled inductor windings and the transformer windings during a switching cycle are zero and for the phase-shift control the outer pair of switches and the inner pair of switches operate with 50% duty cycle, the magnitude of voltage across flying capacitor V_{CS1} and V_{CS2} is equal to half of the voltage across the rail-splitting capacitors, i.e., $V_{CS1}=V_{CS2}=V_{IN}/4$. To further simplify the analysis of operation of the circuit, it is assumed that the resistance of the conducting semiconductor switches is zero, whereas the resistance of the non conducting switches is infinite. In addition, the leakage inductances of both transformer TR and coupled inductor L_C, as well as the magnetizing inductance of transformer TR are neglected since their effect on the operation of the circuit is not significant. However, the magnetizing inductance of coupled inductor L_C and output capacitances C_1-C_4 of primary switches are not neglected in this analysis since they play a major role in the operation of the circuit. Consequently, coupled inductor L_C is modeled as the ideal transformer with turns ratio $n_{LC}=1$ and with parallel magnetizing inductance L_{MC} across the series connection of windings AC and CB, where as transformer TR is modeled only by the ideal transformer with turns ratio n_{TR}. It should be noted that magnetizing inductance of inductor represents the inductance measured between terminals A and B with terminal C open. The following relationships between currents can be established:

$$i_P = i_{P1} + i_{P2} \qquad (1)$$

$$i_1 = i_{P1} + i_{MC} \qquad (2)$$
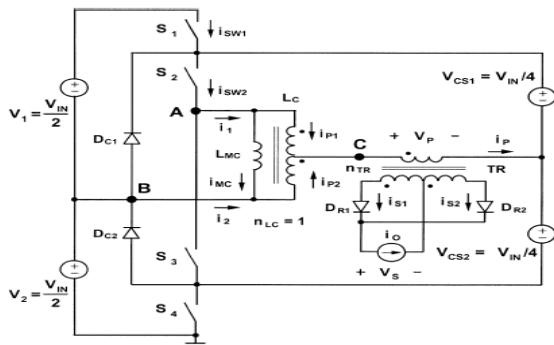
$$i_2 = i_{P2} - i_{MC}. \qquad (3)$$

Fig. 2. Simplified circuit diagram of proposed three-level ZVS converter.

Since the number of turns of winding AC and winding CB of coupled inductor L_C are the same, it must be that

$$i_{P1} = i_{P2}. \qquad (4)$$

Substituting (4) into (1)–(3) gives

$$i_{P1} = i_{P2} = \frac{i_P}{2} \qquad (5)$$

$$i_1 = \frac{i_P}{2} + i_{MC} \qquad (6)$$

$$i_2 = \frac{i_P}{2} - i_{MC}. \qquad (7)$$

As can be seen from (6) and (7), currents and are composed of two components: 1) primary-current component $i_P/2$ and 2) magnetizing-current component i_{MC}. The primary-current component directly depends on the load current, whereas the magnetizing current does not directly depend on the load, but rather on the volt-second product across the magnetizing inductance. Namely, a change of the magnetizing current with a change in the load current occurs only if the phase shift between the turn on instants of outer switches S_1 and S_4 and respective inner switches S_2 and S_3 is changed to maintain the output regulation. Usually, the change of phase shift with a load change is greater at light loads, i.e., as the load decreases toward no load than at heavier loads. Since in the circuit in Fig. 1 the phase shift increases as the load approaches zero, the volt-second product of L_{MC} also increases so that the circuit in Fig. 1 exhibits the maximum magnetizing current at no load, which makes it possible to achieve ZVS at no load. Because magnetizing current i_{MC} does not contribute to the load current, it represents a circulating current. Generally, this circulating current and its associated energy should be minimized to reduce losses and maximize the conversion efficiency. Due to an inverse dependence of the volt-second product of L_{MC} on the load current, circuit in Fig. 1 circulates less energy at full load than at light load, and, therefore, features ZVS in a wide load range with a minimum circulating current. It can be seen that

$$V_{AB} = V_{AC} + V_{CB}. \qquad (8)$$

Since both windings of coupled inductor L_C have the same number of turns, i.e., since the turns ratio of L_C is $n_{LC}=1$, it must be that

$$V_{AC} = V_{CB} \qquad (9)$$

Or

$$V_{AC} = V_{CB} = \frac{V_{AB}}{2}. \qquad (10)$$

Generally for constant-frequency phase-shift control, voltage V_{AB} is a square wave voltage consisting of alternating positive and negative pulses of magnitude $V_{IN}/2$ that are separated by time intervals with $V_{AB}=0$. According to (10) and with reference to fig.2 during the time intervals when either of inner switches S_2 and S_3 is closed and when $V_{AB}=0$, the primary voltage magnitude is $|V_P|= V_{IN}/4$, whereas during time intervals when $|V_{AB}|= V_{IN}/2$, the primary voltage magnitude is $|V_P|=0$. As shown in fig.3 Since during time interval T_0-T_1 switches S_1 and S_2 are closed while switches S_3 and S_4 are open, voltage $V_{AB}=V_1=V_{IN}/2$ so that primary voltage $V_P=0$ In addition,

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during this topological stage, output current i_O flows through output rectifier D_{R2} and the corresponding secondary of the transformer so that primary current $i_P = -i_O/n_{TR}$, where $n_{TR} = N_P/N_S$ is the turns ratio of the transformer, N_P is the number of primary winding turns, and N_S is the number of secondary winding turns.

The primary current is negative, both currents i_1 and i_2 are also negative as shown in Fig. 2. At the same time, magnetizing current i_{MC} is linearly increasing with slope $V_{IN}/(2L_{MC})$, since voltage V_{AB} is positive and equal to half of the input voltage, i.e., $V_{AB} = V_{IN}/2$. As a result, current i_1 increases while current i_2 decreases. During this interval, voltage V_S which is equal to the secondary winding voltage is zero because primary winding voltage V_P is zero. This stage ends at $T = T_1$ when switch is turned off. After switch is turned off at, the current which was flowing through the transistor of switch S_1 is diverted to switch's output capacitance C_1. In this topological stage, current i_2 charges capacitor C_1 and C_4 discharges capacitor at the same rate since the sum of the voltages across capacitors and is equal to constant voltage $V_{IN}/2$. As a result, voltage across switch S_1 increases while voltage across switch S_4 decreases, as illustrated in Fig. 2. In addition, during this stage the potential of point A decreases causing a decrease of voltage V_{AB} from $V_{IN}/2$ toward zero and the
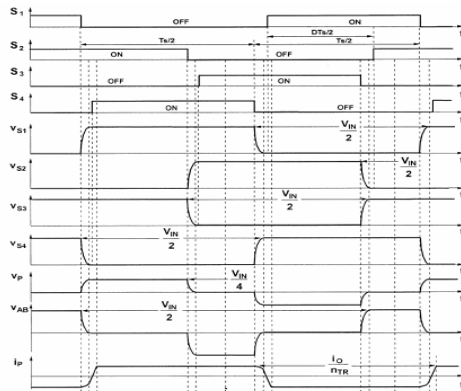

Fig. 3. Key waveforms of three-level ZVS converter.

simultaneous increase of primary voltage from zero toward $V_{IN}/4$, as illustrated in Fig. 2. The positive primary voltage initiates the commutation of output current i_O from rectifier D_{R2} to rectifier D_{R1}. Since the leakage inductance of transformer TR neglected, this commutation is instantaneous. However, in the presence of leakage inductance, the commutation of current from one rectifier to the other takes time. Because during this commutation time both rectifiers are conducting, i.e., the secondary windings of the transformer are shorted, voltage V_S is zero, as shown in Fig. 3.

After capacitor C_4 is fully discharged at $T = T_2$, i.e., after voltage V_{S4} reaches zero, current i_2 continues to flow through antiparallel diode D_4 of switch and clamp diode D_{C1} instead of through capacitors C_1 and C_4. Since it is desirable to minimize the leakage inductance of transformer TR to minimize the secondary-side parasitic ringing, the energy stored in its leakage inductances is relatively small, i.e., much smaller than the energy stored

in output-filter inductance. As a result, in the circuit in Fig. 1, it is easy to achieve ZVS of inner switches S_2 and S_3 in the entire load range, where as ZVS of the outer switches S_1 and S_3 requires a proper sizing of the magnetizing inductance since at light loads almost the entire energy required to create ZVS condition of outer switches and is stored in the magnetizing inductance.

IV. DESIGN CONSIDERATION

In the proposed three-level ZVS circuit with a coupled inductor, it is more difficult to achieve ZVS of the outer pair of switches than the inner pair of switches because the available energies for creating the ZVS conditions in the two pairs of switches are different. Generally, to achieve ZVS this energy must be at least equal to the energy required to discharge the capacitance of the switch which is about to be turned on and at the same time charge the capacitance of the switch that just has been turned off. At heavier load currents, ZVS is primarily achieved by the energy stored in the leakage inductances of transformer TR. As the load current decreases, the energy stored in the leakage inductances also decreases, whereas the energy stored in inductance L_C increases so that at light loads inductance L_C provides an increasing share of the energy required for ZVS. In fact, at no load, this inductance L_C provides the entire energy required to create the ZVS condition. Therefore, if the value of inductance L_C is selected so that ZVS is achieved at no load and maximum input voltage $V_{IN(max)}$, ZVS is achieved in the entire load and input-voltage range.

Neglecting the capacitances of the transformer's windings, magnetizing inductance L_{MC} necessary to achieve ZVS of the outer switches in the implementations in Fig. 1 is

$$L_{MC} \leq \frac{1}{32Cf_S^2}$$

where, C is the total capacitance across the primary switches (parasitic and external capacitance, if any) in the corresponding switch pairs.

Finally, it should be noted that the magnitude of primary current i_P of the proposed converter is approximately two times larger than, for example, that of the conventional three-level converter described in [4] if these converters are designed to meet the same specifications. Namely, because during the energy delivery period voltage V_P across the primary winding of transformer TR in the proposed converter is one half of that of the conventional converter, turns ratio n_{TR} of transformer TR of the proposed converter is one half of that in [4]. However, the switch currents of the proposed converter are similar to those of the conventional converter in [4] because each switch in the converter in Fig. 1 carries approximately one half of primary current i_P therefore, if the transformer is designed to have the primary winding resistance much smaller than the on-resistance of the primary switches, the conduction losses on the primary side of the converter in Fig. 1 are

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approximately the same as those in the converter described in [4].

V. SIMULATION RESULTS

The simulation circuit shown in Fig 4. The simulation results shown in Figs. 5-7. Fig 5 demonstrates that ZVS is achieved with input gate pulse of the switch's Q_1. Fig.6 shows voltage across the primary side of transformer TR. Fig.7 shows voltage across the coupled inductor L_C.
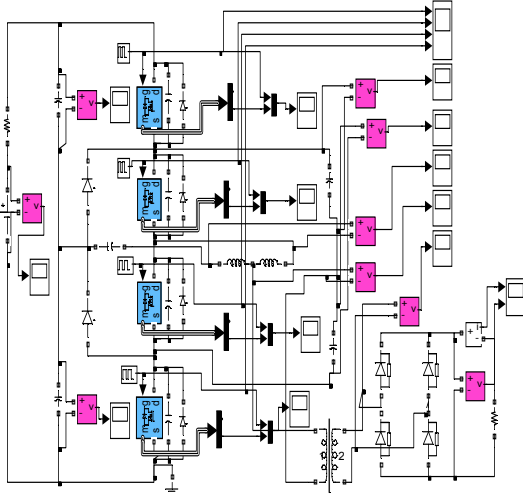

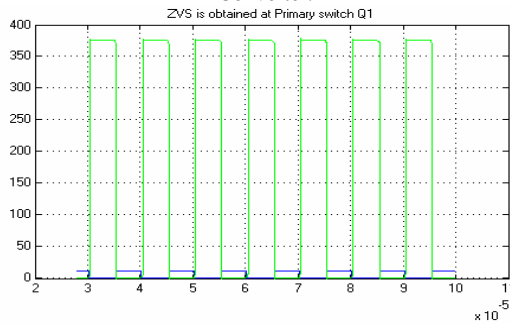Fig.4. Simulation block diagram of three Level ZVS Converter.

Fig.5. Input gate pulse and voltage across the switch Q_1 at ON and OFF states.
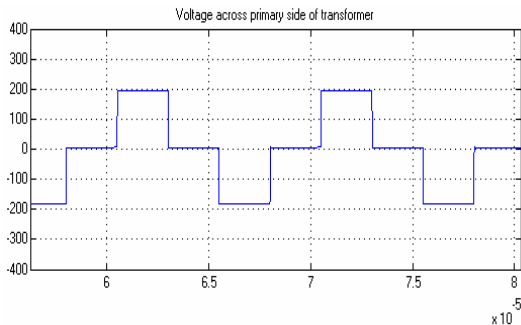

Fig.6. Voltage across the primary side of transformer TR.
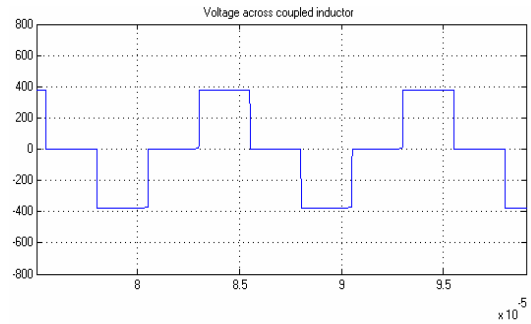

Fig.7. Voltage across the coupled inductor L_C

VI. CONCLUSION

A new isolated, constant-frequency, three-level ZVS converter which employs a coupled inductor on the primary side to achieve ZVS in a wide range of load current and input voltage with reduced circulating energy and conduction losses has been described. Since this coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output rectifiers.

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ON-LINE ESTIMATION OF STATOR-ROTOR RESISTANCE OF AN INDUCTION MOTOR DRIVE USING ARTIFICIAL INTELLIGENCE TECHNIQUES

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Abstract - **Stator and rotor resistance variations occur during normal operation of Induction motors. The performance of a vector-controlled drive to a large extent depends on the accuracy of estimated flux, which in turn depends on rotor resistance. Rotor resistance varies with rotor heating and changes in rotor frequency. Hence estimation of rotor resistance is necessary for enhancing the performance of the drive. However, the rotor resistance estimation algorithm requires the knowledge of stator resistance which may vary during the motor operation. This paper proposes artificial intelligence techniques for estimation of stator and rotor resistances. The performance of the proposed estimators is studied and reported.**

Key words: Artificial neural networks, Rotor resistance estimators, Fuzzy logic, Stator resistance estimators, Induction motor drive.

I. INTRODUCTION

Indirect field oriented vector controlled induction motor drives are increasingly used in high performance drive systems. Three phase induction motors are the most prominently used induction motor drives due to their reliability and cost. However, the performance of vector-controlled drive depends on the accuracy of the estimated rotor flux from the measured stator currents. The accuracy of the estimated rotor flux is greatly influenced by the value of the rotor resistance, which is not constant. Rotor resistance may vary due to the rotor heating and recovering this information either with a thermal model or a temperature sensor is difficult. Estimation of rotor resistance (R_r) requires the knowledge of stator resistance (R_s). However R_s may also vary up to 50% during motor operation. The error in the values of R_s hence leads to errors in R_r estimation. In addition rotor resistance can change significantly with rotor frequency due to skew / proximity effect. The problem related to rotor resistance adaptation has been investigated and reported in [1]-[4].

Conventional methods of estimation techniques are observer based techniques [5], Extended Kalman filtering technique [6], Model reference adaptive techniques [7] etc. All these methods are useful only for steady state operation of the induction motor. This paper describes a method for the on-line estimation of stator and rotor resistance using artificial intelligence techniques. The estimator uses on-line training algorithms, so that the dynamic variation of resistances can be tracked. The total error between the desired and actual state variables is back propagated to adjust the weights of the neural model, so that the output of this model tracks the actual output [8]. When the training is

completed, the weights of the neural network should correspond to the parameters in the actual motor. However the R_r estimation algorithm requires the knowledge of stator resistance R_s which may also vary up to 50% during operation. It has been observed that the error in R_s, leads to significant errors in R_r estimation. Hence, this problem can be overcome by adding another on-line estimation for R_s to the system using a fuzzy non-linear observer.

II. ROTOR RESISTANCE ESTIMATION USING ARTIFICIAL NEURAL NETWORKS

The rotor resistance of an induction motor can be estimated using the neural network system as illustrated in Fig. 1. Two independent observers are used to estimate the rotor flux vectors of the induction motor.
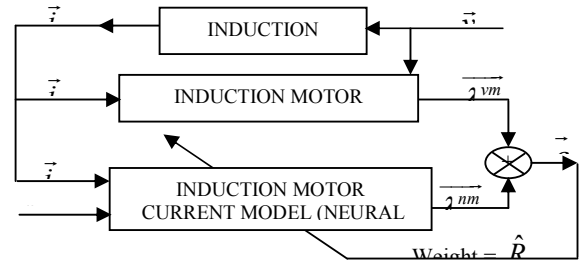

Fig -1 Structure of Neural Network System for Rr Estimation

Equation (1) based on stator voltages and currents called as voltage model equation and equation (2) is based on stator currents and rotor speed called as current model equations. [9]

$$\begin{bmatrix} \dfrac{d\lambda_{dr}}{dt} \\ \dfrac{d\lambda_{qr}}{dt} \end{bmatrix} = \dfrac{L_r}{L_m} \left(\begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} - \begin{bmatrix} R_s + s\sigma L_s & 0 \\ 0 & R_s + s\sigma L_s \end{bmatrix} \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} \right)$$

$$(1)$$

$$\begin{bmatrix} \dfrac{d\lambda_{dr}}{dt} \\ \dfrac{d\lambda_{qr}}{dt} \end{bmatrix} = \begin{bmatrix} \dfrac{-1}{T_r} & -\omega_r \\ \omega_r & \dfrac{-1}{T_r} \end{bmatrix} \begin{bmatrix} \lambda_{dr} \\ \lambda_{qr} \end{bmatrix} + \dfrac{L_m}{T_r} \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix}$$

$$(2)$$

The discrete current model equations are given as

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$$\lambda_{dr}(k) = W_1 \cdot \lambda_{dr}(k-1) - W_2 \cdot \lambda_{qr}(k-1) + W_3 \cdot i_{ds}(k-1) \qquad (3)$$

$$\lambda_{qr}(k) = W_1 \cdot \lambda_{qr}(k-1) + W_2 \cdot \lambda_{dr}(k-1) + W_3 \cdot i_{ds}(k-1) \qquad (4)$$

where $W_1 = 1 - \dfrac{T}{T_r}$; $W_2 = \omega_r.T$; $W_3 = \dfrac{T.L_m}{T_r}$ (5)

Here T is the sampling period, T_r is the rotor time constant, ωr is electrical rotor angular velocity, λ_{dr} and λ_{qr} are d-axis and q-axis rotor fluxes, I_{ds} and I_{qs} are d-axis and q-axis stator currents and σ is called leakage coefficient. The neural model represented by Equation (3) and (4) is shown in Fig.2, where W_1, W_2, W_3 represent the weights of the network.
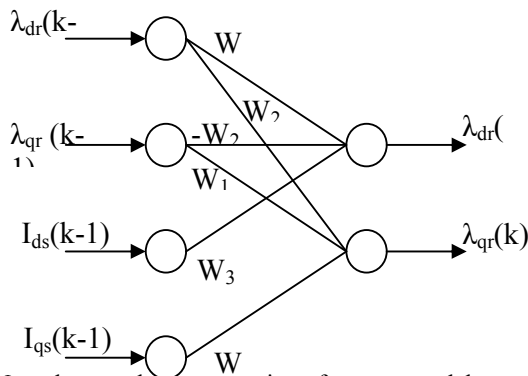

Fig -2 Neural network representation of current model

If the network shown in Fig.2 is used to estimate Rr, W_2 is already known and W_1 and W_3 need to be updated. The weights between neurons, W_1 and W_3 are trained, so as to minimize the energy function E,

$$E = \frac{1}{2}\left[\lambda_r{}^{vm} - \lambda_r{}^{nm}\right] = \frac{1}{2}\left[\varepsilon_d(k)^T \; \varepsilon_q(k)\right] \qquad (6)$$

The rotor resistance can be calculated from either W_1 or $W3$ from (7) and (8)

$$R_r = \left(\frac{L_r * W_3}{L_m * T}\right) \qquad (7)$$

$$R_r = \frac{L_r}{T}(1 - W_1) \qquad (8)$$

III. STATOR RESISTANCE ESTIMATION USING FUZZY LOGIC

The stator resistance of an induction motor can be estimated using the fuzzy system as illustrated in Fig. 3. This estimator is designed to estimate the change in stator resistance while the drive is in operation. The error between the estimated stator current $I_s^*(k)$ and the measured stator current $I_s(k)$ is used to determine the incremental value of stator resistance $(\Delta\hat{R}_s)$ through a fuzzy estimator. The inputs to the fuzzy estimator are the current error and change in current error [10].

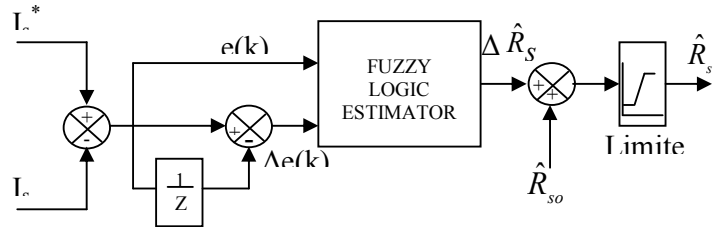
Fig -3 Structure of fuzzy estimator for Rs estimation

The error is represented as

$$e(k) = \Delta I_s(k) = I_s^*(k) - I_s(k) \qquad (9)$$

The change in error is represented as

$$\Delta e(k) = e(k) - e(k-1) \qquad (10)$$

The fuzzification stage input variables for the resistance estimator are current error e(k), change in current error Δ e(k) and the output variable is the change in stator resistance ΔR_s. The magnitude of the stator current vector can be obtained from the equations given below. The rotor flux estimation using the voltage model and current model can be written as

$$\sigma L_S \frac{di_{ds}}{dt} = \frac{Lm}{L_r T_r}\lambda_{dr}^{im} + \frac{L_m}{L_r}\omega_r\lambda_{qr}^{im} - \frac{Lm^2}{L_r T_r}i_{ds} + V_{ds} - R_s i_{ds} \qquad (11)$$

$$\sigma L_S \frac{di_{qs}}{dt} = \frac{Lm}{L_r T_r}\lambda_{qr}^{im} - \frac{L_m}{L_r}\omega_r\lambda_{dr}^{im} - \frac{Lm^2}{L_r T_r}i_{qs} + V_{qs} - R_s i_{qs} \qquad (12)$$

The discrete form of Equation (11) and (12) is

$$i_{ds}^*(k) = W_4 i_{ds}^*(k-1) + W_5\lambda_{dr}^{im}(k-1) + W_6\lambda_{qr}^{im}(k-1) + W_7 V_{ds}(k-1) \qquad (13)$$

$$i_{qs}^*(k) = W_4 i_{qs}^*(k-1) + W_5\lambda_{qr}(k-1) - W_6\lambda_{dr}(k-1) + W_7 V_{qs}(k-1) \qquad (14)$$

Where, $W_4 = 1 - \dfrac{T_s}{\sigma L_s}\dfrac{Lm^2}{L_r T_r} - \dfrac{T_s}{\sigma L_s}R_s$; $W_5 = \dfrac{T_s}{\sigma L_s}\dfrac{Lm}{L_r T_r}$

$W_6 = \dfrac{T_s}{\sigma L_s}\dfrac{Lm}{L_r}\omega_r$; $W_7 = \dfrac{T_s}{\sigma L_s}$

The amplitude of the stator current is represented as

$$I_s^*(k) = \sqrt{i_{ds}^*(k)^2 + i_{qs}^*(k)^2} \qquad (15)$$

The membership function of the fuzzy stator resistance estimator is shown below. They are divided into seven fuzzy segments namely where NL, NM, NS, Z, PS, PM, PL. The crisp input variables are converted into fuzzy variables using triangular membership functions as shown in Figs. 4 and 5. The range of control, which is the universe of

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discourse, is from -0.3 to 0.3A for current error and from -0.25 to 0.25 for change in current error respectively.
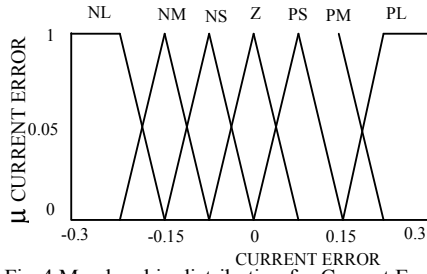

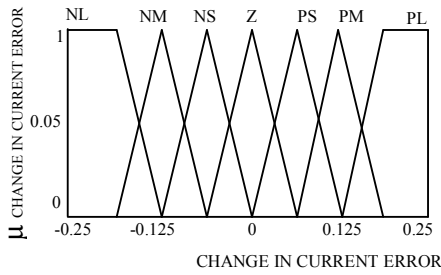Fig-4 Membership distribution for Current Error

Fig-5 Membership distribution for Change in Current Error
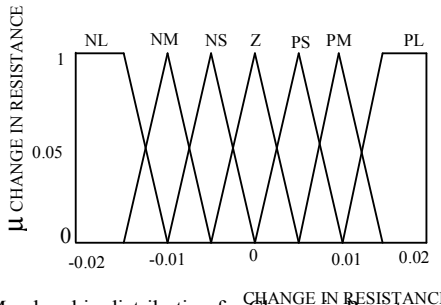

Fig-6 Membership distribution for Change in Resistance

The rule base of the fuzzy logic estimator is shown in Fig. 7, which has 49 rules.

The firing strength of ith rule is given by

$$\alpha_i = \min\{\mu_{ei}(e), \mu_{\Delta ei}(\Delta e)\} \qquad (16)$$

where $\mu ei(e)$ is the membership grade of e_i segment of current error e and $\mu\Delta ei(\Delta e)$ is the membership grade of Δei segment of change in current error Δe. The interface method used is basic and is developed from the minimum operation rule as the fuzzy implementation function. The membership function of the resultant aggregation is by the maximum method. The maximum method takes the maximum of their degree of support (DoS) values. In the defuzzification stage, a crisp value for the output variable, change in resistance (ΔRs) is obtained by using the mean of maximum (MoM) operator. The membership functions for defuzzification stage are shown in Fig. 6. The incremental stator resistance $(\Delta \hat{R}_s)$ is continuously added to the previously stimated stator resistance $\hat{R}_{so}$. The final estimated value $\hat{R}_s$ is obtained as the output of a limiter.

	CURRENT ERROR						
	NL	NM	NS	Z	PS	PM	PL
NL	NL	NL	NL	NL	NL	NM	NS	Z
NM	NL	NL	NL	NM	NS	Z	PS
NS	NL	NL	NM	NS	Z	PS	PM
Z	NL	NM	NS	Z	PS	PM	PL
PS	NM	NS	Z	PS	PM	PL	PL
PM	NS	Z	PS	PM	PL	PL	PL
PL	Z	PS	PM	PL	PL	PL	PL

(CHANGE IN CURRENT ERROR — row labels)

Fig-7 Rule Base for Fuzzy Stator Resistance Estimator

V. SIMULATON RESULTS & DISCUSSIONS

Simulations with the aid of MATLAB/SIMULINK verify the use of artificial intelligence techniques in identification algorithms. For rotor resistance Rr = 0.45 ohms, the pattern in which estimator tracks the actual resistance is as shown in Fig. 8.
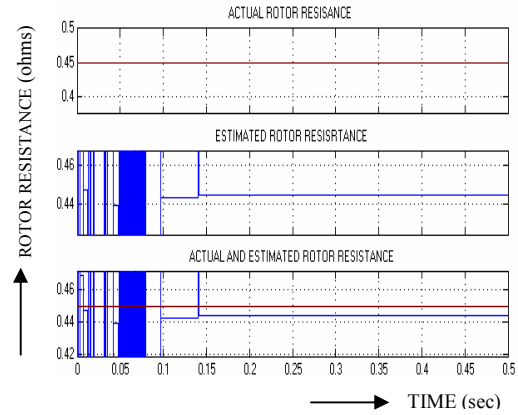

Fig-8 Actual and Estimated Rotor Resistance for Rr = 0.45 Ω

The estimator is then tested for 45% step variation in rotor resistance that is Rr is varied from 0.45 to 0.75.
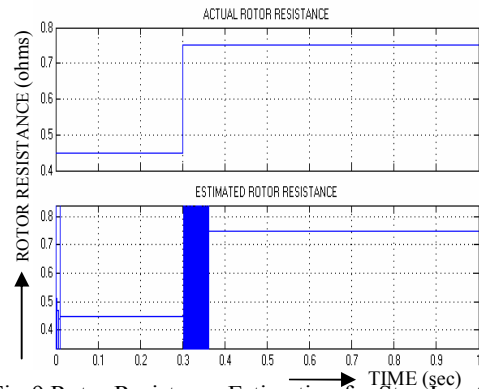

Fig-9 Rotor Resistance Estimation for Step Input

Here the neural network is trained in such a way that the flux obtained from the voltage model tracks the flux

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obtained from the neural model. The corresponding wave forms validating the statement are shown in Figs. 10 and 11 for both d- as well as q-axes.
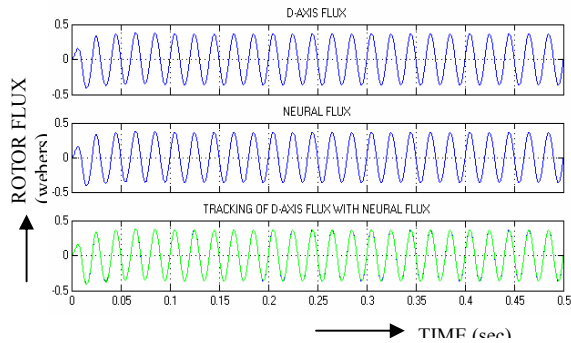
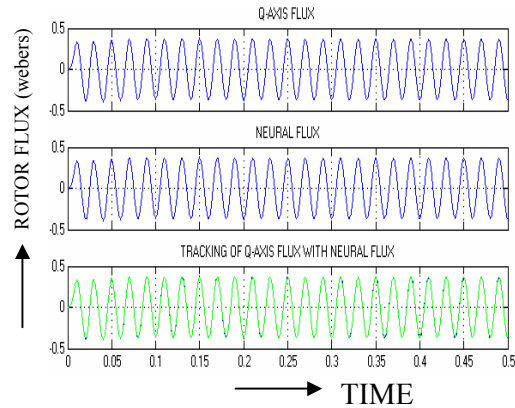| R_r(act)	R_r(est)	%Error
0.45	0.4461	0.8
0.55	0.5472	0.5
0.65	0.6481	0.2
0.75	0.751	0.1
0.85	0.845	0.5

Fig-10 Tracking of D-axis flux with neural model
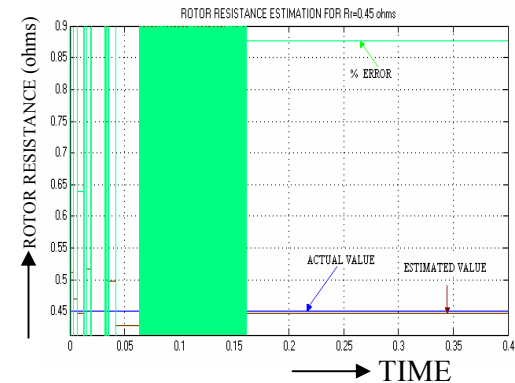

Fig-11 Tracking of Q-axis flux with neural model

Fig-12 % Error waveform for Rr = 0.45 Ω

The rotor resistance estimation and the % error is shown in Table 1. It can be seen that the maximum % error is 1%.

For stator resistance Rs = 0.6 ohms, the pattern in which estimator tracks the actual resistance is as shown in Fig. 13.
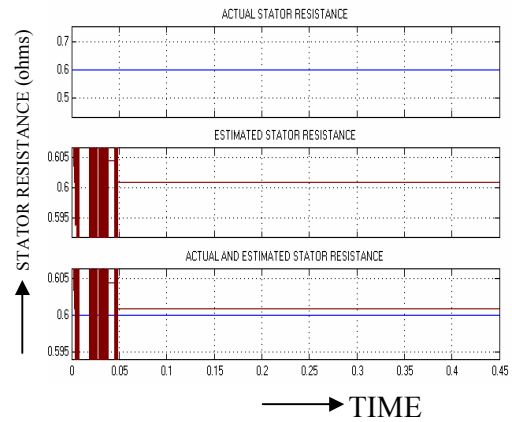
Fig-13 Stator resistance estimation for Rs = 0.6Ω

The estimator is tested for 50% step variation in stator resistance (i.e.) Rs is varied from 0.4 to 0.7 and the corresponding waveform is shown in Fig.14.

Fig-14 Stator resistance estimation for step input
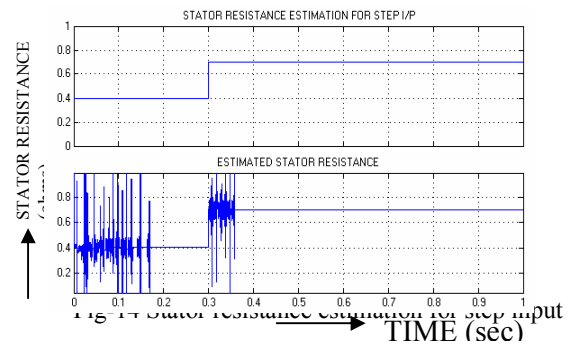
The stator resistance estimation and the % error is shown in Table 2.It can be seen that the maximum % error is 1%.

\

Table-Rotor Resistance Estimation Using Neural Networks

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STATOR RESISTANCE ESTIMATION FOR Rs=0.4 ohms

Fig-15 % Error waveform for Rs= 0.4 Ω

Table-2 Stator resistance estimation using neural networks

R$_s$(act)	R$_s$(est)	%Error
0.4	0.402	0.5
0.5	0.5016	0.3
0.6	0.6009	0.1
0.7	0.6976	0.3
0.8	0.7939	0.7

VI. CONCLUSION

This paper presents a new estimator for the rotor resistance of an indirect vector controlled induction motor drive using artificial neural networks supplemented by a fuzzy logic based stator resistance estimator. For a 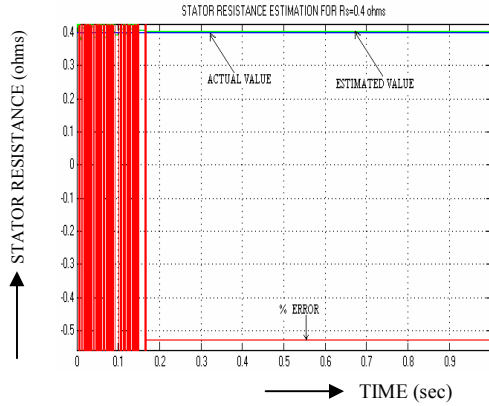step variation in the resistances is successfully estimated. The rotor resistance estimation was found to be insensitive to stator resistance variation. In all the practical applications the variation of stator and rotor resistance time constants will be in seconds. From the results obtained, it is observed that the error in estimation is less than 1%. In the proposed fuzzy-neuro estimator the estimation time is approximately less than 150 msec which is very less compared to practical variations.

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Design and Analysis of Low to High Frequency AC-AC Inverter with Power Factor Improvement

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Abstract----This paper presents a full bridge ac-ac inverter for high frequency Power distribution system with power factor correction stage controlled by unified Controller. The proposed inverter features are Load independent output voltage with constant Frequency, very low total harmonic distortion (THD), Soft switching of the full bridge switches For a wide range of input voltage and load conditions, low dc bus voltage, Simple control and Cost effectiveness for the power factor correction stage. The proposed inverter is used for low Power high frequency applications. The input voltage is given to the rectifier circuit. The rectifier Circuit converts the AC into DC voltage. The DC bus voltage is given to the full bridge inverter. The full bridge inverter converts the DC bus voltage into quasi square waveform. This voltage is given to the resonant network. The resonant network converts the quasi square waveform into a high frequency sinusoidal output.

1. INTRODUCTION

1.1 General

High frequency power distribution architecture (HFPDA) as an option for computer and telecom power distribution power systems will continue to be explored due to many of its merits over conventional dc distribution architecture. Actually a power distribution system for computer and telecom systems consists of three parts: a front-end converter, distributed wire and point-of-use-power supplies (PUPS) on electronic cards.

1.2 DC distributed Architecture

In conventional dc distributed power system, front-end is an ac-dc converter. The dc output voltage of ac-dc converter is distributed through connectors and wires to the points of use. The PUPS on electronic cards are dc-dc converters which convert the distributed high dc voltage into various lower dc voltages.

1.3 AC distributed Architecture

In view of HFPDA has the same three parts. But here the front-end is a high frequency ac-ac inverter instead, which generates a high frequency voltage,100KHz.The voltage waveform is normally sinusoidal with amplitude below 30Vrms.The high frequency is then distributed to PUPS. Here PUPS is a high frequency ac-dc converter, which rectify the distributed high frequency ac voltage waveform into required dc voltages. Here the output rectification and output filter stage in the front-end converter as well as the inversion stage in the point of use converters are eliminated.

The elimination results in simpler system, which can potentially reduce the number of components, reduce cost and increase the system reliability. As resonant components will be used in the front-end ac-ac converter and ac-dc rectifier to generate high frequency ac voltage and to rectify the high frequency ac voltage, Zero voltage switching can be achieved simultaneously both in ac-ac and ac-dc converters. Because of using this higher and higher switching frequency has become a trend in industry for the purposes of reducing size and providing a high quality output voltage under dynamic load conditions.

The front-end converter in HFPDA is an ac-ac inverter. Some of the requirements on it are as follows:

1. High input power factor.
2. High efficiency.
3. High frequency sinusoidal ac voltage with low total Harmonic distortion.
4. High power density.
5. Simplicity.
6. Low cost.

In order to satisfy the above requirements the following design issues to be considered. They are as follows:

1. Input current harmonics
2. Output voltage THD
3. Output voltage regulation
4. Dc bus voltage
5. ZVS in full bridge inverter
6. Conduction losses in the full bridge inverter.

It has been known that two-stage power factor correction (PFC) converter with Multiplier approach control can provide an almost unity power factor and a regulated dc bus voltage. They are well suited for high power applications but appear to be complex and expensive for low power applications. Single-stage PFC topologies are preferable in low power applications for their simplicity and cost effectiveness, but they suffer from high dc bus voltage, which is load dependent. Solutions to this problem include letting the output of the ac-dc converters work in discontinuous conduction mode (DCM), so that the load effect on the dc bus voltage can be minimized. However, all the single-stage PFC approaches are targeted to ac-dc converters. Due to the significant difference between the ac-dc converter and the high frequency ac-ac inverter, the existing knowledge and conclusions based on single-stage PFC for ac-dc converters can not be applied to the after mentioned ac-ac inverters directly.

2 HIGH FREQUENCY AC-AC INVERTER

2.1 General

One of the major differences between the ac-dc converter and the ac-ac inverter is that the dc-dc output stage in the ac-dc converter can work under either DCM,

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which is load dependent, or under continuous conduction mode(CCM), which is load independent, but the dc-ac output stage in the ac-ac inverter is always load independent. There is no DCM or CCM at all. AS we have known, the combination of DCM or CCM on the PFC circuit and the dc-dc stage in an ac-dc converter can help limit the dc bus voltage. Since there is no DCM and CCM combination to choose in an ac-ac inverter, we found that single-stage PFC approach for ac-ac inverter will result in a very high dc bus voltage, even if the PFC circuit is designed to work under CCM. Hence greatly increasing the voltage ratings of related components. Therefore, single-stage PFC is not an effective solution to this application.

2.2 HIGH FREQUENCY AC-AC INVERTER

The high frequency ac-ac inverter, which provides a good solution to the above problem for low power application is shown in fig.2.1.The inverter has two stages: a PFC stage and a high frequency dc-ac stage. The boost converter in the PFC stage is working under DCM mode with constant switching frequency and a variable duty cycle. However instead of using one controller for the PFC stage to correct the power factor and regulate the dc bus voltage, and another controller for the dc-ac stage to regulate the final output voltage, a unified controller is introduced to control two stages simultaneously. The unified controller will regulate the final output voltage; correct the input current power factor.

To operate the boost PFC stage under DCM is a better for the particular application. It is determined by the inherent nature of the high frequency ac-ac inverter and the proposed control method. The DCM of operation for the ac-ac inverter provides better input power factor while maintaining similar dc bus voltage level as the CCM.

A full bridge inverter is used in the dc-ac stage. It is suitable for 250W output power in this design. More important, it adopts constant frequency and phase-shift control pattern. As will be explained later on, this full bridge inverter with the above control pattern can generate the required high frequency sinusoidal voltage waveform, which is load dependent and has very low THD. In addition, with proper design all the switches of the full bridge inverter can work under zero voltage switching (ZVS), hence a high efficiency at high switching frequency can be realized.

However, the unification of the control circuits will not automatically lead to the compliance with the previous listed five major requirements on the low power and high frequency ac-ac inverters. Therefore, a thorough investigation on the feasibility, performance, and design of this approach need to be carried out.

2.3 CIRCUIT DESCRIPTION

The ac-ac high frequency inverter given in fig 2.1 consists of the following functional blocks.

2.3.1 BOOST CONVERTER

It works in discontinuous conduction mode (DCM) to correct the power factor. The unified controller generates its gate signal.

2.3.2 FULL BRIDGE INVERTER

The dc/ac stage adopts full bridge topology with phase-shift control pattern and outputs a quasi square waveform to the resonant network.

2.3.3 RESONANT NETWORK

It is made up of a series branch and a parallel branch by two capacitors and inductors, converting the quasi square waveform from the full bridge inverter into a high frequency sinusoidal waveform and letting the full bridge inverter working under ZVS.
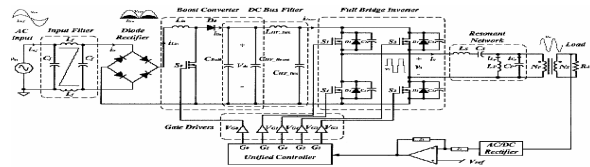
2.3.4 UNIFIED CONTROLLER

The controller gets the feedback from the output voltage and generates phase-shifted signal to the four switches of the full bridge inverter, and generates the gate signals for the boost converter.

2.3.5 INPUT FILTER

The input filter is made our of capacitors and inductors to filter out the high frequency harmonics contained in the line current, which is produced by the boost converter working in DCM, so that a near sinusoidal input current waveform can be obtained.

2.3.6 DC BUS FILTER

The dc bus filter is made up a buck capacitor for 120Hz ripple and hold-up time, a high frequency capacitor for the high frequency harmonics of the dc bus current, and an LC filter for filtering out the input harmonics of the DC-DC stage.

2.4 PRINCIPLE OF OPERATION

The gate signals generated by the unified controller are illustrated in fig 2.2 here V_{G1} to V_{G4} are the gate signals of the full bridge inverter. To implement the feedback loop, in which the high frequency ac output voltage is first rectified and compared with the reference voltage and then is sent to the unified controller after compensation. S0 is turned on whenever S1 and S3, or S2 and S4 are conducting simultaneously.

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With the given gate pattern of switch S0, the boost converter is designed to work under discontinuous conduction mode (DCM). The waveform has a sinusoidal envelope and consists of many chopped triangles. It implies that the current waveform contains a fundamental component at 50Hz, the same frequency as the line voltage, and other high frequency harmonics, whose frequencies are the integer times of the switching frequency. The input filter can filter out the high frequency harmonics and let the low frequency pass. It is these low frequency harmonics that determines the power factor and THD of the input current.

In order to reduce the dc bus voltage, we may not keep all the pulses of S0 given previously. We may keep only 1/m of them. Here m is called Gate Signal Constant. For example, when m=1, we may keep all the pulses. When m=2 or 4, we keep ½ or ¼ of the pulses respectively. By changing the value of m, the dc bus voltage can be changed.

3 STEADY STATE ANALYSIS

3.1 Steady State Analysis of Resonant Network

The Resonant Network is the key part of the ac-ac Inverter for generating the high frequency sinusoidal output voltage and achieving ZVS for all the full bridge switches. In order to understand the mechanism of how the resonant network works, steady state analysis should be carried out. Before we start the following assumptions must be made in order to simplify the analysis;

1. The output voltage of the full bridge inverter is an ideal quasi square waveform.
2.
3. The resonant inductors and capacitors are ideal.
4. The inverter switches are ideal.
5. The load is resistive.

A resistive load is assumed in this paper for the purpose of simplifying the theoretical analysis. Moreover, in a telecommunication or computer ac distributed power system, the high frequency ac-dc converter after the high frequency ac-ac inverter is required to have a unity power factor which has been achieved. In order to let the first harmonic at switching frequency pass the series branch without any voltage loss, the series branch inductor Ls and Cs are turned to the switching frequency. Therefore, the impedance of the series branch inductor and capacitor at the switching frequency are the same.

1) Three important constants

They are given from (1) to (3), where Xs, Xp, Xcp and Rd are defined above. Before going into the more quantitative steady state analysis some rough qualitative analysis first with the three key constants frequency capacitor for the high frequency harmonics of the dc bus current, and LC filter for filtering out the input current harmonics of the dc-ac stage.

K1= Xs / Xp	(1)
K2= Xcp / Xp	(2)
K3= Xp / Rd	(3)

A larger K1 in (1) indicates a relatively large Xs compared with Xp, which means a relatively larger series branch inductor Ls. The series branch can then absorb more n^{th} harmonic voltages by dividing the source voltage with the parallel branch. Therefore, less n^{th} harmonic voltage is applied on the parallel branch; hence lower THD at the output voltage.

A smaller K2 in (2) means larger parallel capacitance with respect to the parallel inductor and resistive load. It implies that the parallel capacitor will absorb more n^{th} harmonic current fed from the series branch, hence less n^{th} harmonic current flows in the load, which will result in lower THD at the output voltage. However, larger parallel capacitance, i.e. smaller impedance will result in a larger current stress on the parallel capacitor. In addition the series branch is tuned to the switching frequency i.e. the frequency of the first harmonic, and then the overall inductive impedance of the parallel branch and the resistive load determine the phase lag of the first harmonic current to the full bridge inverter output voltage. A large parallel capacitor will make the parallel branch less inductive; hence the first harmonic current lags its voltage less. Small phase lag angle makes it more difficult to achieve ZVS for the full bridge under all conditions. In order to have an inductive parallel branch, should be Xcp larger than Xp, therefore K2 should be greater than one according to (2).

A larger case K3 in (3) means larger impedance of the parallel inductor, hence larger impedance of the parallel capacitor and larger impedance of the series inductor and capacitor, given K1 and K2 are fixed in (1) and (2) respectively. The increased impedance of the resonant components will reduce the series branch current; hence reduce the current stress on the series inductor and capacitor. It will also reduce the circulating current in the parallel capacitor. However, a larger K3 will result in less inductive parallel branch, which is not very obvious but can be proven later on in the quantitative analysis.

Initially K3 is used to design the value of the parallel inductor Lp with respect to the rated load resistance. However, once Lp is determined, K3 will vary with the load change during the circuit operation. Under the circumstance, K3 is not a constant anymore. Special attentions needs on K3 to be paid in the later analysis on the phase lag angle and the minimum phase-shift angle for ZVS.

1) (a) Input voltage of resonant network

The steady state analysis starts with the input voltage of the resonant network, which is also the output voltage of the full bridge inverter. Based on the assumption that the output voltage waveform of the full bridge inverter is an ideal quasi square, and then the Fourier series can be written in (4), in which Vdc is the dc bus voltage and ωs is the angular speed of the switching frequency fs

$$Vs(t) = \sum_{n=1,3}^{\infty} 4Vdc/n\pi * \sin(n\delta/2) * \sin(n\pi/2) * \sin(n\omega st) \quad (4)$$

b) Current through the series branch

The overall impedance of the resonant network is given in (5), for the definition Zn, Zs and Zp,d

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$$Z_n = Z_s + Z_{p,d} = Re(Z_n) + Im(Z_n). j \quad (5)$$

Where $Re(Z_n) = \dfrac{R_d}{[1+(1/K_3)^2*((n/k_2) - (1/n)^2)]} \quad (6)$

$$Im(Z_n)=[X_s*(n-(1/n))+(X_s/K_3{}^2)(n-(1/n))*((n/k_2)-(1/n))^2-(R_d/k_3)*((n/k_2)-(1/n))]*[1/(1/K_3)^2*((n/k_2)-(1/n))^2] \quad (7)$$

Therefore, the current through the series branch is

$$I_s(t) = \sum_{n=1,3}^{\infty}[4Vdc/n\pi * |Z_n| * \sin(n\delta/2) * \sin(n\pi/2) * \sin(n\omega_s t - \Phi_n)] \quad (8)$$

where

$$|Z_n| = \sqrt{(Re(Z_n)^2 + Im(Z_n)^2)} \quad (9)$$

$$\Phi_n = \tan^{-1}|Im(Z_n) / Re(Z_n)| \quad (10)$$

2)   Phase lag angle Φ of the resonant network

The $n^{th}(n>1)$ harmonics occupy only a small portion of series branch current, which can be obtained from the equation I_s of (8). Therefore all the $n^{th}(n>1)$ harmonics can be ignored and the first harmonic current can be used to represent the series branch current I_s to calculate the phase lag angle of the resonant network. The simulation and experiment waveforms are also verified that the current through the series branch is very close to sinusoidal. Substituting (6) and (7) into (10) under the condition of n=1 will given the phase lag angle of the first harmonic, ie. the approximate phase lag angle of the resonant network. The equation of Φ given in (11) verifies the previous qualitative analysis. If $K_2 < 1$ then Φ is positive which means the resonant network is capacitive. If $K_2 >1$ then the smaller K_3 is the more inductive then the resonant network would be

$$\Phi = \tan^{-1}|Im(Z_n) / Re(Z_n)|_{n=1} = \tan^{-1}[-(1/K_3)*((1/K_2)-1)] \quad (11)$$

3)   Minimum phase-shift Angle for ZVS

In order to achieve ZVS, the phase lag angle Φ must be large enough to satisfy the expression in (12).

$$\Phi > (\pi - \delta)/2 \quad (12)$$

Therefore $\delta > \pi - 2\Phi \quad (13)$

The minimum phase shift angle for ZVS is obtained by combining (11) and (13)

$$\delta_{min} = \pi - 2\Phi = \pi - 2*\tan^{-1}[-(1/K_3)*((1/K_2)-1)] \quad (14)$$

4)   Output voltage across the load

The output voltage across the load is given in (15) by dividing the source voltage in (4)

$$v0(t)=\sum_{n=1,3}^{\infty}[4Vdc/(n\pi * |Z_i|) * \sin(n\delta/2) * \sin(n\pi/2) * \sin(n\omega_s t - \Phi_i)] \quad (15)$$

where $|Z_i|$ and Φ_i is given from

$$\dfrac{Z_{p,load}}{Z_{p,load}+Z_s} = \dfrac{1}{Z_i} = \dfrac{1}{|Z_i|\angle\Phi i} \quad (16)$$

$$Z_i= Re(Z_i) + Im(Z_i). j \quad (17)$$

$$|Z_i| = \sqrt{(Re(Z_i)^2 + Im(Z_i)^2)} \quad (18)$$

$$Re(Z_i) =1- K_1*(n - (1/n))*((n/k_2) - (1/n)) \quad (19)$$

$$Im(Z_i) = K_1 * K_3 * (n-(1/n)) \quad (20)$$

$$\Phi_i = \tan^{-1}[Im(Z_i) / Re(Z_i)] \quad (21)$$

If resonant network is properly designed so that the THD of the output voltage is very small (< 5%), then the nth harmonics (n > 1) in (15) can be ignored. Thus the RMS value of the first harmonic determines the output voltage. The output voltage given in (22) shows that it is only a function of input voltage and controlled phase shift angle, which means it is load independent.

$$V_0 = |V_0(t)|_{n=1} = 0.9 * \sin(\delta/2) * V_{dc} \quad (22)$$

3.2 Steady state analysis of boost converter

The duty cycle of the full bridge inverter is defined in (23) where δ is the phase shift angle.

$$D = \delta / \pi \quad (23)$$

The switching frequency of the boost converter is given by $D_{boost} = (1 / m) . D \quad (24)$

$$f_{boost} = 2fs / m \quad (25)$$

where m is the gate signal constant.
The output voltage given in (22) is rewritten in (26) which includes the transformer turn ratios N defined in

$$V_0 = (1/N) * 0.9 * \sin(\delta/2) * V_{dc} \quad (26)$$

$$N = N_p / N_s \quad (27)$$

The phase shift angle given in (28), in which Rd is the load resistance, Lin is the inductance of the boost inductor and η is the efficiency.

$$\delta = \pi * \sqrt{((V_0/V_{in}) . ((V_0/V_{in}) - (0.9 * \sin(\delta/2) / N)) . (4m . L_{in} . f_s / R_d. \eta))} \quad (28)$$
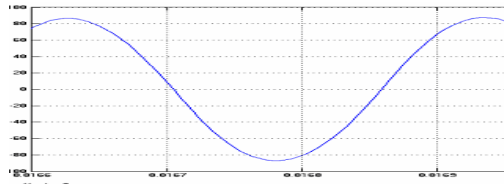
The dc bus voltage is given in

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$$V_{dc} = (V_0^2/V_{in}) \; / \; (V_0^2 - ((V_{in}^2 \cdot D^2 \cdot R_d \cdot \eta) \; / \; (4m \cdot L_{in} \cdot f_s)))) \qquad (29)$$

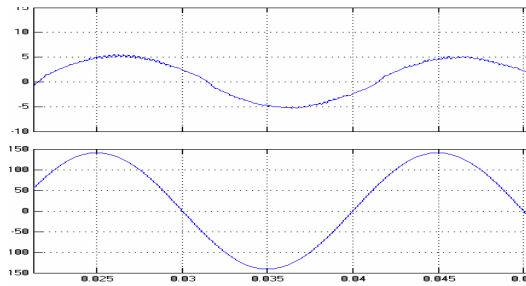In order to let the boost converter work in DCM, the expression in (30) must be satisfied

$$\frac{[0.9 * \sin(D_{\pi}/2)]^2}{D.(1-(D/m)^2)} < \frac{N^2 \cdot R_d \cdot \eta}{4 \cdot L_{in} \cdot f_s} \qquad (30)$$

SIMULATION WAVEFORMS

Output Voltage of the Load

Input Current and Voltage to the Rectifier Circuit

5 CONCLUSION

A Low frequency AC to High frequency AC inverter with unified controller has been presented. Detailed study analysis to select power circuit parameters and control circuit constraints has been given. The Inverter system has been built to convert 90-265v, 50Hz into 100 KHz ac at 250W power output.

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TORQUE RIPPLE MINIMIZATION IN DIRECT TORQUE CONTROL OF INDUCTION MACHINES

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Abstract—**Direct torque control (DTC) of an induction motor fed by a voltage source inverter is a simple scheme that does not need long computation time, can be implanted without mechanical speed sensors and is insensitive to parameter variations. In principle, the motor terminal voltages and currents are sampled and used to estimate the motor flux and torque. Based on estimates of the flux position and the instantaneous errors in torque and stator flux magnitude, a voltage vector is selected to restrict the torque and the flux errors within their respective torque and flux hysteresis bands. In conventional DTC, the selected voltage vector is applied for the whole switching period regardless of the magnitude of the torque error. This can result in high torque ripple. A better drive performance can be achieved by varying the duty ratio of the selected voltage vector during each switching period according to the magnitude of the torque error and position of the stator flux. A duty ratio control scheme for an inverter-fed induction machine using DTC method is presented in this paper. The use of the duty ratio control resulted in improved steady state torque response, with less torque ripple than the conventional DTC. Fuzzy logic control was used to implement the duty ratio controller. The effectiveness of the duty ratio method was verified by simulation using matlab SIMULINK®**

Index Terms—**Direct torque control (DTC), induction machines, fuzzy logic, torque ripple minimization.**

INTRODUCTION

BEFORE the introduction of micro-controllers and high switching frequency semiconductor devices, variable speed actuators were dominated by DC motors. Today, using modern high switching frequency power converters controlled by micro controllers, the frequency, phase and magnitude of the input to an AC motor can be changed and hence the motor's speed and torque can be controlled. AC motors combined with their drives have replaced DC motors in industrial applications due to their lower cost, better reliability, lower weight, and reduced maintenance requirement. Squirrel cage induction motors are more widely used than all the rest of the electric motors put together as they have all the advantages of AC motors and they are easy to build [1].

Controllers used in AC motor drivers are generally referred to as vector or field-oriented controllers. The field – oriented control methods are complex and sensitive to inaccuracy in the motor's parameter values [1], [2].

A simplified variation of field orientation known as direct torque control (DTC) was developed by Takahasi [3] and Depenbrock [4]. Fig. 1.1 shows a DTC of an induction motor. In direct torque controlled induction motor drives, it is possible to control directly the stator flux linkage and the electromagnetic torque by the selection of an optimum inverter switching state. The selection of the switching state is made to restrict the flux and the torque errors within their respective hysteresis bands and to obtain the fastest torque response and highest efficiency at every instant. DTC is simpler than field-oriented control and less dependent on the motor model, since the stator resistance value is the only machine parameter to estimate the stator flux.

One of the disadvantages of DTC is the high torque ripple. Under constant load in steady state, an active switching state causes the torque to continue to increase past its reference value until the end of the switching period; then a zero voltage vector is applied for the next switching period causing the torque to continue to decrease below its reference value until the end of the switching period. A possible solution to reduce the torque ripple is to use a high switching frequency; however, that requires expensive processors and switching devices. A less expensive solution is to use duty ratio control. In DTC with duty ratio control, the selected voltage vector is applied for a part of the switching period rather than the complete switching period as in conventional DTC.

By applying a nonzero voltage vector for only a portion of the switching period, and the zero voltage vector for the remainder of the period, the effective switching frequency is doubled. Therefore, over any single switching period, the torque variations above and below the average value are
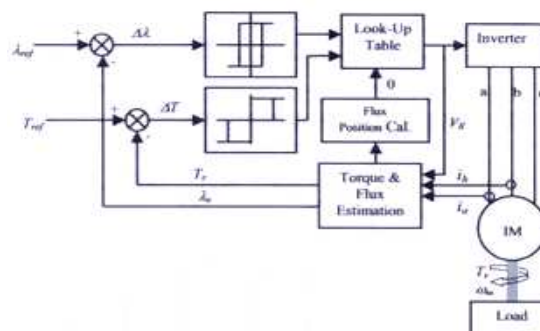

Fig. 1.1 Direct torque control scheme

smaller. Further, because the duty ratio controlled, the average stator voltage is adjusted directly. There is no need to make coarse corrections by the use of multiple switching periods with a nonzero voltage vector or a whole switching period with a zero voltage vector. The average phase voltage is adjusted more smoothly, and the overall torque ripple is reduced.

The use of a duty ratio fuzzy controller is proposed in [5].

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The aim of this paper is to verify by simulation that a DTC with a duty ratio fuzzy controller reduces the torque ripple compared to conventional DTC.

DIRECT TORQUE CONTROL OF INDUCTION MOTORS

Direct torque control was developed by Takahashi [3] and Depenbrock [4] as an alternative to field oriented control [6], [7]. In a direct torque controlled (DTC) induction motor drive supplied by a voltage source inverter, it is possible to control directly the stator flux linkage λ_s (or the rotor flux λ_r or the magnetizing flux λ_m) and the electromagnetic torque by the selection of an optimum inverter voltage vector. The selection of the voltage vector of the voltage source inverter is made to restrict the flux and torque error within their respective flux and torque hysteresis bands and to obtain the fastest torque response and highest efficiency at every instant. DTC enables both quick torque response in the transient operation and reduction of the harmonic losses and acoustic noise.

VOLTAGE SOURCE INVERTER

There are many topologies for the voltage source inverter used in DTC control of induction motors that give high number of possible output voltage vectors [8], [9] but the most common one is the six step inverter. A six step voltage inverter provides the variable frequency AC voltage input to the induction motor in DTC method. The DC supply to the inverter is provided either by a DC source like a battery, or a rectifier supplied from a three phase (or single phase) AC source. The inductor L is inserted to limit shot through fault current. A large electrolytic capacitor C is inserted to stiffen the DC link voltage.

The switching devices in the voltage source inverter bridge must be capable of being turned off and on. Insulated gate bipolar transistors (IGBT) are used because they have this ability in addition; they offer high switching speed with enough power rating. Each IGBT has an inverse parallel – connected diode. This diode provide alternate path for the motor current after the IGBT, is turned off.

Each leg of the inverter has two switches one connected to the high side (+) of the DC link and the other to the low side (-); only one of the two can be on at any instant. When the high side gate signal is on the phase is assigned the binary number 1, and assigned the binary number 0 when the low side gate signal is on. Considering the combination of status of phases a, b and c the inverter has eight switching modes (V_a V_b V_c = 000 – 111) two are zero voltage vectors V_0 (000) and V_7 (111) where the motor terminals is short circuited and the others are nonzero voltage vectors V_1 to V_6.

The dq model for the voltage source inverter in the stationary reference frame is obtained by applying the dq transformation to the inverter switching modes. The six nonzero voltages space vectors will have the orientation shown in Fig.2.1.Each vector lies in the center of a sector of

60^0 width named S1 to S6 according to the voltage vector it contains.

STATOR FLUX BASED DTC

Since the stator flux based direct torque control will be used in this paper a detailed description of the method is presented. In direct torque control fast torque response can be obtained by selecting the optimal VSI switching state if the flux magnitude is kept constant the proof is as follows [6]:
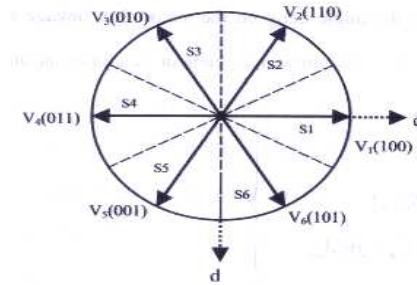

Fig. 2.1 Voltage vectors for the VSI switching states

$$T_e = (3/2) \ (P/2) \ | \lambda_{qds}| \ |i_{qds}| \ \sin \sigma_s\text{-}k_s) \qquad 2.1$$

where (σ_s-k_s) is the angle between the stator flux linkage and stator current space vectors as in Fig. 2.2. The rotor variable can be eliminated in Equations 2.2 to get Equation2.3

From Equation 2.3 the stator current is function of the stator flux linkage i.e.i_{qds} = f (λ_{qds}) substituting in Equation 2.1we can concludes T_e = g (λ_{qds}), this together with the fact that the stator flux magnitude is constant ($|\lambda_{qds}|$ =c i.e. λ_{qds} = c.exp ($j\sigma_s$)) makes the resulting equation for the electromagnetic torque a function of the motor parameters, the constant stator flux modulus ($|\lambda_{qds}|$) and the stator flux position (σ_s). Examining the proposed equation (T_e=g (c.exp ($j\sigma_s$))) it shows that the rate of change of the electromagnetic torque (dT_e/dt) is proportional to the rate of nge of the stator flux position ($d\sigma_s$ /dt), thus a fast torque response can be obtained by controlling the stator flux
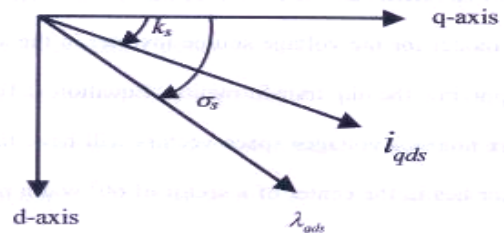

Fig.2.2 Stator flux linkage and stator current space vectors position. The stator flux linkage position can be adjusted by selecting the appropriate stator flux vector. This can be achieved considering the following

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Flux Error $d\lambda$	Torque Error dT	S1	S2	S3	S4	S5	S6
1	1	V_2	V_3	V_4	V_5	V_6	V_1
	0	V_0	V_7	V_0	V_7	V_0	V_7
	-1	V_6	V_1	V_2	V_3	V_4	V_5
0	1	V_3	V_4	V_5	V_6	V_1	V_2
	0	V_0	V_7	V_0	V_7	V_0	V_7
	-1	V_5	V_6	V_1	V_2	V_3	V_4

$$\lambda_{qds} = L_s i_{qds} + L_m i_{qdr}$$

$$\lambda_{qdr} = \frac{L_r}{L_m}(\lambda_{qds} - \sigma L_s i_{qds})$$

$$v_{qdr} = 0 = r_r i_{qdr} + p\lambda_{qdr} - jw_r \lambda_{qdr}$$

$$(\frac{r_r}{L_m} - j\omega_r \frac{L_r}{L_m})\lambda_{qds} + \frac{L_r}{L_m} p\lambda_{qds} = (\frac{r_r L_s}{L_m} - j\omega_r \frac{L_r L_s \sigma}{L_m})i_{qds} + \frac{L_r L_s \sigma}{L_m} pi_{qds}$$

The stator voltage is represented by

$V_{qds} = r_s i_{qds} + p\lambda_{qds}$ 2.4

If we assume that the stator resistance voltage drop can be neglected then Equation 2.5 is valid

$V_{qds} = p\lambda_{qds}$ 2.5

From Equation 2.5 it can be seen that the inverter voltage directly force the stator flux, the required flux locus will be obtained by choosing the appropriate inverter switching state. Thus the stator flux linkage move in space in the direction of the stator voltage space vector at a speed that is proportional to the magnitude of the stator voltage space vector. By selecting step by step the appropriate stator voltage vector, it is then possible to change the stator flux in the required way. If an increase of the torque is required then the torque is controlled by applying voltage vectors
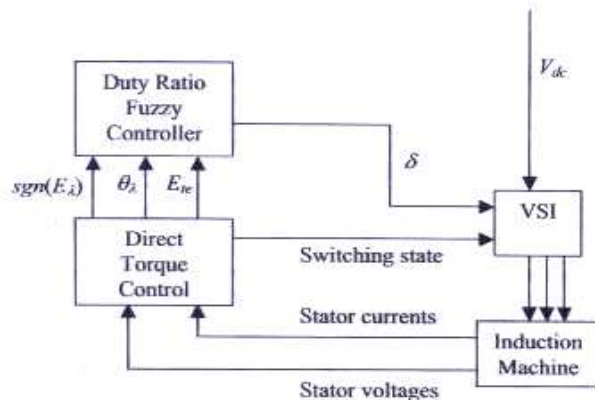

Fig. 3.1 DTC with the duty ratio fuzzy control

that advance the flux linkage space vector in the direction of the rotation. If a decrease in torque is required then zero switching vector is applied, the zero vector that minimize inverter switching is selected. In summary if the stator flux vector lies in the k-th sector and the motor is running anticlockwise torque can be increased by applying stator voltage vector V_{k+1} or V_{k+2}, and decreased by applying a zero voltage vector V_0 or V_7. Decoupled control of the torque and stator flux is achieved by acting on the radial and tangential components of the stator voltage space vector in the same directions, and thus can be controlled by the appropriate inverter switching. In general, if the stator flux linkage vector lies in the k-th sector its magnitude can be increased by using switching vectors V_{k-1} (for clockwise rotation) or V_{k+1} (for anticlockwise direction), and can be decreased by applying voltage vectors V_{k-2} (for clockwise rotation) or V_{k+2} (for anticlockwise).

The above can be tabulated in the look-up Table2.1 (Takahashi look-up table). The inputs to the look-up table are the torque error and the flux error generated by a three level hysteresis comparator and a two level hysteresis comparator respectively. The torque error is 1 if an increase in torque is required, 0 if a decrease is required. That is for anticlockwise rotation:

$dT = 1$ if $T \leq T_{ref} - |\Delta T|$ 2.6a

$dT = 0$ if $T \geq T_{ref}$ 2.6b

and for clockwise rotation:

$dT = -1$ if $|T| \leq |T_{ref}| - |\Delta T|$ 2.7a

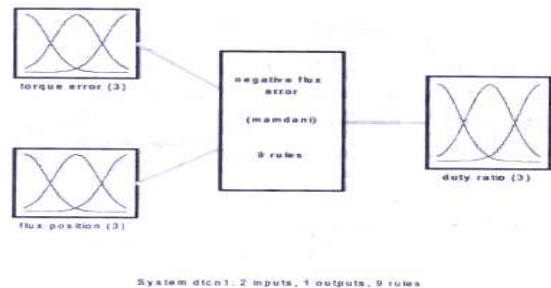$dT = 0$ if $T \leq T_{ref}$

Fig .3.2 General view of the duty ratio fuzzy controller

2.7b

The flux error is 1 if an increase in the flux is required, 0 if a decrease is required that is:

$d\lambda = 1$ if $|\lambda| \leq |\lambda_{ref}| - |\Delta\lambda|$ 2.8a

$d\lambda = 0$ if $|\lambda| \geq |\lambda_{ref}| + |\Delta\lambda|$ 2.8b

General layout of the DTC scheme is shown in Fig.1.1.

DESIGN OF THE DUTY RATIO FUZZY CONTROLLER

There are many types of fuzzy logic controller for this particular application. A Mamdani-type fuzzy logic controller, which contains a rule base, a fuzzifier, and a defuzzifier, is chosen. In this fuzzy controller, two sets of rule base are used. The first set is used when the stator flux is smaller than the reference value (positive flux error) and the second set is used when the stator flux is greater than the reference value (negative flux error). The inputs and the output of the fuzzy controller are assigned Gausian membership functions. The universe of discourse for the torque error and the duty ratio is adjusted using simulations to get optimal torque ripple reduction. Since there are three membership functions for each input, it follows that there are nine rules in each set of fuzzy rules. The presented fuzzy controller is for both forward and backward rotation, for backward rotation the absolute value of the torque error is used, and the flux position calculation is adjusted according to the rotation direction.

The emphasis in the fuzzy rule is to reduce the torque

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ripple. Generally the duty ratio is proportional to the torque error, since the torque rate of change is proportional to the angle between the stator flux and the applied voltage vector, the duty ratio depends also on the flux position within each sector. The use of two fuzzy sets is due to the fact that when the stator flux is greater than its reference value a voltage vector that advance the stator flux vector by two sectors is applied which result in a higher rate of change for the torque compared to the application of a voltage vector that advance the stator flux vector by one sector when the stator flux linkage is less than its reference value.

The duty ratio is selected proportional to the magnitude of the torque error so if the torque error is small, medium or large then the duty ratio is small, medium or large respectively. The fuzzy rules are then adjusted and tuned to reflect the effects of the flux error and position. If the torque error is medium and the stator flux lies in sector k with a magnitude greater than its reference value (negative flux error) then the voltage vector V_{k+2} is selected. If the flux position is small that means there is a large angle between the flux and the selected voltage vector that makes the selected vector more effective in increasing the torque so the duty ratio is set as small rather than medium, the fuzzy rule is stated as

If (torque error is medium) and (flux position is small) then (duty ratio is small)

If (torque error is large) and (flux position is small) then (duty ratio is medium)

Using the above reasoning and simulation to find the fuzzy rules, the two sets of fuzzy rules are summarized in Table 3.1.

SIMULATION RESULTS

Conventional DTC and DTC with the duty ratio fuzzy control for a 2-pole induction machine were simulated and compared. Constant torque and flux commands of 1.5Nm and 0.16Wb were used. The simulation was run at switching frequency of 5 kHz with a 110-V Dc bus voltage. The parameters for the three phase induction motor are

$r_s = 1.7\Omega$

$r_r = 4.3\ \Omega$

$L_s = 0.084\ H$

$L_r = 0.084\ H$

$L_m = 0.082\ H$

MATLAB$^{®}$SIMULINK$^{®}$ was used in the simulation. The induction motor was simulated using a state space model obtained by Equation 3.1

The rotor speed was simulated using Equation 3.2.

$\{(2J\ /P)\ (d\omega_r/dt)\} = T_e - T_l$ 3.2

An s-function (part of SIMULINK$^{®}$ nonlinear library) was written using C-language to simulate the induction motor

model presented by Equation 3.2.The inputs to the S-function are the stator voltage dq components and the rotor speed, the outputs of the S-function are the stator current dq components. The electric torque (T_e) was simulated using Equation 3.3.The stator flux magnitude was simulated using Equations 3.4a-c.

$T_e = (3/2)\ (P/2)\ (\lambda_{ds}\ i_{qs} - \lambda_{qs} i_{ds})$ 3.3

$\lambda_{qs} = \int (V_{qs} - r_s i_{qs})\ dt$ 3.4a

$\lambda_{ds} = \int (V_{ds} - r_s i_{ds})\ dt$ 3.4b

$\lambda_s = \sqrt{(\lambda_{qs}^2 + \lambda_{ds}^2)}$ 3.4c

The DTC controller that decides the flux sector and selects the switching vector was simulated using an S-function written using C-language, the inputs to the S-functions are the outputs of the torque and the flux hysteresis comparators and the stator flux dq components. The outputs of the S-function are the selected voltage vector dq components.

MATLAB$^{®}$ fuzzy logic toolbox was used in the implementation of the duty ratio fuzzy controller. The Graphic User Interface (GUI) included in the toolbox was used to edit the membership functions for the inputs (the torque error and the flux position), the output (the duty ratio) and the two sets of fuzzy rules summarized in Table 3.1. A Mamdani type fuzzy inference engine was used in the simulation. The membership functions and the fuzzy rules were adjusted using the simulation until an optimal torque ripple reduction was achieved. Fig 3.2 shows the general view of the fuzzy controller when the stator flux is greater than its reference value.

DTC controller performance improves as the switching frequency of the drive increases. Industrial DTC controllers such as the one introduced by ABB run at a switching frequency of 40 kHz [6]. To examine the performance of the duty ratio controller the simulation was run at switching frequency of 5 kHz.

Figs 3.3 and 3.4 show the torque response of the motor using conventional DTC and DTC with the duty ratio fuzzy control respectively for a step torque command of 1.5Nm with the drive output updated at a rate of 5kHz. The torque reaches its steady state value in less than 20ms in both controllers.

The torque ripple is 0.6Nm (approximately 1.8-1.2 Nm maximum and minimum values respectively) with the conventional DTC while with DTC with the duty ratio fuzzy control the ripple is reduced to 0.32 Nm (approximately 1.62-1.38 Nm maximum and minimum values respectively, neglecting the undershoot in the torque value at the beginning of each voltage sector).

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To implement the duty ratio fuzzy control, a look-up table was used for the implementation of the fuzzy controller. Each flux position sector (Fig.2.2) is divided into three equal non-overlapped subsections: small, medium and
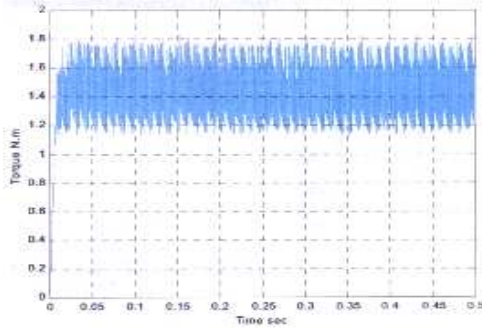

Fig 3.3   Electric torque using conventional DTC at 5 kHz
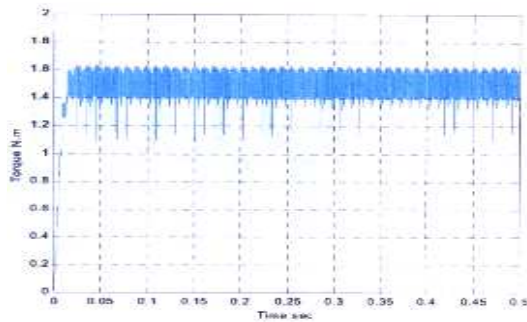

Fig 3.4   Electric torque using DTC with the duty ratio fuzzy control at

large; similarly the universe of discourse for the torque error is divided into three non-overlapped subsections: small, medium and large. The duty ratio values are shown in Table 3.2; they are based on the MATLAB fuzzy logic toolbox duty ratio controller used previously in this topic the duty ratio output for each inputs membership's combination is tuned by simulation to get optimal torque ripple reduction.

The value of the switching frequency in the DTC drives is inversely proportional to the width of the torque and flux hysteresis controllers. In order to get a torque response that has an average value equal to the reference value the

Table 3.2 Duty ratio look-up table

Flux Error	Torque error $dT=1$ Flux Angle	Small	Medium	Large
Negative $d\lambda=0$	Small	0.55	0.55	0.65
	Medium	0.55	0.65	0.90
	Large	0.55	0.65	0.90
Positive $d\lambda=1$	Small	0.55	0.65	0.90
	Medium	0.55	0.65	0.90
	Large	0.65	0.90	0.90

switching frequency must be high enough and variable to keep the torque from decreasing deep below its reference value. Since a fixed switching frequency is used in this paper the variations of the torque above and below its reference value is decided by the time delay. This usually results in a torque response that has an average value less than the reference, multiplying the torque reference value by a proportional gain can rectify this. In addition the DTC

induction motor drives are usually used in applications that have an open loop speed control such as cranes and locomotives where the operator can adjust the torque reference value.

CONCLUSION

The theoretical claim that duty ratio control can reduce torque ripple in DTC induction motor drives was verified by simulation. The use of fuzzy logic control gave satisfactory results and reduce the computation burden by avoiding unnecessary complex mathematical modeling of the nonlinear systems. By using duty ratio control a specific motor performance can be achieved at lower switching frequency compared to the conventional DTC, which in turn increases the efficiency of the drive by reducing losses due to currents and flux harmonics.

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A NOVEL CONTROL TECHNIQUE FOR COMPENSATION OF LINE CURRENT IN UTILITY SIDE OF UPS

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Abstract: **The Single-phase Pulse Width-Modulated (PWM) rectifiers have been the source of interest in the literature over recent years. Tougher regulations on the harmonics generated by electronic equipment, together with the lower cost of control circuits and power semiconductors, have made PWM boost rectifiers more attractive. Electric power utilities are also demonstrating a trend for restricting the harmonic pollution of the utility system. It is for these reasons that this project is concerned with rectifier circuit topology that control the rectifier input current wave shape to achieve unity power factor operation and very low current distortion levels.**

The PWM AC/DC converter has been increasingly employed in recent years owing to its advanced features including sinusoidal input current at unity power factor and high quality dc output voltage with a filter capacitor of small size. The control of this converter is done by using (DSP) TMS320LF2407A since due to the low cost and advanced features such as built-in Pulse Width Modulator (PWM) units, and on-chip Analog-to-Digital (A/D) converters compared with traditional analog controllers.

Index Terms— **AC–DC Converters, Harmonic Reduction, Power Factor Correction (PFC), Power Quality, Single Stage Converters, Uninterruptible Power Supply Power Supplies.**

I. INTRODUCTION

Single-phase AC-DC converters are being used as front-end rectifiers for a variety of applications such as UPS, due to the advantages of high efficiency and power density. These classical converters, however, draw-non-sinusoidal input AC currents leading to low input power factors and injection of harmonics into the utility lines. Research in improved power quality utility interface has gained importance due to stringent power quality regulation and strict limits on Total Harmonic Distortion (THD) of input current placed by standards such as IEC 61000-3-2 and IEEE 519-1992. This has led to consistent research in the various techniques for power quality improvement. They are classified into passive and active techniques for input current wave shaping has highlighted their inherent drawbacks. Passive filters have the demerits of fixed compensation, large size and resonance whereas the use of active filters is limited due to added cost and control complexity.

The research into switch mode power factor corrected AC-DC converters has been in two directions namely buck and boost type topologies. The Buck type topology can provide variable output voltage but results in increase in input current THD. The design of input filters for power factor improvement is complex. On the other hand the boost type converter generates DC voltage, which is higher than the input AC voltage. However, the input current in these converters flows through the inductor and therefore can easily be actively wave-shaped with appropriate current mode control.

The preferred power circuit configuration of single-phase boost converter is the most popular and economical power factor converter consisting of diode bridge rectifier with step-up chopper. Problems like low efficiency and reduced reliability has made the use of Voltage Source Converter (VSC) topology with reduced input current THD than other topologies. The single-phase Voltage Source Converter (VSC) topology with bi-directional power flow capability finds application in drives with regenerative breaking, line interactive Uninterruptible Power Supply (UPS), static VAR compensator and battery energy storage system.

II. ANALYSIS OF UPS SYSTEMS

Uninterruptible Power Supplies (UPS's) provide electric power for critical functions and equipment [1] when the quality of the normal supply, i.e. utility power, is not adequate or fails entirely. With the rapid growth in the utilization of data processing systems, life care medical equipment, the demand for high quality uninterruptible power is required. These electrical loads are nonlinear, and generate harmonics. The simplest line-commutated converters use diodes to transform the electrical energy from AC to DC [2]. The main disadvantage of these naturally commutated converters is the generation of harmonics and reactive power.
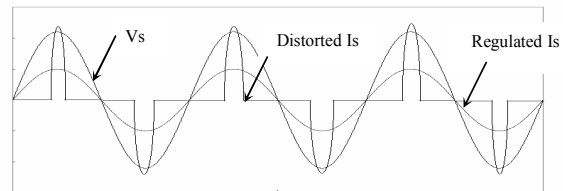

Fig.1 Waveform with input voltage, distorted current and regulated current

Due to that the degree of waveform distortion increases, as shown in the Figure1. Harmonics have a negative effect on the operation of the electrical system. Therefore, harmonic filtering techniques must be applied in order to maintain a high quality in phase line current.

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III. COMPENSATION OF VOLTAGE AND CURRENT

One basic and typical method to reduce input current harmonics is the use of multipulse connections based on transformers with multiple windings. An additional improvement is the use of passive power filters. The active filters have been introduced to reduce the harmonics injected to the mains.

The other, different way of harmonics reduction is the so called Power Factor Correction (PFC)[3]. In these converters, power transistors are included in the power circuit of the rectifier to change actively the waveform of the input current, reducing the distortion. These circuits reduce harmonics and consequently they improve the power factor, which is the origin of their generic name of PFC. Pulse-width modulated AC to DC voltage source converters, compensates the source current and maintains better input power factor.

IV. THE OPERATION OF PROPOSED PWM

The Figure 2(a) shows the power circuit of the fully controlled single-phase PWM rectifier in bridge connection, which uses four transistors with antiparallel diodes to produce a controlled DC voltage Vo. For an appropriated operation of this rectifier, the output voltage must be greater than the input voltage, at any time $(V_0 > V_s)$ [2]. This rectifier can work with two (bipolar PWM) or three (unipolar PWM) levels.

The possible combinations are
1. Switch T_1 and T_4 are in ON state and T_2 and T_3 are in OFF state, (Fig.2-b)).
2. Switch T_1 and T_4 are in OFF state and T_2 and T_3 are in ON state, (Fig. 2-c))
3. Switch T_1 and T_3 are in ON state and T_2 and T_4 are in OFF state, or T_1 and T_3 are in OFF state and T_2 and T_4 are in ON state, (Fig. 2-d).
The inductor voltage can be expressed as
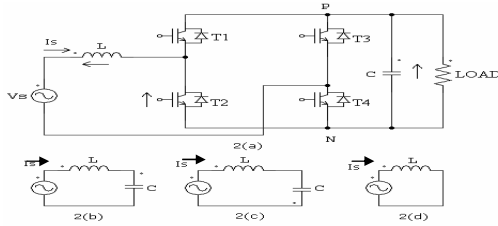
$$V_L = L \, di_s / dt = V_s (t) - kV_o \qquad ..(1)$$

Fig. 2. Operation of the PWM rectifier

Where   k=1, -1 or 0.

If k=1, then the inductor voltage will be negative, so the input current i_s will decrease its value.
If k=-1, then the inductor voltage will be positive, so the input current i_s will increase its value.
Finally, if k=0 the input current increase or decrease its value depending of V_s. This allows for a complete control of the input current.

V. CONTROL SCHEME

The objective of the control scheme of the boost converters is to regulate the power flow ensuring tight output voltage regulation as well as unity input power factor [1] The cascaded control structure shown in Fig.3.
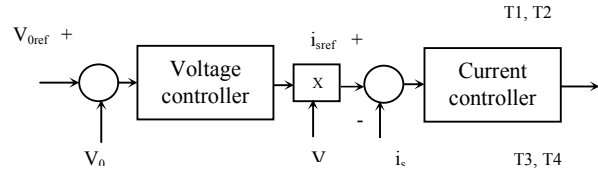

Figure.3 Control scheme for the proposed boost converter.

A. Control of the DC-Link Voltage

The control of the dc-link voltage requires a feedback control loop. The dc voltage V_o is compared with a reference V_{oref}, and the error signal (e) obtained from this comparison is used to generate a template waveform[4]. The template should be a sinusoidal waveform with the same frequency of the mains supply. This template is used to produce the PWM pattern, and allows controlling the rectifier.

B. Voltage source current controlled PWM rectifier

This control includes a voltage controller, typically a Proportional-Integrative (PI) controller, which controls the amount of power required to maintain the DC-link voltage constant. The voltage controller delivers the amplitude of the input current. For this reason, the voltage controller output[2] is multiplied by a sinusoidal signal with the same phase and frequency than V_s, in order to obtain the input current reference, i_{sref}. The inductor current is forced to track its reference current using current controller, which generates appropriate gating signals for the active device(s). This controller can be a hysteresis or a linear controller with a PWM-modulator.

VI. DESIGN CRETERIA

A. Power Circuit Design

Input Voltage $[V_s]$ =230V
Line Frequency [F] =50Hz
Required Output Voltage $[V_o]$=400Vdc
IGBT Ratings =1200V, 60A
The diodes are used a high speed, high voltage type with 25ns reverse recovery, $600V_{DC}$ breakdown & 8A forward current ratings.

B. Inductor Design

Inductor value [6] selection begins with the peak current of the sinusoidal. The maximum peak current ($I_{line (pK)}$) at the minimum line voltage and is given by [5],

$$I_{line (pk)} = \frac{\sqrt{2} * p}{V_{in (min)}} \qquad ..(2)$$

Where,   P is the actual power in watts
$V_{in (min)}$ is minimum line Input voltage in volts

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The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the Duty factor (D)[9] at the input voltage

$$D = \frac{V_o - V_{in}}{V_0}$$ ..(3)

$$L = \frac{V_m * D}{f_s * \Delta l}$$ ..(4)

Where, V_{in} is the Input voltage in volts
V_0 is the Output voltage in volts and
V_m is the Maximum voltage in volts

C. DC-Link Capacitor Design

Transient changes in the instantaneous power absorbed by the load generate voltage fluctuations in the DC voltage. The amplitude of these voltage fluctuations can be controlled effectively with an appropriate DC capacitor value.

$$C = \frac{1}{\Delta V} \int_{t_1}^{t_2} i_c(t)\, dt$$ ..(5)

The factors involved in the selection of the capacitor, the total current through the output capacitor is the RMS value of the switching frequency ripple current [7], the hold-up time and the second harmonic of the line current.

$$C_0 = \frac{2 * P_{out} * \Delta t}{V_0^2 - V_{0(min)}^2}$$ ..(6)

Where P_{out} is the Output voltage in watts
Δt is the Small time different
V_0 is the Maximum output voltage in volts
$V_{0(min)}$ is the Minimum output voltage

VII. SIMULATION RESULTS

A. Observation of 1KVA UPS

a) Utility Side Voltage and Current

The input voltage and source current thus obtained from the 1KVA traditional UPS is 214.8Vand 8.55A.
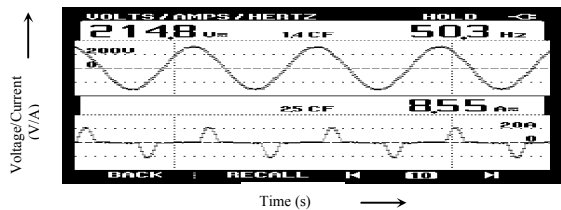

Fig 4. Input voltage and distorted current of UPS

b) Harmonic Level of source current

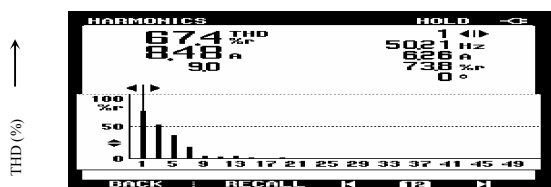The harmonic profile that 1 KVA UPS is also taken and it is about 67.4%

Order of Harmonics

Fig. 5.Harmonics level of Distorted Current in UPS

c) Input Power Factor

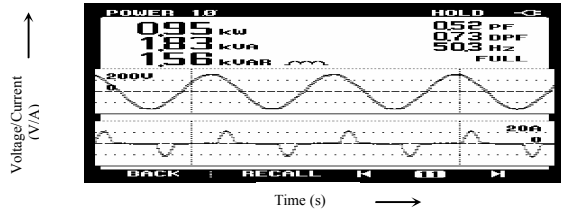The reduced power factor from a traditional UPS is about 0.52 and is given in the Figure 6.

Fig 6.Power Factor of the UPS

B.Reduction of Harmonics through PWM boost rectifier

The control circuit for the proposed PWM boost rectifier is shown below. It is simulated using the PSIM
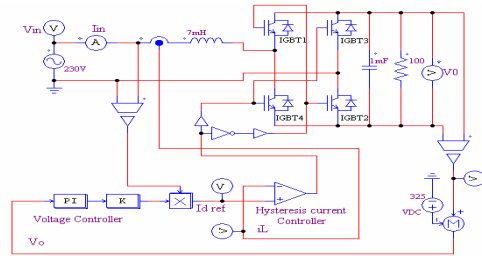

Fig 7. Control Circuit of Boost Rectifier

for 230V, 50Hz.This circuit uses the voltage controller and hysteresis band current controller for compensation of source current and also the output voltage.

C.Regulated Source Current

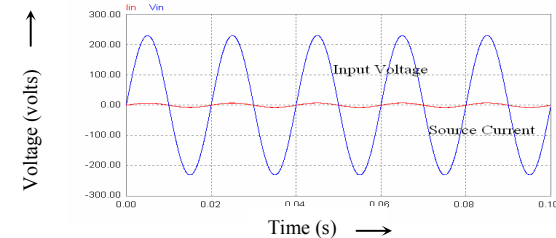The regulated input current is shown in the Figure 8..

Fig. 8. Input voltage and Source current after compensation

The level of harmonics is limited according to the standards.
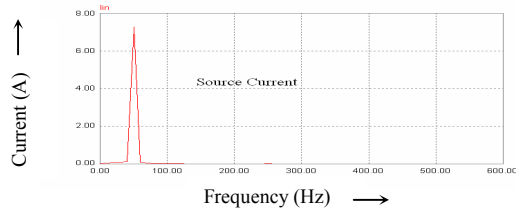
D.HarmonicProfile

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Figure 9. Harmonic Profile Compensated Current
The source current is compensated and the order harmonics in the utility side is reduced.
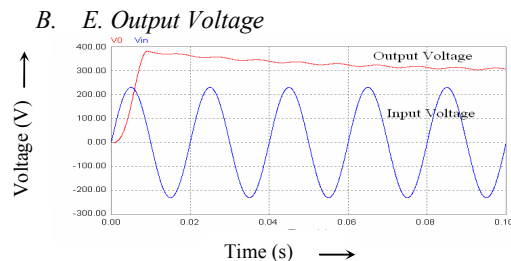
B. E. Output Voltage

Figure 10. Boosted output voltage

The output voltage that is resulted after the simulation is 325V dc, which is given as in Figure 10.

VIII. CONCLUSION

The proposed method thus compensates the source current for UPS under nonlinear load conditions. It improves the input power factor and also maintains the output DC link voltage constantly under varying load conditions. Strict harmonic limit such as IEC 1000-3,IEEE 519 [8]are maintained as said in the standards. To meet the limits and come up with growing AC/DC power supply markets, the PFC stage is currently required. The analog PFC control is the current industry choice but this type of control is not flexible. Several implementation aspects of digital control of power factor correction (PFC) stage of have been explored with low cost digital controllers such as TMS320C2407A[5]. They guarantee higher bandwidth and higher switching frequency for AC/DC power supply.

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HIGH POWER-FACTOR SOFT-SWITCHED BOOST CONVERTER

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Abstract - **A novel implementation of the High-Power-Factor (HPF) boost converter with active snubber is described. The snubber circuit reduces the reverse-recovery-related losses of the rectifier and also provides zero-voltage switching for the boost switch and zero-current switching for the auxiliary switch. The switching losses are reduced. The proposed technique improves the efficiency.**

I. INTRODUCTION

In modern power applications a reliable ac-dc power converter is required. For power applications above 250 W, a two stage process is usually used to provide an isolated and regulated dc output voltage. The first stage of such a converter is a rectifying stage that converts the ac voltage to dc and the second stage is an isolated dc-dc converter that converts the dc input voltage into a regulated dc voltage at the output. One of the most important functions of the rectifying stage is to provide Power Factor Correction (PFC) of the input current in order to minimize the harmonics in it.

The reasons why boost topology is preferred as a PFC pre-regulator are:

The input current in the boost topology has the smallest current ripple. Thus the filtering requirements for this topology are the lowest resulting in a small filter.

The boost converter topology has been extensively used in various ac/dc and dc/dc applications. In fact, the front end of today's ac/dc power supplies with power-factor correction (PFC) is almost exclusively implemented with boost topology. Also, the boost topology is used in numerous applications with battery-powered input to generate a high output voltage from a relatively low battery voltage. As a result, in recent years, significant effort has been made to improve the performance of high-power boost converters. The majority of these development efforts have been focused on reducing the adverse effects of the reverse-recovery characteristic of the boost rectifier, especially for the conversion efficiency and Electro Magnetic Compatibility (EMC).

Generally, the reduction of reverse-recovery-related losses and EMC problems require that the boost rectifier is "softly" switched off, which is achieved by controlling the turn-off rate of its current [1]. So far, a number of soft-switched boost converters and their variations have been proposed [2]. All of them use additional components to form passive snubber or active snubber circuits that control the turn-off di/dt rate of the boost rectifier. The passive snubber approaches in[4] use only passive components such

as resistors, capacitors, inductors, and rectifiers, whereas active snubber approaches employ one or more active switches.

Although passive lossless snubbers can marginally improve efficiency, their performance is not good enough to make them viable candidates for applications in high-performance PFC circuits. Generally, they suffer from increased component stresses and are not able to operate with the soft switching of the boost switch, which is detrimental in high-density applications that require increased switching frequencies.

The simultaneous reduction of reverse-recovery losses and the soft switching of the boost switch can be achieved by active snubbers. So far, a large number of active snubber circuits have been proposed [5]. The majority of them offer the soft turn off of the boost rectifier, ZVS of the boost switch, and "hard" switching of the active-snubber switch [5]. However, a number of active-snubber implementations feature soft switching of all semiconductor components, i.e., in addition to the soft turn off of the boost rectifier, the boost switch and the active-snubber switch operate with ZVS or ZCS [10].

In this paper, a novel implementation of the soft-switched boost converter with active snubber is described.

The major feature of these circuits is the soft switching of all semiconductor components. Specifically, the boost rectifier is switched off with a controlled turn-off di/dt rate, the boost switch is turned on with ZVS, and the auxiliary switch in the active snubber is turned off with ZCS. As a result, switching losses are reduced, which has beneficial effects on the conversion efficiency and EMC performance.

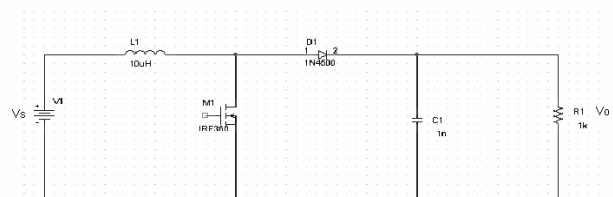## II. BASIC BOOST CONVERTER

Fig 1. Boost Converter

The Fig 1 shows the circuit of a boost converter. The output voltage is greater than the input voltage. Hence the name boost converter. It increases the voltage without a transformer. It has high efficiency. The boost converter topology has been extensively used in various ac/dc and dc/dc applications. In fact, the front end of today's ac/dc

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power supplies with power-factor correction (PFC) is almost exclusively implemented with boost topology. Also, the boost topology is used in numerous applications with battery-powered input to generate a high output voltage from a relatively low battery voltage.

$$V_O = V_S /1\text{-}k$$

V_O = output voltage
V_S = supply voltage
k = duty cycle
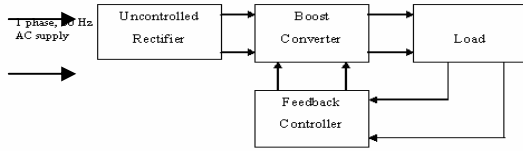
III.SOFT-SWITCHED BOOST CONVERTER

Fig 2 Block Diagram

The Fig 2 shows the block diagram of a boost converter. The single phase ac supply is given to an uncontrolled rectifier. To reduce the ripple in the dc output voltage a large filter capacitor is used at the rectified output.

The out put is given to the boost converter and then given to the load. To make the output voltage stable it is given to a feed back controller.
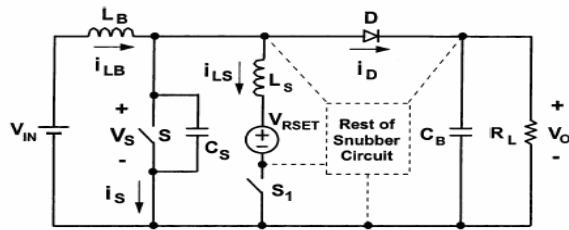

Fig 3 Soft switched Boost Converter (conceptual circuit)

Fig. 3 shows a conceptual implementation of the proposed soft-switched boost converter with ZCS of auxiliary switch S_1. After auxiliary switch S_1 is turned on, snubber inductor L_S controls the rate of change of current in the rectifier to reduce reverse- recovery-related losses in boost rectifier D. In addition, since the auxiliary-switch current cannot increase immediately because of snubber inductor Ls, the auxiliary switch turns on with ZCS. During the period when auxiliary switch S_1 is turned on, snubber inductor Ls and output capacitance Cs of boost switch S form a resonant circuit, hence the voltage across boost switch S falls to zero by resonant ringing. As a result, boost switch S turns on when its drain-to-source voltage is zero.

To reset the snubber inductor current, it is necessary to provide reset voltage V_{RESET} in the loop consisting of snubber inductor Ls and conducting switches S and S1, as shown in Fig. 3.
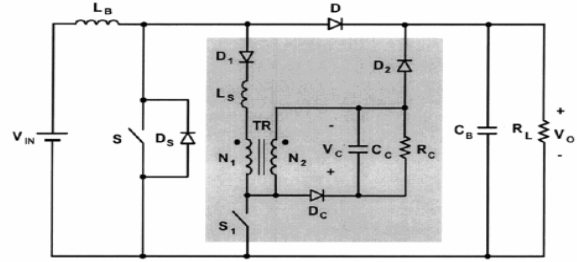

Fig 4 Proposed Soft-switched Boost Converter

The proposed implementation of the soft-switched boost circuit is shown in Fig. 4. The circuit consists of voltage source V_{IN} , boost inductor ,L_B , boost switch S, boost rectifier D, energy-storage capacitor C_B , load R_L, and the active snubber circuit formed by auxiliary switch S_1 , snubber inductor L_S, transformer TR, blocking diode D_1 , and clamp circuit $R_C - C_C - D_C.$
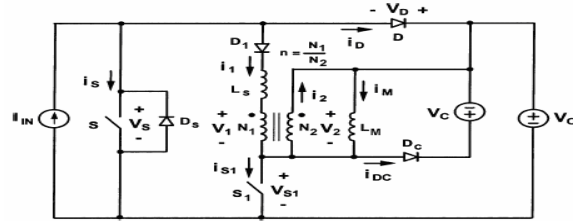

Fig 5 Simplified circuit diagram

To facilitate the explanation of the circuit operation, Fig 5 shows a simplified circuit diagram of the circuit in Fig. 4. In the simplified circuit, energy-storage capacitor CB and clamp capacitor CC are modeled by voltage sources VO and VC, respectively, by assuming that the values of CB and CC are large enough so that the voltage ripples across the capacitors are small compared to their dc voltages. In addition, boost inductor LB is modeled as constant current source iIN by assuming that inductance is LB large enough so that during a switching cycle the current through it does not change significantly.

Also, transformer TR is modeled by magnetizing inductance LM and an ideal transformer with turns ratio n =N1 /N2. Since the leakage inductance of transformer TR is connected in series with snubber inductor LS, it is not separately shown in Fig. 5. Finally, it is assumed that in the on state, semiconductors exhibit zero resistance, i.e., they are short circuits. However, the output capacitance of the switches, as well as the junction capacitance and the reverse-recovery charge of the rectifier are not neglected in this analysis.

Prior to turn on of switch S1 at t=T0, switches S and S1 are open and entire input current iIN flows through boost rectifier D into load RL. After switch S1 is turned on at t=T0, current i1 starts flowing through winding N1 of transformer TR, inducing the flow of current i2 in winding N2. Because, during this stage, output voltage V_0 is impressed across winding N_2, transformer winding voltages v_1 and v_2 are given by

$$v_2 = V_0 \quad \text{and}$$

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$$v_1 = \frac{N_1}{N_2}V_0 = nV_0$$

Where it is required n=NI/N2<1 for proper operation of the circuit.

Since v_1 is constant, voltage applied across snubber inductor L_S is also constant so that current i_1 increases linearly.

As current linearly increases, boost rectifier current linearly decreases at the same rate since the sum of i_1 and i_D is equal to constant input current i_{IN}. Due to a stored charge in the rectifier, the rectifier current continues to flow in the negative direction.

Generally, for a properly selected snubber inductor and turns ratio n, this reverse-recovery current is substantially reduced compared to the corresponding current in a circuit without the boost rectifier turn-off rate control. After the stored charge is removed from the rectifier, the rectifier regains its voltage blocking capability. During this stage, junction capacitance of boost rectifier is charged and output capacitance of boost switch discharged through a resonance between parallel connection of and with snubber inductor.

If a turn's ratio of n< 0.5 is selected, output capacitance of boost switch can be always discharged to zero regardless of the load and line conditions. Once the capacitance is fully discharged, current i_1 continues to flow through the antiparallel diode of boost switch since the voltage v_1 is impressed in the negative direction across snubber inductor L_S, current i_1 starts linearly decreasing.

To achieve ZVS of boost switch S, it is necessary to turn on boost switch S before its current becomes positive. i.e., while current i_S flowing through the antiparallel diode of switch S.

With boost switch S turned on, boost-switch current iS continues to flow through closed switch S after it becomes positive. The current i1 continues to decrease linearly toward zero, while boost-switch current continues to linearly increase at the same rate. When current i1 becomes zero at, boost-switch current reaches iIN so that the entire input current flows through boost switch. At the same time, auxiliary switch only carries a magnetizing current. If the magnetizing inductance of the transformer is made high, the magnetizing current can be minimized, i.e., it can be made much smaller than input current so that auxiliary switch can be turned off with virtually zero current.

When auxiliary switch is turned off with near ZCS, magnetizing iM current begins charging output capacitance COSS1 of auxiliary switch. When voltage VS1 across auxiliary switch reaches clamp voltage VO+VC , where VC is the voltage across clamp capacitor CC , magnetizing current is commutated into voltage source VC through clamping diode DC , which models the clamp circuit. The switching and conduction losses of clamping diode are negligible because magnetizing current is designed to be very small. The negative voltage VC resets the magnetizing current until magnetizing current becomes zero.

After transformer TR is reset, the boost switch is opened and the input current is commutated from switch S to its output capacitance C_{OSS}. Due to C_{OSS} charging with constant

current i_{IN}, voltage v_S is increasing linearly until it reaches V_O at and input current i_{IN} is instantaneously commutated to boost rectifier. Auxiliary switch S1 is turned on again.

It should be noted that in the previous analysis the junction capacitance of diode was neglected since it has no significant effect on the operation of the circuit. In fact, this capacitance plays a role only during a brief interval after current i1 reaches zero. Specifically, the junction capacitance of diode D1 and snubber inductor resonate creating small negative current i1 that makes auxiliary-switch current iS1 flow in the negative direction through the antiparallel diode of switch S1. Due to the conduction of its antiparallel diode, auxiliary switch voltage vS1 does not immediately start to increase after switch S1 is turned off, i.e., shortly after iS1 falls to zero. Instead, the rise of vS1 is briefly delayed until the current through the antiparallel diode resonates back to zero. This delay has no tangible effect on the operation or the performance of the circuit.

In summary, the major feature of the proposed circuit is the soft-switching of all semiconductor devices. Specifically, boost switch is turned on with ZVS; auxiliary switch is turned off with ZCS, and boost diode D is turned off with a controlled turn-off rate. As a result, the turn-on switching loss of the boost switch, the turn-off switching loss of the auxiliary switch, and reverse-recovery-related losses of the boost rectifier are greatly reduced, which minimizes the overall switching losses and, therefore, maximizes the conversion efficiency. In addition, soft-switching has a beneficial effect on EMI that may result in a smaller volume input filter.

Due to ZVS of the boost switch, the most suitable implementation of the circuit in Fig. 4 is with the boost switch consisting of a metal oxide semiconductor field effect transistor MOSFET) device or a parallel combination of MOSFETs. Similarly, due to the zero-current turn off of the auxiliary switch, the circuit in Fig. 4 is suitable for an insulated gate bipolar transistor (IGBT) auxiliary switch. Auxiliary switch is turned on while voltage across it is equal to output voltage VO . Despite this "hard" turn on of auxiliary switch, there is no significant performance penalty, since the output capacitance of IGBTs is much smaller than that of MOSFETs.

In fact, since the overall switching loss of IGBTs is dominated by its turn-off loss due to the current tailing effect, the optimum switching strategy of IGBT is soft turn off, rather than soft turn on. Moreover, even an implementation with an IGBT boost switch is possible provided that a turn-off snubber capacitor is connected across the IGBT boost switch to reduce the turn-off loss due to the IGBTs current-tail effect. In this case, an IGBT with a co-packaged antiparallel diode or an external diode must be used. In the proposed circuit, the voltage and current stress on boost switch and boost rectifier are identical to the corresponding stress in the conventional boost converter without a snubber.

IV. SIMULATION CIRCUIT AND RESULT

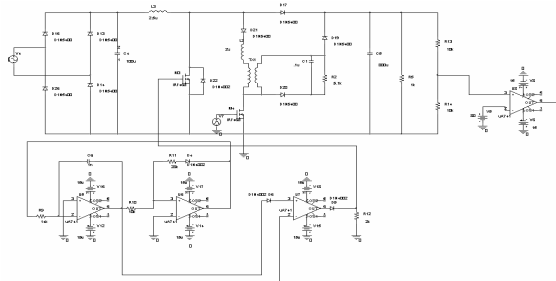*Proceedings of Third National Conference-PCID 2007*
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Fig 6 Closed loop Boost Converter
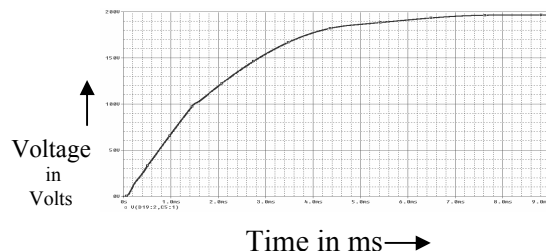

Voltage in Volts

Time in ms →

Fig 7 Closed loop Output

V CONCLUSION

A novel implementation of the PFC boost converter with an active snubber that can achieve soft-switching of all semiconductor devices in the power stage has been introduced. By using an active snubber that consists of an auxiliary switch, a snubber inductor, and a reset circuit, boost switch is turned on with ZVS, auxiliary switch is turned off with ZCS, and boost diode is turned off softly using a controlled rate. As a result, the turn-on switching losses in the boost switch, the turn-off switching loss in the auxiliary switch, and reverse-recovery- related losses in the boost diode are greatly reduced, which maximizes the conversion efficiency.

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Z-SOURCE INVERTER FOR UPS APPLICATION

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Abstract- **This project proposes an impedance-source inverter and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. The Z-source converter employs a unique impedance network to couple the converter main circuit to the power source. The Z-source converter overcomes the conceptual and theoretical barriers and limitations of the traditional voltage-source converter and current-source converter and provides a novel power conversion concept. The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. To describe the operating principle and control, this paper focuses on an Uninterrupted Power Supply (UPS) applications.**

I INTRODUCTION

Traditionally there are two inverters available. These are voltage source inverters and current source inverters. Each inverter has two switches in the main circuit. These switches are power switches with anti-parallel diodes. These diodes provide bidirectional current flow and reverse voltage blocking capability. Traditional inverters have following limitations .They can operate either as a boost or buck inverter and cannot be a buck-boost inverter. Their output voltage range is limited to either greater or smaller than the input voltage. Their main circuit is not being interchangeable. In other words neither the voltage source inverter can be used for the current source inverter nor vice versa. They are vulnerable to EMI noise in terms of reliability. The above limitations can be rectified in impedance source inverter to get higher efficiency. This concept can be applied to all AC to DC, AC to AC, DC to DC, DC to AC power conversions [4].

II. TRADITIONAL SOURCE INVERTERS

Traditional source inverters are voltage source inverters and current inverters. The output of voltage source inverter is a stiff dc voltage supply, which can be a battery or a controlled rectifier (both single phase and single phase voltage source inverter). The switching device can be a conventional MOSFET, thyristor or a power transistor.

*Traditional source inverters:-*Traditional source inverters are voltage source inverters and current inverters. The output of voltage source inverter is a stiff dc voltage supply, which can be a battery or a controlled rectifier (both single phase and single phase voltage source inverter). The switching device can be a conventional MOSFET, thyristor or a power transistor. Voltage source inverter is one in which the dc source has small or negligible impedance. In other words a voltage source has stiff dc source voltage at its input terminals. A current source- fed inverter or current source inverter is fed with adjustable dc current source. In current source inverter, output current waves are not affected by the load.

Voltage source inverter [VSI]:-The traditional voltage-source inverter input is a dc voltage source supported by a relatively large voltage source can be a battery, fuel-cell stack, diode rectifier, and/or capacitor. Four switches are used in the main circuit; each in traditionally bidirectional current flow and unidirectional voltage blocking capability. The V-source inverter is widely used however; it has the following conceptual limitations [5].

*Limitations of voltage source inverter:-*The V-source inverter is buck (step down) inverter for dc-to-ac power conversion. For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost (step up) stage is needed to obtain a desired ac output [1]. The additional power converter stage increases system cost and lowers efficiency.

The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a shoot-through would occur and destroy the devices. The shoot-through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the inverter to the inverter's reliability. Dead time to block both upper and lower devices has to be provided in the V-source inverter, which causes waveform distortion, etc.[1] An output LC filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity.

Current source inverter [CSI]*:-*The traditional current-source inverter input is a dc current source feeds by the main converter circuit. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel-cell stack, diode rectifier, or thyristor converter. Four switches are used in the main circuit; each is traditionally composed of a semiconductor switches device with reverse block capacity such as gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking. However, the current -source inverter has the following conceptual barriers and limitations.[2]

*Limitations of current source inverter:-*The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. For applications where a

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wide voltage range is desirable, an additional dc-dc boost stage is needed. The additional power conversion stage increases system cost and lowers efficiency. [1]At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open-circuit problem by EMI noise's misgating-off is a major concern of the converter's reliability [3].overlap time for safe current commutation is needed in the I-source converter, which also causes waveform distortion. The main switches of the I-source inverter have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBT). This prevents the direct use of low-cost and high-performance IGBT modules.

Limitations in both voltage and current source inverter:- Their obtained output voltage range is limited to either greater or smaller than the input voltage [2]. Their main circuit cannot be interchangeable. In other words, neither the V-source inverter main circuit can be used for the I-source inverter nor vice versa. They are vulnerable to EMI noise in terms of reliability [5].

III. IMPEDANCE SOURCE INVERTER

Block diagram of impedance source inverter- To overcome the above limitations of the traditional V-source and I-source inverter, this thesis deals an impedance-source inverter and its control method for impedance dc-to-ac power conversion. This thesis also deals with how to overcome the limitations of voltage source inverter and current source inverter
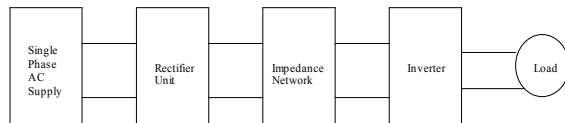

Figure 1 Block diagram of Impedance Source Inverter

The proposed impedance source inverter block diagram is shown in figure 1. It is consists of rectifier unit, Impedance network, single phase inverter and load. AC voltage is rectified to DC voltage by the rectifier. The rectified output DC voltage is fed to the network

*Advantages of the impedance source network:-*The impedance source inverter concept can be applied in all ac-ac, dc-dc, ac-dc, dc-ac power conversion. The output voltage range is not limited. The impedance source inverter is used as a buck-boost inverter. The impedance source inverter does not affect the electro magnetic interference noise. The impedance source inverter cost is low. The impedance source inverter provides the buck-boost function by two stage power conversion.

Table 1. Comparison of VSI, CSI and ZSI

Current Source Inverters	Voltage Source Inverter	Impedance Source Inverters
1. As inductor is used in the d.c link, the source Impedance is high. It acts as a constant current source.	As capacitor is used in the d.c link, it acts as a low impedance voltage source.	As capacitor and inductor is used in the d.c link, it acts as a constant high impedance voltage source.
2. A current source inverter is capable of withstanding short circuit across any two of its output terminals. Hence momentary short circuit on load and mis-firing of switches are acceptable.	A VSI is more dangerous situation as the parallel Capacitor feeds more powering to the fault. This is also used in a buck or boost operation of inverter.	In ZSI mis-firing of the switches are also acceptable sometimes. This is used in both buck and boost operation of Inverter.
3. This is used in only buck or boost operation of inverter.	The main circuit cannot be Interchange able here also.	Here the main circuits are Interchange able
4.The main circuits cannot be interchangeable.	It is affected by the EMI noise	It is less affected by the EMI noise.
5. It is affected by the EMI noise.	It has a considerable amount of harmonic distortion	Harmonics Distortion is low
6. It has a considerable amount of harmonic distortion	Power loss is high	Power loss should be low
7. Power loss should be high because of filter	Efficiency should be low because of high power loss	Higher efficiency because of less power loss
8.Lower efficiency because of high power loss		

IV. ANALYSIS AND DESIGN OF THE IMPEDANCE NETWORK

Equivalent circuit, operating principle, and control:-
The unique feature of the impedance-source inverter is that the output ac voltage can be any value between zeros to infinity regardless of the DC voltage. That is, the impedance-source inverter is a buck-boost inverter that has a wide range of obtainable voltage. The traditional V-and I-source inverters cannot provide such feature. To describe

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the operating principle and control of the impedance-source inverter in Figure 2 let us briefly examine the impedance-source inverter structure.
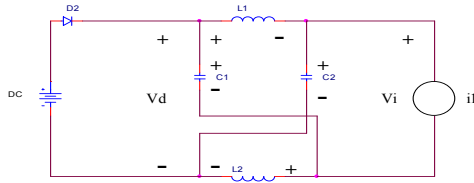

Fig.2. Equivalent Circuit of Impedance Source Inverter

The single -phase Z-source Inverter Bridge has six permissible switching states unlike the traditional single-phase V-source inverter that has five. The traditional single-phase V-source inverter has five active vectors when the dc voltage is impressed across the load and one zero vector when the load terminals are shorted through either the lower or upper single devices, respectively. However, the single-phase impedance-source inverter bridge has one extra zero state.

When the load terminals are shoot-through both the upper and lower devices of any one phase leg. This shoot-through zero state is forbidden in the traditional V-source inverter, because it would cause a shoot-through. We call this third zero state the shoot-through zero state, which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs, and all single phase legs. The impedance source network makes the shoot-through zero state possible.
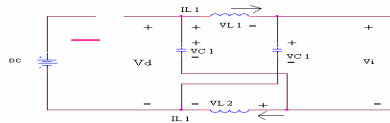

Fig. 3. Equivalent circuit of the impedance source inverter viewed form the dc link

The inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state, as shown in Figure.3, whereas the inverter bridge becomes an equivalent current source as shown in Figure 3 when in one of the six active states.

The inverter bridge can be also represented by a current source with zero value (i.e., an open circuit) when it is in one of the two traditional zero states. Therefore, figure3 shows the equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight nonshoots-through switching states. All the traditional pulse width-modulation (PWM) schemes can be used to control the Z-source inverter and their theoretical input–output relationships still hold [1].

V. CIRCUIT ANALYSIS AND OBTAINABLE OUTPUT VOLTAGE

From the symmetry and the equivalent circuits, we have

$$V_{C1}=V_{C2}=V_C; \ V_{L1}=V_{L2}=V_L \qquad (1)$$

Given that the inverter bridge is in the shoot-through zero state for an interval ofT0, during a switching cycle, $\mathbf{T}$ and from the equivalent circuit, Fig. 3 one has

$$V_L=V_C; \ V_d=2V_C; \ V_i=0 \qquad (2)$$

Now consider that the inverter bridge is in one of the eight nonshoots- through states for an interval of T, during the switching cycle, from the equivalent circuit,

$$V_l=V_0-V_C: \ V_d=V_0; \ Vi=V_C=V_L=2V_C-V_0 \qquad (3)$$

Where V_O is the dc source voltage and $T=T_0+T_1$.

The average voltage of the inductors over one switching period (T) should be zero in steady state, from eqn (2) and eqn(3), we have

$$V_L=V_l=T_0.V_C+(T_1(V_0-V_C))/T=0 \qquad (4)$$
$$V_C/V_0=T_1/(T_1-T_0) \qquad (5)$$

Similarly, the average dc-link voltage across the inverter bridge can be found as follows:

$$V_l=V_{i1}=T_0+T_1(2V_C-V_0))/T=(T_1/(T_1-T_0))V_0=V_C \qquad (6)$$

For the traditional V-source PWM inverter, we have the well known relationship:

$$V_S=M.BV_0/2 \qquad (7)$$

Equation shows that the output voltage can be stepped up and down by choosing an appropriate buck-boost factor,

$$Bb=M*B \ (0 \ to \ \alpha) \qquad (8)$$

From (1),(6) and (7), the capacitor voltage can expressed as

$$V_C1=V_C2=((1-(T_0/T))/ \ (1-2(T_0/T))V_0 \qquad (9)$$

The buck–boost factor is determined by the modulation index and boost factor. The boost factor can be controlled by duty cycle (i.e., interval ratio) of the shoot-through zero state over the nonshoots-through states of the inverter PWM. Note that the shoot-through zero state does not affect the PWM control of the inverter, because it equivalently produces the same zero voltage to the load terminal.

The available shoot through period is limited by the zero-state period that is determined by the modulation index. The impedance source network should require less capacitance and smaller size compared with the traditional V-source inverter. Similarly, when the two capacitors are small and approach zero the impedance source network reduces to two inductors in series and becomes a traditional I-source. Therefore, a traditional I-source inverter's inductor requirements and physical size is the worst case requirement for the impedance source network. Considering additional filtering and energy storage by the capacitors, the impedance source network should require less inductance and smaller size compared with the traditional I-source inverter [1].

VI. SIMULATION CIRCUIT AND RESULTS OF THE IMPEDANCE SOURCE INVERTER

Simulations have been performed to confirm the above analysis. Figure shows the main circuit configuration of impedance source inverter for UPS application. The impedance network parameters are L1=L2=160µH and C1=C2=C=1000µF. The purpose of the system is to produce single phase 208V rms power from the DC source

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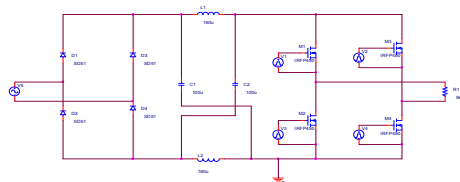whose voltage changes 150-240V dc depending on load current.

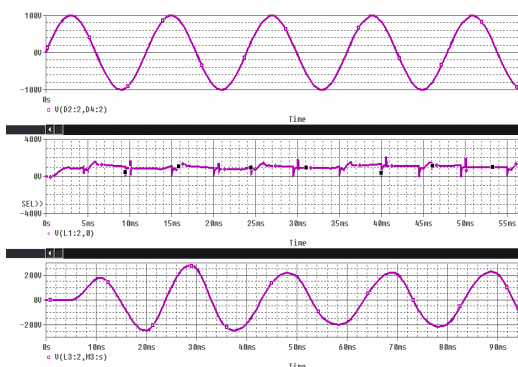Fig. 4. Circuit Diagrams of impedance source inverter

Fig. 5 Input and Output voltage waveform

Figure 5 shows the input voltage and output voltage of the z-source inverter. Input voltage is 100V AC supply. The output voltage 100V DC is given by the rectifier unit. The output voltage of impedance source inverter is shown above.

The simulation proved the impedance source inverter concept. The waveforms are consistent with the simulation results.
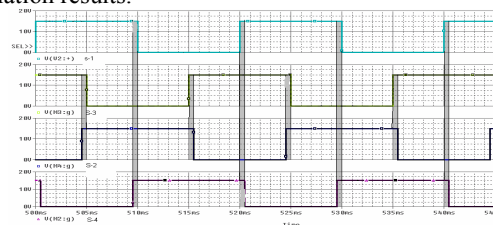

Figure 6 Modified gating pulse

VII. CONCLUSION

A new type of inverter for UPS application has been proposed and corresponding simulated waveforms are verified. The Impedance source inverter is specially suited for above applications. Unique features like single stage power conversion, improved reliability, strong EMI immunity and low EMI. The impedance source technology can be applied to the entire spectrum of power conversion.

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