Variable Structure Controller for AC/DC Boost Converter

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Abstract - **Control of AC/DC converter in presence of unknown time-varying load is a complex task due to the strong nonlinearity inherent in the converter structure and to the ones introduced by the load. When robust control techniques are used for stabilizing converter output voltage, particular care must be used to avoid degradation of the input power factor. A Variable Structure Controller for AC/DC boost converter ensuring both robustness to load variations and near-unity power factor is considered. Owing to the separate dynamics of the input current and of the output voltage, a cascade control structure is used. The reference for the inner current loop is a sinusoidal waveform whose amplitude is modulated by the external voltage controller. The current regulator is a hysteresis-type one, in which the zero-voltage control is purposely used within the hysteresis band in order to reduce high frequency chattering and hence harmonic distortion. In the external voltage loop a dynamical sliding-mode regulator is used that guarantees system robustness without introducing discontinuous control action. Use of Variable Structure Techniques results in a very simple controller that can be implemented directly in hardware. Experimental results obtained with a low-cost high-performance hardware are reported.**

I. Introduction

Use of PWM voltage-source rectifiers offers many advantages with respect to conventional uncontrolled diode bridge [1]. Both input and output characteristics of controlled converters are superior. Nearly-sinusoidal input current and good power factor can be achieved, ensuring a good load to the power line and reduced harmonic pollution. Good regulation of the DC output voltage is the most appealing property. The ripple is reduced with respect to uncontrolled rectifier and the load is decoupled from the line. When the rectifier feeds the DC-link of a variable speed drive a regenerating load can be applied to the converter and a bidirectional converter topologies may help solving this problem [5].

Most papers in the literature focuse on converter topologies and pose no particular emphasis on control strategy. Standard linear techniques are often proposed to control this strongly nonlinear system. It will be shown how the control strategy used for this kind of converters is a key factor in order to fully obtain the previous features. Moreover, any attempt to reduce the converter hardware complexity and to minimize the use of additional passive elements or sensors, turns the control problem into a more difficult task. The main goals of a controlled rectifier are: a) sinusoidal input current in phase with the line voltage, b) fast stabilization of the output voltage in response to line and/or load variations. When the converter load is time-varying, as in the case of motor drive, these two goals cannot be achieved contemporaneously. Increasing stabilization of the output voltage leads to poor input current shape, with reduced power factor and increased harmonic pollution.

When considering single-phase rectifier, this problem is even bigger, since output voltage ripple must be tolerated if sinusoidal input current is requested. The voltage control must not act on this structural ripple. Two alternative solutions can be adopted to cope with this problem.

1) the controller bandwidth is kept lower than the ripple frequency; no fast dynamical response to line/load variations is possible.

2) the controller bandwidth is kept larger than the ripple frequency; a notch filter must be used to prevent the controller acting on the structural ripple. The notch filter is quite difficult to tune and may lead to instability of the closed loop system when converter load is unknown and time varying.

These difficulties in the use of linear controllers naturally lead to the investigation of nonlinear ones. This is not surprising since the considered problem presents strong nonlinearity, which can be divided into two types: discontinuous characteristic of the converter switching matrix and load induced nonlinearity. As an example of this second nonlinearity consider a variable speed motor drive. It can draw power from the line or give it back when the motor operates in the generator region.

Solutions reported in the literature usually consider one specification at a time. Control strategies referring to power factor control usually assume the knowledge of the load while, on the other hand, robust control for unknown load results in low-quality input-current.

A further constraint is imposed in low-power applications, where the control structure should be simple enough in order to be cost-effective with respect to the converter.

In this paper a robust controller for single-phase AC/DC boost converter is proposed. Output voltage stabilization with respect to line/load variations while keeping high-quality input current are the main control specifications. The previously mentioned ambiguity in satisfying both requirements is resolved with a cascade control structure where the outer voltage controller is switched between two sets of parameters.

The nominal set is adopted when the voltage error is lower than a fixed threshold. This threshold is selected greater than the maximum amplitude of the structural ripple. Controller parameters are defined in order to compensate only slowly varying disturbances that do not include the structural ripple. This allows the line current to be sinusoidal. When the error becomes larger than the threshold, the second set of parameter is adopted. This is defined to ensure fast compensation of voltage variations. Sinusoidality of current-line is temporarily lost, but the recovery of the voltage error is ensured and the associated transient is very short compared to the line period.

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The use of a dynamic sliding-mode controller ensures the desired performances, in particular the very high robustness of the second controller structure [3], [4].

The paper is organized as follows. In Section II the converter model and the adopted controller structure are presented. In Section III the hysteresis current controller is presents. A two band controller is adopted. It gives the possibility of using the zero voltage as a control input, allowing a reduction of the current ripple and of the converter switching frequency with respect to the standard hysteresis control. Section IV is devoted to the design of the voltage control loop. A sliding-mode controller with a dynamical action is adopted, ensuring the very-high robustness typical of VS controller without introducing big discontinuities in the control action and hence eliminating the chattering problem. In Section V the controller realization is discussed, showing how the adopted controller can be easily implemented by low-cost hardware. Experimental results are reported for a 1 kVA converter subjected to step variation of the load current. They demonstrate how the proposed converter is able to combine very good steady state characteristic (power factor greater that 0.98) with high robustness to load variation and fast dynamical response.

II. Converter Model and Controller Structure

In Fig. (1) the simplified schematic of a single-phase bidirectional AC-DC boost converter is shown and the adopted nomenclature defined.

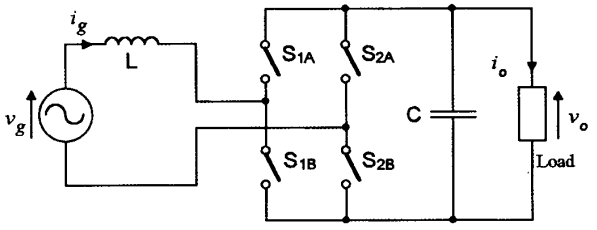

Figure 1 - AC/DC Boost Converter schematic

Let define the line voltage, and the converter three-level switch command as:

$v_g(t) = V_g \sin(\omega t)$

u = 1 if S_{1A} and S_{2B} are closed

u = -1 if S_{1B} and S_{2A} are closed

u = 0 if S_{1A} and S_{2A} or S_{1B} and S_{2B} are closed.

The converter dynamical equations can be directly derived from physical laws as:

$$v_g - L\frac{di_g}{dt} = u \cdot v_o \tag{1}$$

$$C\frac{dv_o}{dt} + i_o = u \cdot i_g \tag{2}$$

Selecting v_o and i_g as the state variables, the converter state-space model is:

$$\begin{cases} \dfrac{di_g}{dt} = \dfrac{V_g}{L}\sin(\omega t) - \dfrac{v_o}{L}u \\ \dfrac{dv_o}{dt} = -\dfrac{i_o}{C} + \dfrac{i_g}{C}u \end{cases} \tag{3}$$

A time-varying nonlinear system results, owing to the sinusoidal term in the first equation and to the multiplication of the control u by the state variables in both equations. Moreover the control input is a three level signal.

The control goals are: a) the converter output voltage must be regulated to a reference value v_{ref} greater than V_g (boost converter); b) the line current i_g must be sinusoidal, independently of the load current i_o..

To stress the efficiency of our controller and to minimize the complexity of the final realization it was decided not to measure the load current, which is viewed as a non-measurable disturbance acting on the system.

Equation (3) clearly shows that the two control goals cannot be achieved simultaneously, since perfect regulation of v_o implies $dv_o/dt = 0$ and hence $|i_o(t)| = |i_g(t)|$. Moreover, only one control input is available to control the two independent state variables separately.

The analysis of the converter equation (3) shows that the system dynamics can be divided into fast motion (input current) and slow motion (output voltage). Substituting typical values for system parameters L and C in the equations, it can be shown that the two dynamics may differ more than two orders of magnitude. This suggests the use of a cascade control structure composed of an external voltage controller that gives the reference to an inner current loop. The block diagram of the controller is reported in Fig. (2).

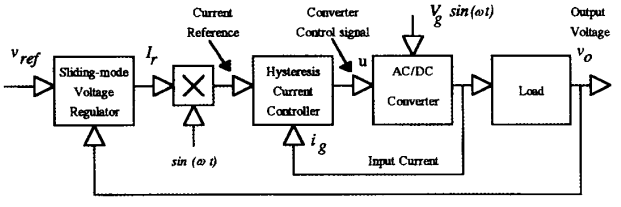

Figure 2 - Block diagram of the controller

In order to provide sinusoidal input current, the output of the voltage controller controls the amplitude of a sinusoidal signal in phase with the line. This process can be viewed as a structural multiplicative disturbance acting on the system, which is added to the exogenous disturbance introduced by the load (current i_o). The voltage regulator must compensate for the load disturbance only. It will be shown in section IV how this task can be accomplished by a Variable Structure Controller.

III. Current Controller

According to the first of eq.(3), we are dealing with a variable structure system, since control u is a three-level signal. An hysteresis controller is adopted for the inner current loop, since this kind of controller is a particular type of VS controller. The variable structure nature of the system is directly considered in the controller design and a continuous approximation of the plant is not required. Hysteresis controllers present two main drawbacks, both related to the finite switching frequency of the converter: the first one is that this switching frequency is variable and the second one is the high frequency chattering resulting in the input current, which causes harmonic distortion and leads to lower power factor.

In order to reduce this disadvantages, two hysteresis bands are used in the current controller, as shown in Fig. (3). The reference for the controller is given by $i_r = I_r \sin(\omega t)$ where I_r is the output of the voltage regulator. When the input current error $i_e = i_r - i_g$ is outside the inner band ($|i_e| > \delta$), two level control action ($u = \pm 1$) is applied to force it inside again. However, when the inner band is reached ($|i_e| < \delta$), a second control strategy is adopted that purposely uses the zero-voltage input ($u = 0$) to minimize the converter switching frequency required to maintain the system inside the band. Since the maximum switching frequency is defined by the selected converter technology, this second control strategy allows the reduction of the hysteresis amplitude δ, leading to lower current chattering.

The current error dynamic is:

$$\frac{di_e}{dt} = \frac{di_r}{dt} + \frac{v_o}{L}u - \frac{v_g}{L}. \tag{4}$$

When zero-voltage input is applied, current error trajectory is driven only by the disturbance term $d = \frac{di_r}{dt} - \frac{v_g}{L}$. If the sign of disturbance term changes, the current error can diverge, going outside the hysteresis band, as shown in Fig. (3). To avoid instability, a second hysteresis band, larger than the first, is introduced. Two-level control is applied outside this band.

The typical behavior of the proposed current regulator is shown in Fig. (3), in which the two hysteresis bands, the trajectory of the current error and the control action, in occurrence of disturbance sign changing, are represented.

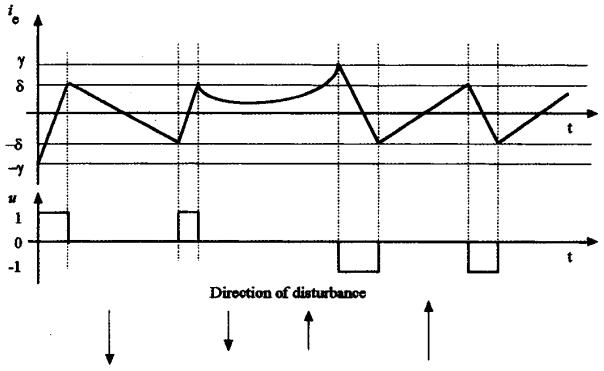

Figure 3 - Typical current error trajectory

Note that eq. (4) relates the output voltage v_o with the current dynamics. Error stability or, equivalently, current tracking is ensured if [2]:

$$\mathrm{sgn}(i_e)\frac{di_e}{dt} < 0 \tag{5}$$

By putting

$$u = -\mathrm{sgn}(i_e) \tag{6}$$

and multiplying eq. (4) by $\mathrm{sgn}(i_e)$, we obtain:

$$\mathrm{sgn}(i_e)\frac{di_e}{dt} = -\frac{v_o}{L} + \left(\frac{di_r}{dt} - \frac{v_g}{L}\right)\mathrm{sgn}(i_e) \tag{7}$$

Error stability is obtained if and only if:

$$v_o > \max\left|L\,di_r/dt + v_g\right| = L\left|di_r/dt\right|_{\max} + V_g \tag{8}$$

Remembering that $i_r = I_r \sin(\omega t)$, we obtain form eq. (8) the following:

$$v_o > L\left|dI_r/dt\right|_{\max} + L\omega\left|I_r\right|_{\max} + V_g \tag{9}$$

which is the design equation for v_o once the quantity $\left|dI_r/dt\right|_{\max}$ is known. Since I_r is the output of the voltage controller, this value and its derivative can be fixed by the voltage regulator design.

IV. Voltage Regulator

Due to the dynamic order reduction ensured by sliding-mode controller, when designing the external voltage regulator it can be assumed that the inner loop is in perfect tracking.

Under this assumption we have:

$$i_g = I_r \sin(\omega t) \tag{10}$$

that, substituted in the second of eq. (3), gives:

$$\frac{dv_o}{dt} = \frac{I_r}{C}\sin(\omega t)u(t) - \frac{i_o}{C}. \tag{11}$$

The control action $u(t)$ in eq. (11) is completely determined by the internal current controller. Assuming perfect current tracking, according to [2] we can derive from eq. (4) the equivalent control $u_{eq}(t)$, that results:

$$u_{eq}(t) = \frac{1}{v_o}\left(V_g - L\frac{dI_r}{dt}\right)\sin(\omega t) - \frac{\omega L}{v_o}I_r\cos(\omega t) \tag{12}$$

The reduced model (11) becomes:

$$\frac{dv_o}{dt} = \frac{I_r}{Cv_o}\sin(\omega t)\left[\left(V_g - L\frac{dI_r}{dt}\right)\sin(\omega t) - \omega L I_r \cos(\omega t)\right] - \frac{i_o}{C}. \tag{13}$$

Eq. (13) is time-varying and strongly nonlinear. It is not affine in the control I_r, that enters also in a quadratic way in one term. Moreover, the control derivative is present in (13). Design of a regulator that stabilize the output voltage at a reference value v_{ref} based on model (13) is a very complex task, considering the additional requirement of rejection of the disturbance i_o too. The following relationships will be assumed valid for the regulator design:

$$V_g > \left|L\frac{dI_r}{dt}\right| \tag{14}$$

$$V_g - L\frac{dI_r}{dt} >> \left|\omega L I_r\right| \tag{15}$$

Let rewrite eq. (13) as:

$$\frac{dv_o}{dt} = \frac{1}{C}k(v_o, I_r, dI_r/dt, t)I_r - \frac{i_o}{C} \tag{16}$$

where

$$k(v_o, I_r, dI_r/dt, t) =$$

$$= \frac{V_g - L\,dI_r/dt}{v_o} \sin(\omega t) \left[\sin(\omega t) - \frac{\omega L I_r}{V_g - L\,dI_r/dt} \cos(\omega t) \right] \quad (17)$$

can be viewed as an equivalent nonlinear gain.

Remark 1. $k(v_o, I_r, dI_r/dt, t)$ can be physically interpreted as the portion of the reference current that actually is injected in the converter capacitor and drives the output voltage.

Eq. (17) shows that the equivalent gain changes its sign in time. In particular, it is greater than zero when:

$$\frac{\omega L I_r}{V_g - L\,dI_r/dt} \sin(\omega t)\cos(\omega t) - \sin^2(\omega t) < 0 \quad (18)$$

which is always verified when:

$$\left| \frac{\omega L I_r}{V_g - L\,dI_r/dt} \right| < \tan(\omega t) \quad (19)$$

Due to assumption (15), the time intervals in which the equivalent gain is less or equal to zero are negligible. Hence, in the following we will design the voltage regulator based on the assumption:

$$k(v_o, I_r, dI_r/dt, t) \geq k_m \quad (20)$$

with k_m a positive constant.

Remark 2. Assumption (20) is surely not exactly verified. In particular, its accuracy in the closed loop system depends on the chosen control strategy, due to the presence of I_r and its derivative. Hence, at the end of the design procedure of the voltage regulator, their validity must be verified. •

A dynamical sliding-mode algorithm is used for the voltage regulator design, based on the simplified model (16) and assumption (20). This control algorithm, proposed in [4], offers the very high robustness properties of SM regulators without introducing large discontinuous control action. We report here the design equations without proofs, that can be found in the literature (see [4] for the case of time invariant systems and [6] for the extension to the time-varying ones).

Defining the voltage error as $v_e = v_{ref} - v_o$, where v_{ref} is the constant set point for the output voltage, the dynamics of the voltage error results:

$$\frac{dv_e}{dt} = -\frac{1}{C} k(v_e, v_{ref}, I_r, dI_r/dt, t) I_r + \frac{i_o}{C} \quad (21)$$

and the adopted regulator expression is given by:

$$I_r = \lambda v_e + \kappa\, \mathrm{sgn}(v_e) + \eta \int \mathrm{sgn}(v_e)\,dt\,. \quad (22)$$

It can be proved that a sliding mode arises in the system along the surface $v_e = 0$ if the regulator parameters are chosen according to the following relationships:

$$\kappa > 0; \qquad \eta > \frac{1}{k_m}\Delta; \qquad \lambda > \frac{\eta + \Delta}{2 k_m \kappa} \quad (23)$$

where $\Delta = \max\{di_o/dt\}$. However, by using eqs. (23) for the regulator synthesis the good power factor specification is not achieved, since all the disturbances are perfectly compensated (within the limit of assumption (20)) and hence the modulation process between the two loops is canceled.

In order to eliminate this effect, upper and lower bounds for the admissible voltage are defined and two different sets of regulator parameters are used. The first one is designed to compensate only for slowly varying disturbances (having no influence on the modulation disturbance and hence on the input current waveform) and it is used when the output voltage is within the bounds. During steady-state and slowly varying operating conditions, a sinusoidal input current results with a near-unity power factor. In presence of strong load variations, the output voltage would exit the admissible bounds. In this case the second set of parameters is used, which is designed according to eqs. (23) in order to achieve complete robustness of the system. Output voltage error is quickly recovered but, during the transient, input current is no longer sinusoidal. As soon as the transient ends, the first set of parameters is used again.

Some remarks are noteworthy as far as the design of the first parameters set is concerned. In this case the voltage regulator should compensate only for slowly varying load induced disturbances without interfering with the modulation process. This can still be done on the basis of eqs. (23), in which the quantity Δ is set accordingly to a slowly varying $i_o(t)$ and the constant k_m is replaced by a new constant k_M defined as:

$$k_M = \max\{k(v_e, v_{ref}, I_r, t)\}. \quad (24)$$

In this case, sliding mode motion on $v_e = 0$ does not arise in the system and the line current remains almost sinusoidal.

Remark 3. The first set of parameters can be viewed as the result of a design procedure done on an "average" system. Typical values for the ratio k_M/k_m are around 10 (see remark 4 below). •

Remark 4. Once the voltage regulator has been defined, the assumptions used in the synthesis should be checked. The main problem in this case is to prove that both quantities $|dI_r/dt|$ and $|I_r|$ remain bounded in the closed loop system by values for which assumptions (14), (15) are still verified. Actually, it can be proved that for each initial condition $v_e(0) = v_{eo}$, in the closed loop system a compact positively invariant region $\Omega(v_{eo}) \subset R^2$ exists, such that $(v_e(t), I_r(t)) \subset \Omega(v_{eo})$ for every $t > 0$. This region defines bounds (functions of the initial value v_{eo}) on the state variables of the c.l.s. which satisfy

$$|v_e(t)| \leq v_{eM}(v_{eo}) \quad \lim_{v_{eo} \to 0} v_{eM}(v_{eo}) = 0 \quad (25)$$

$$|I_r(t)| \leq I_{rM}(v_{eo}) \quad \lim_{v_{eo} \to 0} |I_{rM}(v_{eo})| \leq \frac{i_{oM}}{k_m} \quad (26)$$

with $i_{oM} = \max|i_o|$. Moreover, a bound on the reference current derivative can be computed as well, resulting in:

$$\lim_{v_{eo} \to 0} \left(\max \left| \frac{dI_r}{dt} \right| \right) \leq \frac{1}{k_m} \Delta \quad (27)$$

Actual proof of eqs. (25) - (27) is beyond the scope of the paper and is not reported. However, it can be related to the physics of the converter. Based on eqs. (26), (27) assumption (15) can be replaced by

$$V_g - L\frac{\Delta}{k_m} >> \frac{\omega L}{k_m} i_{oM} \qquad (28)$$

that express the fact that the line voltage minus the drop on the input inductor must be big enough to impose a line current whose useful portion can compensate for the load current (remember remark 1 on the physical interpretation of k). Eq. (28) shows that the key parameter in the regulator design is k_m. It should be small enough to guarantee that eq. (20) is not verified only for time interval small with respect to the line period. On the other side, it should be large enough to satisfy eq. (28). Usually, this trade-off can be accomplished in a typical converter set-up. For the converter used in the experimental set-up of the following section, where L = 2 mH and i_{oM} = 5 A and Δ = 100 A/s (corresponding to a variation from 0 to maximum power in one line period), a value $k_m = 0.02$ results a good choice. Moreover, note that bound (28) is somewhat conservative. It will be shown in the following section that step variations in the converter load are tolerated as well.

V. Hardware Set-up and Experimental Results

One of the main features of the proposed control scheme is that it can be implemented with low-cost hardware without degrading the system performances. Both inner and outer loops can be realized with simple analog-logic circuits, without resorting to powerful general purpose microcontrollers. The robustness properties of both regulators lead to two main advantages:

- an additional sensor is not required to measure the load current;
- being inequalities, the design eqs. (23) guarantee that the system performances are preserved even if the controller gains are different from the ones resulting from the synthesis. This gives the system robustness with respect to the gains of the analog acquisition channels. Errors in the nominal values of the used analog elements and their thermal drift are of no influence on the controller's performances.

In implementing the converter, the analog parts of the controllers can be realized through simple chains of operational amplifiers and comparators, while the logic networks that achieve the hysteresis mechanisms of the inner loop and the switching in the voltage regulator parameters can be implemented by a simple Progammable Logic Device driven by an high frequency clock. Note that the design procedure discussed in the previous sections results in the cascade of sliding mode loops. To avoid this potentially critical operation, a sample-and-hold device should be inserted between the two loops. Hence, the reference for the inner loop is transformed in a sequence of step changes. Again, the use of the dynamical sliding mode regulator for the voltage loop in which the amplitude of the discontinuous action is almost negligible is a key point in obtaining step changes of small size in the current reference. Due to the separation in the dynamics of the two loops, the sampling time of the S/H interface can be selected large enough for the inner current loop to track its reference and small enough not to interfere with the outer voltage loop.

Experimental results have been obtained for a single-phase rectifier whose characteristics are reported in Table 1.

Table 1. Converter characteristics		
V_g = 100 V	L = 2 mH	C = 500 μF
P_{out} = 1 kW	v_o = 200 V	i_{oM} = 5 A

Fig. (4) reports the steady state response when the converter is operating at the maximum power. Note the structural ripple on the output voltage (12 V peak-to-peak) whose level is determined by the sinusoidal input current value. The mean value of converter switching frequency is about 10 kHz.

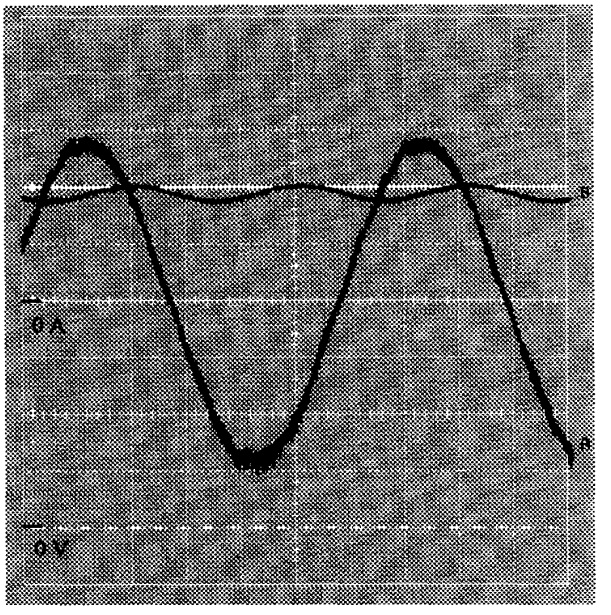

Figure 4 - Steady state behavior of AC/DC rectifier. Time base = 3.2 ms/div. A) Line current (7 A/div); B) Output voltage (35 V/div)

The spectral quality of the AC line current is shown on Fig. (5). All the undesired current harmonics lie more than -35 dB below the 50Hz in-phase fundamental component. The corresponding power factor is better than 0.98 for every load.

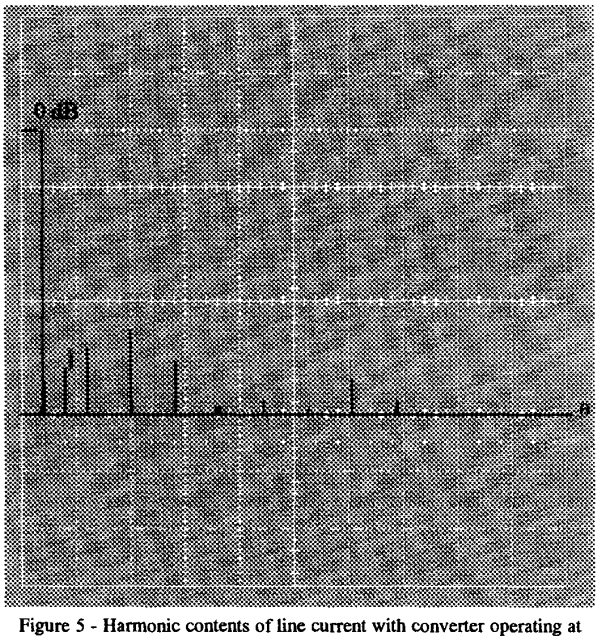

Figure 5 - Harmonic contents of line current with converter operating at maximum power. Horizontal scale 125 Hz/div. Vertical scale 10 dB/div

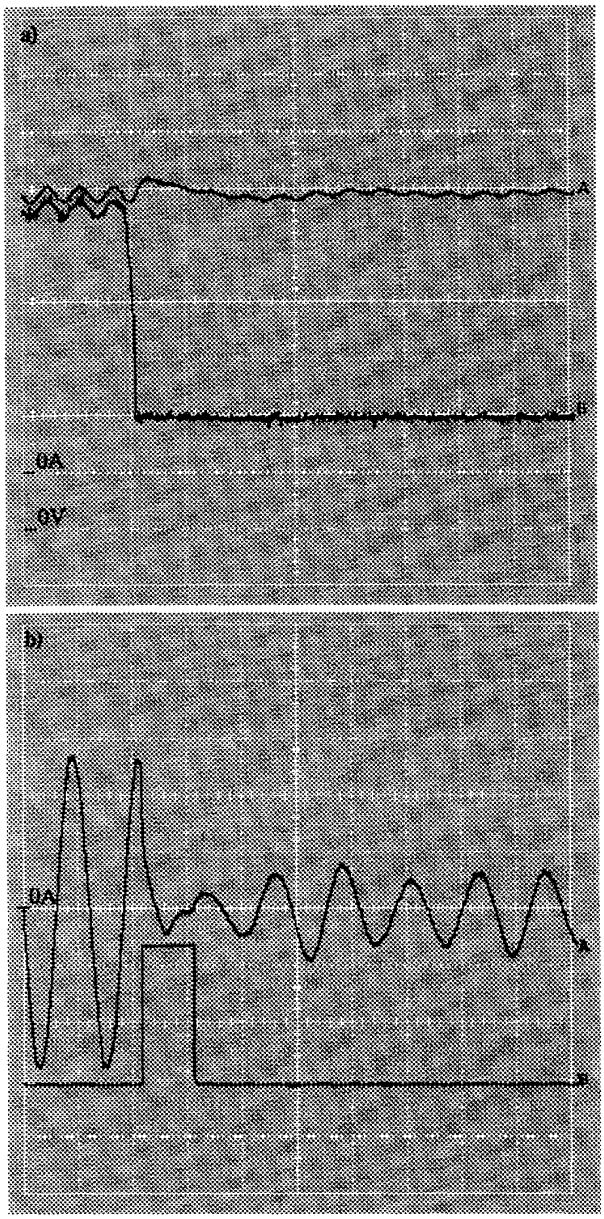

Figure 6 - System response to step change in output power. Time base = 16 ms/div. a) A) Output Voltage (35 V/div); B) Load current (1 A/div); b) A) Line current (8 A/div); B) Variation of voltage regulator structure.

The system behavior during large load transient is shown in Fig. (6). A resistive load is switched from 900W to 200W. The DC output voltage and the load current are reported on Fig. (6-a), while input current and the logic signal corresponding to adoption of the second set of voltage regulator parameters are reported on Fig. (6-b). Thanks to the switchable parameters policy on the voltage regulator, the sinusoidal input current condition is recovered after 16 ms from load step, and the output voltage error remains under 10% of the output nominal value. This results shows that the inherent robustness of sliding mode regulators allows good control performances with every load, and fast recovery from large system structure variations.

VI. Conclusions

A cascade Variable Structure Controller for AC/DC boost converter has been proposed. The controller is mainly intended to achieve nearly-sinusoidal input current and good power factor in AC to DC conversion, also for regenerative DC loads. A double hysteresis band controller that uses the zero-voltage control has been presented for the inner current loop. This controller allows current ripple amplitude reduction and lower mean switching frequency related to the standard hysteresis one.

The calculation of the nonlinear and time varying gain of the inner closed loop, and the design of voltage regulator have been discussed. A dynamical sliding mode robust controller has been proposed for the voltage control. The design of regulator's parameters and the switching criteria between two set of parameters have been defined in order to obtain either sinusoidal input current during steady-state conditions and good DC voltage regulation during load transient.

Converter hardware implementation based on low-cost standard analog and logic components, and related experimental results has been presented. The results show that the design goals have been fully satisfied.

Acknowledgments

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