

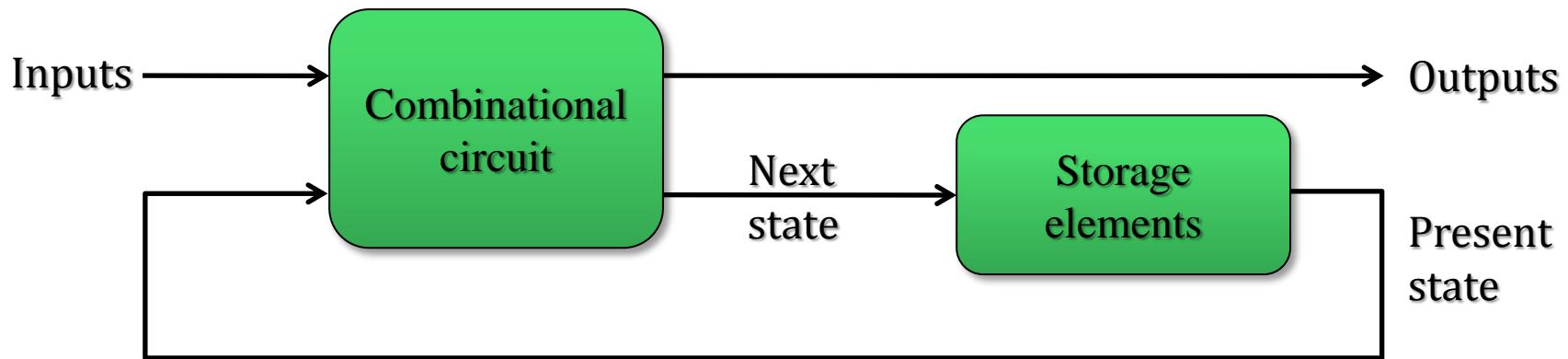
WEEK 5-2017

Synchronous Sequential Circuit I



Sequential Circuit

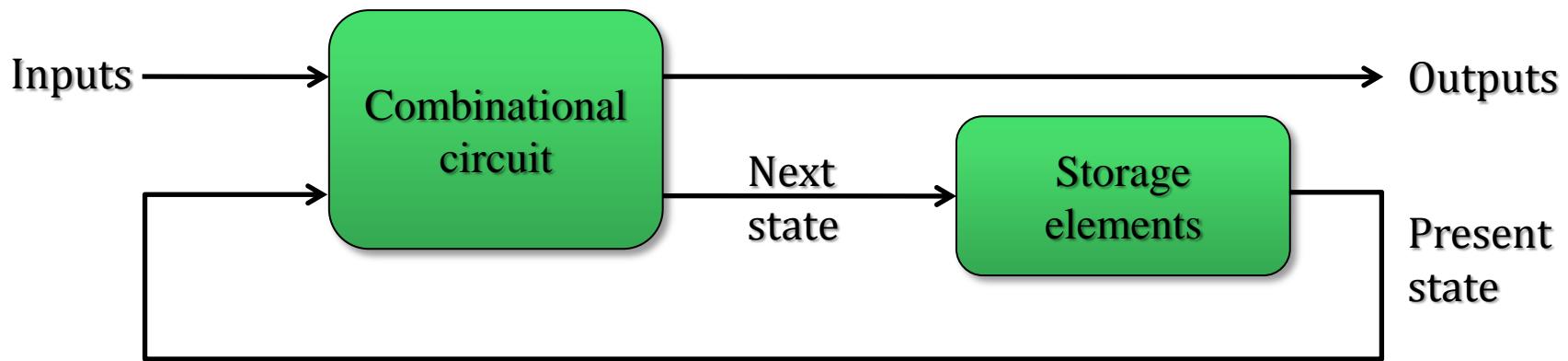
- Most digital circuits encountered in practice include storage elements. Such circuits are described as Sequential.



- Sequential circuits consist of a combinational circuit to which storage elements are connected to form a feedback path.
- Storage elements are devices capable of storing binary data.

Sequential Circuit

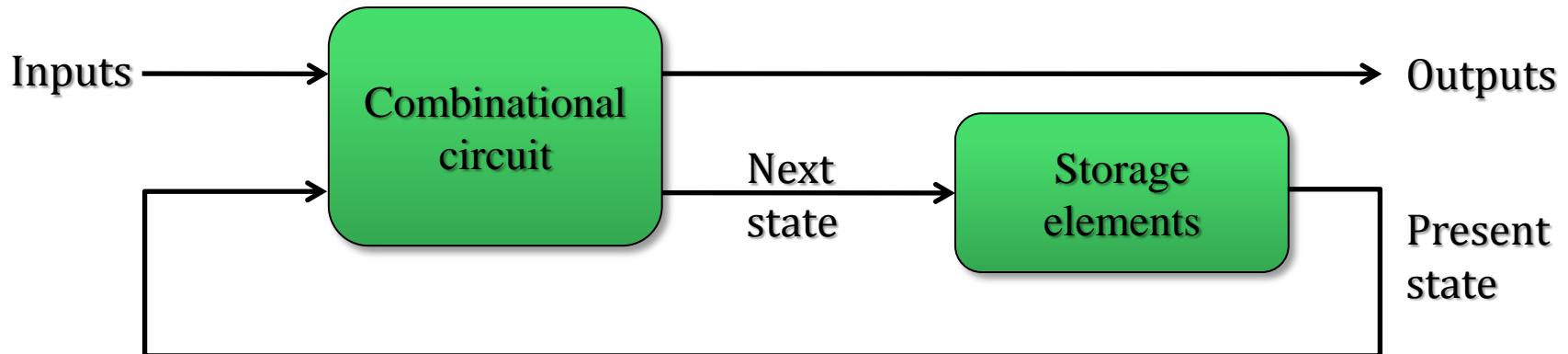
- The binary information that is stored in the storage element of the sequential circuit at any given time defines the state of the sequential circuit.



- The binary information applied externally to the sequential circuit as an input together with the present state determines the next state of the sequential circuit.
- The output of the sequential circuit is also determined by the binary information applied as an input and the present state of the sequential circuit.

Sequential Circuit

- Thus, the behavior of the sequential circuit is specified by a time sequence of inputs, internal states and outputs



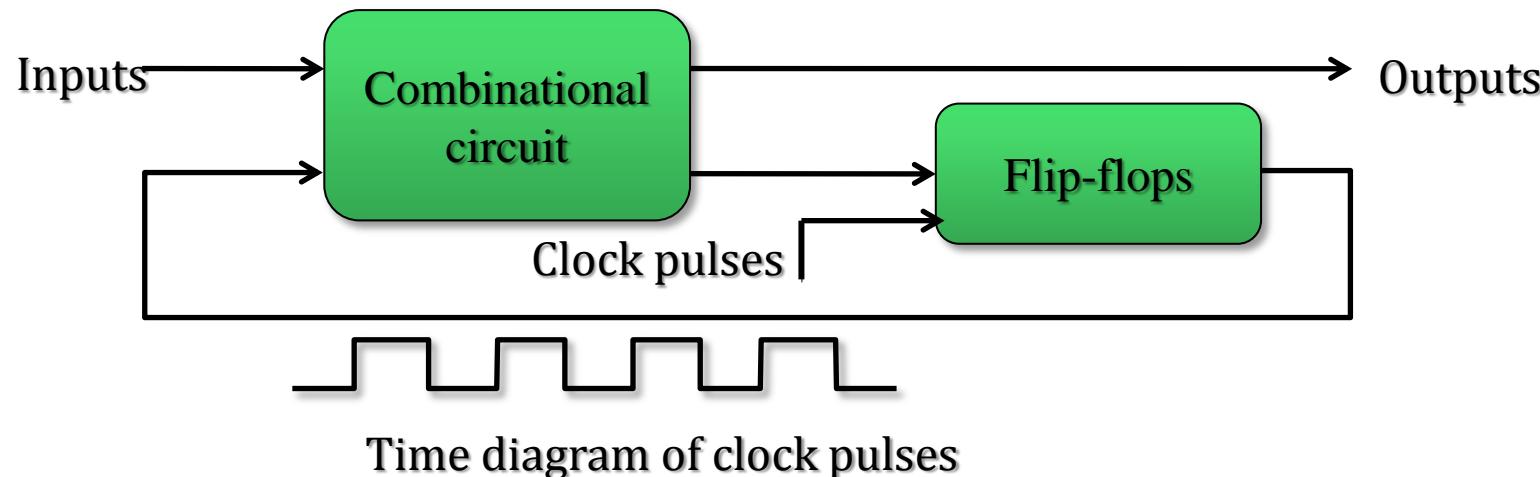
- Sequential circuits are divided into Synchronous and Asynchronous sequential circuits.
- In synchronous sequential circuits, the outputs and states are modified (or changed) only at a discrete instants of time.

Sequential Circuit

- In asynchronous sequential circuits, the outputs and states are modified (or changed) only at any instant of time depending upon the inputs.
- The storage elements commonly used in asynchronous sequential circuits are time delay devices.
- Propagation delay in a gate or through interconnected gates can constitute time delay device.
- Therefore, asynchronous sequential circuits can be regarded as combinational circuits with feedback.
- The feedback may introduce instabilities at times. The instability problem imposes many difficulties on the designer.

Synchronous Sequential Circuit

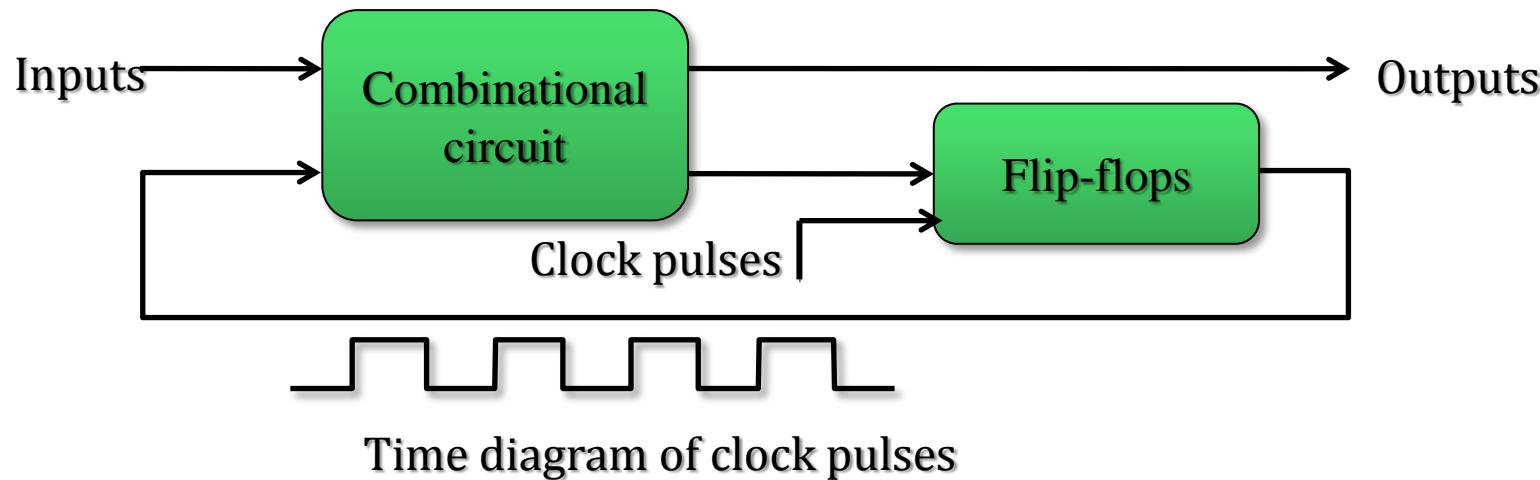
- In synchronous sequential circuit, synchronization is achieved by a timing device called a clock generator.



- A **clock generator** provides a **clock signal** having the form of **periodic train of pulses**, and identified by **clock** or **clk**.
- As a result, **synchronous sequential circuit** are also called **clocked sequential circuits**.
- They are **commonly used digital circuits** because they do not manifest instability and make design of digital circuit feasible.

Synchronous Sequential Circuit

- The storage elements used in clocked sequential circuits are called flip-flops.



- A flip-flop is a binary storage device that is capable of storing one bit of information.
- Flip-flops change states only in response to a clock pulse.
- A flip-flop has normally two outputs: Normal and its complement

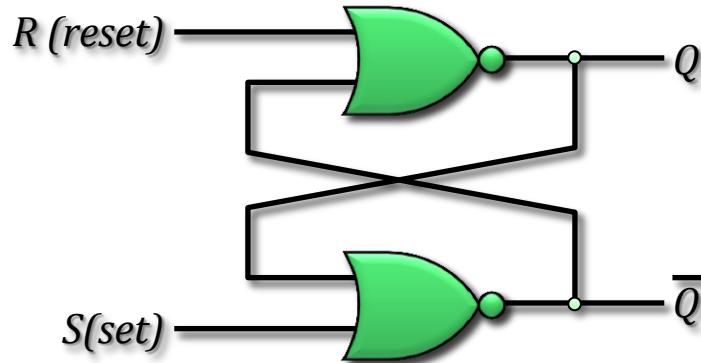
Storage elements: Latches

- Latches are also storage elements.
- Storage elements are characterized by (a) the number of inputs they posses; (b) the manner in which the inputs affect the binary state.
- Latches – storage elements that operate with signal levels. They are signal level sensitive devices.



- Flip-flops – storage elements controlled by a clock transition. They are edge sensitive devices.

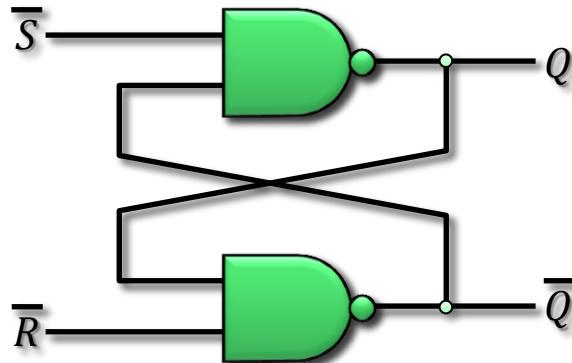
SR Latch



S	R	Q	\bar{Q}	

- Two cross-coupled NOR gates and two inputs labeled as S (set) and R (reset).
- The latch has two states. When $Q = 1$ and $\bar{Q} = 0$, the latch is said to be in the set state.
- When $Q = 0$ and $\bar{Q} = 1$, the latch is said to be in the reset state.

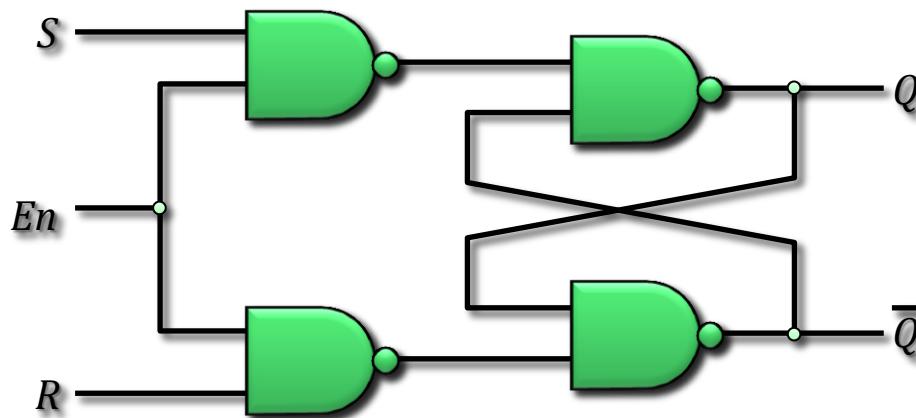
SR Latch



\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	1	0	
1	0	0	1	
0	1	0	1	
0	0	1	0	

- Two cross-coupled NAND gates and two active low inputs labeled as \bar{S} (set) and \bar{R} (reset).
- The latch has two states. When $Q = 1$ and $\bar{Q} = 0$, the latch is said to be in the set state.
- When $Q = 0$ and $\bar{Q} = 1$, the latch is said to be in the reset state.

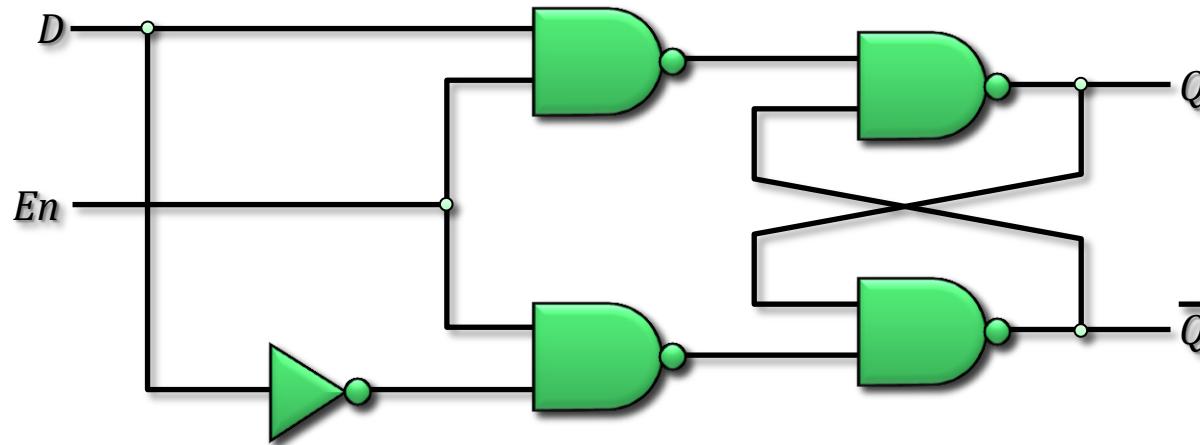
SR Latch with control



En	S	R	Next state of Q
0			
1			
1			
1			
1			

- The basic operation of SR latch can be modified by adding an enable input signal that determines when the state of the latch can be changed.
 - It consists of the basic SR latch and two additional NAND gates.
 - With $En=1$, $S=1$ and $R=1$, the next state of indeterminate condition occurs.

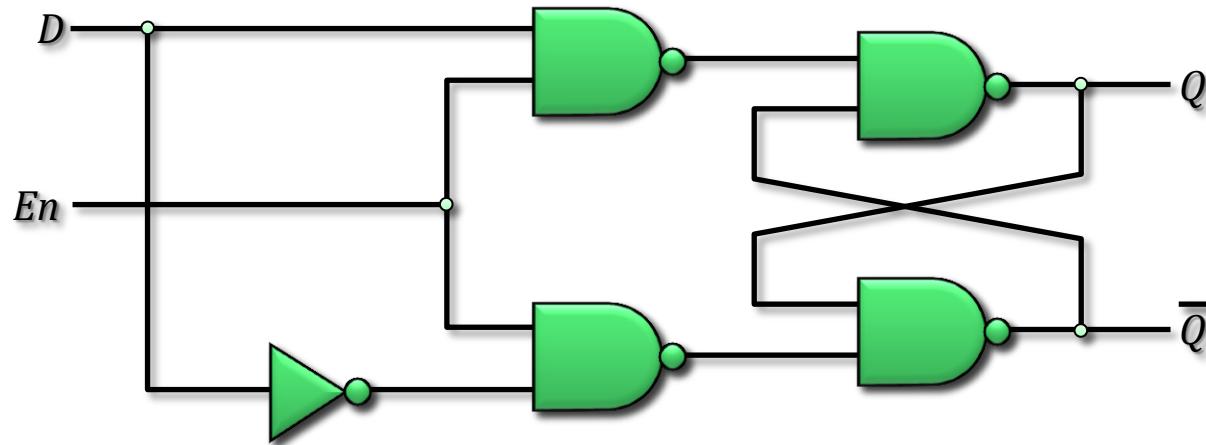
D Latch



En	D	Q
0	X	No change
1	0	0 (Reset)
1	1	1 (Set)

- If $D=1$, the Q output goes to 1, placing the circuit in the set state. If $D = 0$, the Q output goes to 0, placing the circuit in the reset state.
- The binary information present at the data input of the D-latch is transferred to the Q output when enable input is asserted.

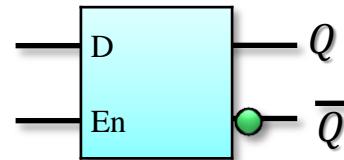
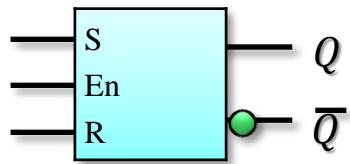
D Latch



En	D	Q
0		
1		
1		

- The **indeterminate condition with SR latch when S=1, R=1 and En= 1 can be eliminated by ensuring that inputs S and R are never equal to 1 at the same time.**
- This is done by D latch
- En = 0 produces $S' =1$ and $R'=1$, which drives the basic SR latch to remain in same state.
- The D-input is sampled when En=1.

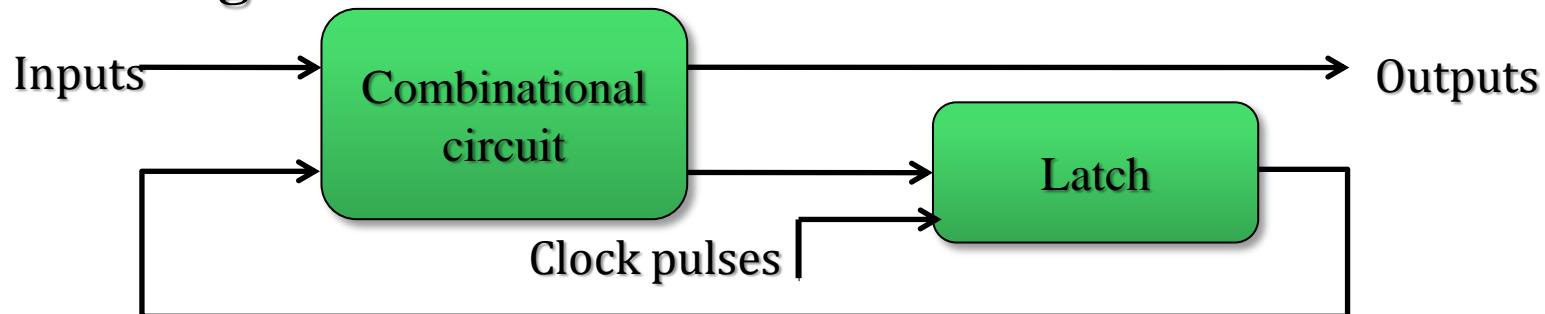
Latch-designations



- **A latch is designated by a rectangular block with inputs on the left and outputs on the right.**
- **One output designates the normal output and the other designates the complement output.**

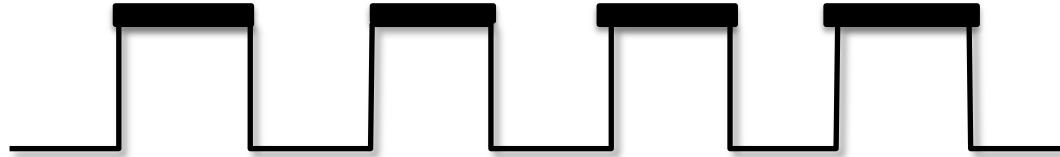
Storage elements: Flip-flops

- The use of latches as storage elements in a synchronous logic circuit will give rise to a serious malfunction.
- The state of the storage element will continue to change as long as the input changes while the clk is high. Therefore, it is difficult to get a stable output when latches are used as storage elements.



- This problem of latches can be solved by constructing flip-flops whose states can only change in response to signal transition rather than signal level.
- Flip-flops – storage elements controlled by a clock transition. They are edge sensitive devices.

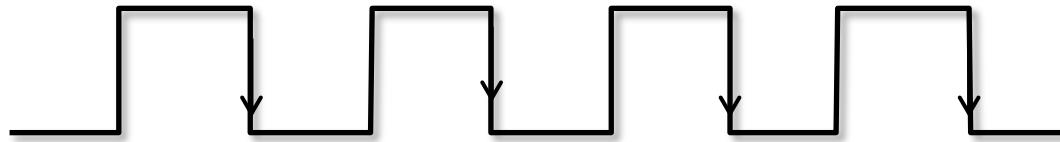
Storage elements: Flip-flops



Response to positive level



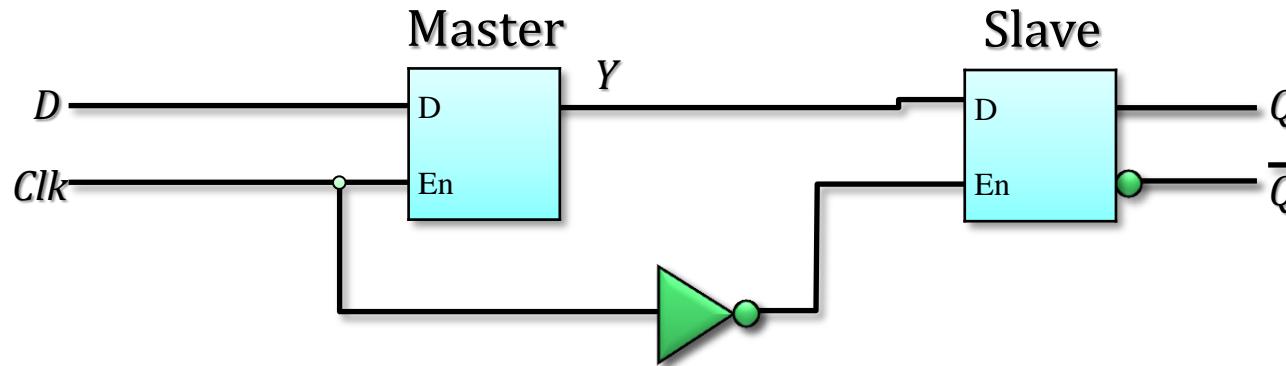
Positive-edge response



Negative-edge response

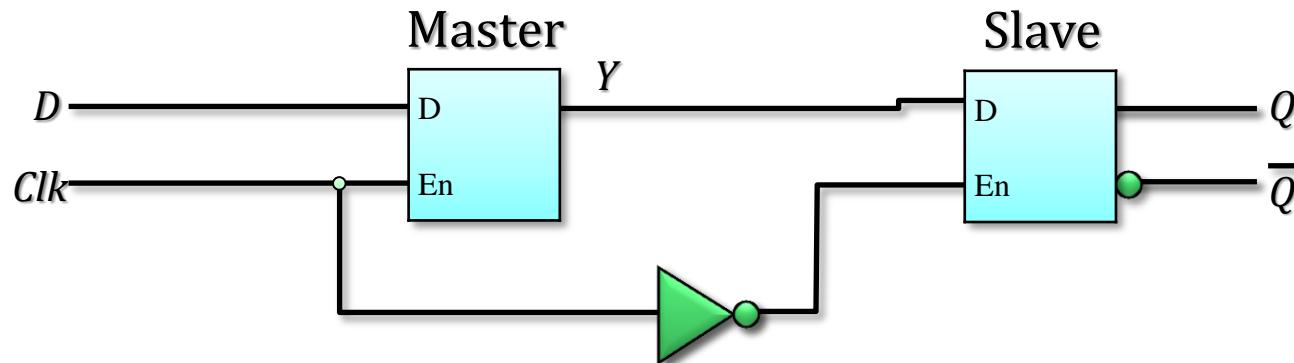
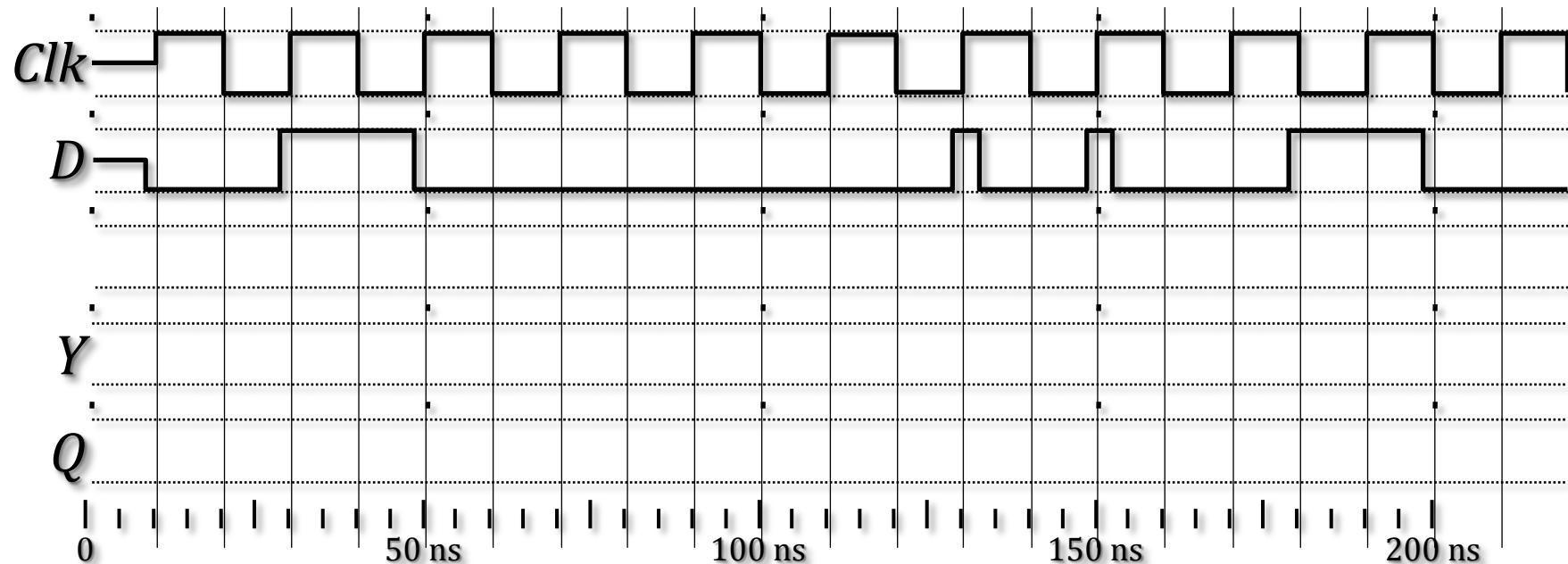
Edge-triggered D flip-flop

- Consider D flip-flop constructed from two D latches and an inverter as shown below



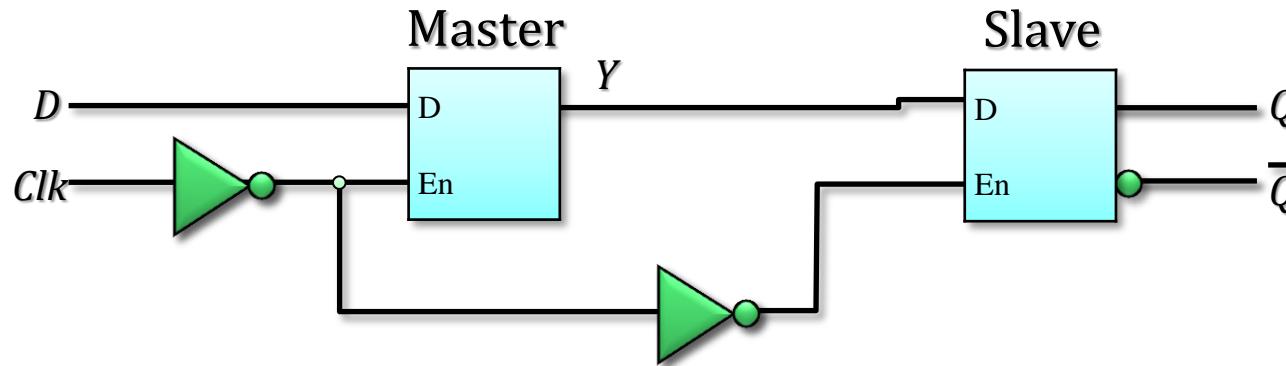
- When $clk = 1$, master D latch will be enabled while slave D latch is disabled. $Y = D$
- When $clk = 0$, master D latch is disabled while slave D latch is enabled. $Q = D$
- This output remains unchanged until the clock transition from 0 to 1 occurs. In other word, the configuration is negative edge triggered.

Edge-triggered D flip-flop



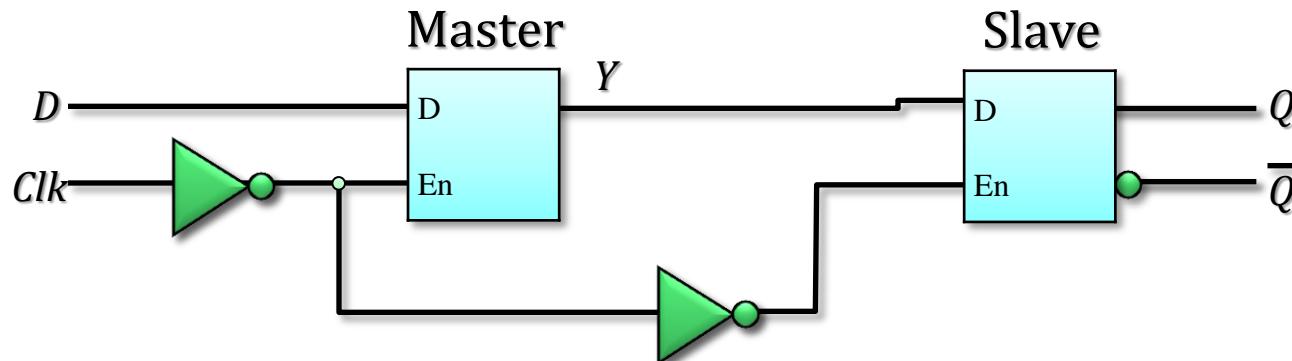
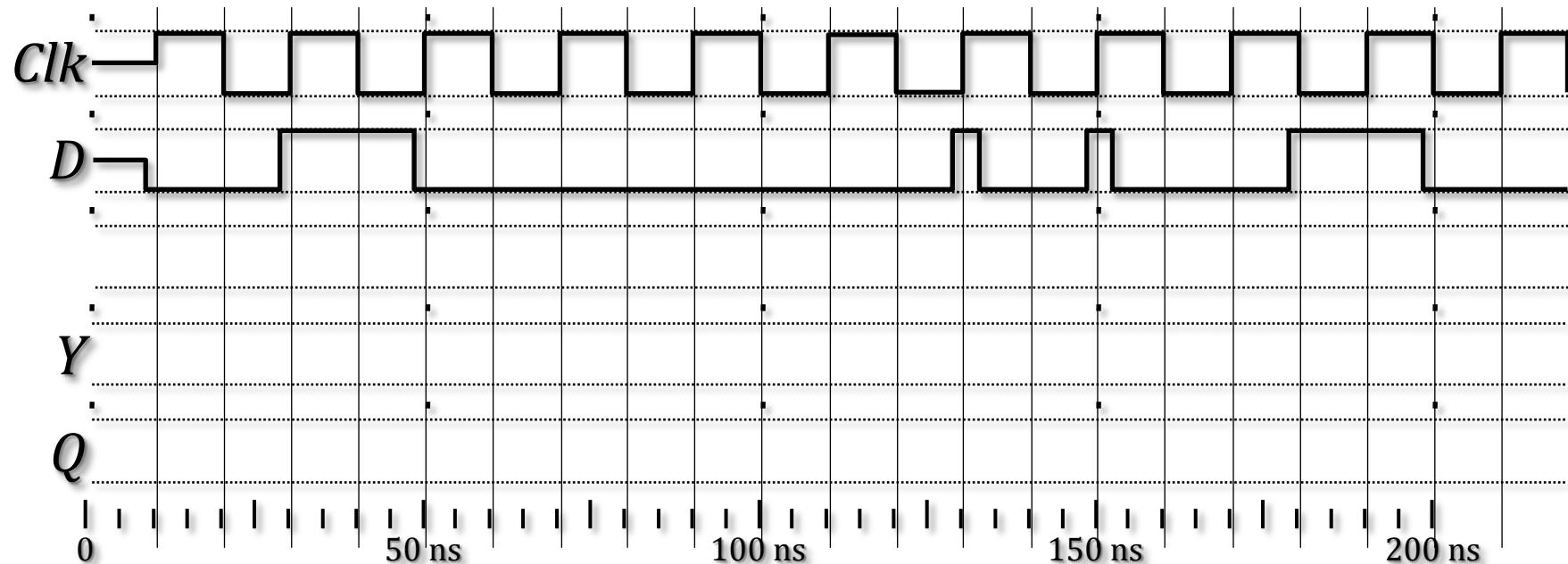
Edge-triggered D flip-flop

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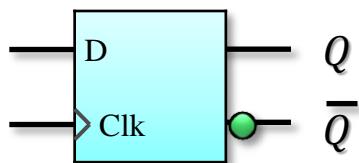
- When $\text{clk} = 0$, master D latch will be enabled while slave D latch is disabled. $Y = D$
- When $\text{clk} = 1$, master D latch is disabled while slave D latch is enabled. $Q = D$
- This output remains unchanged until the clock transition from 1 to 0 occurs. In other word, the configuration is positive-edge triggered.

Edge-triggered D flip-flop

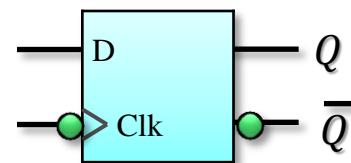


Flip-Flop Symbols

- The positive and negative edge-triggered D flip-flops are represented by:



↑ Triggered

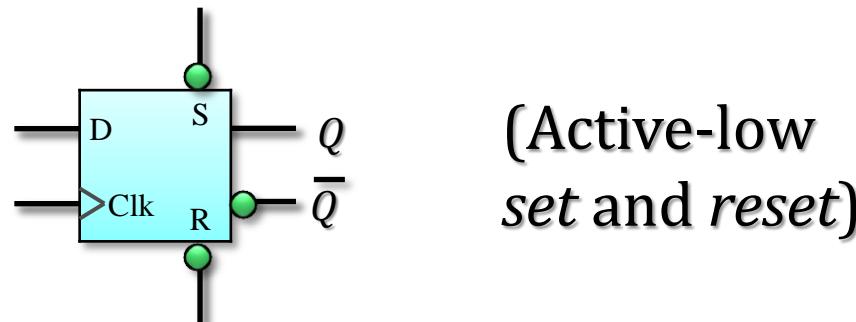


↓ Triggered

- The symbols \uparrow and \downarrow are used to denote positive and negative edge triggering, respectively

Direct Inputs

- **Asynchronous Set and Reset input signals**
- **Used to force a value to the output of the flip-flop, independent of the clock**
- **Usually used to initialize the circuit to known values at system start-up**



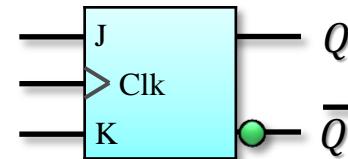
Other Flip-Flops

- Edge triggered D flip-flop requires the smallest number of gates and hence the most economical and efficient flip-flop
- Other types of flip-flops can be constructed by using D flip-flop and external logic
- The other two flip-flops less widely used in the design of digital systems are JK and T flip-flops

JK Flip-Flops

- The JK flip-flop has a similar behavior to the SR flip-flop with the exception that 1-1 input is allowed

J	K	Q
0	0	
0	1	
1	0	
1	1	



T Flip-Flops

- The T (Toggle) flip-flop maintains its stored value when $T = 0$, and complements it when $T = 1$

T	Q
0	
1	

