

**WEEK 11-2017**

# Digital Integrated Circuits

ELEC2141: Digital Circuit Design



**UNSW | ENGINEERING**  
THE UNIVERSITY OF NEW SOUTH WALES

# Integrated Circuits

- Integrated circuit (informally, a “chip”) is a semiconductor crystal (most often silicon) containing the electronic components for the digital gates and storage elements which are interconnected on the chip.
  - Terminology - Levels of chip integration
    - *SSI (small-scale integrated)* - fewer than 10 gates
    - *MSI (medium-scale integrated)* - 10 to 100 gates
    - *LSI (large-scale integrated)* - 100 to thousands of gates
    - *VLSI (very large-scale integrated)* - thousands to 100s of millions of gates
- IC's

# Digital logic families

- The IC digital logic families are
  - RTL – Resistor-transistor logic
  - DTL – Diode-transistor logic
  - TTL – Transistor-transistor logic
  - ECL – Emitter-coupled logic
  - MOS - Metal oxide semiconductor
  - CMOS – Complementary metal-oxide semiconductor
- The basic circuit in each IC digital logic family is a NAND or NOR gate.
- Each IC logic family has a data book that lists all the integrated circuits in that family.
- The differences in the logic functions are in the specific electrical characteristics of the basic gate from which the circuit is constructed.

BJT

MOSFET

# Digital logic families

- The first four digital logic families listed above – RTL, DTL, TTL, ECL- use bipolar junction transistors
- A bipolar junction transistor (BJT) can be a npn or pnp junction transistor.
- The operation of a bipolar transistor depends on the flow of two types of carriers: electrons and holes.
- The last two families- MOS and CMOS- employ a type of unipolar transistor called a metal-oxide-semiconductor field effect transistor (MOSFET or MOS in short).
- The operation of a unipolar transistor depends of the flow of one type of majority carrier ( electrons or holes).

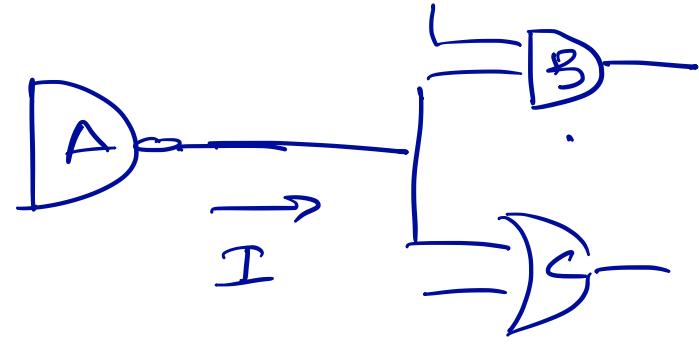
# Characteristics of logic families

- The most important parameters that are evaluated and compared in IC digital logic families are:

- Fan-out
- Power dissipation
- Propagation delay
- Noise margin
- Cost

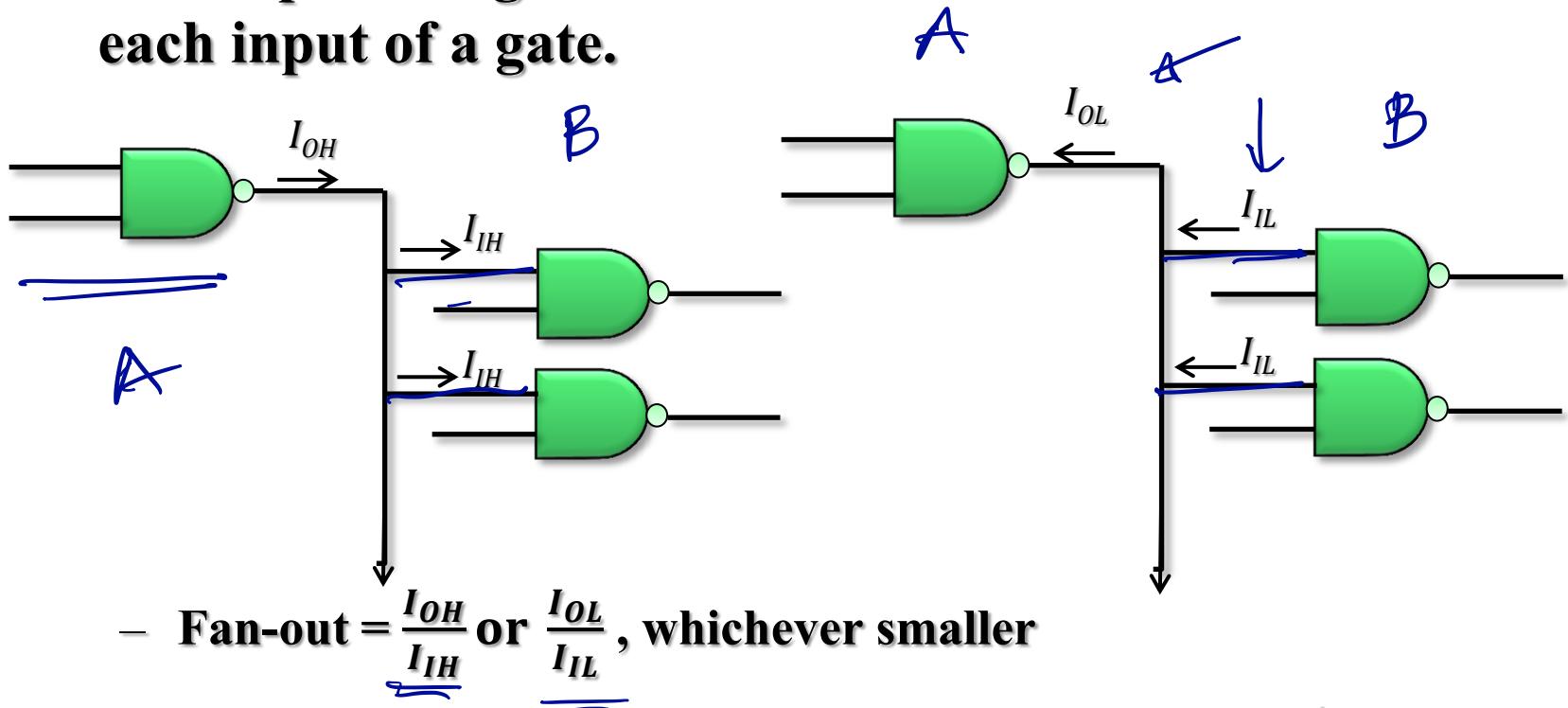
## Fan- out

- Specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation.
- A standard load refers to the amount of current needed by an input of another gate in the same logic family.



# Fan-out

- The fan-out is the maximum number of inputs that can be connected to the output of a gate and is expressed in number.
- It is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate.



# Fan-out

- For example, the standard TTL gate have the following values for the currents:

$$I_{OH} = 400\mu A \quad I_{IH} = 40\mu A$$

$$\frac{I_{OH}}{I_{IH}} = \frac{400\mu A}{40\mu A} = 10$$

$$I_{OL} = 16mA \quad I_{IL} = 1.6mA$$

$$\frac{I_{OL}}{I_{IL}} = \frac{16}{1.6} = 10$$

- The fan-out of standard TTL is 10. This means the output of a TTL gate can drive up to 10 inputs of other gates in the same logic family.

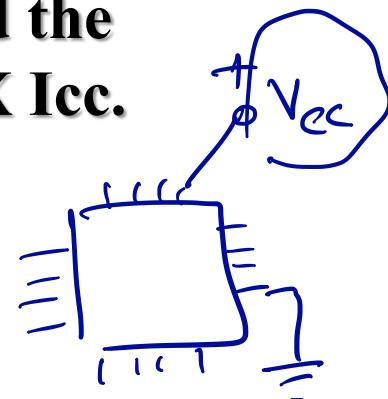
# Power Dissipation

- Specifies the amount power needed by the gate and represents the power delivered to the gate from the power supply.
- It is calculated from the supply voltage,  $V_{cc}$  and the current  $I_{cc}$  that is drawn by the circuit as  $V_{cc} \times I_{cc}$ .

$$\underline{P_D(\text{avg})} = \underline{I_{CC}(\text{avg})} \times \underline{\underline{V_{cc}}}$$

where

$$I_{CC(\text{avg})} = \frac{\underline{\underline{I_{CCH}}} + \underline{\underline{I_{CCL}}}}{2}$$

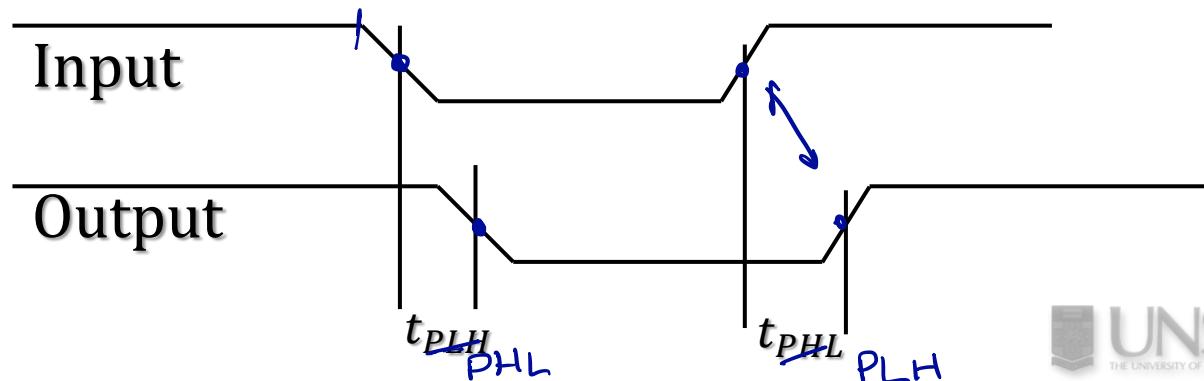


$I_{CCH}$  is the current drawn from the power supply when the output of the gate is in the high level

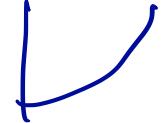
$I_{CCL}$  is the current drawn from the power supply when the output of the gate is in the low level

# Propagation delay

- Specifies the transition delay time for the signal to propagate from input to output when the binary input signal changes in value.
- The propagation delay is measured in nanoseconds (ns).
- The signals that travel from the inputs of a digital circuit to its output pass through a series of gates. The sum of the propagation delays through the gates is the total delay of the circuit.
- Propagation delay is calculated from the input and output waveforms.

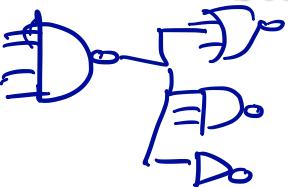


# Propagation delay

- Two delays are often considered: Low to High and High to Low.
- The two delays are not always the same and vary depending on the loading conditions.
- The longer delay of the two is taken as the propagation delay
- Example: the delays for a standard TTL are  $t_{PLH} = 7\text{ns}$  and  $t_{PHL} = 11\text{ns}$  and are measured with a load resistance of 400 ohms and a load capacitance of 15pF.
- Propagation delay of a transistor circuit depends on two factors: storage time and RC time constants.
- Usually, manufacturers supply a formula or table that considers a fixed delay plus a delay per standard load times the standard loads driven.

# Propagation delay

- Example: A 4 input NAND gate output is attached to the inputs of the following gates with the given number of standard loads representing their inputs:



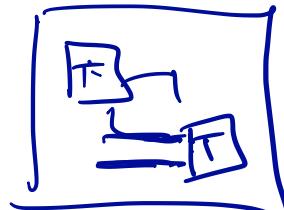
4-input NOR gate - 0.8 standard load

3-input NAND gate – 1.00 standard load, and  
inverter – 1.00 standard load.

The formula for the delay of the 4-input NAND gate is

$$t_{Pd} = 0.07 + 0.021 \times SL \text{ ns}$$

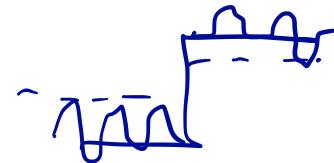
$$t_{Pd} = \underline{0.07} + 0.021 \underline{(0.8 + 1 + 1)} \text{ ns} = \underline{0.129 \text{ ns}}$$



- In modern high-speed circuits, the portion of the gate delay due to wiring capacitance is often significant. Often it is difficult to evaluate since it depends of the layout of the wires in the integrated circuit.

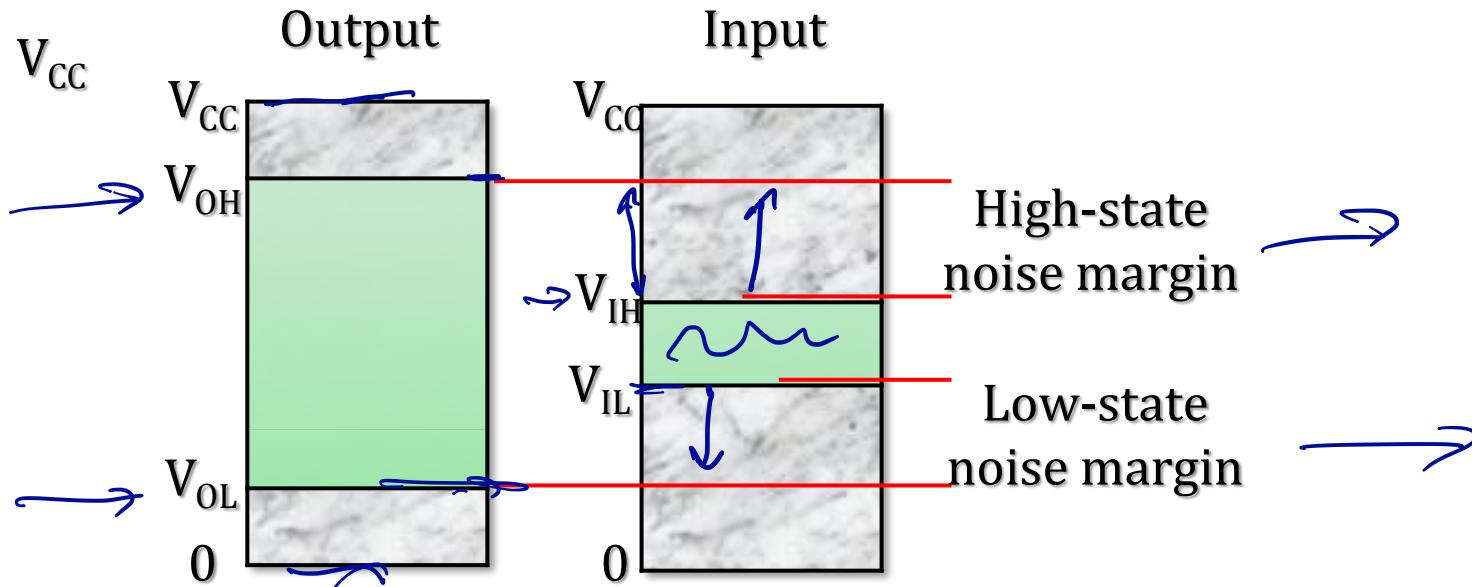
# Noise Margin

- It refers to the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit's output.
- Noises are unwanted signals that are superimposed on the normal operating signal.
- It is expressed in volts and represents the maximum noise that can be tolerated by the gate.
- Calculated for the knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate.



# Noise Margin

- It is expressed in volts and represents the maximum noise that can be tolerated by the gate.
- Calculated for the knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate.



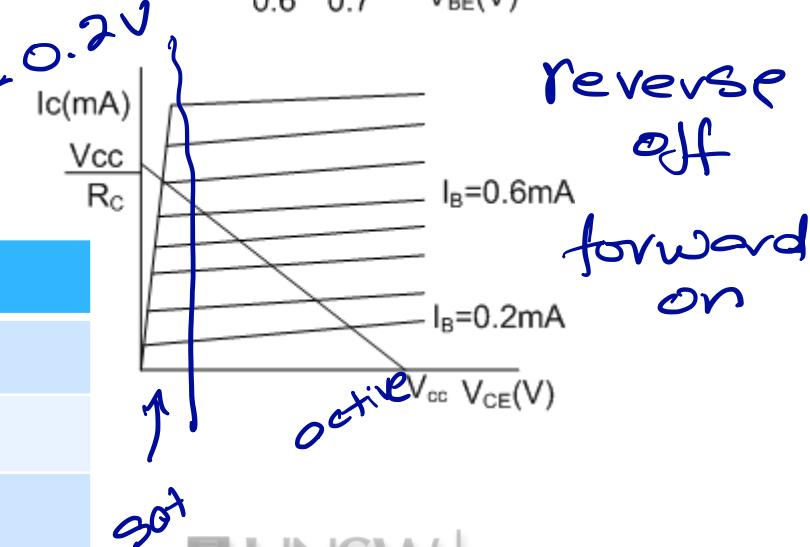
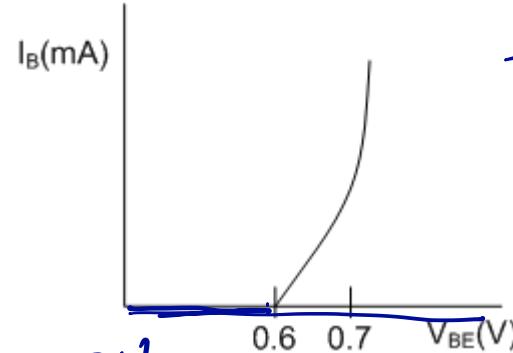
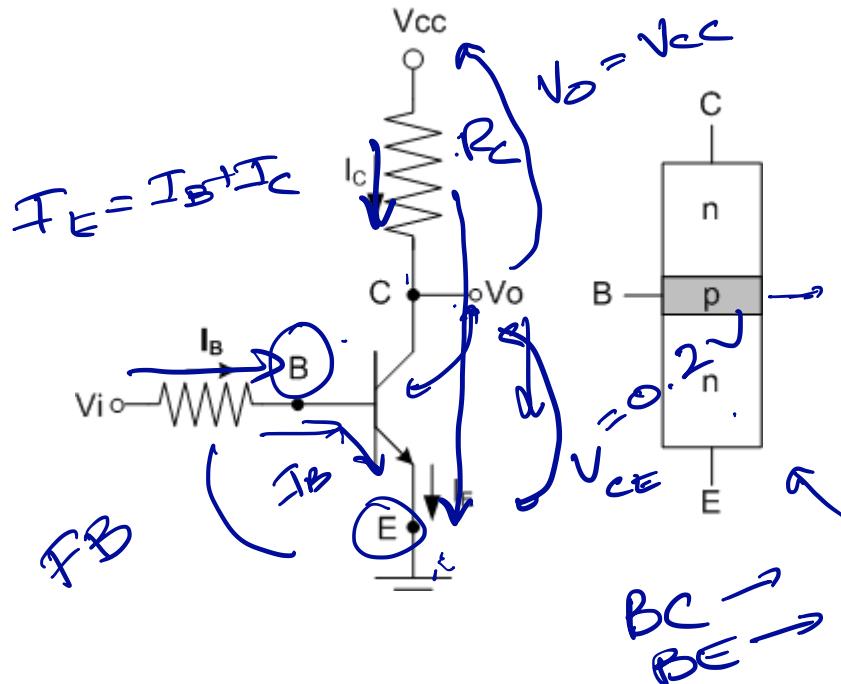
# Cost

- In an integrated circuit:
  - The cost of a gate is proportional to the chip area occupied by the gate
  - The gate area is roughly proportional to the number and size of the transistors and the amount of wiring connecting them
  - Ignoring the wiring area, the gate area is roughly proportional to the gate input count
  - So gate input count is a rough measure of gate cost
- If the actual chip layout area occupied by the gate is known, it is a far more accurate measure

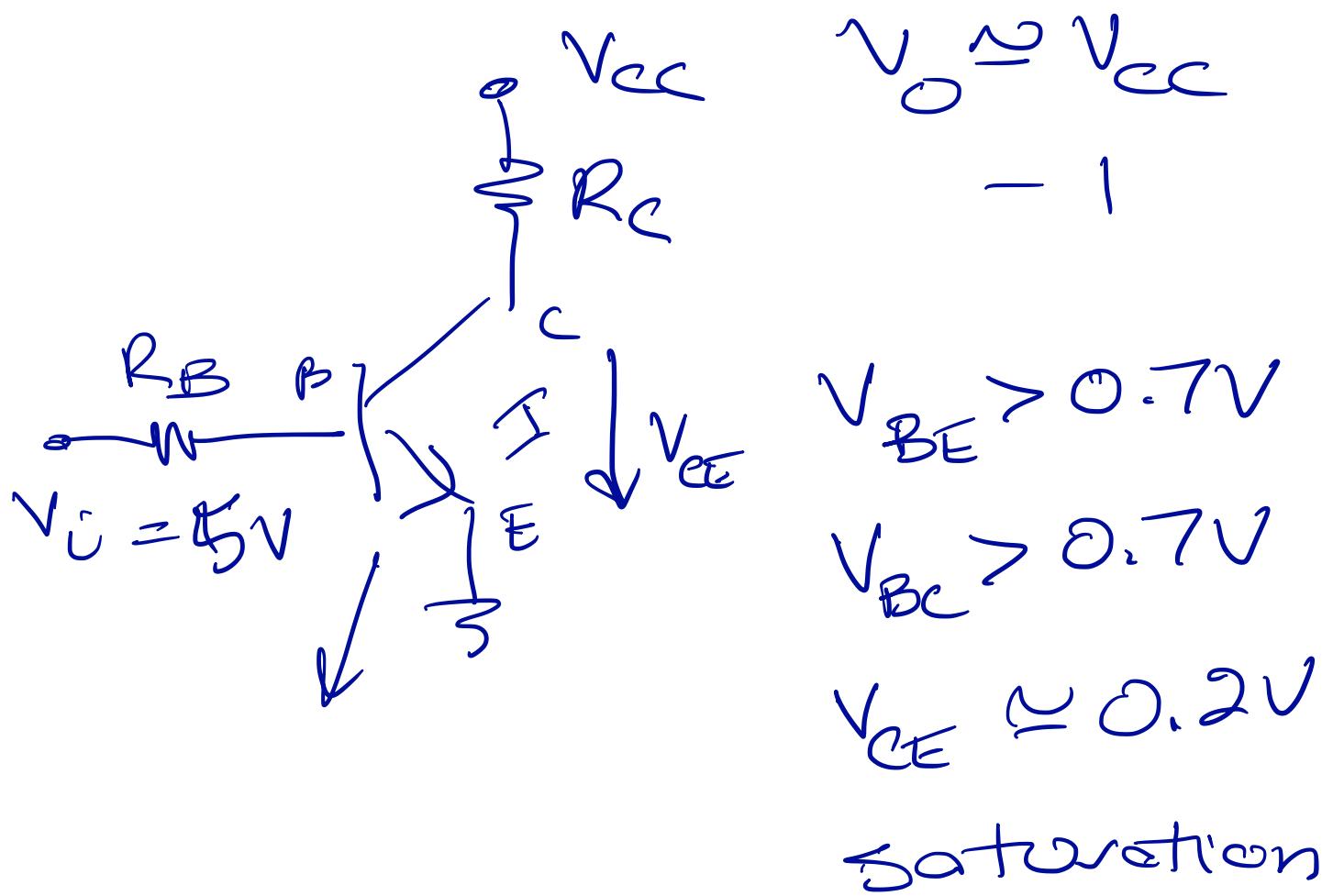
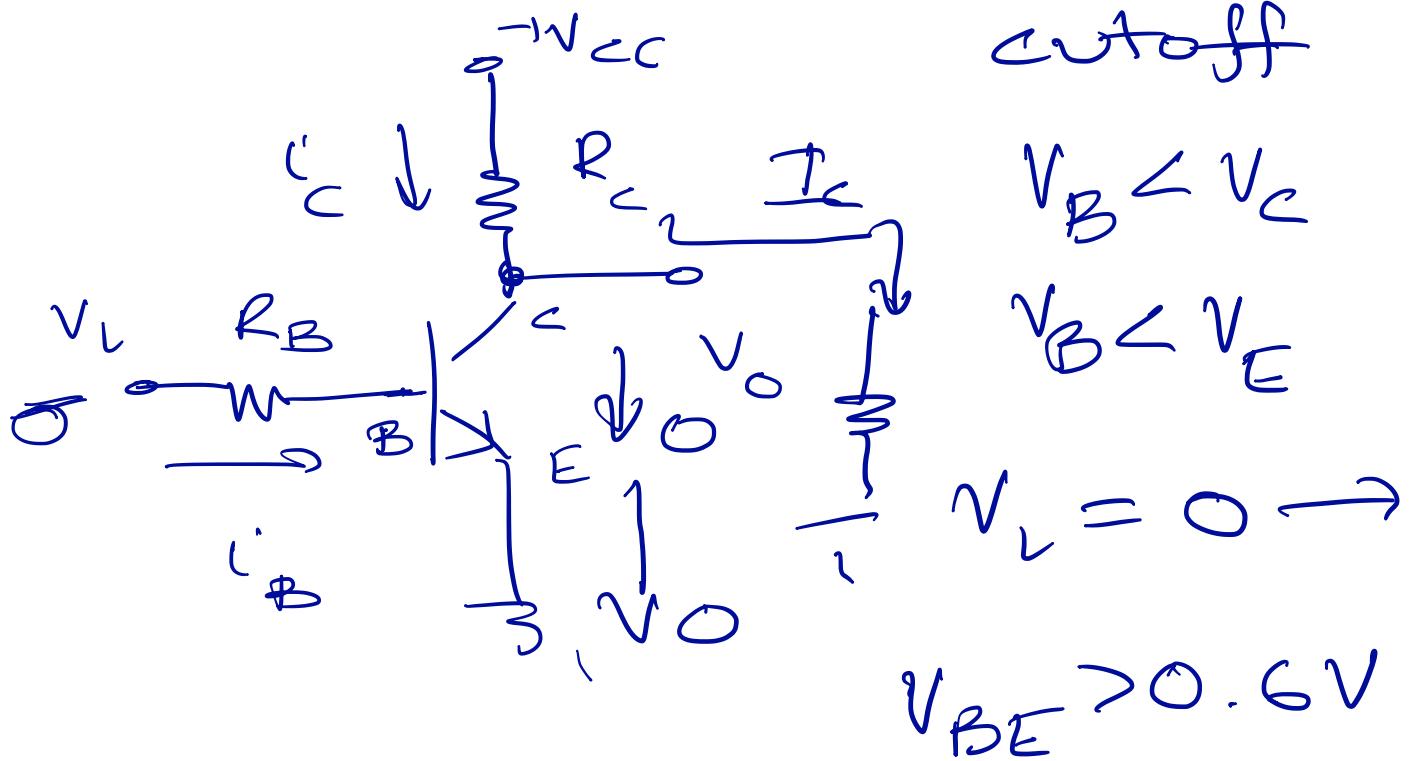
# Bipolar-Transistor characteristics

- Bipolar transistors may be of the npn or pnp type.  
Typical bipolar IC transistors are npn type.

C B E  
NPN  
PnP



Region	$V_{BE}$ (V)	$V_{CE}$ (V)	Current
Cutoff	<0.6	Open Circuit	$I_B = I_C = 0$
Active	0.6-0.7	>0.8	$I_C = h_{fe} I_B$
Saturation	0.7-0.8	0.2	$I_B \geq I_{CS}/h_{fe}$

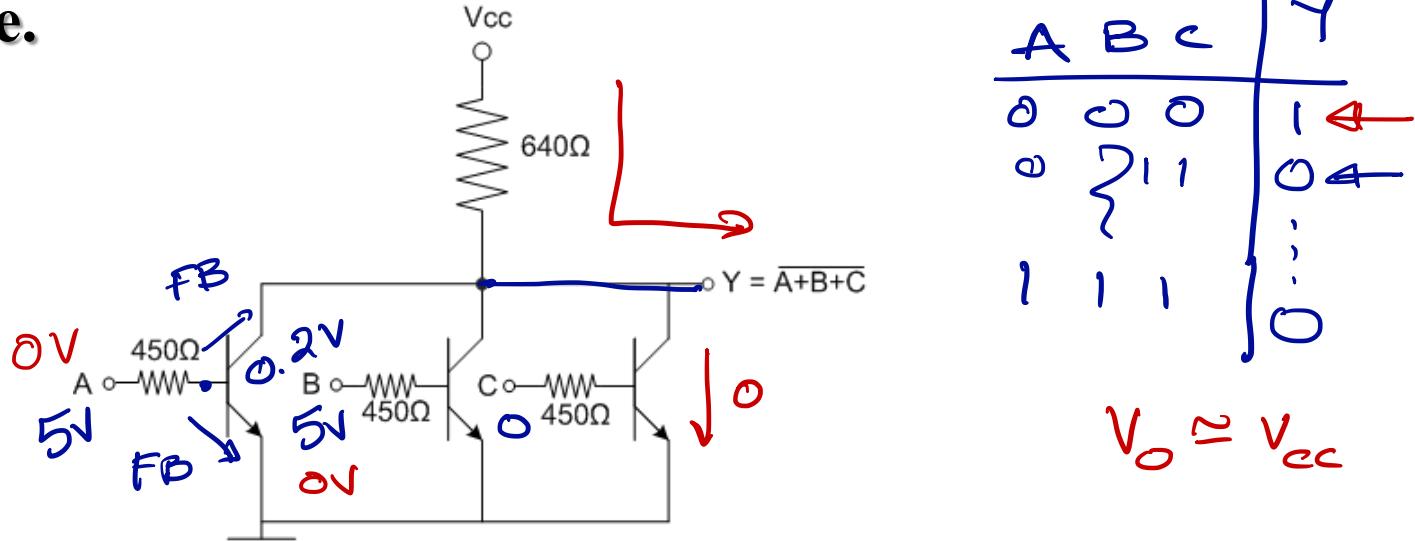


$$V_O \approx 0.2V$$

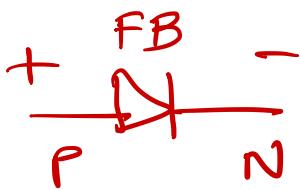
- C

# RTL circuits

- The basic circuit of the RTL digital logic family is the NOR gate.



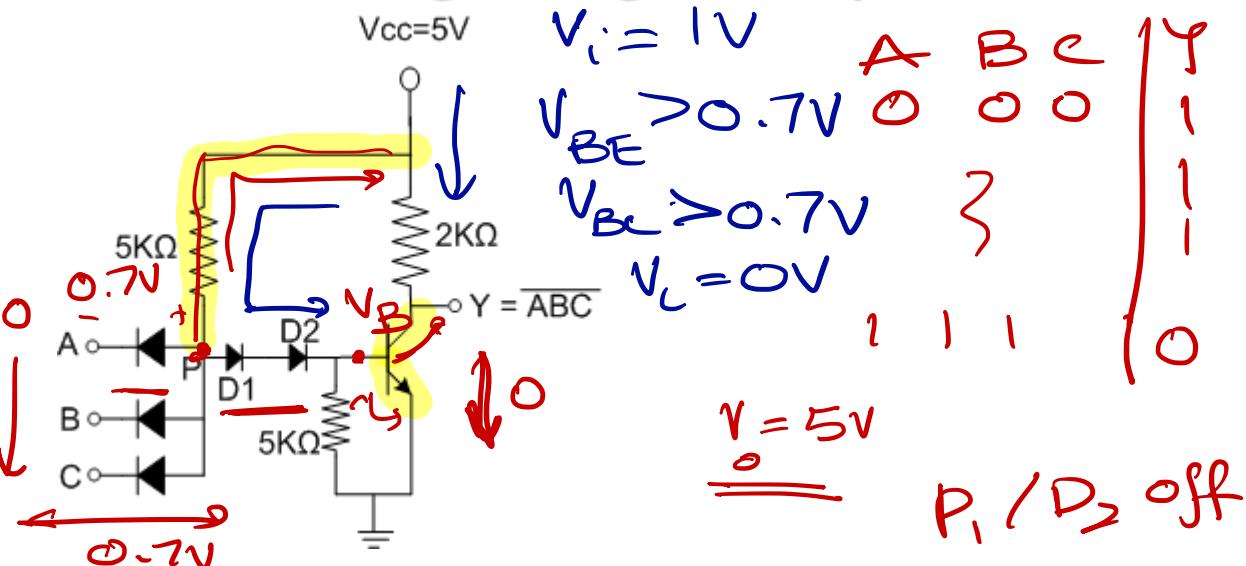
- The noise margin for low signal input is  $0.6 - 0.2 = 0.4$
- The fan-out of the RTL is limited by a high output voltage. Any voltage below 1V in the output may not drive the next transistor into saturation.
- Fan out, power dissipation, and propagation delay are 5, 12mW and 25ns respectively.



# DTL circuits

- The basic circuit of the DTL digital logic family is the NAND gate.

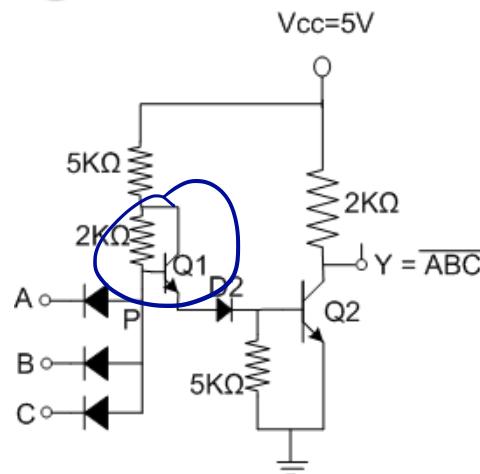
$V_P > V_A > 0.7V$   
 FB - diodes  
 $V_P = 0.7V$



- The two voltage levels are 0.2 V for low and 4-5V for high level.
- If any input of the gate is low at 0.2V, the corresponding input diode conducts current through Vcc and the 5-KΩ resistor into the input node. The potential at P will not be sufficient enough to forward drive the two diodes and Q1. Hence, Q1 will be switched off, sending Y to high.

# DTL circuits

- When all inputs are high, D1, D2 and Q1 will be driven by Vcc through  $5\text{K}\Omega$ . With Q1 in saturation region, the output voltage Y will sit at 0.2V ( low).
- The power dissipation is about 12mW and the propagation delay averages 30ns. The noise margin is about 1V and the fan-out can go as high as 8.
- The fan-out is limited by the maximum current that flow in the collector of the saturated transistor. It can be increased by replacing D1 with a transistor.



# TTL circuits

- The original basic transistor-transistor logic (TTL) gate was a slight improvement over DTL gate.
- TTL is now the most commonly used BJT based logic family in the design of digital systems.
- Currently, MOS and CMOS are the dominant technologies in VLSI circuits.
- The basic logic circuit of TTL digital logic family is NAND gate.
- There are several subfamilies or series of TTL technology.

# TTL circuits

TTL series name	Prefix	Fan-out	Power dissipation (mW)	Propagation delay	Speed-power product
Standard	74	10	10	9	90
Low Power	74L	20	1	33	33
High speed	74H	10	22	6	132
Schottky	74S	10	19	3	57
Low-power Schottky	74LS	20	2	9.5	19
Advanced Schottky	74AS	40	10	1.5	15
Advanced low-power schottky	74ALS	20	1	4	4
Fast	74F	20	4	3	12

# TTL circuits

- The standard TTL gate has been designed with different resistor values to produces gates with lower power dissipation or with higher speed.
  - In high speed TTL: reduce resistor to reduce propagation delay, but causes more power dissipation
  - In low power TTL: increase resistor to reduce power dissipation, but causes longer propagation delay.
- The schottky TTL increase speed of operation without an excessive increase in power dissipation. It removes the storage time delay by preventing the transistor from going into saturation.
- TTL gates come in three different types of output configuration: Open- collector output, Totem-pole output and Three-state output.

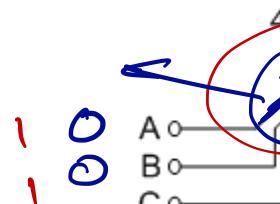
# TTL circuits

- Open-collector output

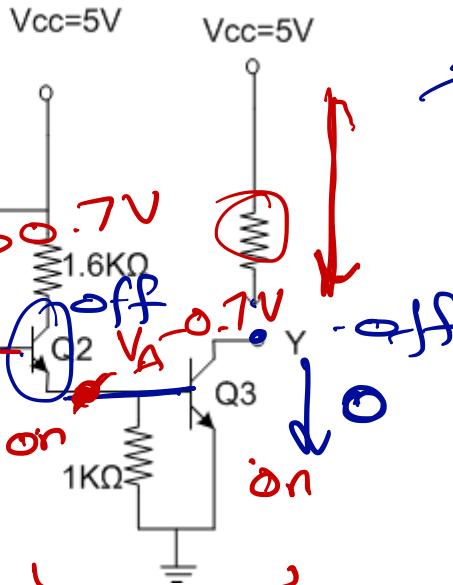
$$V_C = A = B = C = 1$$

$$V_O = 0$$

$$V_{BE} - \text{on}$$



$$V_{BE} - \text{off}$$



$$\begin{matrix} A \\ 1 \\ 1 \\ 1 \end{matrix} \quad \begin{matrix} B \\ 0 \\ 0 \\ 1 \end{matrix} \quad \begin{matrix} C \\ 0 \\ 1 \\ 1 \end{matrix}$$

$$\left. \begin{matrix} Y \\ 1 \\ 1 \\ 0 \end{matrix} \right\}$$

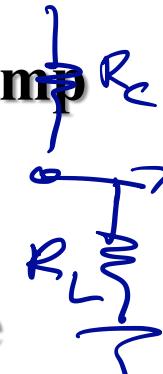
B K npn  
E

K

pnp

$$Y \approx V_{cc} \approx V_O$$

— High



$$R_L \gg R_C$$

$$V_O \approx V_{cc}$$

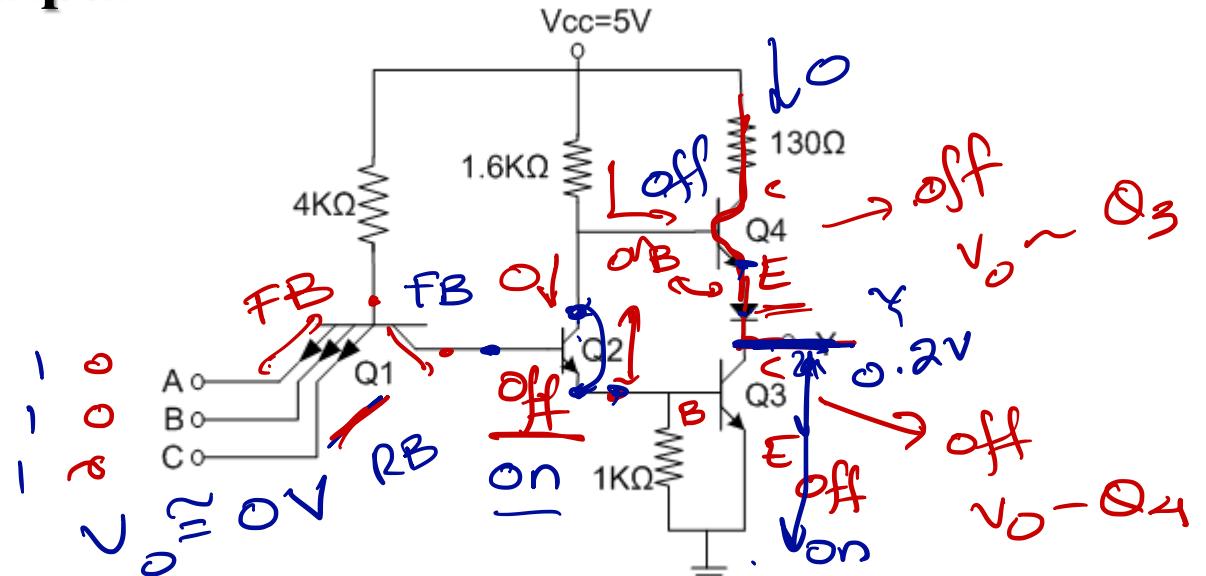
- Three applications of open-collector gates: driving a lamp or relay, perform wired logic and constructing a common-bus system.
- The propagation delay is limited by the load resistance and capacitance.

# TTL circuits

- Totem-Pole output

A	B	C	Y
0	0	0	1
1	1	1	0
1	0	0	1
0	1	0	1

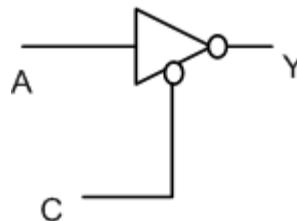
$Q_4$  on  $V_o \sim V_{cc}$



- Replacing the passive pull-up resistor  $R_L$  with active pull-up circuit, it is possible to reduce propagation by almost 4 fold.
- This comes at a price of higher power dissipation.  $V_o = V_{CE}$
- Schottky TTL gate can achieve higher speed at lower power dissipation.  $\Delta 0.2V$  — low

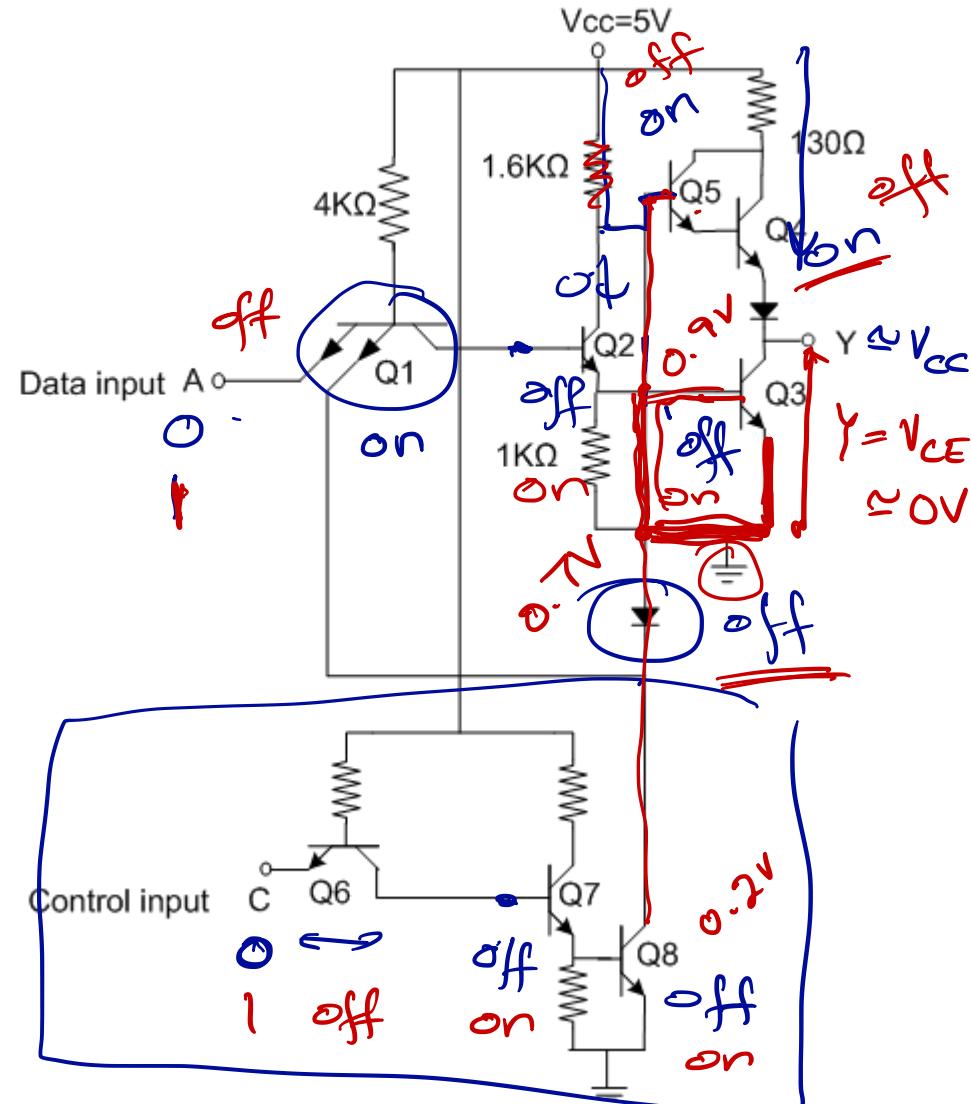
# TTL circuits

## Three-state Gate



- $Y = A'$  if  $C = \text{low}$  and  
 $Y$  high impedance if  
 $C = \text{high}$

$C$	$A$	$Y$
0	0	1
0	1	0
1	0	high Z
1	1	high Z

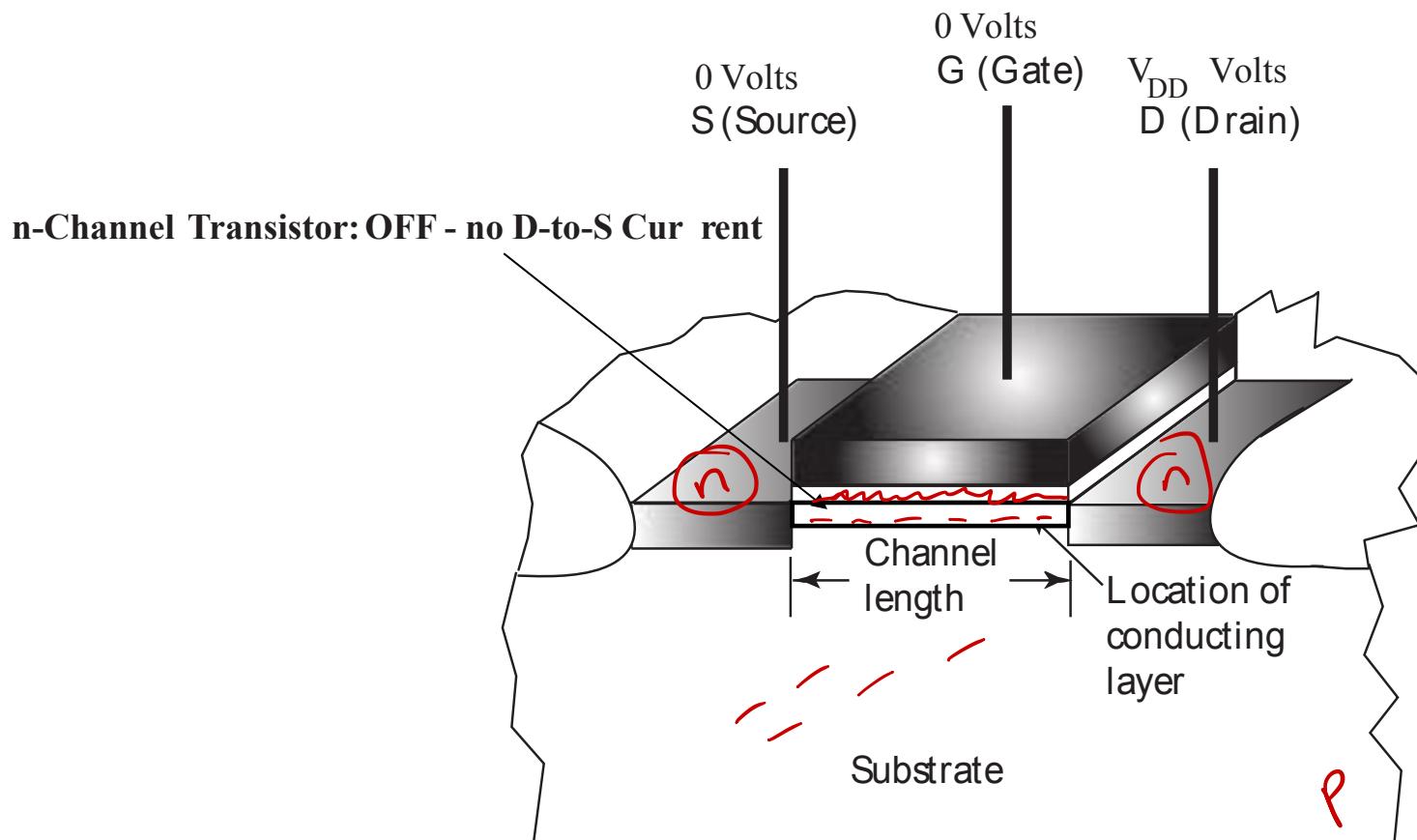


# ECL circuits

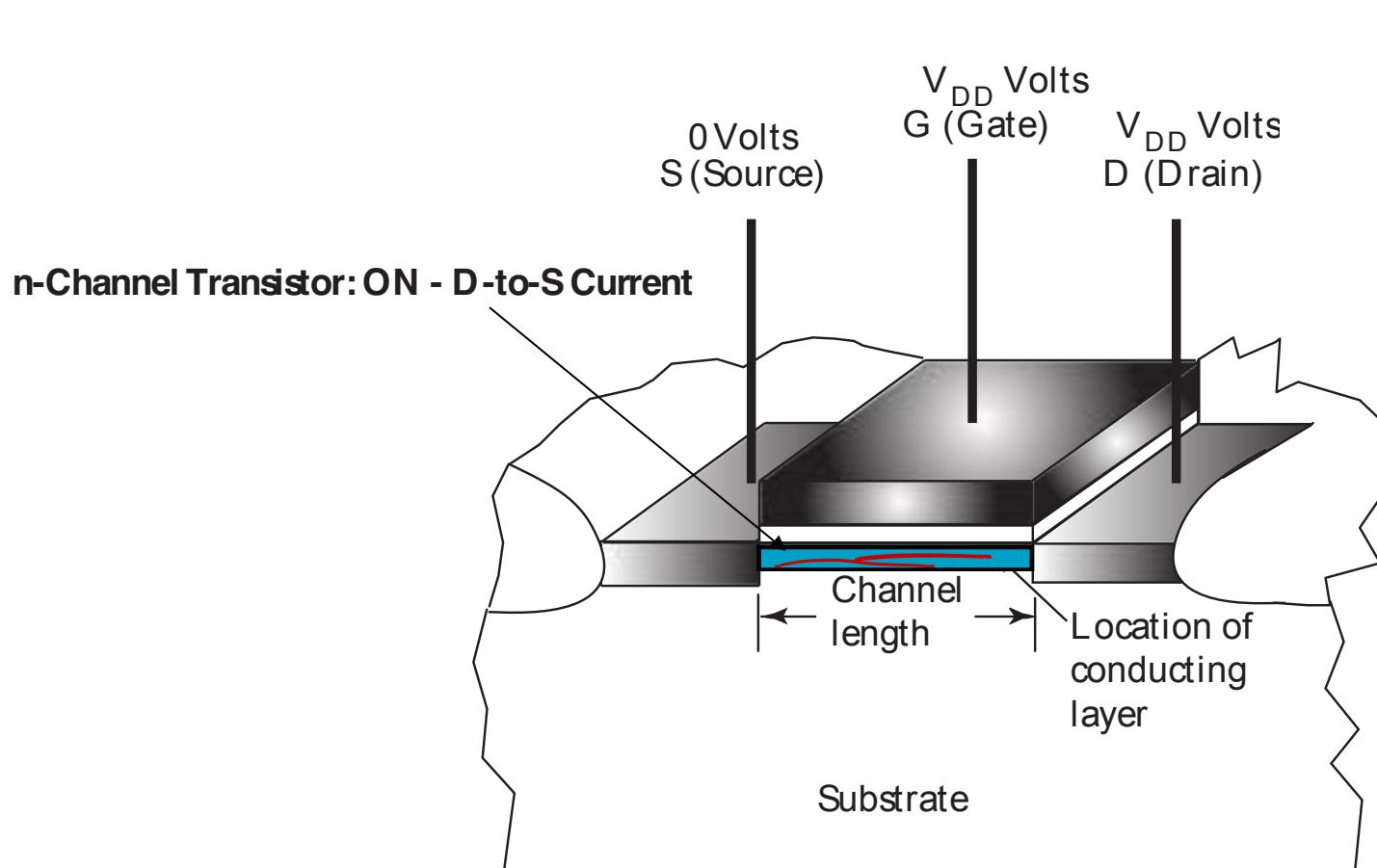
- ECL ( Emitter-coupled logic) is a nonsaturated digital logic family. Since transistors do not saturate, it is possible to achieve propagation delays as low as 1-2ns.
- Its noise immunity and power dissipation are the worst of all the logic families available. 

# MOS circuits

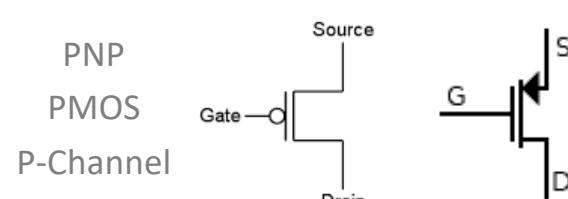
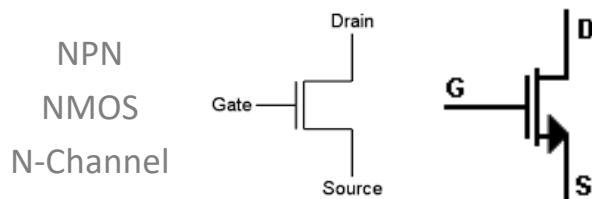
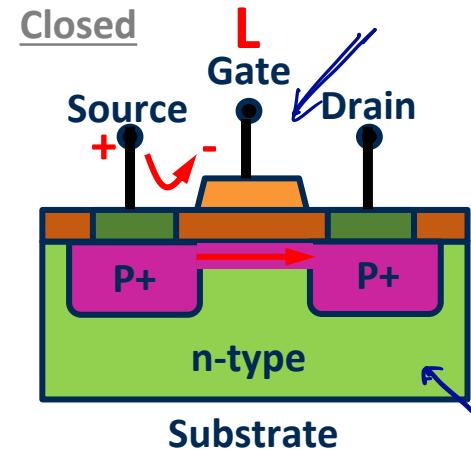
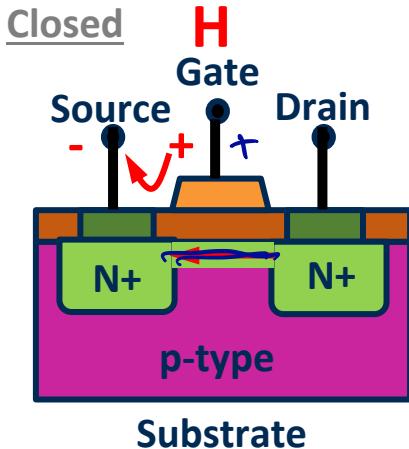
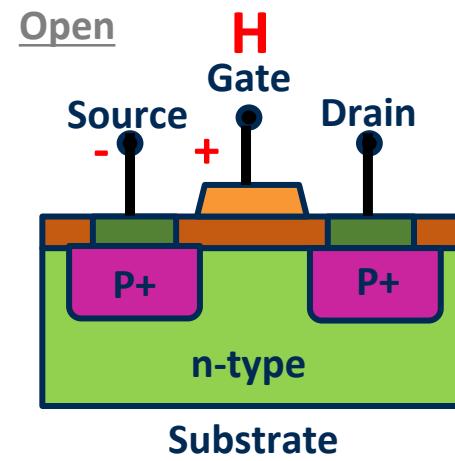
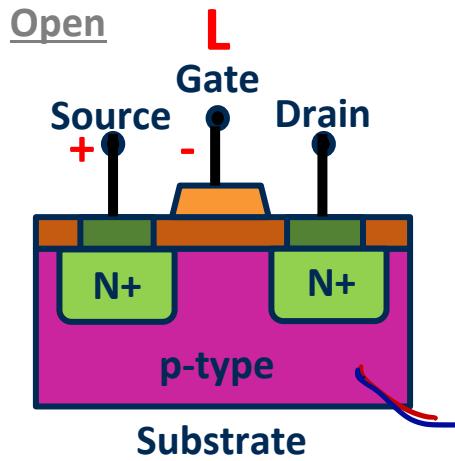
- 



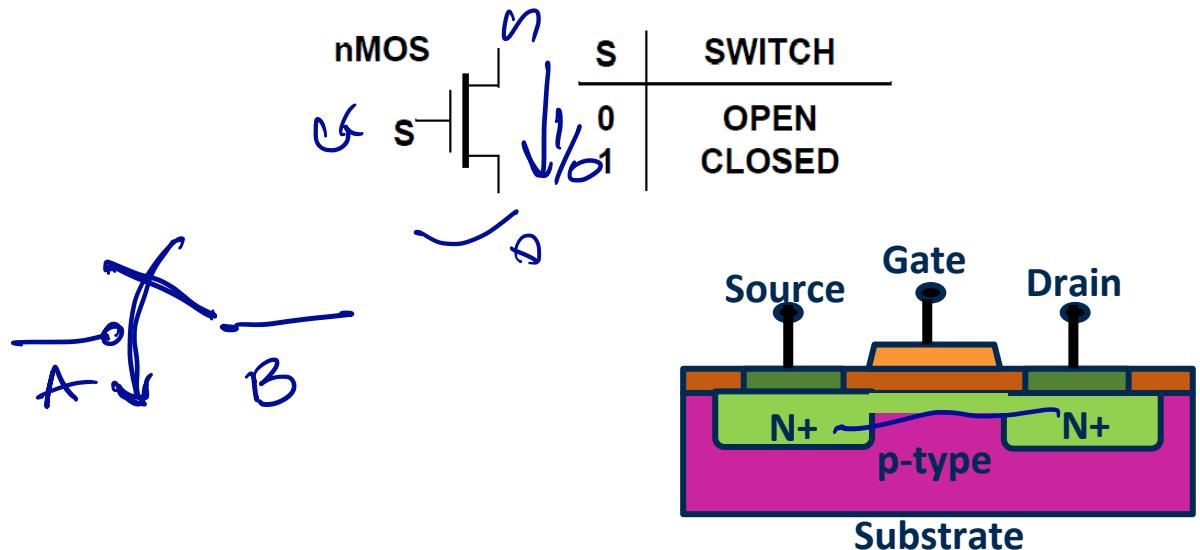
# MOS circuits



# Semiconductor switches: n-type & p-type

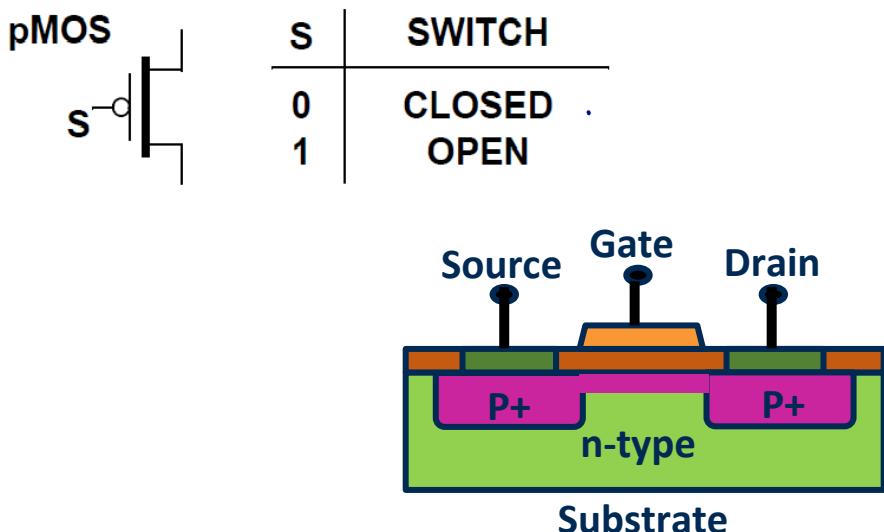


# Semiconductor switches: n-type & p-type



## nMOS when CLOSED

- Transmits logic level 0 well ↗
- Transmits logic level 1 poorly

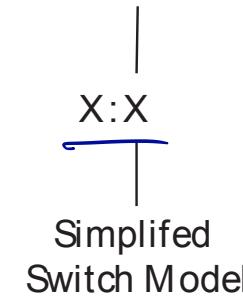
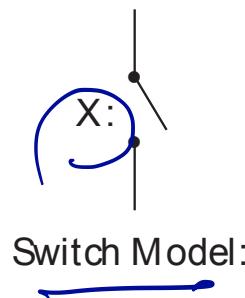
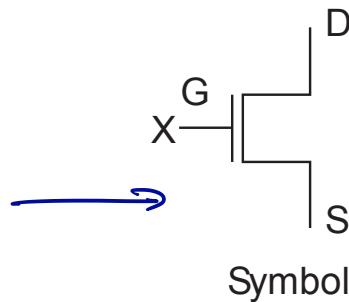


## pMOS when CLOSED

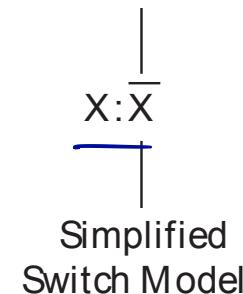
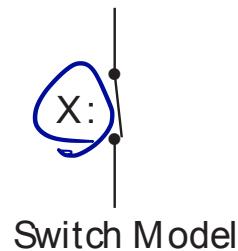
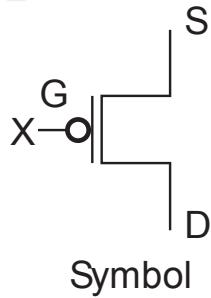
- Transmits logic level 1 well ↗
- Transmits logic level 0 poorly

# Switching model of MOS

- **n-Channel – Normally Open (NO) Switch Contact**

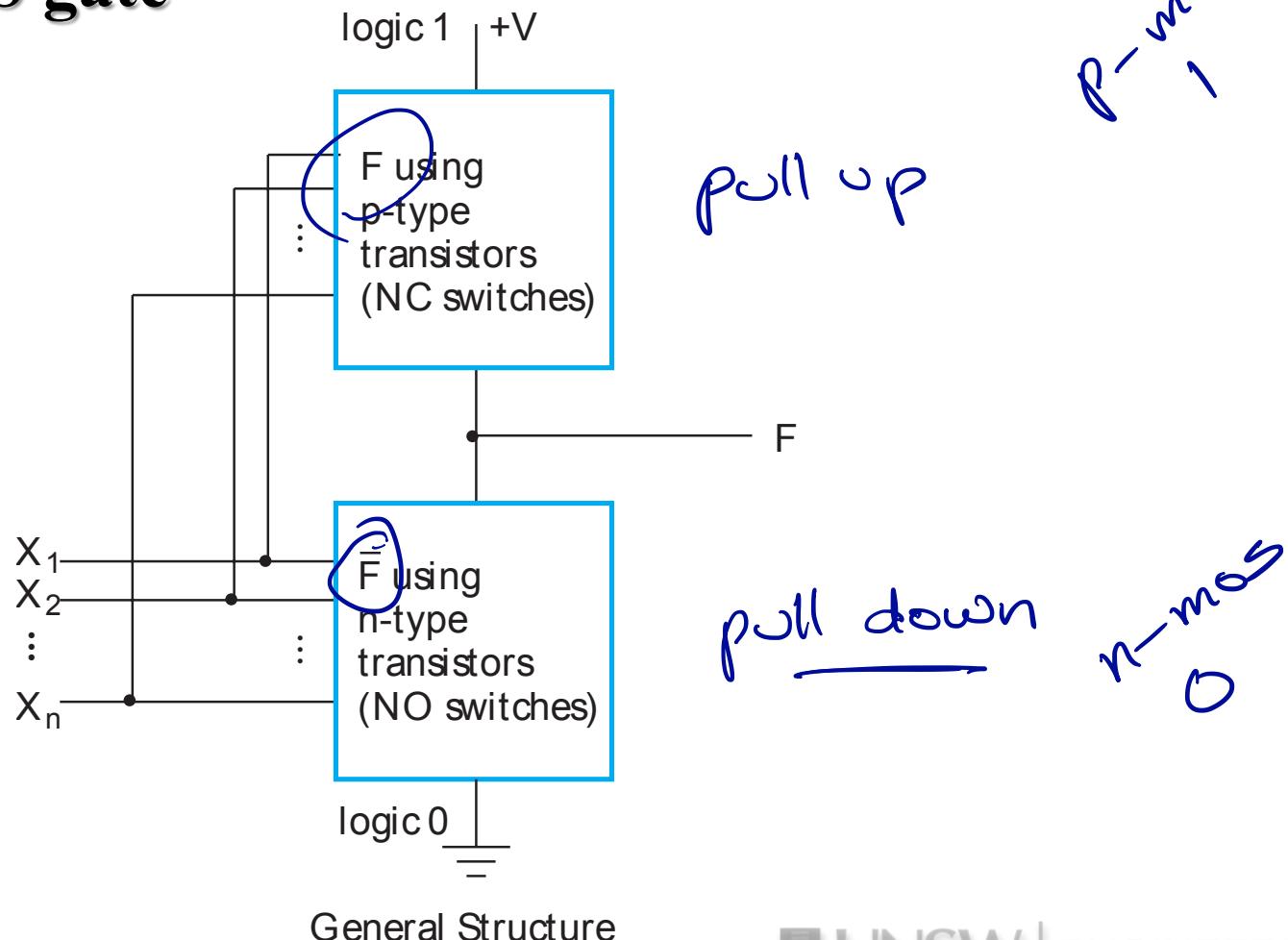


- **p-Channel – Normally Closed (NC) Switch Contact**



# Fully complementary MOS

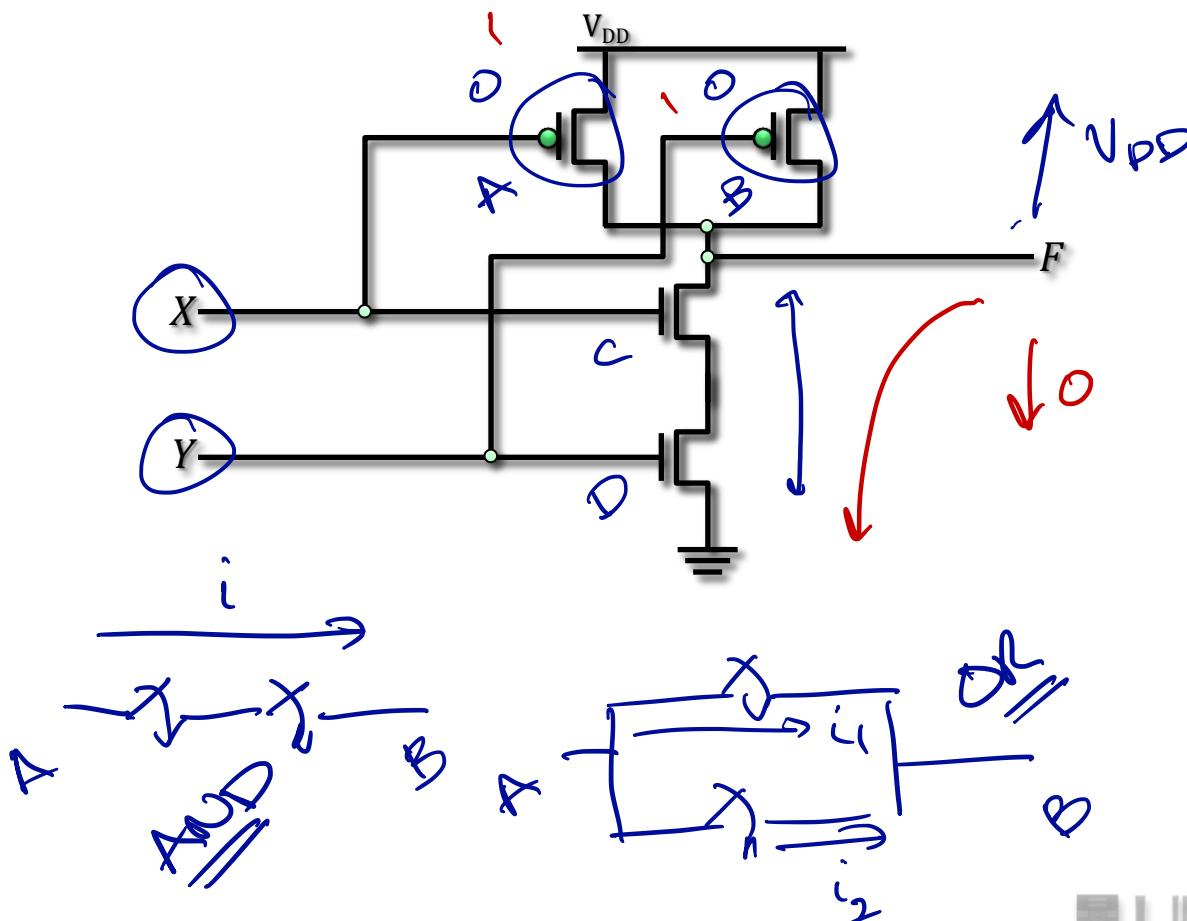
- Circuit structure for fully-complementary CMOS gate



# CMOS NAND implementation

## Implement NAND

$$F = \overline{AB} = \overline{A} + \overline{B}$$
$$\overline{F} = \underline{AB}$$

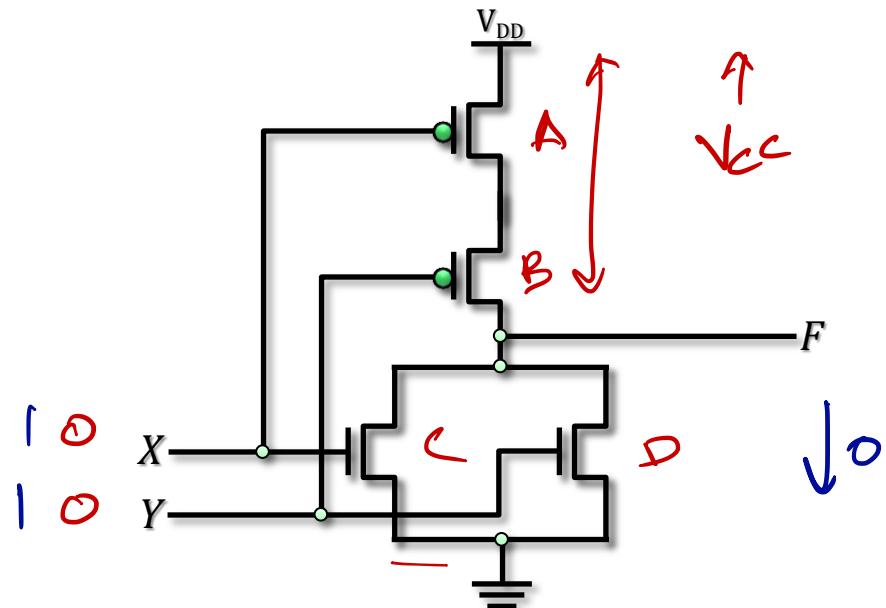


X	Y	F
L	L	H
L	H	H
H	L	H
H	H	L

# CMOS NOR implementation

- Implement NOR

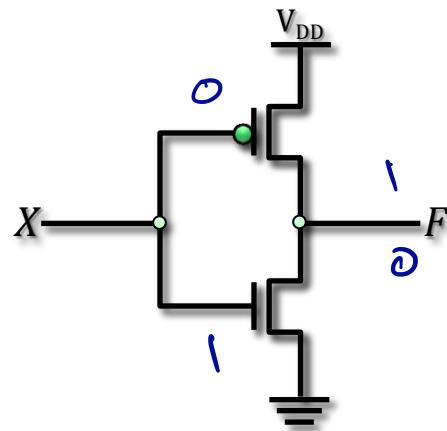
$$F = \overline{X+Y} = \overline{\overline{X}\overline{Y}}$$
$$\bar{F} = X+Y$$



X	Y	F
L	L	H
L	H	L
H	L	L
H	H	L

# CMOS NOT implementation

- Implement NOT



X	F
L	H
H	L

# CMOS for any Boolean function

- Find a CMOS gate with the following function:

$$F = \bar{X}Z + \bar{Y}Z = (\bar{X} + \bar{Y})Z$$

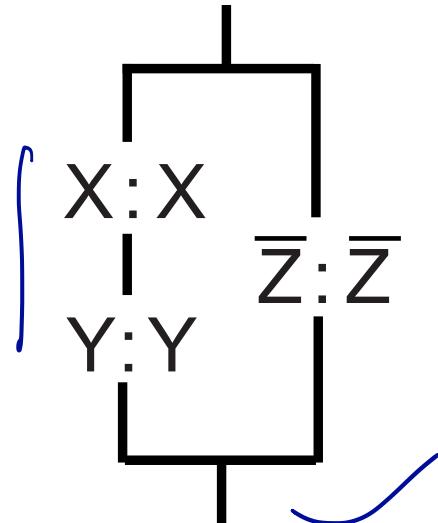
p-mos  
NC  
F

- Beginning with  $F_0$ , and using  $\bar{F}$

$F_0$  Circuit:  $\bar{F} = X\bar{Y} + \bar{Z}$

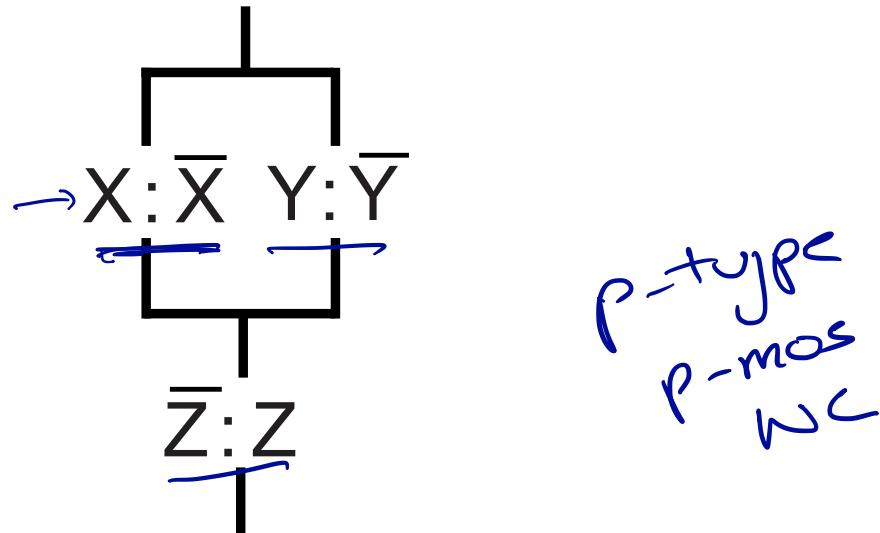
$\bar{F}$   
NO  
n-mos

- The switch model circuit in terms of NO switches:



# CMOS any Boolean function

- The switch model circuit for F1 in terms of NC contacts is the dual of the switch model circuit for F0:



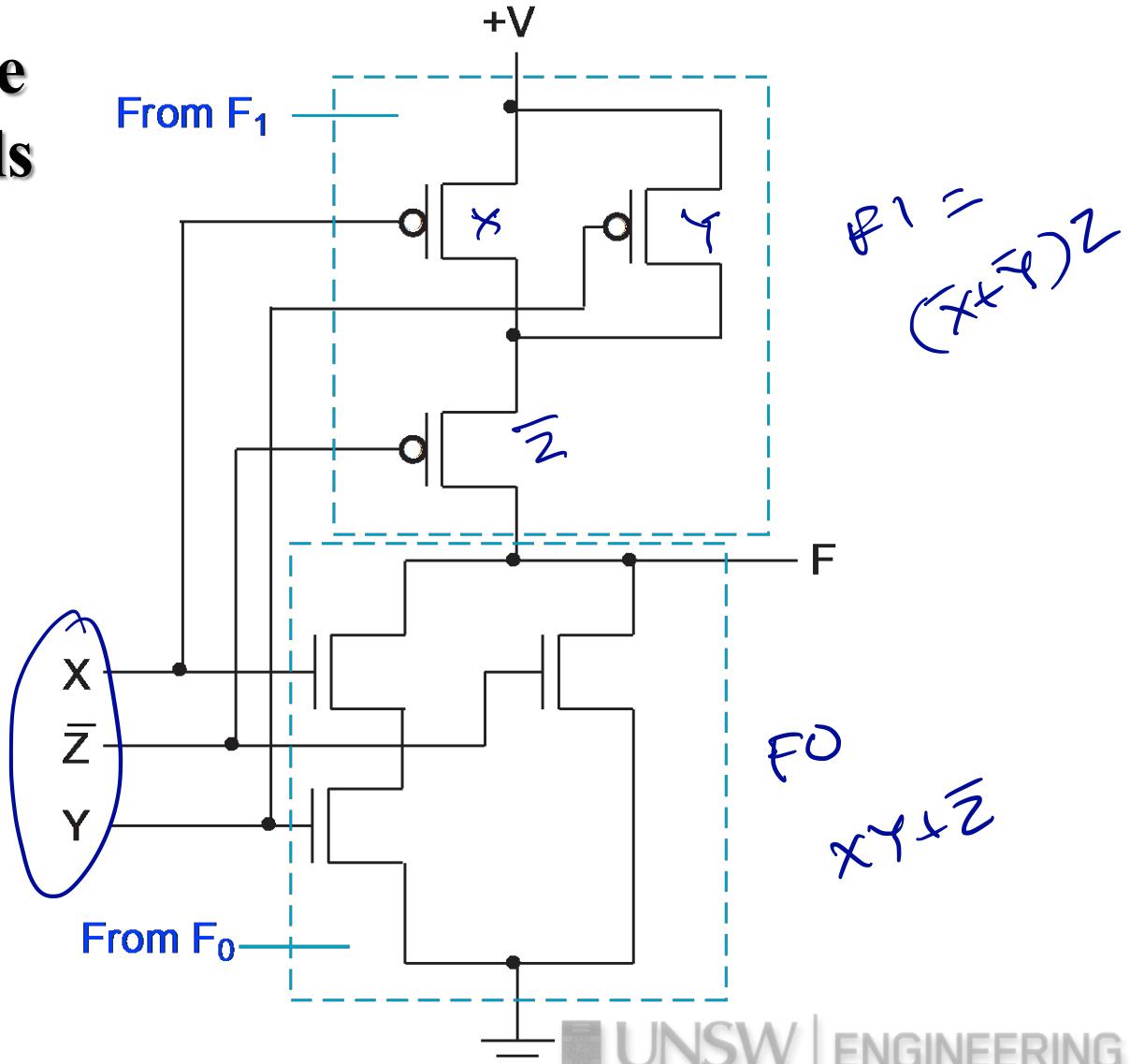
- The function for this circuit is:

$$F1 \text{ Circuit: } F = (\overline{\underline{X}} + \overline{\underline{Y}}) \underline{\underline{Z}}$$

which is the correct F.

# CMOS any Boolean function

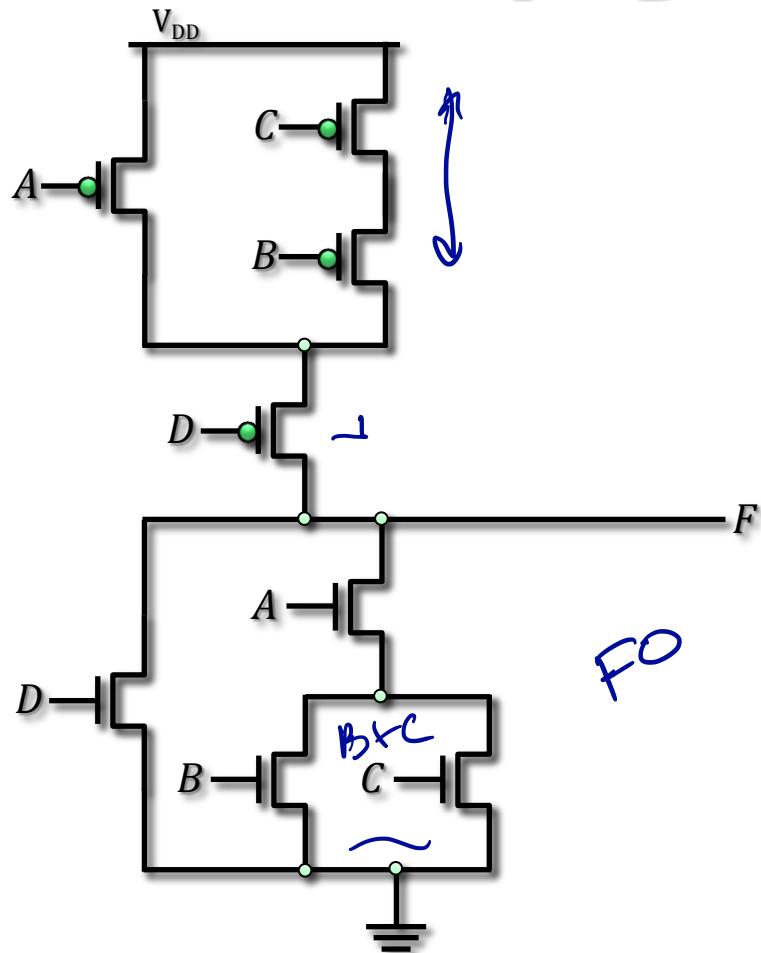
- Replacing the switch models with CMOS transistors; note input Z must be used.



# CMOS any Boolean function

- Example – implement the function:

$$F = \overline{D + A(B + C)}$$

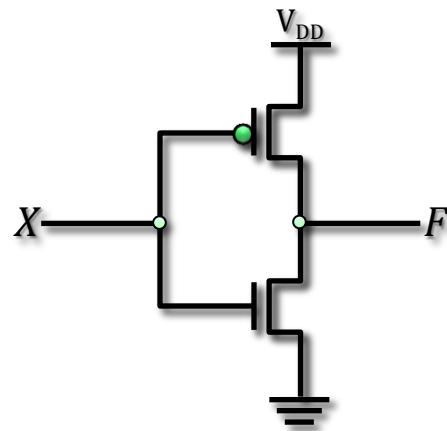


$$\begin{array}{l} FO \\ \overline{F} = \underline{D} + \underline{A}(\underline{B} + \underline{C}) \end{array}$$

$$\begin{aligned} F &= \overline{D} [\overline{A(B+C)}] \\ &= \overline{D} [\overline{A} + (\overline{B+C})] \\ &= \overline{D} [\overline{A} + \overline{B}\overline{C}] \end{aligned}$$

# CMOS NOT implementation

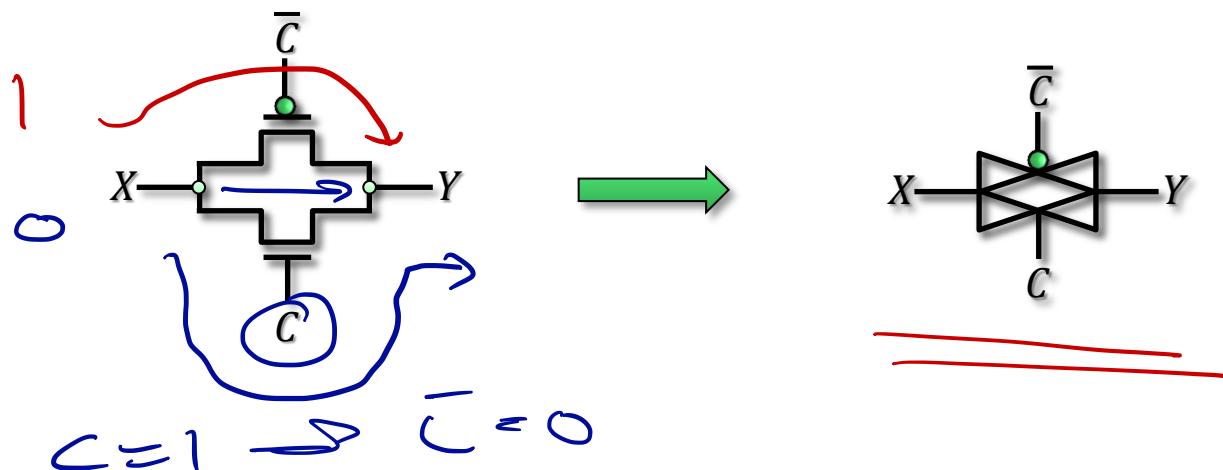
- Implement NOT



X	F
L	H
H	L

# Transmission Gates

- A *Transmission Gate* is constructed using one NMOS and one PMOS transistors:



$$C=0 \Rightarrow \bar{C}=1 \quad X \neq Y$$

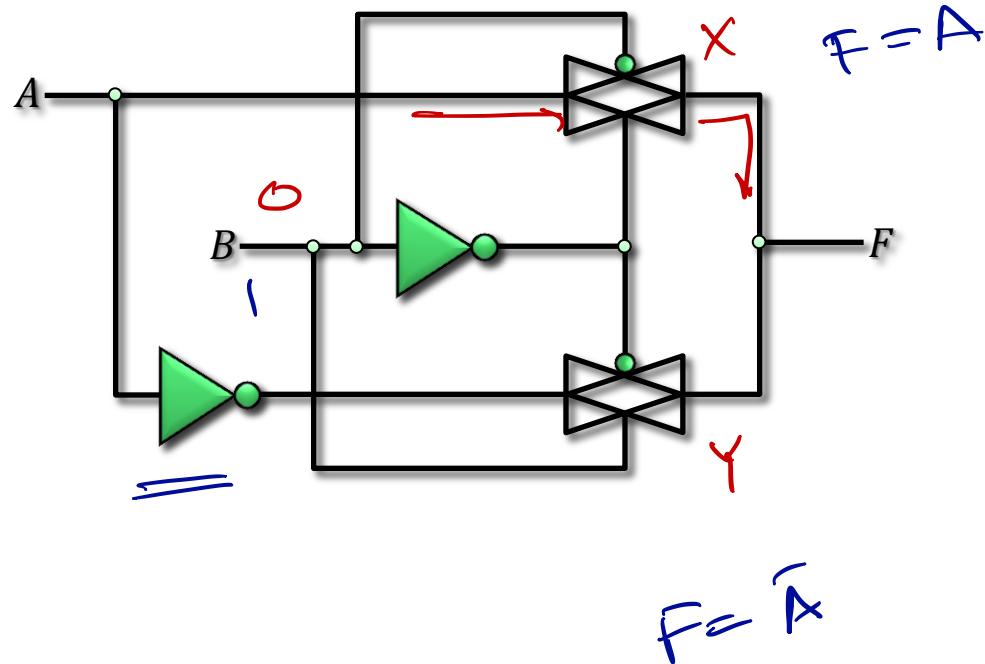
High-Z

# Transmission gates

- A transmission gate acts as an electronic switch
- It is used to pass or block a signal between two points in the circuit
- When  $C = 1$  ( $\bar{C} = 0$ ), one of the transistors will be on (depending on the value of  $X$ ) and a path exists between  $X$  and  $Y$
- When  $C = 0$  ( $\bar{C} = 1$ ), both transistors will be off (regardless of the value of  $X$ ) and no path exists between  $X$  and  $Y$

# CMOS XOR gates

- Example – implement an XOR gate using transmission gates:



A	B	F
L	L	L
L	H	H
H	L	H
H	H	L