luna UART Registers

Contents

1. UART

1.1. Features

The UART is 16450 compatible, which contains 16 byte FIFOs. In addition, auto flow control is provided, in which, auto-CTS mode (CTS controls transmitter) and auto-RTS mode (Receiver FIFO contents and threshold control RTS) are both supported. The baud rate can be up to 1 Mbps and programmable baud rate generator allows division of any input reference clock by 1 to (2^16-1) and generates an internal 16x clock. It provides a fully programmable serial interface, which can be configured to support 6, 7, 8 bit characters, even, odd, no parity generation and detection, and 1 or 2 stop bit generation. Last, fully prioritized interrupt control and loopback functionality for diagnostic capability are also provided.

Note1. 16C450 supports 5,6,7,8 bit characters and 1, 3/2, 2 stop bit generation.

1.2. Interface Pins

The UART interface pins are shown in the following table.

Table. UART Control Interface Pins

Signal Name	Type	Function
TXD#	O	Transmit Data.
RXD#	I	Receive Data.
RTS#	O	Request To Send.
CTS#	I	Clear To Send.

1.2.1. UART Register Set (Base Address: UART0 = 0xB800_2000, UART1=0xB8002100, UART2=0xB8002200, UART3=0xB8002300)

Table. UART Control Register Set

Offset	Size (byte)	Name	Description	Access
0x000	1	UART0_RBR	Receiver buffer register (DLAB=0).	R
0x000	1	UART0_THR	Transmitter holding register (DLAB=0).	W
0x000	1	UART0_DLL	Divisor latch LSB (DLAB=1).	R/W
0x004	1	UART0_IER	Interrupt enable register (DLAB=0).	R/W
0x004	1	UART0_DLM	Divisor latch MSB (DLAB=1).	R/W
0x008	1	UART0_IIR	Interrupt identification register.	R
0x008	1	UART0_FCR	FIFO control register.	W
0x00c	1	UART0_LCR	Line control register.	R/W
0x010	1	UART0_MCR	Modem control register.	R/W
0x014	1	UART0_LSR	Line status register.	R/W
0x018	1	UART0_MSR	Modem status register.	R/W
0x01c	1	UART0_SCR	Scratch register.	R/W
…				
0x100	1	UART1_RBR	Receiver buffer register (DLAB=0).	R
0x100	1	UART1_THR	Transmitter holding register (DLAB=0).	W
0x100	1	UART1_DLL	Divisor latch LSB (DLAB=1).	R/W
0x104	1	UART1_IER	Interrupt enable register (DLAB=0).	R/W
0x104	1	UART1_DLM	Divisor latch MSB (DLAB=1).	R/W
0x108	1	UART1_IIR	Interrupt identification register.	R
0x108	1	UART1_FCR	FIFO control register.	W

Offset	Size (byte)	Name	Description	Access
0x10c	1	UART1_LCR	Line control register.	R/W
0x110	1	UART1_MCR	Modem control register.	R/W
0x114	1	UART1_LSR	Line status register.	R/W
0x118	1	UART1_MSR	Modem status register.	R/W
0x11c	1	UART1_SCR	Scratch register.	R/W
…				
0x200	1	UART2_RBR	Receiver buffer register (DLAB=0).	R
0x200	1	UART2_THR	Transmitter holding register (DLAB=0).	W
0x200	1	UART2_DLL	Divisor latch LSB (DLAB=1).	R/W
0x204	1	UART2_IER	Interrupt enable register (DLAB=0).	R/W
0x204	1	UART2_DLM	Divisor latch MSB (DLAB=1).	R/W
0x208	1	UART2_IIR	Interrupt identification register.	R
0x208	1	UART2_FCR	FIFO control register.	W
0x20c	1	UART2_LCR	Line control register.	R/W
0x210	1	UART2_MCR	Modem control register.	R/W
0x214	1	UART2_LSR	Line status register.	R/W
0x218	1	UART2_MSR	Modem status register.	R/W
0x21c	1	UART2_SCR	Scratch register.	R/W
…				
0x300	1	UART3_RBR	Receiver buffer register (DLAB=0).	R
0x300	1	UART3_THR	Transmitter holding register (DLAB=0).	W
0x300	1	UART3_DLL	Divisor latch LSB (DLAB=1).	R/W
0x304	1	UART3_IER	Interrupt enable register (DLAB=0).	R/W
0x304	1	UART3_DLM	Divisor latch MSB (DLAB=1).	R/W
0x308	1	UART3_IIR	Interrupt identification register.	R
0x308	1	UART3_FCR	FIFO control register.	W
0x30c	1	UART3_LCR	Line control register.	R/W
0x310	1	UART3_MCR	Modem control register.	R/W
0x314	1	UART3_LSR	Line status register.	R/W
0x318	1	UART3_MSR	Modem status register.	R/W
0x31c	1	UART3_SCR	Scratch register.	R/W

Table. UART Receiver Buffer Register (DLAB=0) (0xB8002000)

Bit	Bit Name	Description	R/W	InitVal
31:24	RBR[7:0]	Receiver buffer data.	R	00H

Table. UART Transmitter Holding Register (DLAB=0) (0xB8002000)

Bit	Bit Name	Description	R/W	InitVal
31:24	THR[7:0]	Transmitter holding data.	W	00H

Table. UART Divisor Latch LSB (DLAB=1) (0xB8002000)

Bit	Bit Name	Description	R/W	InitVal
31:24	DLL[7:0]	Divisor latch LSB.	W/R	00H

Table. UART Divisor Latch MSB (DLAB=1) (0xB8002004)

Bit	Bit Name	Description	R/W	InitVal
31:24	DLM[7:0]	Divisor latch MSB.	W/R	00H

Table. UART Interrupt Enable Register (0xB8002004)

Bit	Bit Name	Description	R/W	InitVal
24	ERBI	Enable received data available interrupt.	R/W	0

25	ETBEI	Enable transmitter holding register empty interrupt.	R/W	0
26	ELSI	Enable receiver line status interrupt.	R/W	0
27	EDSSI	Enable modem status register interrupt.	R/W	0
28	ESLP	Sleep mode enable.	R/W	0
29	ELP	Low power mode enable.	R/W	0
31:30		Reserved.		00

Table. UART Interrupt Identification Register (0xB8002008, Read)

Bit	Bit Name	Description	R/W	InitVal
24	IPND	Interrupt pending. 0=Interrupt pending	R	1
27:25	IID[2:0]	Interrupt ID. IID[1:0] indicates the interrupt priority.	R	000
29:28		Reserved.	R	00
31:30	FIFO16[1:0]	00=No FIFO 11=16-byte FIFO	R	11

Table. UART FIFO Control Register (0xB8002008, Write)

Bit	Bit Name	Description	R/W	InitVal
24	EFIFO	Enable FIFO. When this bit is set, enables the transmitter and receiver FIFOs. Changing this bit clears the FIFOs.	W	0
25	RFRST	Receiver FIFO Reset. Writes 1 to clear the receiver FIFO.	W	0
26	TFRST	Transmitter FIFO Reset. Writes 1 to clear the transmitter FIFO.	W	0
27	Reserved	Reserved. Should be '0'.		0
29:28		Reserved		00
31:30	RTRG[1:0]	Receiver Trigger level. Trigger level: 16-byte 00=01, 01=04, 10=08, 11=14	W	11

Table. UART Line Control Register (0xB800200C)

Bit	Bit Name	Description	R/W	InitVal
25:24	WLS[1:0]	Word Length Select. 00=Reserved 01=6 bits 10=7 bits 11=8 bits	R/W	11
26	STB	Number of Stop Bits. 0=1 bit 1=2 bits	R/W	0
27	PEN	Parity Enable.	R/W	0
29:28	EPS[1:0]	Even Parity Select. 00=odd parity 01=even parity 10=mark parity 11=space parity	R/W	0
30	BRK	Break control. Set this bit force TXD to the spacing (low) state (break). Clear this bit to disable break condition.	R/W	0
31	DLAB	Divisor Latch Access Bit.	R/W	0

Table. UART Modem Control Register (0xB8002010)

Bit	Bit Name	Description	R/W	InitVal
24	DTR	Data Terminal Ready. 0=Set DTR# high 1=Set DTR# low	R/W	0
25	RTS	Request To Send. 0=Set RTS# high 1=Set RTS# low	R/W	0
26	OUT1	Out 1	R/W	0
27	OUT2	Out 2	R/W	0
28	LOOP	Loopback	R/W	0
29	AFE	Auto Flow control Enable	R/W	0

Table. UART Line Status Register (0xB8002014)

Bit	Bit Name	Description	R/W	InitVal
24	DR	Data Ready. Character mode: Data ready in RBR FIFO mode: Receiver FIFO is not empty.	RC	0
25	OE	Overrun Error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the receiver shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0
26	PE	Parity Error.	R	0
27	FE	Framing Error.	R	0
28	BI	Break Interrupt indicator.	R	0
29	THRE	Transmitter Holding Register Empty. Character mode: THR is empty FIFO mode: Transmitter FIFO is empty	R	1
30	TEMT	Transmitter Empty. Character mode: Both THR and TSR are empty. FIFO mode: Both transmitter FIFO and TSR are empty	R	1
31	RFE	Receiver FIFO Error. Either a parity, framing, or break error in the FIFO.	R	0

Table. UART Modem Status Register (0xB8002018)

Bit	Bit Name	Description	R/W	InitVal
31	ΔCTS	Delta clear to send. CTS# signal transmits.	R	0
30	ΔDSR	Delta data set ready. DSR# signal transmits. Returns 0.	R	0
29	TERI	Trailing edge ring indicator. RI# signal changes from low to high. Returns 0.	R	0
28	ΔDCD	Delta data carrier detect. DCD# signal transmits. Returns 0.	R	1
27	CTS	Clear To Send. 0=CTS# detected high 1=CTS# detected low	R	0

26	DSR	Data Set Ready.
		0=DSR # detected high
		1=DSR# detected low
		In loopback mode, returns bit 0 of MCR
		In normal mode, returns 1.
			R	0

Bit	Bit Name	Description	R/W	InitVal
25	RI	Ring Indicator. 0=RI# detected high 1=RI# detected low In loopback mode, returns bit 3 of MCR. In normal mode, returns 0.	R	0
24	DCD	Data Carrier Detect. 0=DCD# detected high 1=DCD# detected low In loopback mode, returns bit 2 of MCR. In normal mode, returns 1.	R	0

1.2.2. Baud Rate

Value of divisor latch = [System Clock / (16 * Baud Rate)] - 1

System Clock = Lexra Bus Clock

Example of the Divisor Latch value:

System CLK	2400 bps	4800 bps	9600 bps	19200 bps	38400 bps	57600 bps	115200 bps
200MHz	5207	2603	1301	650	325	162	80

1.2.3. Time-out Interrupt

A time-out interrupt occurs when the following conditions exists in at least one byte in the active descriptor buffer or receiver FIFO.

The most recent serial character was received more than four character times ago.

1.2.4. Auto-flow Control

Auto-RTS — When the receiver FIFO reaches the trigger level, the RTS# is de-asserted. RTS# is automatically re-asserted once the FIFO is emptied. If RTS# is de-asserted, the UART must receive the incoming data until the FIFO is full.

Auto-CTS — The transmitter checks CTS# before sending the next data byte. When CTS# is active, the transmitter sends the next data byte, otherwise it stops the transmission.

1.2.5. Loopback Diagnostic

When the LOOP bit is set, the following occurs.

TXD# is asserted high

RXD# is disconnected.

CTS#, DSR#, DCD#, and RI# are disconnected.

The output of the transmitter shift register is looped back into the input of the receiver shift register.

The MCR's DTR, RTS, OUT1, and OUT2 bits are internally connected to CTS#, DSR#, DCD#, and RI# respectively.

The DTR#, RTS#, OUT1#, and OUT2# pins are forced high.

1.2.6. Interrupt Priority

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
Bit3	Bit2	Bit1	Bit0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun, parity, framing errors or break	Read LSR
0	1	0	0	2	Received data available	DR bit is set	Read RBR
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to FIFO during the last character times and at 1 character in it.	Read RBR
0	0	1	0	3	Transmitter holding register empty	THRE bit set	Reading IIR or write THR
0	0	0	0	4	Modem status	CTS#, DSR#, RI#, DCD#	Reading MSR

Bit[7:6]={EFIFO,EFIFO} Bit[5:4]={0,0} Bit[0]={~uart_ip}

1.2.7. Loopback Diagnostic

A break characters is an all-zero character whose length is start bit (1) + word length (7 or 8) + parity bit (0 or 1) + stop bits (1 or 2). The break event occurs after the first break character is received.

1.2.8. Break

A break characters is an all- zero character whose length is start bit (1) + word length (7 or 8) + parity bit (0 or 1) + stop bits (1 or 2). The break event occurs after the first break character is received