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# RTL9601-CG

# IEEE 10/100/1000M ETHERNET/ PON NETWORK BRIDGE PROCESSOR

## PRELIMINARY DATASHEET

**(CONFIDENTIAL: Development Partners Only)**

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## USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek Ethernet/PON network bridge processor.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## REVISION HISTORY

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|---|---|---|
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# Table of Contents

**1. GENERAL DESCRIPTION ..... 1**

**2. FEATURES ..... 2**

**3. SYSTEM APPLICATIONS ..... 5**

**4. APPLICATION EXAMPLES ..... 5**

4.1. 1-PORT 1000BASE-T PON BRIDGE ..... 5

**5. BLOCK DIAGRAM ..... 6**

**6. PIN ASSIGNMENTS ..... 7**

6.1. PACKAGE IDENTIFICATION ..... 7
6.2. PIN ASSIGNMENTS TABLE ..... 8

**7. PIN DESCRIPTIONS ..... 11**

7.1. DDR2 / DDR3 SHARED I/O PIN MAPPING ..... 11
7.2. DDR2 SHARED I/O PIN MAPPING ..... 12
7.3. MEDIA DEPENDENT INTERFACE PINS ..... 13
7.4. SHARED I/O PIN MAPPING ..... 13
7.5. GPIO ..... 14
7.6. PARALLEL LED PINS ..... 15
7.7. SERIAL LED PINS ..... 16
7.8. SERIAL SPI FLASH CONTROL ..... 16
7.9. UART ..... 16
7.10. JTAG ..... 16
7.11. PON SERDES INTERFACE ..... 17
7.12. POWER & GND ..... 18
7.13. CONFIGURATION UPON POWER ON STRAPPING ..... 18
7.14. TEST PINS ..... 21
7.15. MISCELLANEOUS PINS ..... 21

**8. MEMORY CONTROLLER ..... 22**

8.1. DDR2 SDRAM CONTROLLER ..... 22
*8.1.1. Features ..... 22*
8.2. DDR3 SDRAM CONTROLLER ..... 22
*8.2.1. Feature lists ..... 22*
8.3. SPI FLASH CONTROLLER ..... 23
*8.3.1. Features ..... 23*
*8.3.2. Pin Mode and Definition of Serial and Dual I/O ..... 23*

**9. INTERFACE DESCRIPTIONS ..... 24**

9.1. SMI HOST TO SMI SLAVE ..... 24

**10. PON INTERFACE ..... 25**

10.1. GPON INTERFACE OVERVIEW ..... 25
10.2. EPON INTERFACE OVERVIEW ..... 25
10.3. PON TX ..... 26
*10.3.1. CML Mode ..... 26*
*10.3.2. LVPECL Mode ..... 26*

10.4. PON RX ..... 27

**11. PHYSICAL LAYER FUNCTIONAL OVERVIEW ..... 28**

11.1. MDI INTERFACE ..... 28
11.2. 1000BASE-T TRANSMIT FUNCTION ..... 28
11.3. 1000BASE-T RECEIVE FUNCTION ..... 28
11.4. 100BASE-TX TRANSMIT FUNCTION ..... 28
11.5. 100BASE-TX RECEIVE FUNCTION ..... 29
11.6. 10BASE-T TRANSMIT FUNCTION ..... 29
11.7. 10BASE-T RECEIVE FUNCTION ..... 29
11.8. AUTO-NEGOTIATION FOR UTP ..... 29
11.9. CROSSOVER DETECTION AND AUTO CORRECTION ..... 30
11.10. POLARITY CORRECTION ..... 30

**12. GENERAL FUNCTION DESCRIPTION ..... 31**

12.1. RESET ..... 31
*12.1.1. Hardware Reset ..... 31*
*12.1.2. Software Reset ..... 31*
12.2. IEEE 802.3X FULL DUPLEX FLOW CONTROL ..... 31
12.3. HALF DUPLEX FLOW CONTROL ..... 32
*12.3.1. Back-Pressure Mode ..... 32*
12.4. SEARCH AND LEARNING ..... 33
12.5. SVL AND IVL/SVL ..... 33
12.6. ILLEGAL FRAME FILTERING ..... 34
12.7. IEEE 802.3 RESERVED GROUP ADDRESSES FILTERING CONTROL ..... 35
12.8. BROADCAST/MULTICAST/UNKNOWN DA STORM CONTROL ..... 36
12.9. PORT SECURITY FUNCTION ..... 36
12.10. MIB COUNTERS ..... 36
12.11. PORT MIRRORING ..... 36
12.12. VLAN FUNCTION ..... 37
*12.12.1. Port-Based VLAN ..... 37*
*12.12.2. IEEE 802.1Q Tag-Based VLAN ..... 37*
*12.12.3. Protocol-Based VLAN ..... 38*
*12.12.4. Port VID ..... 38*
12.13. QOS FUNCTION ..... 39
*12.13.1. Input Bandwidth Control ..... 39*
*12.13.2. Priority Assignment ..... 39*
*12.13.3. Priority Queue Scheduling ..... 40*
*12.13.4. IEEE 802.1p/Q and DSCP Remarking ..... 40*
*12.13.5. ACL-Based Priority ..... 41*
12.14. IEEE 802.1X FUNCTION ..... 41
*12.14.1. Port-Based Access Control ..... 41*
*12.14.2. Authorized Port-Based Access Control ..... 41*
*12.14.3. Port-Based Access Control Direction ..... 42*
*12.14.4. MAC-Based Access Control ..... 42*
*12.14.5. MAC-Based Access Control Direction ..... 42*
*12.14.6. Optional Unauthorized Behavior ..... 42*
*12.14.7. Guest VLAN ..... 42*
12.15. IEEE 802.1D FUNCTION ..... 43
12.16. CLASSIFICATION ..... 43
12.17. REALTEK CABLE TEST (RTCT) ..... 44
12.18. LED INDICATOR ..... 44
*12.18.1. Parallel LED Indicator ..... 45*
*12.18.2. Serial LED Indicator ..... 46*
12.19. GREEN ETHERNET ..... 47

*12.19.1. Link-On and Cable Length Power Saving ..... 47*
*12.19.2. Link-Down Power Saving ..... 47*
12.20. IEEE 802.3AZ ENERGY EFFICIENT ETHERNET (EEE) FUNCTION ..... 47

**13. DC SPECIFICATIONS ..... 48**

13.1. ABSOLUTE MAXIMUM RATINGS ..... 48
13.2. OPERATING CONDITIONS ..... 48
13.3. TOTAL POWER CONSUMPTION ..... 49
13.4. DDR SDRAM BUS DC PARAMETERS ..... 49
13.5. FLASH BUS DC PARAMETERS ..... 49
13.6. UART DC PARAMETERS ..... 50
13.7. GPIO DC PARAMETERS ..... 50
13.8. JTAG DC PARAMETERS ..... 50
13.9. PON SERDES DC PARAMETERS ..... 51
13.10. RESET DC PARAMETERS ..... 51
13.11. LED DC PARAMETERS ..... 51

**14. AC SPECIFICATIONS ..... 52**

14.1. CLOCK SIGNAL TIMING ..... 52
*14.1.1. 25MHz System Clock Timing ..... 52*
14.2. BUS SIGNAL TIMING ..... 53
*14.2.1. DDR SDRAM Bus ..... 53*
*14.2.2. Serial Flash Interface ..... 55*
*14.2.3. JTAG Boundary Scan ..... 56*
*14.2.4. Power Sequence ..... 57*
*14.2.5. Power Configuration Timing ..... 57*

**15. THERMAL CHARACTERISTICS ..... 58**

15.1. ASSEMBLY DESCRIPTION ..... 58
15.2. MATERIAL PROPERTIES ..... 58
15.3. SIMULATION CONDITIONS ..... 58
15.4. THERMAL PERFORMANCE OF LQFP-128 ON PCB UNDER STILL AIR CONVECTION ..... 59
15.5. THERMAL PERFORMANCE OF LQFP-128 ON PCB UNDER FORCED CONVECTION ..... 59

**16. MECHANICAL DIMENSIONS ..... 60**

**17. ORDERING INFORMATION ..... 61**

17.1. PACKAGE MARKING ..... 61

# List of Tables

TABLE 1. PIN ASSIGNMENTS TABLE ..... 8
TABLE 2. DDR2 / DDR3 SHARED I/O PIN MAPPING ..... 11
TABLE 3. DDR2 SDRAM PINS ..... 12
TABLE 4. DDR3 SDRAM PINS ..... 12
TABLE 5. MEDIA DEPENDENT INTERFACE PINS ..... 13
TABLE 6. SHARED I/O PIN MAPPING ..... 13
TABLE 7. GPIO PINS ..... 14
TABLE 8. PARALLEL LED PINS ..... 15
TABLE 9. SERIAL LED PINS ..... 16
TABLE 10. SERIAL SPI FLASH CONTROL PINS ..... 16
TABLE 11. UART PINS ..... 16
TABLE 12. JTAG PINS ..... 16
TABLE 13. PON SERDES INTERFACE ..... 17
TABLE 14. POWER & GND PINS ..... 18
TABLE 15. CONFIGURATION UPON POWER ON STRAPPING ..... 18
TABLE 16. TEST PINS ..... 21
TABLE 17. MISCELLANEOUS PINS ..... 21
TABLE 18. MEDIA DEPENDENT INTERFACE PIN MAPPING ..... 30
TABLE 19. RESERVED MULTICAST ADDRESS CONFIGURATION TABLE ..... 35
TABLE 20. LED BASIC ELEMENTS ..... 44
TABLE 21. ABSOLUTE MAXIMUM RATINGS ..... 48
TABLE 22. OPERATING CONDITIONS ..... 48
TABLE 23. TOTAL POWER CONSUMPTION ..... 49
TABLE 24. DDR SDRAM BUS DC PARAMETERS ..... 49
TABLE 25. FLASH BUS DC PARAMETERS ..... 49
TABLE 26. UART DC PARAMETERS ..... 50
TABLE 27. GPIO DC PARAMETERS ..... 50
TABLE 28. JTAG DC PARAMETERS ..... 50
TABLE 29. RESET DC PARAMETERS ..... 51
TABLE 30. LED DC PARAMETERS ..... 51
TABLE 31. 25MHZ SYSTEM CLOCK TIMING ..... 52
TABLE 32. DDR SDRAM INPUT TIMING ..... 53
TABLE 33. DDR SDRAM OUTPUT TIMING ..... 53
TABLE 34. DDR SDRAM ACCESS CONTROL TIMING ..... 53
TABLE 35. SERIAL FLASH INTERFACE OUTPUT TIMING ..... 55
TABLE 36. SERIAL FLASH INTERFACE INTPUT TIMING ..... 55
TABLE 37. JTAG BOUNDARY SCAN INTERFACE TIMING VALUES ..... 56
TABLE 38. POWER-UP TIMING PARAMETERS ..... 57
TABLE 39. ASSEMBLY DESCRIPTION ..... 58
TABLE 40. MATERIAL PROPERTIES ..... 58
TABLE 41. SIMULATION CONDITIONS ..... 58
TABLE 42. THERMAL PERFORMANCE OF LQFP-128 ON PCB UNDER STILL AIR CONVECTION ..... 59
TABLE 43. THERMAL PERFORMANCE OF LQFP-128 ON PCB UNDER FORCED CONVECTION ..... 59
TABLE 44. ORDERING INFORMATION ..... 61

# List of Figures

FIGURE 1. 1-PORT 1000BASE-T/PON BRIDGE ..... 5
FIGURE 2. BLOCK DIAGRAM ..... 6
FIGURE 3. PIN ASSIGNMENTS ..... 7
FIGURE 4. SMI START AND STOP COMMAND ..... 24
FIGURE 5. SMI HOST TO SMI SLAVE ..... 24
FIGURE 6. SMI HOST MODE FRAME ..... 24
FIGURE 7. PON SERDES TX CML MODE ..... 26
FIGURE 8. PON SERDES TX LVPECL MODE ..... 26
FIGURE 9. PON SERDES TX LVPECL MODE ..... 27
FIGURE 10. PON SERDES RX CML MODE ..... 27
FIGURE 11. CONCEPTUAL EXAMPLE OF POLARITY CORRECTION ..... 30
FIGURE 12. PROTOCOL-BASED VLAN FRAME FORMAT AND FLOW CHART ..... 38
FIGURE 13. RTL9601 MAX-MIN SCHEDULING DIAGRAM ..... 40
FIGURE 14. PULL-UP AND PULL-DOWN OF LED PINS FOR SINGLE-COLOR LED ..... 45
FIGURE 15. PULL-UP AND PULL-DOWN OF LED PINS FOR BI-COLOR LED ..... 45
FIGURE 16. SERIAL LED OUTPUT SIGNAL ..... 46
FIGURE 17. TYPICAL CONNECTION TO A CRYSTAL ..... 52
FIGURE 18. TYPICAL CONNECTION TO AN OSCILLATOR ..... 53
FIGURE 19. DDR SDRAM ACCESS CONTROL TIMING ..... 54
FIGURE 20. SERIAL FLASH INTERFACE OUTPUT TIMING ..... 55
FIGURE 21. SERIAL FLASH INTERFACE INTPUT TIMING ..... 55
FIGURE 22. BOUNDARY-SCAN GENERAL TIMING ..... 56
FIGURE 23. BOUNDARY-SCAN RESET TIMING ..... 56
FIGURE 24. POWER UP SEQUENCE TIMING DIAGRAM ..... 57
FIGURE 25. POWER UP CONFIGURATION TIMING ..... 57
FIGURE 26. PACKAGE MARKING INFORMATION ..... 61

# 1. General Description

The RTL9601 is an integrated System-on-a-Chip (SoC) Application Specific Integrated Circuit (ASIC) with dual core CPU that implements a L2 switch functions. The RTL9601 integrated an Realtek processor and the clock rate can be up to 700MHz. A standard 5-signal P1149.1 compliant EJTAG test interface is supported for CPU testing and software development.

Via table configuration and look-up, the RTL9601 can perform hard-wired network traffic forwarding. The CPU may be used to handle upper layer functions, such as DHCP, HTTP, and some other protocols, and to operate with a hard-wired forwarding engine.

The RTL9601 integrates one Gigabit Ethernet physical layer transceivers for 10Base-T, 100Base-TX, and 1000Base-TX, and one SerDes interface type to work with an external PON transceiver.

The RTL9601 supports flexible IEEE 802.3x full-duplex flow control and optional half-duplex backpressure control. For full-duplex, standard IEEE 803.3x flow control will enable pause ability only when both sides of UTP have auto-negotiation ability and have enabled pause ability. The RTL9601 also provides optional forced mode IEEE 802.3x full-duplex flow control. Based on optimized packet memory management, the RTL9601 is capable of Head-Of-Line blocking prevention.

Due to its powerful protocol parser, the RTL9601 can recognize and hard-wire-forward VLAN-tagged, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP and IGMP packets. Layer 2, 3, and 4 information is stored in look-up tables. For VLAN and PPPoE protocols, the RTL9601 can automatically encapsulate and decapsulate VLAN tagged frames and PPPoE headers.

The RTL9601 supports port-based, protocol-based, and tagged VLANs. Up to four thousand VLAN groups can be assigned. VLAN tags are inserted or removed based on the VLAN table configuration. The spanning tree protocol is supported and the states are divided into four types: Disabled, Blocking/Listening, Learning, and Forwarding.

For peripheral interfaces, one 16550-compatible UARTs are supported. An MDI/MDIX auto crossover function is supported.

The RTL9601 requires only a single 25MHz crystal clock input for the system PLL. The RTL9601 also has six hardware timers and one watchdog timer to provide accurate timing and watchdog functionality. For extension and flexibility, the RTL9601 has up to 22 GPIO pins.

The RTL9601 is provided in a Low Profile Plastic Quad Flat Package, 128-Lead (LQFP128-EPAD) package.

# 2. Features

- CPU
  - Realtek 700MHz CPU
    - I-Cache: 64KB, 4-way set
    - D-Cache: 32KB, 4-way set
    - Virtually indexed, physically tagged
    - PREF instruction
  - Misc.
    - Power-down mode (Sleep instruction)
    - EJTAG support
    - Internal real-time timer interrupts (Count/Compare registers)
    - 2 HW instruction breakpoint/1 HW data breakpoint.

- CPU Interface (NIC)
  - The NIC DMA support multiple-descriptor-ring architecture for QoS applications

- Memory Interfaces
  - Serial Flash (SPI Type)
    - Supports dual I/O channels for SPI Flash application
    - Each Flash bank could be configured as 256K/512K/1M/2M/4M/8M/16M/32M Bytes
    - Boot up from SPI flash is supported
  - DDR2 SDRAM
    - Supports one DDR2 SDRAM bank that can be configured as 32M/64M/128M/256M bytes
    - 8-bit DDR2 SDRAM data bus supported. System totally supports up to 128Mbyte DDR2 SDRAM memory space
  - DDR3 SDRAM
    - Supports one DDR3 SDRAM bank that can be configured as 128M/256M bytes
    - 8-bit DDR3 SDRAM data bus supported. System totally supports up to 128Mbyte DDR3 SDRAM memory space

- GPON
  - Compliant with ITU G.984.x
  - Bandwidth US: 1.24416G/DS: 2.48832G
  - Supports 32 TCONT, 128 GEM
  - Supports AES, key switching
  - Supports upstream and downstream FEC
  - Supports DBRu
  - HW dying gasp

- EPON
  - Compliant with IEEE 802.3 EPON MAC standard
  - Bandwidth US: 1.25G/DS: 1.25G
  - Supports DS/US FEC
  - Supports downstream traffic decryption
  - US scheduling
    - Per Queue rate control setting (CIR/PIR)
    - Support Strict Priority and Weighted Fair Queuing (WFQ) mode
  - Counter–Support RFC4837
  - HW dying gasp

- L2 Capabilities
  - Three Gigabit Ethernet MACs switch with one IEEE 802.3 10/100/1000Mbps physical layer transceivers

- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking/forwarding
- Internal 2048 entry 4-way hash L2 look-up table
- Supports source and destination MAC address filtering

- Supports ACL Rules
  - Supports MAC, IP, TCP/UDP, ICMP, IGMP, IPv6 Format
  - Supports mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, SVLAN assignment, interrupt, LLID, SID assignment and Extension forward portmask.
  - Supports 4 templates of user defined ACL rule format
  - Supports VID/IP/L4/Packet Length Port range check
  - Up to 16 user defined field selectors
- Support 512 PON Classification Rules
  - Supports SVLAN tagging/removing
  - Supports CVLAN tagging/removing
  - Supports indirect LLID/GEMPort assignment
  - Supports forced UNI ports forwarding and queueing priority assignment
  - VLAN translation/aggregation functions
- Supports GPON 128 GEM Port within 32 T-CONT
- Supports IEEE 802.1Q VLAN
  - Supports 4K VLAN and 32 Extra Enhanced VLAN
  - Supports Untag definition in each VLAN
  - Supports VLAN policing
  - Supports Port Based and Port-and-Protocol-based VLAN
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLAN
  - Supports 8 L2/IPv4 Multicast mapping to SVLAN
  - Support 128 CLVAN to SVLAN
  - Support MAC-based customer CVID decision for 1:N VLAN
- Supports IVL， SVL and IVL/SVL
  - Supports 2K MAC Address Table
  - 4-way hash
  - Up to 16 L2/L3 Filtering Database as 16 MST instance
- Supports Spanning Tree
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree, up to 16 spanning tree
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports IEEE 802.1X access control protocol
- Supports Quality of Service (QoS)
  - Traffic classification based on IEEE 802.1P/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, SVLAN based priority and L4 NAT priority
  - 8 priority queues per port
  - Supports per port Ingress Bandwidth Control and Egress Bandwidth Control
  - Per queue flow control
  - Min-Max Scheduling

  - Strict Priority and Weighted Fair Queuing (WFQ) to provide minimum bandwidth
  - One leaky bucket (APR) to constraint average rate of each queue
- Supports 32 shared meter with 8kpbs granularity
- Supports MIB Counters
  - MIB-II (RFC 1213)
  - Ethernet-like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
  - ITU G.984.4 OMCI ME MIBs
  - User defined Logging Counter
- Supports 8 Enhanced Filtering Database for Stacking VLAN and Port Isolation usage
- Port mirror with multicast monitored source ports to monitorring destination port.
- Supports IEEE 802.3ad Link aggregation port group, up to 4Gpbs bandwidth
- Supports OAM and EEELLDP
- IGMP/MLD snooping trap function
- Green Ethernet Auto Fall-back
- Ethernet AV support with 802.1Qav and 802.1AS/1588v2 timing synchronization
- Storm Filtering Control for broadcast, multicast, unknown unicast, ARP, DHCP and ICMP with 8Kpbs granularity rate.
- DOS attacks prevention
- LQFP128-E-PAD package
- Supports Green Ethernet
  - Cable length power saving
  - Power down power saving
- Supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation and 10Base-T in full/half duplex mode
- Other Add-on-Value Features
  - Supports Link Down Power Saving in Ethernet PHYceivers
  - Supports six hardware timers and one watchdog timer
  - Per-port configurable auto-crossover function
  - Single 25MHz crystal clock input

# 3. System Applications

- 1-Port 1000Base-T/PON bridge.

# 4. Application Examples

## *4.1. 1-Port 1000Base-T PON Bridge*

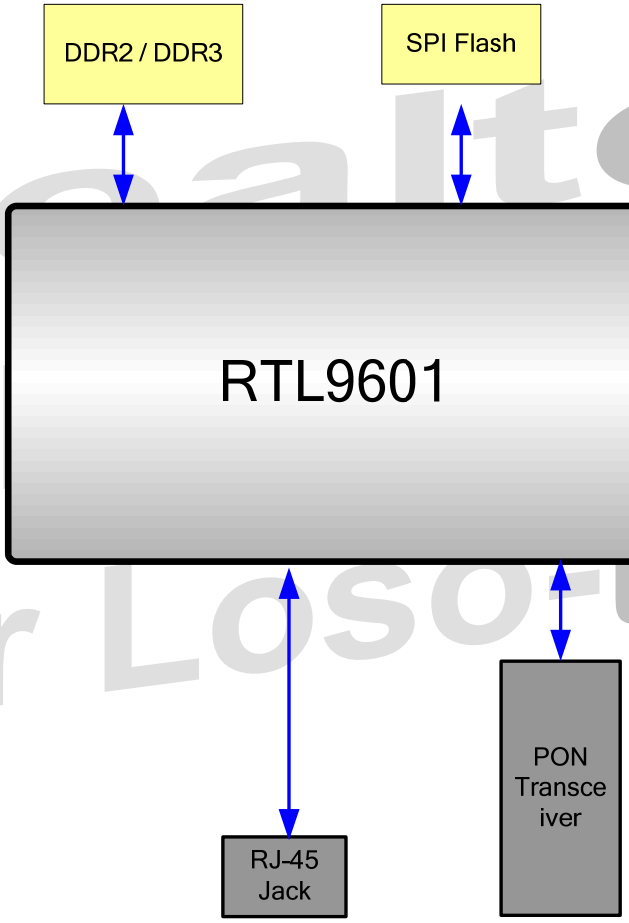



**Figure 1. 1-Port 1000Base-T/PON Bridge**

# 5. Block Diagram

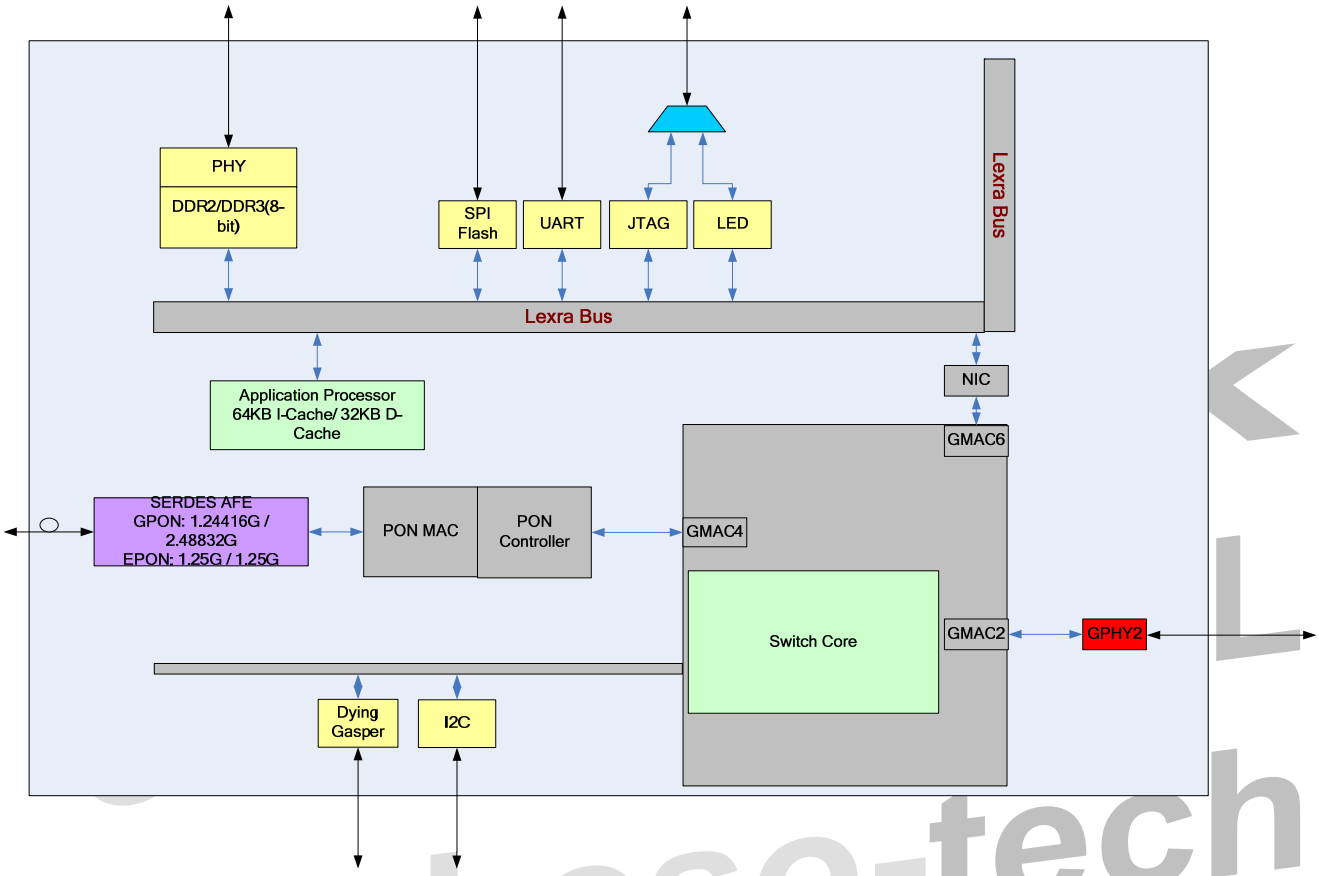



Figure 2. Block Diagram

# 6. Pin Assignments

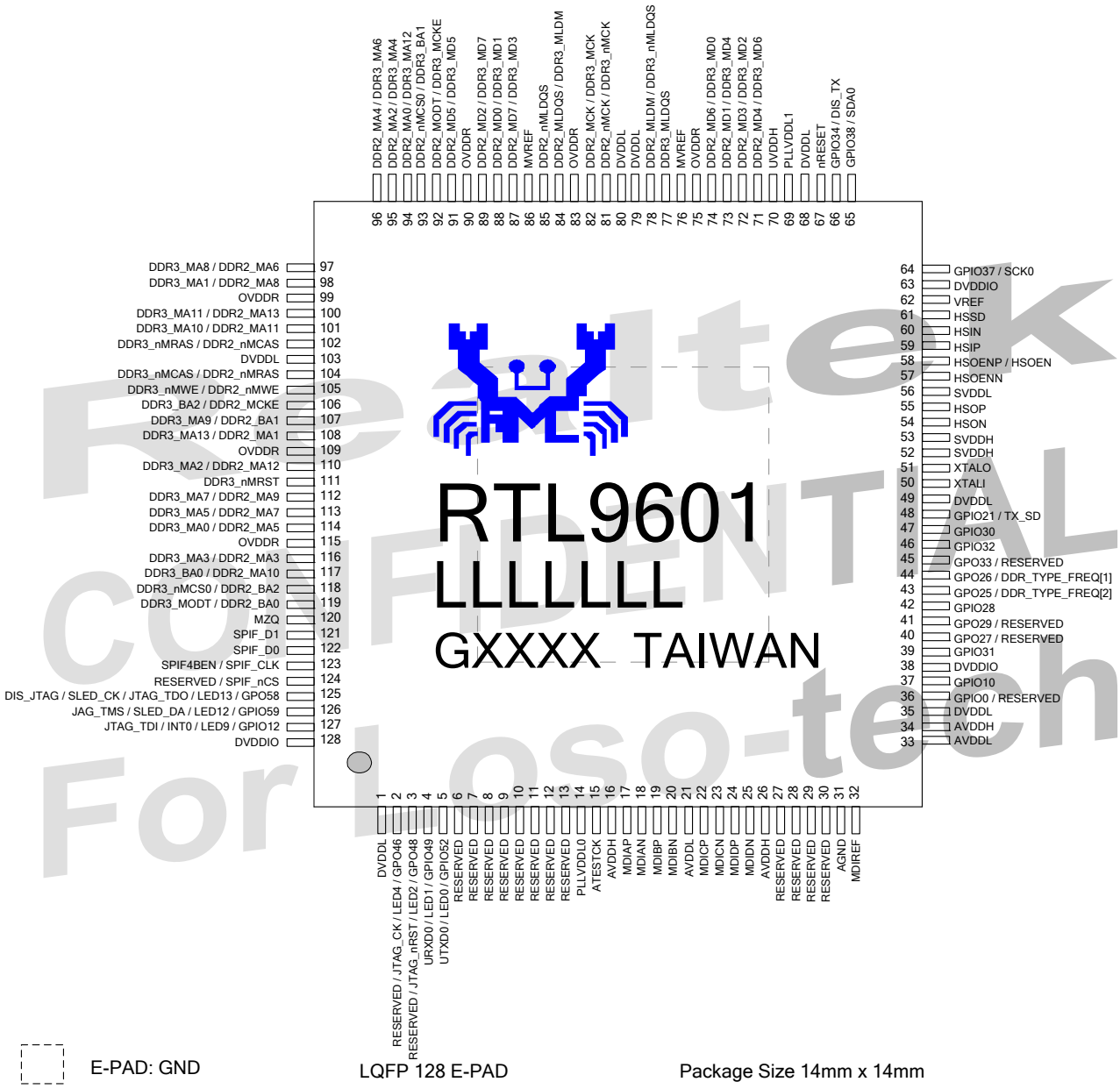



**Figure 3. Pin Assignments**

## *6.1. Package Identification*

Green package is indicated by the 'G' in GXXXX (Figure 3).

## 6.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

$I/O_{PU}$: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

$I/O_{PD}$: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

$I_S$: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

$I/O_{PU}$: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

$I/O_{PD}$: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)



**Table 1. Pin Assignments Table**

| Name | Pin No. | Type |
|---|---|---|
| DVDDL | 1 | P |
| GPO46/LED4/JTAG_CK/ RESERVED | 2 | $I/O_{PU}$ |
| GPO48/LED2/JTAG_nRST/ RESERVED | 3 | $I/O_{PU}$ |
| GPIO49/LED1/URXD0 | 4 | $I/O_{PU}$ |
| GPIO52/LED0/UTXD0/RESERVED | 5 | $I/O_{PU}$ |
| RESERVED | 6 | - |
| RESERVED | 7 | - |
| RESERVED | 8 | - |
| RESERVED | 9 | - |
| RESERVED | 10 | - |
| RESERVED | 11 | - |
| RESERVED | 12 | - |
| RESERVED | 13 | - |
| PLLVDDL0 | 14 | AP |
| ATESTCK | 15 | AO |

| Name | Pin No. | Type |
|---|---|---|
| AVDDH | 16 | AP |
| MDIAP | 17 | AI/O |
| MDIAN | 18 | AI/O |
| MDIBP | 19 | AI/O |
| MDIBN | 20 | AI/O |
| AVDDL | 21 | AP |
| MDICP | 22 | AI/O |
| MDICN | 23 | AI/O |
| MDIDP | 24 | AI/O |
| MDIDN | 25 | AI/O |
| AVDDH | 26 | AP |
| RESERVED | 27 | - |
| RESERVED | 28 | - |
| RESERVED | 29 | - |
| RESERVED | 30 | - |
| AGND | 31 | AG |
| MDIREF | 32 | AO |
| AVDDL | 33 | AP |

| Name | Pin No. | Type |
|---|---|---|
| AVDDH | 34 | AP |
| DVDDL | 35 | P |
| GPIO0/RESERVED | 36 | $I/O_{PD}$ |
| GPIO10/RESERVED | 37 | $I/O_{PU}$ |
| DVDDIO | 38 | P |
| GPIO31 | 39 | I/O |
| GPO27/RESERVED | 40 | $I/O_{PU}$ |
| GPIO29/RESERVED | 41 | $I/O_{PU}$ |
| GPIO28 | 42 | I/O |
| GPO25/DDR_TYPE_ FREQ[2] | 43 | $I/O_{PU}$ |
| GPO26/DDR_TYPE_ FREQ[1] | 44 | $I/O_{PU}$ |
| GPO33/RESERVED | 45 | $I/O_{PU}$ |
| GPIO32 | 46 | I/O |
| GPIO30 | 47 | I/O |
| GPIO21/TX_SD | 48 | $I/O_{PU}$ |
| DVDDL | 49 | P |
| XTALI | 50 | AI |
| XTALO | 51 | AO |
| SVDDH | 52 | AP |
| SVDDH | 53 | AP |
| HSON | 54 | AO |
| HSOP | 55 | AO |
| SVDDL | 56 | AP |
| HSOENN | 57 | AO |
| HSOENP/HSOEN | 58 | AO |
| HSIP | 59 | AI |
| HSIN | 60 | AI |
| HSSD | 61 | I |
| VREF | 62 | AI |
| DVDDIO | 63 | P |
| GPIO37/SCK0 | 64 | I/O |
| GPIO38/SDA0 | 65 | I/O |
| GPIO34/DIS_TX | 66 | I/O |
| nRESET | 67 | $I_S$ |
| DVDDL | 68 | P |
| PLLVDDL1 | 69 | AP |
| UVDDH | 70 | AP |
| DDR2_MD4/DDR3_MD6 | 71 | I/O |
| DDR2_MD3/DDR3_MD2 | 72 | I/O |
| DDR2_MD1/DDR3_MD4 | 73 | I/O |
| DDR2_MD6/DDR3_MD0 | 74 | I/O |
| OVDDR | 75 | P |

| Name | Pin No. | Type |
|---|---|---|
| MVREF | 76 | AO |
| DDR3_MLDQS | 77 | I/O |
| DDR2_MLDM /DDR3_nMLDQS | 78 | I/O |
| DVDDL | 79 | P |
| DVDDL | 80 | P |
| DDR2_nMCK/DDR3_nMCK | 81 | O |
| DDR2_MCK/DDR3_MCK | 82 | O |
| OVDDR | 83 | P |
| DDR2_MLDQS/DDR3_MLD M | 84 | I/O |
| DDR2_nMLDQS | 85 | I/O |
| MVREF | 86 | AO |
| DDR2_MD7/DDR3_MD3 | 87 | I/O |
| DDR2_MD0/DDR3_MD1 | 88 | I/O |
| DDR2_MD2/DDR3_MD7 | 89 | I/O |
| OVDDR | 90 | P |
| DDR2_MD5/DDR3_MD5 | 91 | I/O |
| DDR2_MODT/ DDR3_MCKE | 92 | O |
| DDR2_nMCS0/DDR3_BA1 | 93 | O |
| DDR2_MA0/DDR3_MA12 | 94 | O |
| DDR2_MA2/DDR3_MA4 | 95 | O |
| DDR2_MA4/DDR3_MA6 | 96 | O |
| DDR2_MA6/DDR3_MA8 | 97 | O |
| DDR2_MA8/DDR3_MA1 | 98 | O |
| OVDDR | 99 | O |
| DDR2_MA13/DDR3_MA11 | 100 | O |
| DDR2_MA11/DDR3_MA10 | 101 | O |
| DDR2_nMCAS/DDR3_nMR AS | 102 | O |
| DVDDL | 103 | P |
| DDR2_nMRAS/DDR3_nMC AS | 104 | O |
| DDR2_nMWE/DDR3_nMWE | 105 | O |
| DDR2_MCKE/DDR3_BA2 | 106 | O |
| DDR2_BA1/DDR3_MA9 | 107 | O |
| DDR2_MA1/DDR3_MA13 | 108 | O |
| OVDDR | 109 | P |
| DDR2_MA12/DDR3_MA2 | 110 | O |
| DDR3_nMRST | 111 | O |
| DDR2_MA9/DDR3_MA7 | 112 | O |
| DDR2_MA7/DDR3_MA5 | 113 | O |
| DDR2_MA5/DDR3_MA0 | 114 | O |

| Name | Pin No. | Type |
|---|---|---|
| OVDDR | 115 | P |
| DDR2_MA3/DDR3_MA3 | 116 | O |
| DDR2_MA10/DDR3_BA0 | 117 | O |
| DDR2_BA2/DDR3_nMCS0 | 118 | O |
| DDR2_BA0/DDR3_MODT | 119 | O |
| MZQ | 120 | AO |
| SPIF_D1 | 121 | I/O |
| SPIF_D0 | 122 | I/O |
| SPIF_CLK/SPIF4BEN | 123 | $I/O_{PU}$ |

| Name | Pin No. | Type |
|---|---|---|
| SPIF_nCS/RESERVED | 124 | I/O |
| GPO58/LED13/SLED_CK/JTAG_TDO/DIS_JTAG | 125 | $I/O_{PU}$ |
| GPIO59/LED12/SLED_DA/JAG_TMS | 126 | $I/O_{PU}$ |
| GPIO12/LED9/INT0/JTAG_TDI | 127 | $I/O_{PU}$ |
| DVDDIO | 128 | P |

# 7. Pin Descriptions

## 7.1. DDR2 / DDR3 Shared I/O Pin Mapping

Table 2. DDR2 / DDR3 Shared I/O Pin Mapping

| Pin No. | DDR / DDR2 | DDR3 |
|---|---|---|
| 71 | DDR2_MD4 | DDR3_MD6 |
| 72 | DDR2_MD3 | DDR3_MD2 |
| 73 | DDR2_MD1 | DDR3_MD4 |
| 74 | DDR2_MD6 | DDR3_MD0 |
| 77 | RESERVED | DDR3_MLDQS |
| 78 | DDR2_MLDM | DDR3_nMLDQS |
| 81 | DDR2_nMCK | DDR3_nMCK |
| 82 | DDR2_MCK | DDR3_MCK |
| 84 | DDR2_MLDQS | DDR3_MLDM |
| 85 | DDR2_nMLDQS | - |
| 87 | DDR2_MD7 | DDR3_MD3 |
| 88 | DDR2_MD0 | DDR3_MD1 |
| 89 | DDR2_MD2 | DDR3_MD7 |
| 91 | DDR2_MD5 | DDR3_MD5 |
| 92 | DDR2_MODT | DDR3_MCKE |
| 93 | DDR2_nMCS0 | DDR3_BA1 |
| 94 | DDR2_MA0 | DDR3_MA12 |
| 95 | DDR2_MA2 | DDR3_MA4 |
| 96 | DDR2_MA4 | DDR3_MA6 |
| 97 | DDR2_MA6 | DDR3_MA8 |
| 98 | DDR2_MA8 | DDR3_MA1 |
| 100 | DDR2_MA13 | DDR3_MA11 |
| 101 | DDR2_MA11 | DDR3_MA10 |
| 102 | DDR2_nMCAS | DDR3_nMRAS |
| 104 | DDR2_nMRAS | DDR3_nMCAS |
| 105 | DDR2_nMWE | DDR3_nMWE |
| 106 | DDR2_MCKE | DDR3_BA2 |
| 107 | DDR2_BA1 | DDR3_MA9 |
| 108 | DDR2_MA1 | DDR3_MA13 |
| 110 | DDR2_MA12 | DDR3_MA2 |
| 111 | - | DDR3_nMRST |
| 112 | DDR2_MA9 | DDR3_MA7 |
| 113 | DDR2_MA7 | DDR3_MA5 |
| 114 | DDR2_MA5 | DDR3_MA0 |
| 116 | DDR2_MA3 | DDR3_MA3 |
| 117 | DDR2_MA10 | DDR3_BA0 |
| 118 | DDR2_BA2 | DDR3_nMCS0 |
| 119 | DDR2_BA0 | DDR3_MODT |

## 7.2. DDR2 Shared I/O Pin Mapping

**Table 3. DDR2 SDRAM Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| DDR2_MCKE | 106 | O | DDR2 SDRAM clock enable |
| DDR2_MCK | 82 | O | DDR2 SDRAM differential clock signal 0 |
| DDR2_nMCK | 81 | O | DDR2 SDRAM differential clock signal 1 |
| DDR2_MODT | 92 | O | DDR2 on die termination |
| DDR2_nMWE | 105 | O | Write enable |
| DDR2_nMCAS | 102 | O | Column address strobe |
| DDR2_nMRAS | 104 | O | Row address strobe |
| DDR2_BA[2:0] | 118, 107, 119 | O | Bank address |
| DDR2_MLDM | 78 | O | Data mask for DQ[7:0] |
| DDR2_MLDQS | 84 | I/O | Data strobe for DQ[7:0] |
| DDR2_nMLDQS | 85 | I/O | Data strobe for DQ[7:0] |
| DDR2_MA[13:0] | 100, 110, 101, 117, 112, 98, 113, 97, 114, 96, 116, 95, 108, 94 | O | Address for DDR2 SDRAM |
| DDR2_MD[7:0] | 87, 74, 91, 71, 72, 89, 73, 88 | I/O | Data for DDR2 SDRAM |
| MZQ | 120 | AO | Reference Pin for ZQ calibration. |

**Table 4. DDR3 SDRAM Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| DDR3_MCKE | 92 | O | DDR3 SDRAM clock enable |
| DDR3_MCK | 82 | O | DDR3 SDRAM differential clock signal 0 |
| DDR3_nMCK | 81 | O | DDR3 SDRAM differential clock signal 1 |
| DDR3_nMCS0 | 118 | O | DDR3 SDRAM chip select 0 |
| DDR3_MODT | 119 | O | DDR3 on die termination |
| DDR3_nMWE | 105 | O | Write enable |
| DDR3_nMCAS | 104 | O | Column address strobe |
| DDR3_nMRAS | 102 | O | Row address strobe |
| DDR3_BA[2:0] | 106, 93, 117 | O | Bank address |
| DDR3_MLDM | 84 | O | Data mask for DQ[7:0] |
| DDR3_MLDQS | 77 | I/O | Data strobe for DQ[7:0] |
| DDR3_nMLDQS | 78 | I/O | Data strobe for DQ[7:0] |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| DDR3_MA[13:0] | 108, 94, 100, 101, 107, 97, 112, 96, 113, 95, 116, 110, 98, 114 | O | Address for DDR3 SDRAM |
| DDR3_MD[7:0] | 89, 71, 91, 73, 87, 72, 88, 74 | I/O | Data for DDR3 SDRAM |
| MZQ | 120 | AO | Reference Pin for ZQ calibration. |

## 7.3. Media Dependent Interface Pins

**Table 5. Media Dependent Interface Pins**

| Pin Name | Pin No. | Type | Drive (mA) | Description |
|---|---|---|---|---|
| MDIAP/N<br>MDIBP/N<br>MDICP/N<br>MDIDP/N | 17<br>18<br>19<br>20<br>22<br>23<br>24<br>25 | AI/O | 10 | Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100-ohm termination resistor. |

## 7.4. Shared I/O Pin Mapping

The RTL9601 supports many types of digital interface Parallel LED, Serial LED, EJTAG, and UART.

**Table 6. Shared I/O Pin Mapping**

| PIN No. | GPIO | Parallel LED | Serial LED | EJTAG | Strap | UART |
|---|---|---|---|---|---|---|
| 125 | GPO58 | LED13 | SLED_CK | JTAG_TDO | DIS_JTAG | - |
| 126 | GPIO59 | LED12 | SLED_DA | JTAG_TMS | - | - |
| 127 | GPIO12 | LED9 | - | JTAG_TDI | - | - |
| 2 | GPO46 | LED4 | - | JTAG_CK | RESERVED | - |
| 3 | GPO48 | LED2 | - | JTAG_nRST | RESERVED | - |
| 4 | GPIO49 | - | - | - | - | URXD0 |
| 5 | GPIO52 | - | - | - | RESERVED | UTXD0 |
| 36 | GPIO0 | - | - | - | - | - |
| 37 | GPIO10 | - | - | - | - | - |

## 7.5. GPIO

Table 7. GPIO Pins

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| GPIO0/ RESERVED | 36 | $I/O_{PD}$ | General Purpose Input/Output Interfaces IO0. |
| GPIO10/ RESERVED | 37 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO10. |
| GPIO31 | 39 | I/O | General Purpose Input/Output Interfaces IO31. |
| GPO27/ RESERVED | 40 | $I/O_{PU}$ | General Purpose Output Interfaces O27. |
| GPIO29/ RESERVED | 41 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO29. |
| GPIO28 | 42 | I/O | General Purpose Input/Output Interfaces IO28. |
| GPO25 | 43 | $I/O_{PU}$ | General Purpose Output Interfaces O25. |
| GPO26 | 44 | $I/O_{PU}$ | General Purpose Output Interfaces O26. |
| GPO33 /RESERVED | 45 | $I/O_{PU}$ | General Purpose Output Interfaces O33. |
| GPIO32 | 46 | I/O | General Purpose Input/Output Interfaces IO32. |
| GPIO30 | 47 | I/O | General Purpose Input/Output Interfaces IO30. |
| GPIO21/ TX_SD | 48 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO52. |
| GPIO37/ SCK0 | 64 | I/O | General Purpose Input/Output Interfaces IO37. |
| GPIO38/ SDA0 | 65 | I/O | General Purpose Input/Output Interfaces IO38. |
| GPIO34/ DIS_TX | 66 | I/O | General Purpose Input/Output Interfaces IO34. |
| GPO58/ LED13/ SLED_CK/ JTAG_TDO/ DIS_JTAG | 125 | $I/O_{PU}$ | General Purpose Output Interfaces O58. |
| GPIO59/ LED12/ SLED_DA/ JAG_TMS | 126 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO59. |
| GPIO12/ LED9/ INT0/ JTAG_TDI | 127 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO12. |
| GPO46/ LED4/ JTAG_CK/ RESERVED | 2 | $I/O_{PU}$ | General Purpose Output Interfaces O46. |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| GPO48/<br>LED2/<br>JTAG_nRST/<br>RESERVED | 3 | $I/O_{PU}$ | General Purpose Output Interfaces O48. |
| GPIO49/<br>LED1/<br>URXD0 | 4 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO49. |
| GPIO52/<br>LED0/<br>UTXD0/<br>RESERVED | 5 | $I/O_{PU}$ | General Purpose Input/Output Interfaces IO52. |

## 7.6. Parallel LED Pins

**Table 8. Parallel LED Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| LED13/<br>GPO58/<br>SLED_CK/<br>JTAG_TDO/<br>DIS_JTAG | 125 | $I/O_{PU}$ | LED13 Output Signal.<br>LED13 indicates information is defined by register. |
| LED12/<br>GPIO59/<br>SLED_DA/<br>JAG_TMS | 126 | $I/O_{PU}$ | LED12 Output Signal.<br>LED12 indicates information is defined by register. |
| LED9/<br>GPIO12/<br>INT0/<br>JTAG_TDI | 127 | $I/O_{PU}$ | LED9 Output Signal.<br>LED9 indicates information is defined by register. |
| LED4/<br>GPO46/<br>JTAG_CK/<br>RESERVED | 2 | $I/O_{PU}$ | LED4 Output Signal.<br>LED4 indicates information is defined by register. |
| LED2/<br>GPO48/<br>JTAG_nRST/<br>RESERVED | 3 | $I/O_{PU}$ | LED2 Output Signal.<br>LED2 indicates information is defined by register. |
| LED1/<br>GPIO49/<br>URXD0 | 4 | $I/O_{PU}$ | LED1 Output Signal.<br>LED1 indicates information is defined by register. |
| LED0/<br>GPIO52/<br>UTXD0/<br>RESERVED | 5 | $I/O_{PU}$ | LED0 Output Signal.<br>LED0 indicates information is defined by register. |

## 7.7. Serial LED Pins

**Table 9. Serial LED Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| SLED_CK/<br>GPO58/<br>LED13/<br>JTAG_TDO/<br>DIS_JTAG | 125 | $I/O_{PU}$ | Serial LED Output Signal Clock. |
| SLED_DA/<br>GPIO59/<br>LED12/<br>JAG_TMS | 126 | $I/O_{PU}$ | Serial LED Output Signal Data. |

## 7.8. Serial SPI Flash Control

**Table 10. Serial SPI Flash Control Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| SPIF_nCS | 124 | I/O | SPI Serial Flash Chip Select. |
| SPIF_D[1:0] | 121, 122 | I/O | SPI Serial Flash Dual Data Input/Output. |
| SPIF_CLK | 123 | $I/O_{PU}$ | SPI Serial Flash Serial Clock Output.<br>The SF_SDI will be driven on the falling edge.<br>The SF_SDO will be latched on the rising edge. |

## 7.9. UART

**Table 11. UART Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| UTXD0/<br>GPIO52/<br>LED0/<br>RESERVED | 5 | O | Data Transmit Serial Output of UART0. |
| URXD0/<br>GPIO49/<br>LED1 | 4 | I | Data Receive Serial Input of UART0.<br><br>Note: This pin must be pulled low via an external 4.7k ohm when the UART interface enabled. |

## 7.10. JTAG

**Table 12. JTAG Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| JTAG_CK/<br>GPO46/<br>LED4/<br>RESERVED | 2 | $I_{PU}$ | JTAG Test Clock. |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| JTAG_TMS/<br>GPIO59/<br>LED12/<br>SLED_DA | 126 | $I_{PU}$ | JTAG Test Mode Select. |
| JTAG_TDO/<br>GPO58/<br>LED13/<br>SLED_CK/<br>DIS_JTAG | 125 | $O_{PU}$ | JTAG Test Data Output. |
| JTAG_TDI/<br>GPIO12/<br>LED9/<br>INT0 | 127 | $I_{PU}$ | JTAG Test Data In. |
| JTAG_nRST/<br>GPO48/<br>LED2/<br>RESERVED | 3 | $I_{PU}$ | JTAG Test Reset. |

## 7.11. PON SerDes Interface

**Table 13. PON SerDes Interface**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| HSON | 54 | AO | Transmit Data Analog negative output signals. Internal pull high 50 ohm, CML or LVPECL signal, DC couple for ONU. |
| HSOP | 55 | AO | Transmit Data Analog positive output signals. Internal pull high 50 ohm, CML or LVPECL signal, DC couple for ONU. |
| HSIN | 60 | AI | Receiver Data Analog positive input signals. CML signal, internal pull high 50 ohm, AC couple for ONU. |
| HSIP | 59 | AI | Receiver Data Analog negative input signals. CML signal, internal pull high 50 ohm, AC couple for ONU. |
| HSOENN | 57 | AO | Differential negative burst fiber transceiver burst enable signal, internal pull high 50 ohm, CML signal. |
| HSOENP/HSOEN | 58 | AO | Differential positive fiber transceiver burst enable signal, internal pull high 50 ohm, CML signal.<br>This signal can be set to single end LVTTL BEN signal via register. |
| HSSD | 61 | I | PON Optical Signal Detect, LVTTL signal.<br>High: optical is present at receiver input.<br>Low : No RX signal input |

## 7.12. Power & GND

Table 14. Power & GND Pins

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| DVDDIO | 38, 63, 128 | P | Digital I/O High Voltage Power |
| DVDDL | 1, 35, 49, 68, 79, 80, 103 | P | Digital Low Voltage Power. |
| AVDDH | 16, 26, 34 | AP | Analog High Voltage Power. |
| AVDDL | 21, 33 | AP | Analog Low Voltage Power. |
| PLLVDDL0 | 14 | AP | PLL0 Low Voltage Power. |
| PLLVDDL1 | 69 | AP | PLL1 Low Voltage Power. |
| SVDDH | 52, 53 | AP | SerDes Analog High Voltage Power. |
| SVDDL | 56 | AP | SerDes Analog Low Voltage Power. |
| UVDDH | 70 | AP | Analog High Voltage Power. |
| OVDDR | 75, 83, 90, 99, 109, 115 | P | DDR2/DDR3 SDRAM I/O Power Supply<br>DDR2 SDRAM I/O Power Supply 1.8V<br>DDR3 SDRAM I/O Power Supply 1.5V |
| MVREF | 76, 86 | AO | 1/2 OVDDR reference level |
| GND | EPAD | G | Digital GND. |
| AGND | 31 | AG | Analog GND. |

## 7.13. Configuration Upon Power On Strapping

All mode configuration pins are internal pull low. The 1.0V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 300ms.

Table 15. Configuration Upon Power On Strapping

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| RESERVED/<br>SPIF_nCS | 124 | $I/O_{PD}$ | Reserved for internal use.<br><br>Note: This pin must be left floating or pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED/<br>GPO27 | 40 | $I/O_{PU}$ | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED/<br>GPIO29 | 41 | $I/O_{PU}$ | Reserved for internal use.<br><br>Note: This pin must be left floating or pulled high via an external 4.7k ohm resistor upon power on or reset. |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| DDR_TYPE_FREQ[2]/<br>GPO25<br><br>DDR_TYPE_FREQ[1]/<br>GPO26 | 43,<br><br>44 | I/O$_{PU}$ | DDR type selection:<br>00: DDR2<br>01: Reserved<br>10: DDR3<br>11: Reserved<br><br>Note: Those pins must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED/<br>GPO33 | 45 | I/O$_{PU}$ | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| SPIF4BEN/<br>SPIF_CLK | 123 | I/O$_{PU}$ | SPI flash address byte number<br>0: 3 Bytes<br>1: 4 Bytes<br><br>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset. |
| DIS_JTAG/<br>GPO58/<br>LED13/<br>SLED_CK/<br>JTAG_TDO | 125 | I/O$_{PU}$ | Enable/Disable JTAG interface<br>0: Enable JTAG<br>1: Disable JTAG<br><br>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.<br>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 12.18, page 44 LED Indicator for more details. |
| RESERVED/<br>GPO46/<br>LED4/<br>JTAG_CK | 2 | I/O$_{PU}$ | Reserved for internal use.<br><br>Note: This pin must be left floating or pulled high via an external 4.7k ohm resistor upon power on or reset.<br>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 12.18, page 44 LED Indicator for more details. |
| RESERVED/<br>GPO48/<br>LED2/<br>JTAG_nRST | 3 | I/O$_{PU}$ | Reserved for internal use.<br><br>Note: This pin must be left floating or pulled high via an external 4.7k ohm resistor upon power on or reset.<br>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 12.18, page 44 LED Indicator for more details. |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| RESERVED/<br>GPIO52/<br>LED0/<br>UTXD0 | 5 | $I/O_{PU}$ | Reserved for internal use.<br><br>Note: This pin must be left floating or pulled high via an external 4.7k ohm resistor upon power on or reset.<br>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 12.18, page 44 LED Indicator for more details. |
| RESERVED | 6 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 7 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 8 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 9 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 10 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 11 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 12 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 13 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 27 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| RESERVED | 28 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 29 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |
| RESERVED | 30 | - | Reserved for internal use.<br><br>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset. |

## 7.14. Test Pins

**Table 16. Test Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| ATESTCK | 15 | AO | Reserved for Internal Use. Must be left floating. |

## 7.15. Miscellaneous Pins

**Table 17. Miscellaneous Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| XTALI | 50 | AI | 25MHz Crystal Clock Input and Feedback Pin.<br>25MHz +/-50ppm tolerance crystal reference or oscillator input. |
| XTALO | 51 | AO | 25MHz Crystal Clock Output Pin.<br>25MHz +/-50ppm tolerance crystal output. |
| MDIREF | 32 | AO | Reference Resistor.<br>A 2.49K ohm (1%) resistor must be connected between MDIREF and GND. |
| VREF | 62 | AI | Dying Gasp Voltage Detect Input. |
| nRESET | 67 | $I_S$ | System Reset Input Pin.<br>When low active will reset the RTL9601. |

# 8. Memory Controller

The RTL9601 integrates a memory control module to access external DDR2 SDRAM, DDR3 SDRAM and Flash memory. The DDR SDRAM interface supports one chip, and the memory size and timing is configurable in registers.

The RTL9601 also supports a flash memory chip. The interface supports SPI flash memory. When Flash is used, the system will boot from KSEG1 at virtual address 0xBFC0_0000 (physical address: 0x1FC0_0000). The flash size is configurable from 1M to 32M bytes for each chip. If flash size is set to 4M, 8M, 16M, or 32M byte, 0xBFC0_0000 still maps the first 4M bytes of flash, and there will be a new memory mapping from 0xBD00_0000 (0xBD00_0000 maps to chip 0 byte 0).



## *8.1. DDR2 SDRAM Controller*

### 8.1.1. Features

- Interface (Bus Width): 8-bit
- DDR2 Frequency: Up to 400MHz (DDR2-800)
- Supports one Chip Selects
- Supported DDR SDRAM Chip Specification
  - Bank Counts: 4
  - Row Counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column Counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11), 4K (A0~A9, A11, A12)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

## *8.2. DDR3 SDRAM Controller*

### 8.2.1. Feature lists

- Interface (Bus Width): 8 bit
- Targeted DDR3 Frequency: up to 400MHz (DDR3-800)
- Supports one Chip Select (nMCS0)
- Supported DDR3 SDRAM chip spec
  - Bank counts: 4,8
  - Row counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9,A11), 4K (A0~A9,A11,A12)
- Programmable timing parameters
  - tRAS, tRP, tRCD, tCL, tREFI,…
- Fixed DDR2 parameters.
  - AL = 0.
  - Some DDR2 SDRAM introduces tRPA timing parameter. We merge tRPA with tRP into one parameter.
  - No tRTP. Need to check DDR2 Bus waveform to confirm there is no tRTP violation.

## 8.3. SPI Flash Controller

The SPI flash controller is a new design and incorporates new features.

### 8.3.1. Features

- SPI flash frequency: up to 62.5MHz
- Supports one chip
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

### 8.3.2. Pin Mode and Definition of Serial and Dual I/O

Modes supported on the SPI flash interface:

1. Serial I/O mode:
   - SI: flash chip input pin
   - SO: flash chip output pin
2. Dual I/O mode:
   - SPIF_D0 (SI): flash chip bi-directional pin. This is LSB
   - SPIF_D1 (SO): flash chip bi-directional pin. This is MSB

# 9. Interface Descriptions

## 9.1. SMI Host to SMI Slave

The SMI interface of the RTL9601 uses the serial bus Serial Management Interface (SMI) to access SMI Slave device. The RTL9601 drives SCK and SDA to read or write the registers of the SMI Slave device.

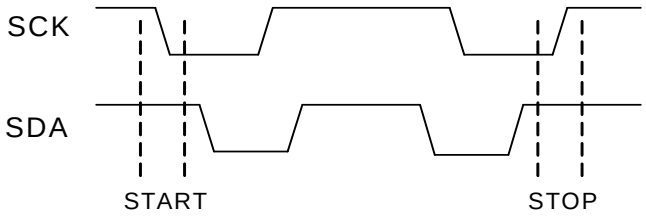



**Figure 4. SMI Start and Stop Command**

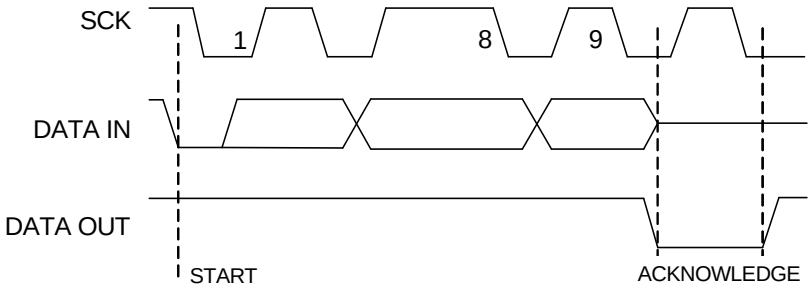



**Figure 5. SMI Host to SMI Slave**

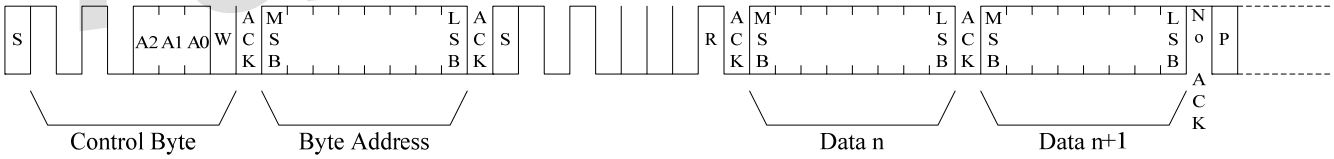



**Figure 6. SMI Host Mode Frame**

# 10. PON Interface

## 10.1. GPON Interface Overview

The RTL9601 supports a PON interface compliant with ITU G.984. It supports upstream and downstream FEC, downstream AES and key switching, DBRu, H/W dying gasp, etc.

The RTL9601 has 128 GEM ports and 32 TCONTs. It has 128 queues in a PON port. For upstream direction, it supports multiple GEM mapping to one queue; and supports one queue mapping to multiple GEMs.

Each TCONT can schedule up to 32 queues. Each queue scheduling type can be configured as Strict Priority (SP) and Weighted Fair Queuing (WFQ). It supports mixed mode SP+WFQ in one scheduler (TCONT).

It supports per queue configurable Committed Information Rate (CIR) and Peak Information Rate (PIR), with SP/WFQ/SP+WFQ operating simultaneously. It is compliant with the traffic management option in ITU G.988.

The PON Interface of the RTL9601 supports CML and LVPEL mode on the SerDes Tx side, and CML mode to a Fiber Transceiver on the SerDes Rx side.



## 10.2. EPON Interface Overview

The RTL9601 supports an EPON interface that is compliant with the IEEE 802.3 EPON MAC standard.

- Point to Multi-point protocol with interoperability
- Single Copy Broadcast (SCB)
- Queue set report

It supports upstream and downstream FEC, downstream traffic decryption, queue set reporting, RFC4837 MIB counter, H/W dying gasp, etc.

Each queue scheduling type can be configured as Strict Priority (SP) and Weighted Fair Queuing (WFQ). It supports mixed mode SP+WFQ.

It supports per queue configurable Committed Information Rate (CIR) and Peak Information Rate (PIR), with SP/WFQ/SP+WFQ operating simultaneously.

# 10.3. PON TX

## 10.3.1. CML Mode

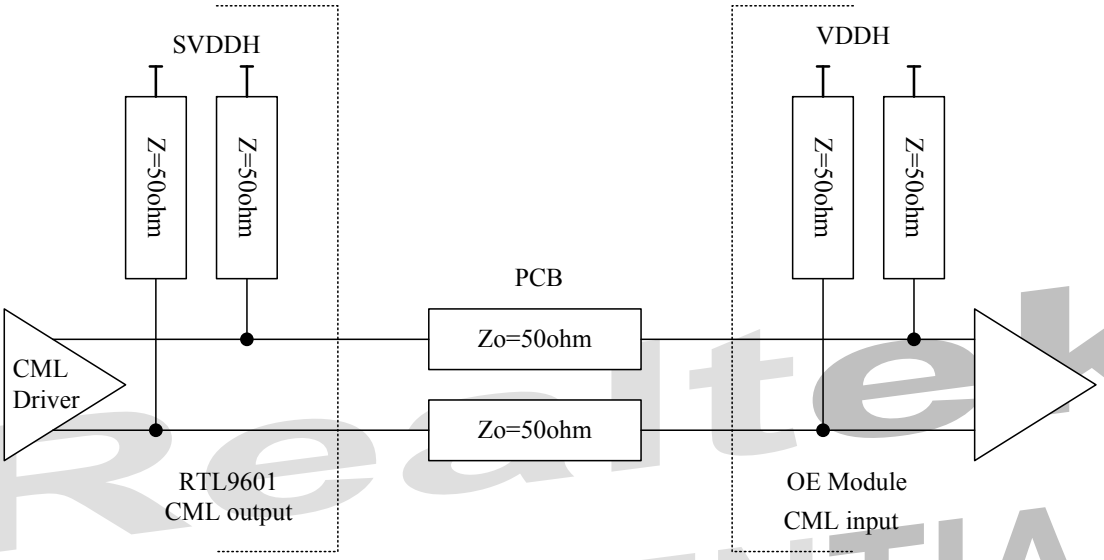



**Figure 7. PON SerDes TX CML Mode**

## 10.3.2. LVPECL Mode

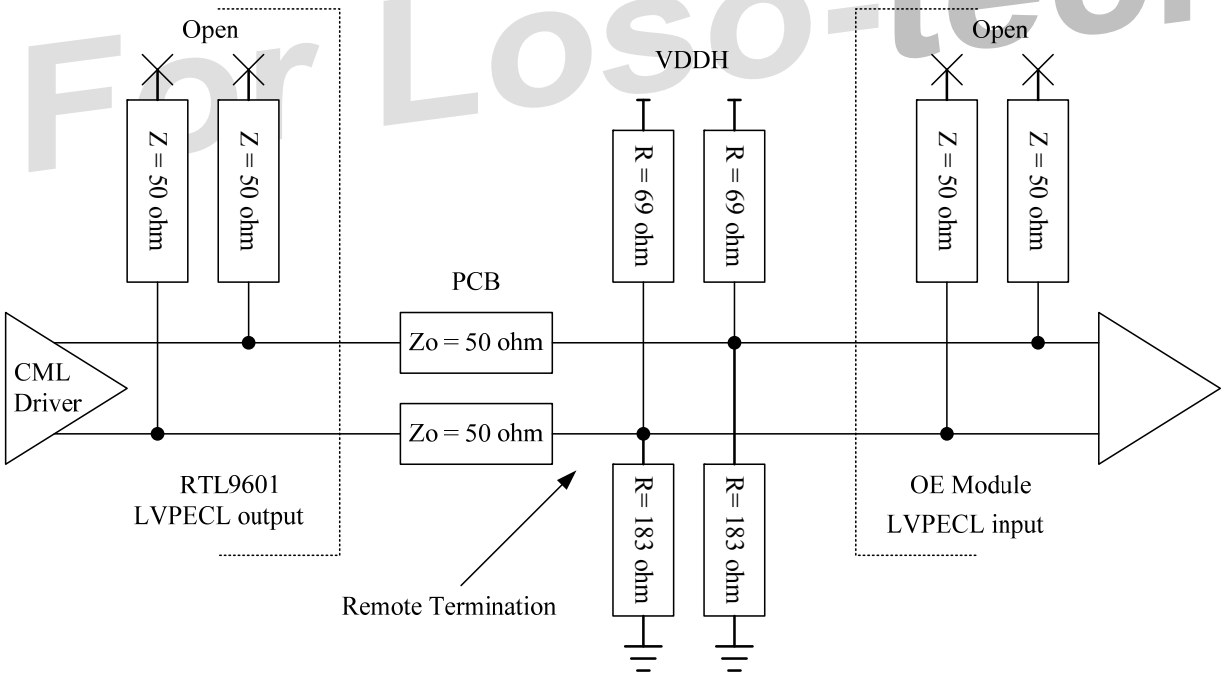



**Figure 8. PON SerDes TX LVPECL Mode**

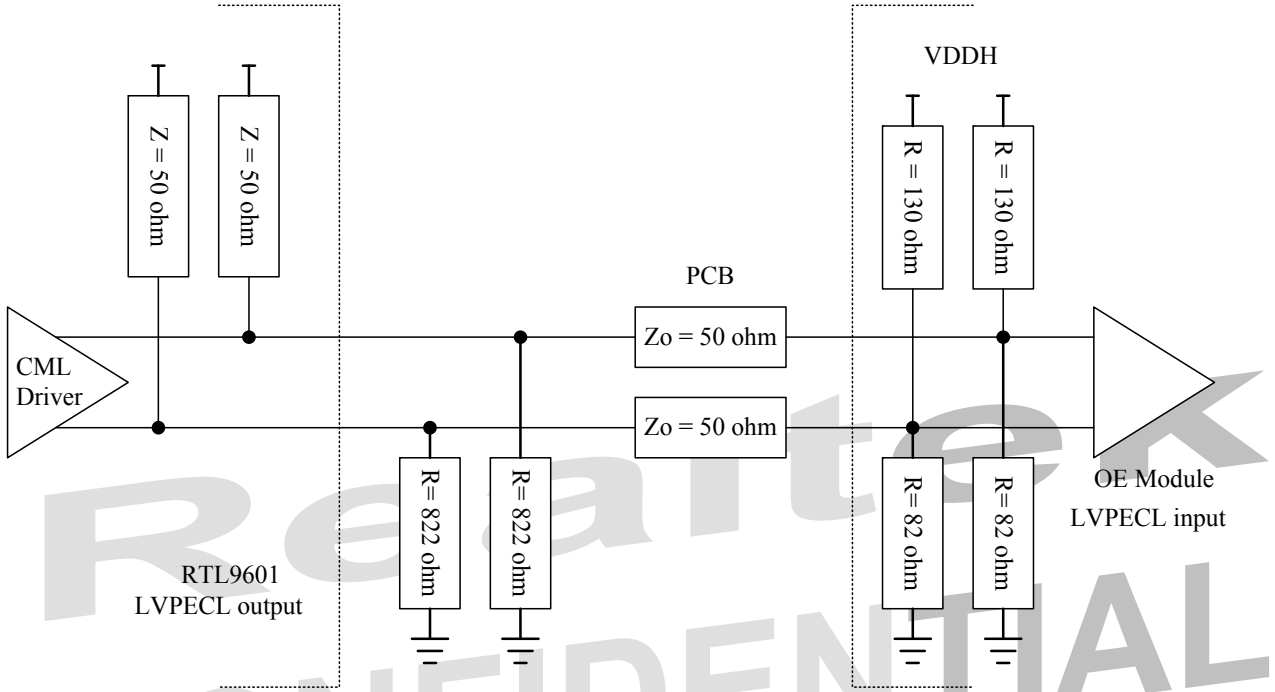



**Figure 9. PON SerDes TX LVPECL Mode**



## *10.4. PON RX*

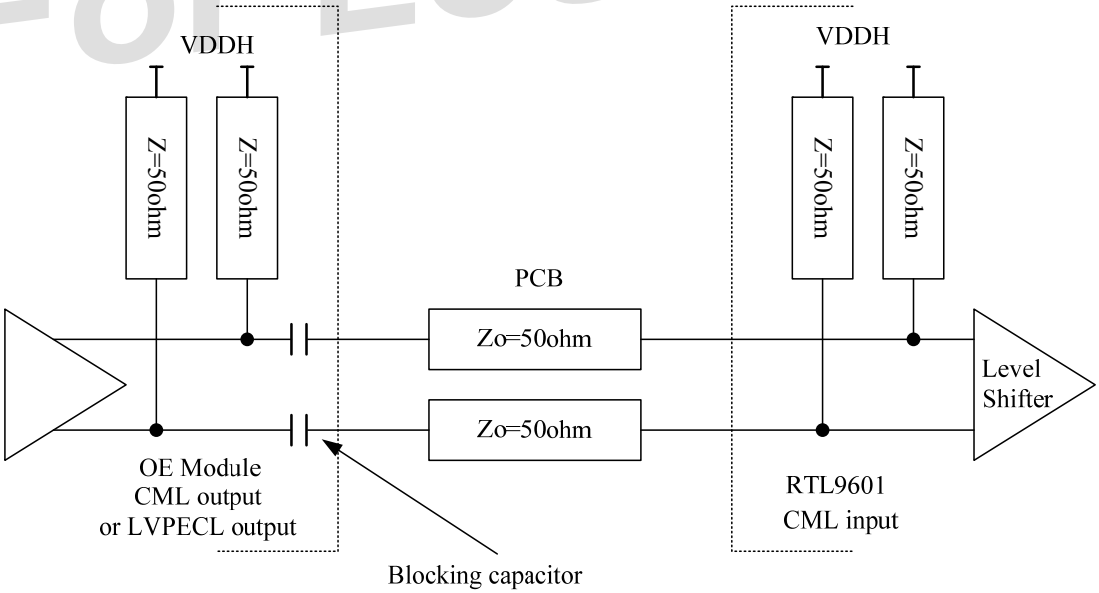



**Figure 10. PON SerDes RX CML Mode**

# 11. Physical Layer Functional Overview

## 11.1. MDI Interface

The RTL9601 embeds one 10/100/1000M Ethernet PHY. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

## 11.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.



## 11.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

## 11.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

## 11.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

## 11.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.



## 11.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

## 11.8. Auto-Negotiation for UTP

The RTL9601 obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL9601 advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

## 11.9. Crossover Detection and Auto Correction

The RTL9601 automatically determines whether or not it needs to crossover between pairs (see Table 18) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL9601 automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

**Table 18. Media Dependent Interface Pin Mapping**

| Pairs | MDI | | | MDI Crossover | | |
|---|---|---|---|---|---|---|
| | 1000Base-T | 100Base-TX | 10Base-T | 1000Base-T | 100Base-TX | 10Base-T |
| A | A | TX | TX | B | RX | RX |
| B | B | RX | RX | A | TX | TX |
| C | C | Unused | Unused | D | Unused | Unused |
| D | D | Unused | Unused | C | Unused | Unused |



## 11.10. Polarity Correction

The RTL9601 automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

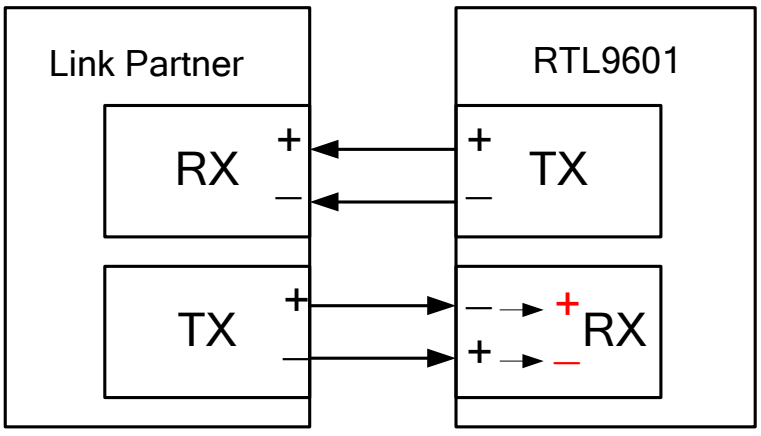



**Figure 11. Conceptual Example of Polarity Correction**

# 12. General Function Description

## 12.1. Reset

### 12.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL9601 will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the boot code and system image from flash if flash is detected.
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the CPU.

### 12.1.2. Software Reset

The RTL9601 supports two software resets; a chip reset and a soft reset.

#### *12.1.2.1 CHIP_RESET*

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and boot code, system image form flash.

2. Clear all the Lookup and VLAN tables

3. Reset all registers to default values

4. Restart the auto-negotiation process

#### *12.1.2.2 SOFT_RESET*

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list

2. Restart the auto-negotiation process

## 12.2. IEEE 802.3x Full Duplex Flow Control

The RTL9601 supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

## 12.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "Truncated Binary Exponential Backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL9601 is 9.

The half duplex back-off algorithm in the RTL9601 does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

### 12.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL9601 sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL9601 supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

## 12.4. Search and Learning

**Search**

When a packet is received, the RTL9601 has two kinds of search key. One uses the destination MAC address, Filtering Identifier (FID) and enhanced Filtering Identifier (EFID) to search the 2K-entry look-up table. The other uses the destination MAC address, VID and EFID to search the look-up table. The 48-bit MAC address, 4-bit FID or 12-bit VID, and 3-bit EFID use a hash algorithm to calculate an 9-bit index value. The RTL9601 uses the index to compare the packet MAC address with the entries (MAC addresses) in the 4-way look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

**Learning**

The RTL9601 has two kinds of search key. It can use the source MAC address, FID, and EFID of the incoming packet or use the source MAC address, VID, and EFID of the incoming packet to hash into a 9-bit index. It then compares the source MAC address with the data (MAC addresses) in this index of 4-way look-up table. If there is a match with one of the entries, the RTL9601 will update the entry with new information. If there is no match and the 4-way entries are not all occupied by other MAC addresses, the RTL9601 will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

If the look-up table is full, the source MAC address will not be learned in the RTL9601.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL9601 is can be set to 0.1 ~ 200, 000 seconds.



## 12.5. SVL and IVL/SVL

The RTL9601 supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. The RTL9601 also supports IVL mode for L2 search and learning. In IVL mode, the search key is MAC address, VID and EFID, the same source MAC address with different VIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

## 12.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL9601. The maximum packet length may be set to 16 ~ 16K bytes.

## 12.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL9601 supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 19 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

**Table 19. Reserved Multicast Address Configuration Table**

| Assignment | Value |
|---|---|
| Bridge Group Address | 01-80-C2-00-00-00 |
| IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation | 01-80-C2-00-00-01 |
| IEEE Std 802.3ad Slow Protocols-Multicast Address | 01-80-C2-00-00-02 |
| IEEE Std 802.1X PAE Address | 01-80-C2-00-00-03 |
| Provider Bridge Group Address | 1-80-C2-00-00-08 |
| Undefined 802.1 Address | 01-80-C2-00-00-04 ~<br>01-80-C2-00-00-07<br>&<br>01-80-C2-00-00-09 ~<br>01-80-C2-00-00-0C<br>&<br>01-80-C2-00-00-0F |
| Provider Bridge MVRP Address | 01-80-C2-00-00-0D |
| IEEE Std 802.1AB Link Layer Discovery Protocol Address | 01-80-C2-00-00-0E |
| All LANs Bridge Management Group Address | 01-80-C2-00-00-10 |
| Load Server Generic Address | 01-80-C2-00-00-11 |
| Loadable Device Generic Address | 01-80-C2-00-00-12 |
| Undefined 802.1 Address | 01-80-C2-00-00-13 ~<br>01-80-C2-00-00-17<br>&<br>01-80-C2-00-00-19<br>&<br>01-80-C2-00-00-1B ~<br>01-80-C2-00-00-1F |
| Generic Address for All Manager Stations | 01-80-C2-00-00-18 |
| Generic Address for All Agent Stations | 01-80-C2-00-00-1a |
| GMRP Address | 01-80-C2-00-00-20 |
| GVRP Address | 01-80-C2-00-00-21 |
| Undefined GARP Address | 01-80-C2-00-00-22<br>\|<br>01-80-C2-00-00-2F |

## 12.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL9601 enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate, all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

## 12.9. Port Security Function

The RTL9601 supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets



## 12.10. MIB Counters

The RTL9601 supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

## 12.11. Port Mirroring

The RTL9601 supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored to multiple mirror ports.

# 12.12. VLAN Function

The RTL9601 supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

**Ingress Filtering**

- The acceptable frame type of the ingress process can be set to 'Admit All' or 'Admit All Tagged'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

**Egress Filtering**

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL9601 will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL9601 also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL9601 supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL9601 also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.



## 12.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached flash or UART interface. The 4K-entry VLAN Table designed into the RTL9601 provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

## 12.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL9601 supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL9601 uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL9601 compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When ‘802.1Q tag aware VLAN’ is enabled, the RTL9601 performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If ‘802.1Q tag aware VLAN’ is disabled, the RTL9601 performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when ‘802.1Q tag aware VLAN’ is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL9601. One is the ‘VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is ‘VLAN member set ingress filtering’, which will drop frames if the ingress port is not in the member set.

## 12.12.3. Protocol-Based VLAN

The RTL9601 supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 12. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be ‘Ethernet’, and value to be ‘0x0800’. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

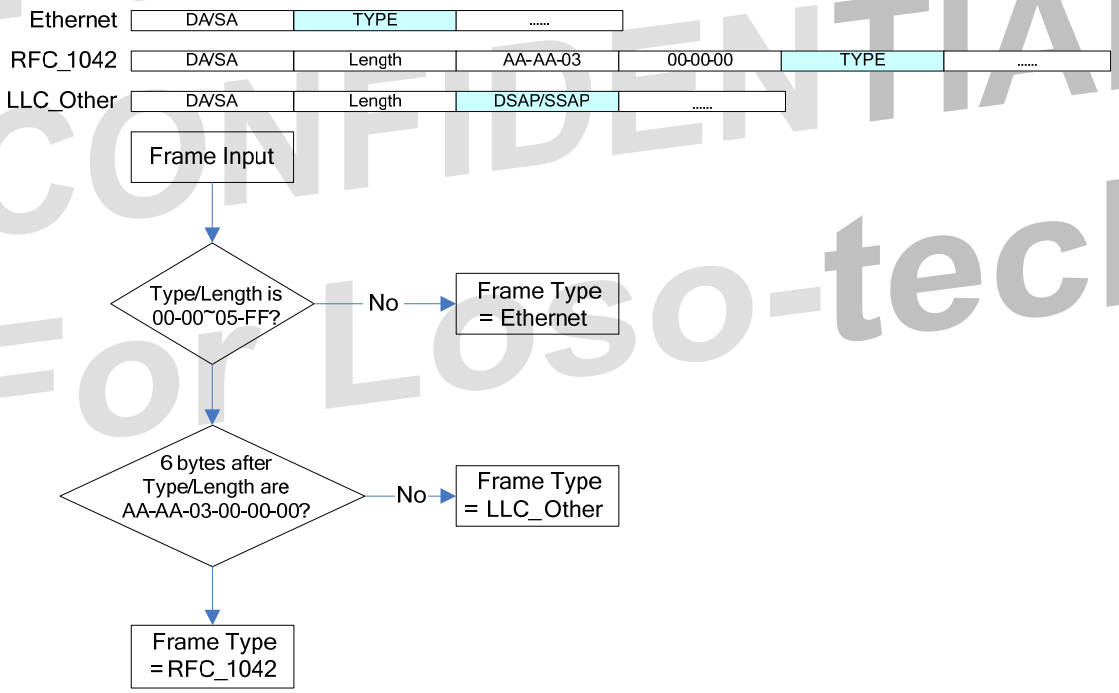



**Figure 12. Protocol-Based VLAN Frame Format and Flow Chart**

## 12.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL9601 supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is

enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL9601 will drop non-tagged packets and packets with an incorrect PVID.

## *12.13. QoS Function*

The RTL9601 supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL9601, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queuing (WFQ) for packet scheduling algorithm.

### 12.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

### 12.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL9601 can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL9601 identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

## 12.13.3. Priority Queue Scheduling

The RTL9601 supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- Average Packet Rate (APR) leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queuing (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 13 shows the RTL9601 packet-scheduling diagram.

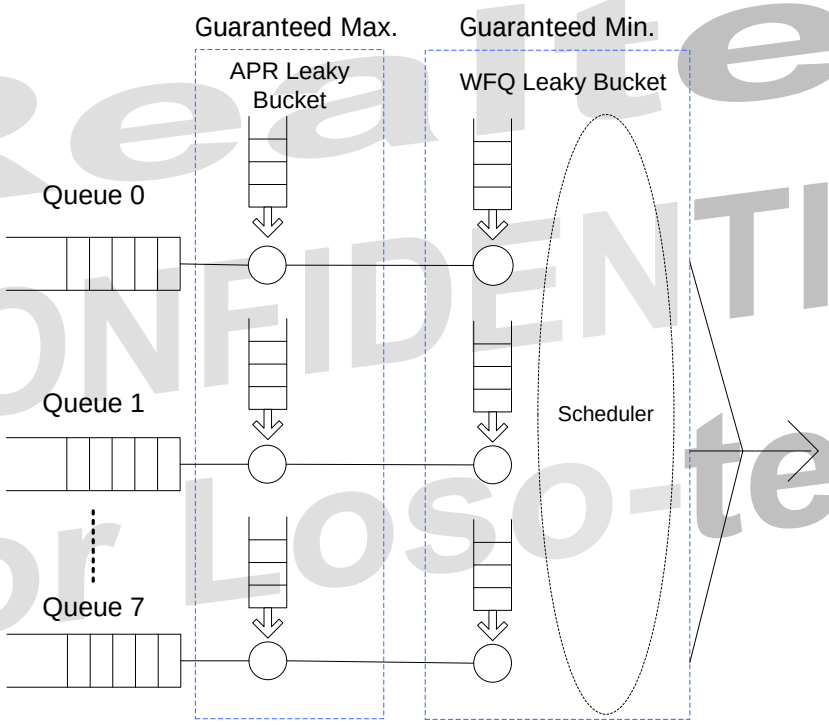



**Figure 13. RTL9601 MAX-MIN Scheduling Diagram**



## 12.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL9601 supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. Each output queue has a 3-bit 802.1p/Q, and a 6-bit IP DSCP value configuration register.

### 12.13.5. ACL-Based Priority

The RTL9601 supports 64-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

## *12.14. IEEE 802.1x Function*

The RTL9601 supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior
- Guest VLAN

### 12.14.1. Port-Based Access Control

Each port of the RTL9601 can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

### 12.14.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

### 12.14.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

### 12.14.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

### 12.14.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction should be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

### 12.14.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

### 12.14.7. Guest VLAN

When the RTL9601 enables the Port-based or MAC-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, the RTL9601 will drop all packets from this port.

The RTL9601 also supports one Guest VLAN to allow unauthorized ports or packets to be forwarded to a limited VLAN domain. The user can configure one VLAN ID and member set for these unauthorized packets.

## 12.15. IEEE 802.1D Function

When using IEEE 802.1D, the RTL9601 supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL9601 also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

## 12.16. Classification

The RTL9601 supports 512-entry classification rules. When a packet is received, its physical port, ether type, VLAN, IP ToS, GPON stream ID, and internal priority are recorded and compared to classification entries.

If a received packet matches valid entries, the actions of the first matched entry will be applied. The action can be devided to upstream action and downstream action. For upstream action, it includs:

- S-tag action
- C-tag action
- User priority action
- GPON stream ID action
- DSCP remarking
- DROP action
- LOG action

For downstream action, it includes:

- S-tag action
- C-tag action
- User priority action
- Forwarding port mask
- DSCP remarking

## 12.17. Realtek Cable Test (RTCT)

The RTL9601 physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair.

## 12.18. LED Indicator

The RTL9601 supports parallel LED mode and serial LED mode. Each LED can be configured for any port, and composes the following basic elements (defined in Table 20) to achieve indicator information, e.g., Indicator 'Link', select 'Spd1000', 'Spd100', 'Spd10'; Indicator 'Link/Act', select 'Spd1000', 'Spd100', 'Spd10','Spd1000 Act', 'Spd100 Act', 'Spd10 Act'.

**Table 20. LED Basic Elements**

| LED Statuses | Description |
|---|---|
| Spd1000 | 1000Mbps Speed Indicator. Low for 1000Mbps. |
| Spd100 | 100Mbps Speed Indicator. Low for 100Mbps. |
| Spd10 | 10Mbps Speed Indicator. Low for 10Mbps. |
| Dup | Duplex Indicator.<br>Low for full duplex, and high for half duplex mode. |
| Spd1000 Act | 1000Mbps Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving. |
| Spd100 Act | 100Mbps Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving. |
| Spd10 Act | 10Mbps Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving. |
| Col | Collision Indicator.<br>Blinking when collision occurs. |

## 12.18.1. Parallel LED Indicator

The RTL9601 supports 6 parallel LEDs. Refer to section 7.6 Parallel LED Pins, page 15 for pin details.

Some of the LED pin also supports pin strapping configuration functions. Those LED pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is pulled high upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. For details refer to Figure 14, page 45, and Figure 15, page 45. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The LED pins also can be configured as a Bi-color LED. However not any two LED pins can be connected as Bi-color mode, as one Bi-color LED pin should operate with the same polarity as the other Bi-color LED pins. Two LED pins with strapping function are not recommended to be connected in Bi-color mode, as two strapping pins could possibly be configured with different polarity.

For example:

- LED12 should pull up upon reset if LED12 is combined with LED13 as a Bi-color LED, and LED13 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset

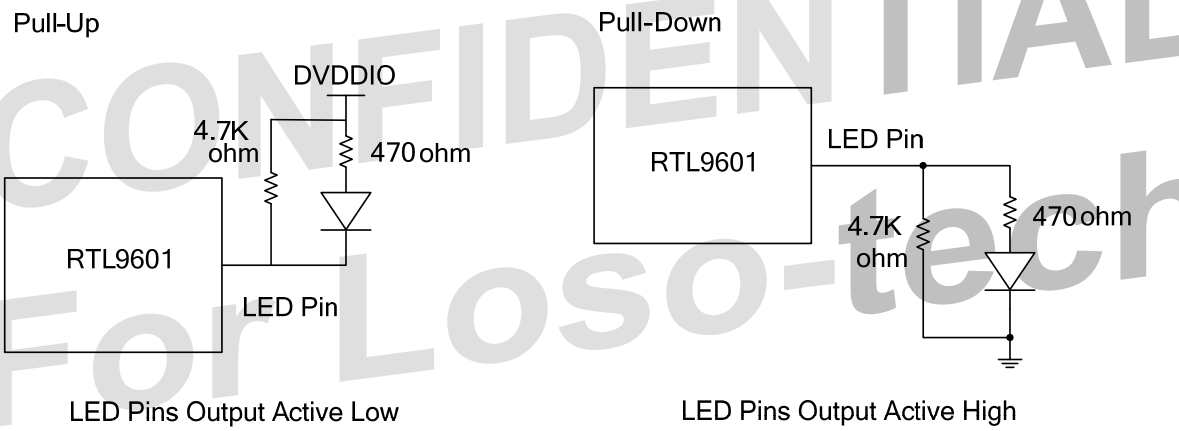



**Figure 14. Pull-Up and Pull-Down of LED Pins for Single-Color LED**

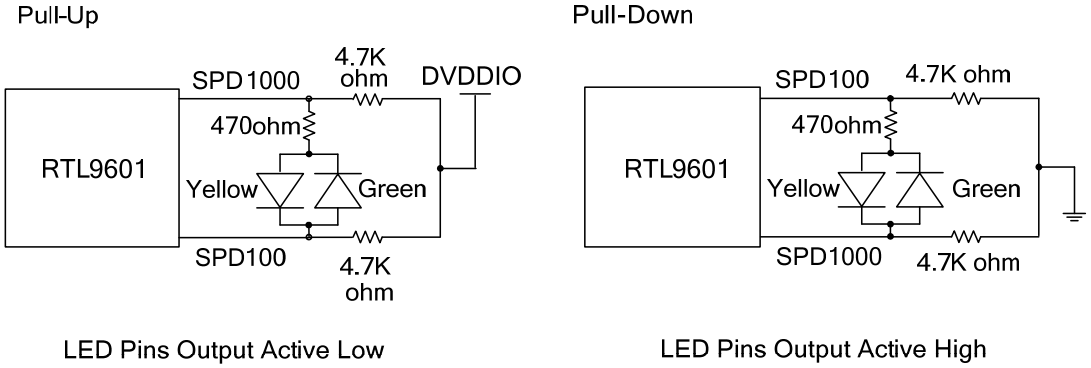



**Figure 15. Pull-Up and Pull-Down of LED Pins for Bi-Color LED**

## 12.18.2. Serial LED Indicator

The RTL9601 also supports 32 serial LEDs. The serial LED mode uses 2 pins SLED_CK/SLED_DA to connect a shift logic circuit, e.g., RTL8231 or 74164. The output sequence is shown in Figure 16. Refer to section 7.7 Serial LED Pins, page 16 for pin details.

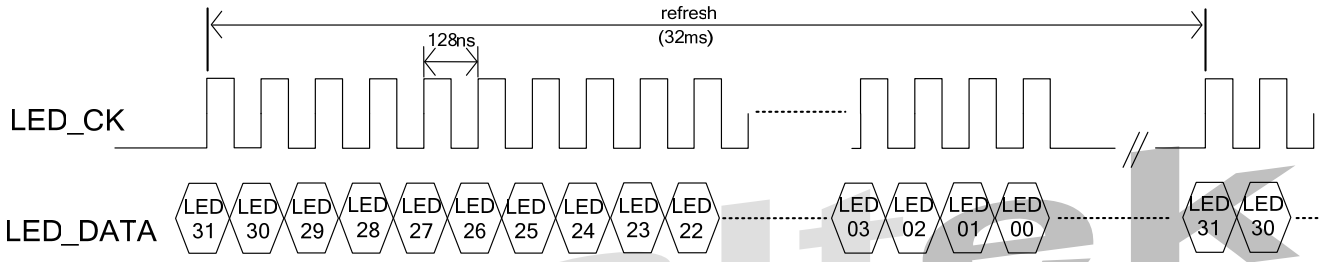



**Figure 16. Serial LED Output Signal**

# 12.19. Green Ethernet

## 12.19.1. Link-On and Cable Length Power Saving

The RTL9601 provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

## 12.19.2. Link-Down Power Saving

The RTL9601 implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

# 12.20. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL9601 support IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL9601 MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

# 13. DC Specifications

## 13.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 21. Absolute Maximum Ratings**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Junction Temperature (Tj) | - | +125 | °C |
| Storage Temperature | -45 | +125 | °C |
| DVDDIO, AVDDH, SVDDH, UVDDH Supply Referenced to GND and AGND | GND-0.3 | +3.63 | V |
| DVDDL, AVDDL, PLLVDDL0, PLLVDDL1, SVDDL, UVDDL, Supply Referenced to GND, AGND. | GND-0.3 | +1.1 | V |
| OVDDR Supply Referenced to GND, AGND. | GND-0.3 | +2.75 | V |
| Digital Input Voltage | GND-0.3 | DVDDIO+0.3 | V |

## 13.2. Operating Conditions

**Table 22. Operating Conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Ta | Ambient Operating Temperature | 0 | - | 70 | °C |
| DVDDIO | Digital I/O High Voltage Power | 3.135 | 3.3 | 3.465 | V |
| DVDDL | Digital Low Voltage Power. | 0.95 | 1.0 | 1.05 | V |
| AVDDH | Analog High Voltage Power. | 3.135 | 3.3 | 3.465 | V |
| AVDDL | Analog Low Voltage Power. | 0.95 | 1.0 | 1.05 | V |
| PLLVDDL0 | PLL0 Low Voltage Power. | 0.95 | 1.0 | 1.05 | V |
| PLLVDDL1 | PLL1 Low Voltage Power. | 0.95 | 1.0 | 1.05 | V |
| SVDDH | SerDes Analog High Voltage Power. | 3.135 | 3.3 | 3.465 | V |
| SVDDL | SerDes Analog Low Voltage Power. | 0.95 | 1.0 | 1.05 | V |
| UVDDH | Analog High Voltage Power. | 3.135 | 3.3 | 3.465 | V |
| UVDDL | Analog Low Voltage Power. | 0.95 | 1.0 | 1.05 | V |
| OVDDR | DDR SDRAM I/O Power Supply<br>DDR2 SDRAM I/O Power Supply 1.8V<br>DDR3 SDRAM I/O Power Supply 1.5V | <br>1.7<br>1.4 | <br>1.8<br>1.5 | <br>1.9<br>1.6 | V |
| MVREF | DDR2 Reference Voltage | 0.49* OVDDR | 0.5* OVDDR | 0.51* OVDDR | V |

## 13.3. Total Power Consumption

**Table 23. Total Power Consumption**

| SYM | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| PS | All LAN Ports Idle and CPU Suspended | - | TBD | - | Watt |
| | All LAN Ports Idle | - | TBD | - | |
| | LAN Full Load Active for Link at 10Base-T | - | TBD | - | |
| | LAN Full Load Active for Link at 100Base-TX | - | TBD | - | |
| | LAN Full Load Active for Link at 1000Base-TX | - | TBD | - | |

*Note: Power consumption is measured at full load of the chip system.*

## 13.4. DDR SDRAM Bus DC Parameters

**Table 24. DDR SDRAM Bus DC Parameters**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | SSTL_2 | MVREF+0.15 | - | MVREF+0.3 | V |
| $V_{IL}$ | Input-Low Voltage | SSTL_2 | -0.3 | - | MVREF-0.15 | V |
| $V_{TT}$ | I/O Termination Voltage | - | MVREF-0.04 | - | MVREF+0.04 | V |
| $I_{IL}$ | Input-Leakage Current | $V_{IN}$=MVREF or 0 | -10 | ±1 | 10 | µA |
| $I_{OZ}$ | Tri-State Output-Leakage Current | - | -10 | ±1 | 10 | µA |

## 13.5. Flash Bus DC Parameters

**Table 25. Flash Bus DC Parameters**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | LVTTL | 2.0 | - | - | V | 1 |
| $V_{IL}$ | Input-Low Voltage | LVTTL | - | - | 0.8 | V | 2 |
| $V_{OH}$ | Output-High Voltage | - | 2.4 | - | - | V | 3 |
| $V_{OL}$ | Output-Low Voltage | - | - | - | 0.4 | V | 3 |
| $I_{IL}$ | Input-Leakage Current | $V_{IN}$=3.3V or 0 | -10 | ±1 | 10 | µA | - |
| $I_{OZ}$ | Tri-State Output-Leakage Current | - | -10 | ±1 | 10 | µA | - |
| $R_{PU}$ | Input Pull-Up Resistance | - | - | 75 | - | KΩ | 4 |
| $R_{PD}$ | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 4 |

*Note 1: VIH overshot: VIH (MAX)=VDDH + 2V for a pulse width ≤ 3ns.*

*Note 2: VIL undershot: VIL (MIN)=-2V for a pulse width ≤ 3ns.*

*Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.*

*Note 4: These values are typical values checked in the manufacturing process and are not tested.*

## 13.6. UART DC Parameters

Table 26. UART DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | LVTTL | 2.0 | - | - | V | - |
| $V_{IL}$ | Input-Low Voltage | LVTTL | - | - | 0.8 | V | - |
| $V_{OH}$ | Output-High Voltage | - | 2.4 | - | - | V | 1 |
| $V_{OL}$ | Output-Low Voltage | - | - | - | 0.4 | V | 1 |
| $I_{IL}$ | Input-Leakage Current | $V_{IN}$=3.3V or 0 | -10 | ±1 | 10 | μA | 2 |
| $R_{PU}$ | Input Pull-Up Resistance | - | - | 75 | - | KΩ | 2 |
| $R_{PD}$ | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 2 |

*Note 1: The output current buffer is 8mA for UART related signals.*

*Note 2: These values are typical values checked in the manufacturing process and are not tested.*

## 13.7. GPIO DC Parameters

Table 27. GPIO DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | LVTTL | 2.0 | - | - | V | - |
| $V_{IL}$ | Input-Low Voltage | LVTTL | - | - | 0.8 | V | - |
| $V_{OH}$ | Output-High Voltage | - | 2.4 | - | - | V | 1 |
| $V_{OL}$ | Output-Low Voltage | - | - | - | 0.4 | V | 1 |
| $I_{IL}$ | Input-Leakage Current | - | -10 | ±1 | 10 | μA | 2 |
| $R_{PD}$ | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 2 |

*Note 1: The output current buffer is 8mA for GPIO related signals.*

*Note 2: These values are typical values checked in the manufacturing process and are not tested.*

## 13.8. JTAG DC Parameters

Table 28. JTAG DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | LVTTL | 2.0 | - | - | V | - |
| $V_{IL}$ | Input-Low Voltage | LVTTL | - | - | 0.8 | V | - |
| $V_{OH}$ | Output-High Voltage | $\lvert I_{OH} \rvert$ =2~16mA | 2.4 | - | - | V | 1 |
| $V_{OL}$ | Output-Low Voltage | $\lvert I_{OL} \rvert$ =2~16mA | - | - | 0.4 | V | 1 |
| $I_{IL}$ | Input-Leakage Current | - | -10 | ±1 | 10 | μA | 2 |
| $R_{PD}$ | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 2 |

*Note 1: The output current buffer is 4mA for JTAG related signals.*

*Note 2: These values are typical values checked in the manufacturing process and are not tested.*

## 13.9. PON SerDes DC Parameters

Table 29. Reset DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | LVTTL | 2.0 | - | - | V |
| $V_{IL}$ | Input-Low Voltage | LVTTL | - | - | 0.8 | V |
| $V_{OH}$ | Output-High Voltage | LVTTL | 2.4 | - | - | |
| $V_{OL}$ | Output-Low Voltage | LVTTL | - | - | 0.4 | |

## 13.10. Reset DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | LVTTL | 2.0 | - | - | V |
| $V_{IL}$ | Input-Low Voltage | LVTTL | - | - | 0.8 | V |

## 13.11. LED DC Parameters

Table 30. LED DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OHED}$ | Output-High Voltage | - | 2.4 | - | - | V |
| $V_{OLLED}$ | Output-Low Voltage | - | - | - | 0.4 | V |

*Note: The output current buffer for LED signals is 8mA.*

# 14. AC Specifications

## *14.1. Clock Signal Timing*

### 14.1.1. 25MHz System Clock Timing

**Table 31. 25MHz System Clock Timing**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input-High Voltage | 2.0 | - | - | V | - |
| $V_{IL}$ | Input-Low Voltage | - | - | 0.8 | V | - |
| $T_{FREQUENCY}$ | Clock Frequency for RTL9601 Crystal or Oscillator | - | 25 | - | MHz | 1 |
| $\Delta_{FREQUENCY}$ | Clock Tolerance Over 0ºC to 50ºC | -50 | - | 50 | ppm | - |
| $C_{SHUNT}$ | Crystal Parameter (Sometimes Referred to as the Holder Capacitance) | - | - | 7 | pF | - |
| $C_1$ | Load Capacitance | - | - | 30 | pF | 2 |
| $C_2$ | Load Capacitance | - | - | 30 | pF | 2 |
| $T_{DC}$ | Duty Cycle | - | 50 | - | % | - |

*Note 1: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.*

*Note 2: The RTL9601 PLL circuit requires an external 25MHz crystal with shunt capacitors. These shunt capacitors cannot be over 30pF due to chip design requirements.*



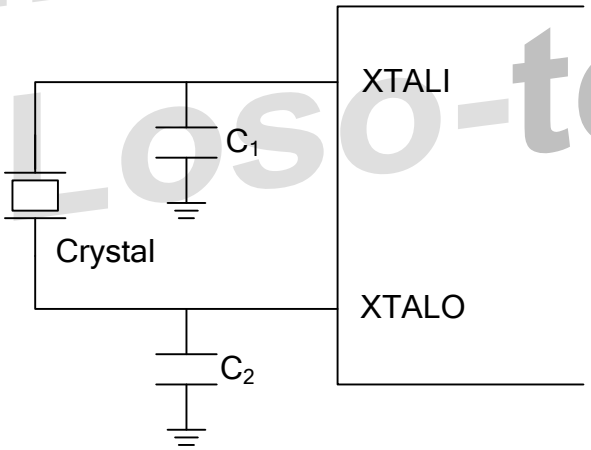



**Figure 17. Typical Connection to a Crystal**

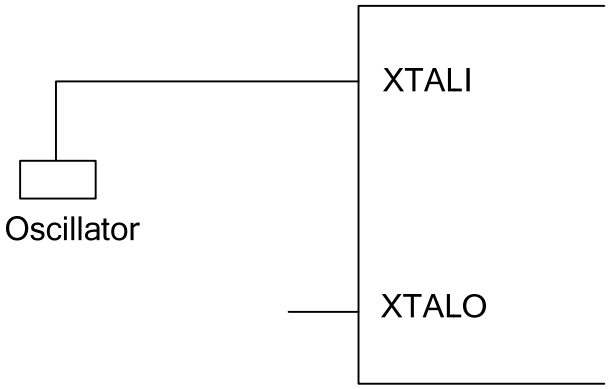



**Figure 18. Typical Connection to an Oscillator**

# 14.2. Bus Signal Timing

## 14.2.1. DDR SDRAM Bus

### 14.2.1.1 DDR SDRAM Input Timing

**Table 32. DDR SDRAM Input Timing**

| Symbol | Parameter | Units | Notes |
|---|---|---|---|
| $T_{SETUP}$ | Input Setup Prior to Rising Edge of Clock.<br>Inputs included in this timing are D[31: 0] (during a read operation) | ns | 1 |
| $T_{HOLD}$ | Input Hold Time after the Rising Edge of Clock.<br>Inputs included in this timing are D[31:0] (during a read operation) | ns | 1 |

*Note1: The RTL9601 integrates some timing control registers on the interface.*

### 14.2.1.2 DDR SDRAM Output Timing

**Table 33. DDR SDRAM Output Timing**

| Symbol | Parameter | Units | Notes |
|---|---|---|---|
| $T_{CLK2OUT}$ | Rising Edge of Clock-to-Signal Output.<br>Outputs include this timing are D[31: 0], CS0#, RAS#, CAS#, LDQM, UDQM, WE#, LDQS, UDQS (during a write operation) | ns | 1 |
| $T_{HOLDOUT}$ | Signal Output Hold Time after the Rising Edge of the Clock.<br>Outputs included in this timing are D[31: 0] (during a write operation) | ns | 1 |

*Note1: The RTL9601 integrates some timing control registers on the interface.*

### 14.2.1.3 DDR SDRAM Access Control Timing

**Table 34. DDR SDRAM Access Control Timing**

| Symbol | Parameter | Units | Notes |
|---|---|---|---|
| $T_{REFRESH}$ | Auto-Refresh Timing.<br>Controlled by Reg. 0xB8001008 (DTR) | µs | - |

| Symbol | Parameter | Units | Notes |
|---|---|---|---|
| $T_{RCD}$ | The Time Interval between RAS# Active and CAS# Active.<br>Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| $T_{RP}$ | The Time Interval between Pre-Charge and the Next Active.<br>Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| $T_{RAS}$ | The Time Interval between Active and Pre-Charge.<br>Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| $T_{RC}$ | The Time Interval between Active and the Next Active.<br>Controlled by Reg. 0xB8001008 (DTR) | ns | 1 |
| $T_{RFC}$ | The Time Interval between Auto-Refresh and Active.<br>Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| $T_{CAS\_LATENCY}$ | The Data Output Delay after CAS# Active.<br>Controlled by Reg. 0xB8001004 (DCR) | ns | - |

*Note 1: TRC=TRAS+TRP.*

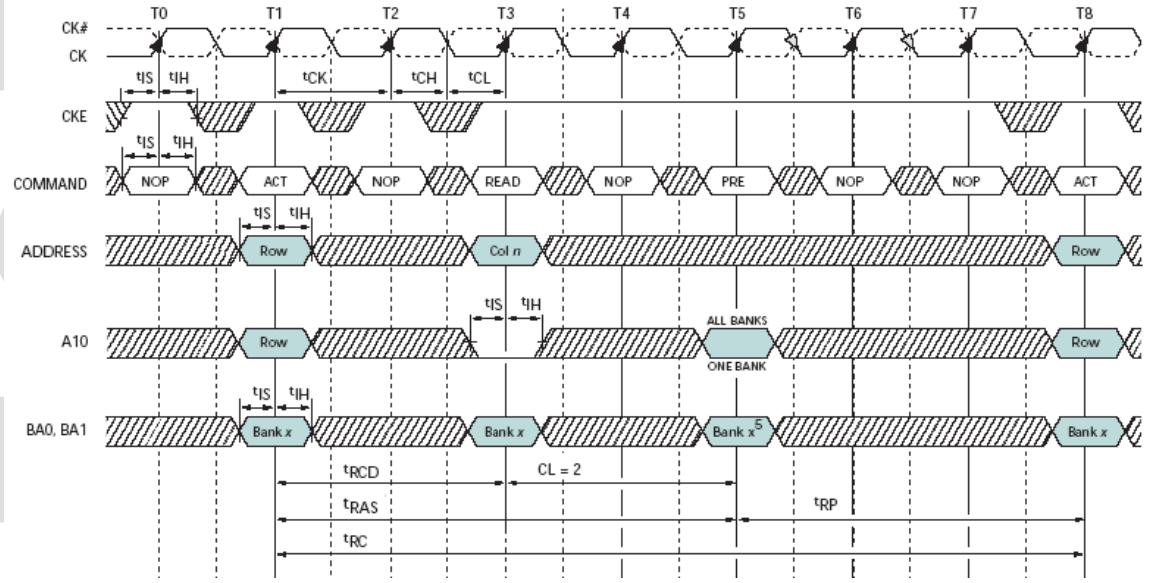



**Figure 19. DDR SDRAM Access Control Timing**

## 14.2.2. Serial Flash Interface

### *14.2.2.1 Serial Flash Interface Output Timing*

**Table 35. Serial Flash Interface Output Timing**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{SLCH}$ | The Timing Interval from Chip-Select Activated to the First Clock Rising Edge | $0.5*T_{SFCK}$ - 1 | - | $0.5*T_{SFCK}$ | ns |
| $T_{CHSH}$ | The Timing Interval from the Last Clock Rising Edge to Chip-Select De-Activated | $T_{SFCK}$ + 7 | - | $T_{SFCK}$ + 9 | ns |
| $T_{CLQV}$ | The Timing Interval from the Last Clock Falling Edge to Data-Out Validated | - | - | 1 | ns |
| $T_{CLQX}$ | The Timing Interval from the Next Clock Falling Edge to Data-Out Invalidated | -1 | - | - | ns |

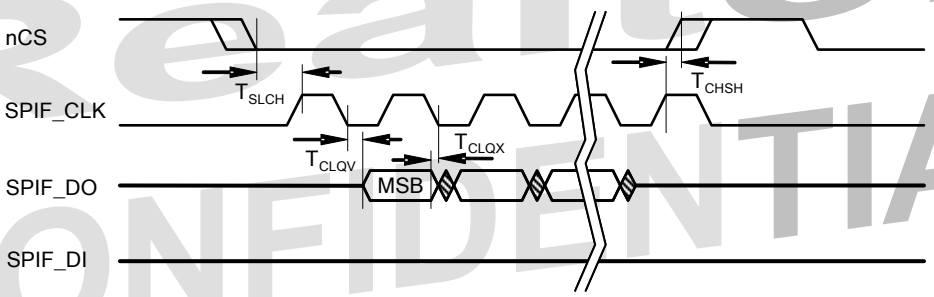



**Figure 20. Serial Flash Interface Output Timing**



### *14.2.2.2 Serial Flash Interface Intput Timing*

**Table 36. Serial Flash Interface Intput Timing**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{DVCH}$ | The Timing Interval from Data-Input Ready to the Clock Rising Edge | 0 | - | - | ns |
| $T_{CHDX}$ | The Timing Interval from the Clock Rising Edge to Data-Input Invalidated | $0.5*T_{SFCK}$ | - | - | ns |

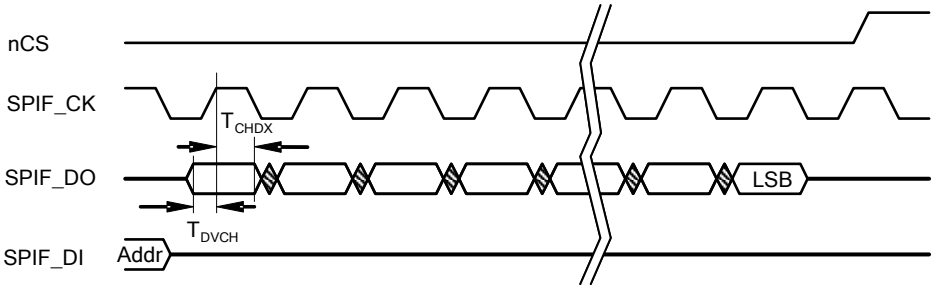



**Figure 21. Serial Flash Interface Intput Timing**

## 14.2.3. JTAG Boundary Scan

**Table 37. JTAG Boundary Scan Interface Timing Values**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{bscl}$ | JTAG Clock Low Time | 50 | - | - | ns | 1 |
| $T_{bsch}$ | JTAG Clock High Time | 50 | - | - | ns | 1 |
| $T_{bsis}$ | TDI, TMS Setup Time to Rising Edge of TCK | 10 | - | - | ns | - |
| $T_{bsih}$ | TDI, TMS Hold Time from Rising Edge of TCK | 10 | - | - | ns | - |
| $T_{bsoh}$ | TDO Hold Time after Falling Edge of TCK | 1.5 | - | - | ns | - |
| $T_{bsod}$ | TDO Output from Falling Edge of TCK | - | - | 40 | ns | - |
| $T_{bsr}$ | JTAG Reset Period | 30 | - | - | ns | - |
| $T_{bsrs}$ | TMS Setup Time to Rising Edge of JTAG Reset | 10 | - | - | ns | - |
| $T_{bsrh}$ | TMS Hold Time from Rising Edge of JTAG Reset | 10 | - | - | ns | - |

*Note 1: JTAG clock TCK may be stopped indefinitely in either the low or high phase.*



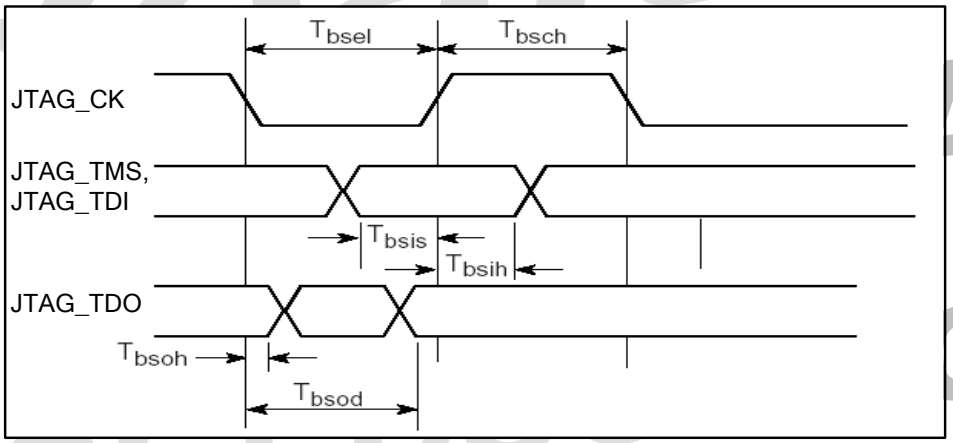



**Figure 22. Boundary-Scan General Timing**

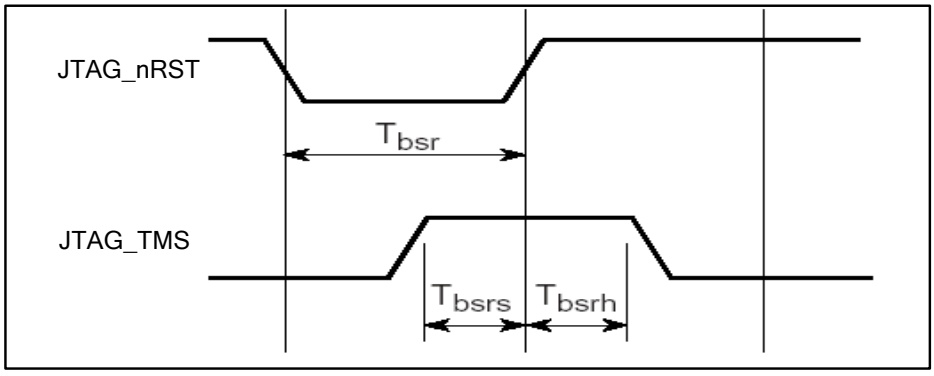



**Figure 23. Boundary-Scan Reset Timing**

## 14.2.4. Power Sequence

**Table 38. Power-Up Timing Parameters**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | 3.3V Stable to 1.0V | TBD | - | TBD | ms |

*Note 1: The 3.3V(I/O) must be powered up before or after 1.0V (core) and 1.0V (analog) voltage in TBD.*

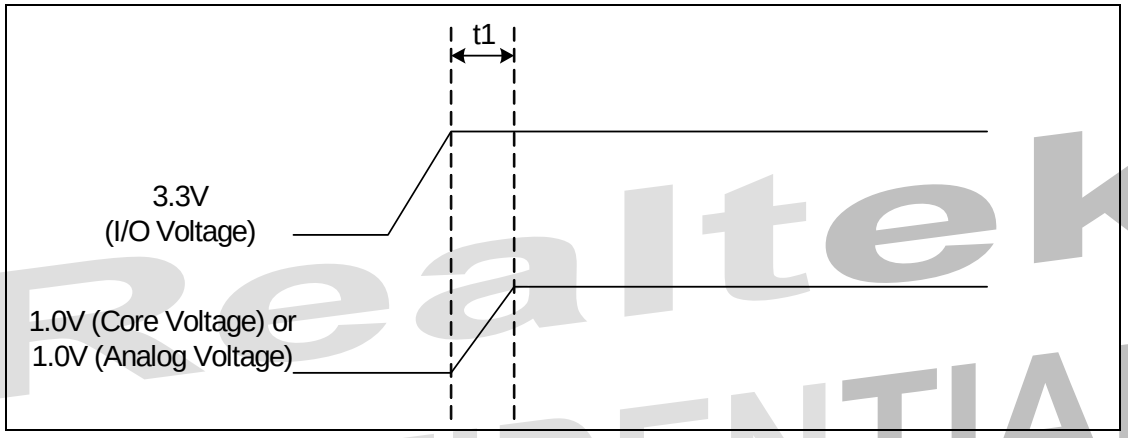



**Figure 24. Power Up Sequence Timing Diagram**



## 14.2.5. Power Configuration Timing

Power up configuration only relates to internal timing. The external hardware pin reset is unconcerned with power up configuration. The Hardware reset pin is valid when an internal reset ends the active state.

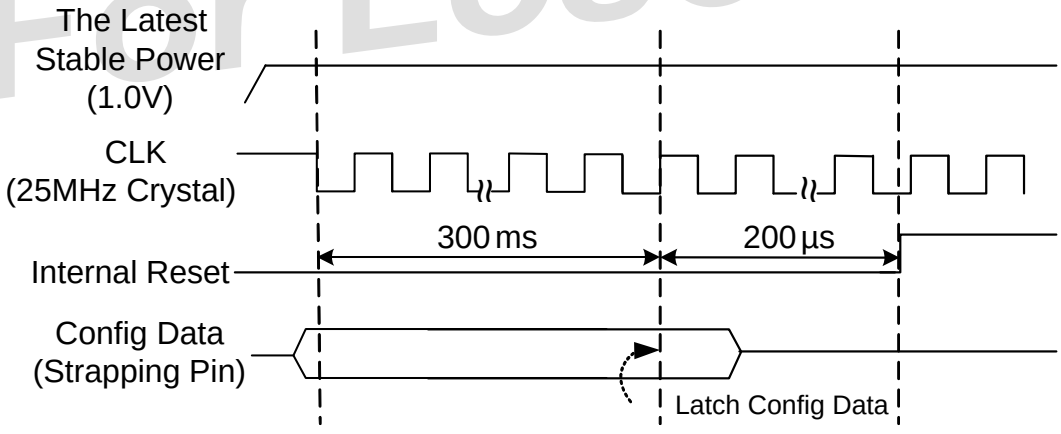



**Figure 25. Power Up Configuration Timing**

# 15. Thermal Characteristics

## 15.1. Assembly Description

**Table 39. Assembly Description**

| | | |
|---|---|---|
| **Package** | Type | E-Pad LQFP-128 |
| | Dimension (L× W) | 14×14mm |
| | Thickness | 1.4mm |
| **PCB** | PCB Dimension (L×W) | 87×80mm |
| | PCB Thickness | 1.6mm |
| | Number of Cu Layer-PCB | 4-Layer:<br>- 1st layer (1oz): 20% coverage of Cu<br>- 2nd layer (1oz): 80% coverage of Cu<br>- 3rd layer (1oz): 80% coverage of Cu<br>- 4th layer (1oz): 75% coverage of Cu |

## 15.2. Material Properties

**Table 40. Material Properties**

| Item | | Material | Thermal Conductivity K (W/m-k) |
|---|---|---|---|
| Package | Die | Si | 147 |
| | Silver Paste | 1033BF | 2.5 |
| | Lead Frame | CDA7025 | 168 |
| | Mold Compound | 7372 | 0.9 |
| PCB | | Cu | 400 |
| | | FR4 | 0.2 |



## 15.3. Simulation Conditions

**Table 41. Simulation Conditions**

| | |
|---|---|
| **Input Power** | 1.6W |
| **Test Board (PCB)** | 4L (2S2P) |
| **Control Condition** | Air Flow = 0, 1, 2 m/s |

## 15.4. Thermal Performance of LQFP-128 on PCB Under Still Air Convection

**Table 42. Thermal Performance of LQFP-128 on PCB Under Still Air Convection**

| | $\theta_{JA}$ | $\theta_{JB}$ | $\theta_{JC}$ | $\Psi_{JB}$ |
|---|---|---|---|---|
| 4L PCB | 20.5 | 14.3 | 5.8 | 14.2 |

*Note:*
*θJA: Junction to ambient thermal resistance*
*θJB: Junction to board thermal resistance*
*θJC: Junction to case thermal resistance*
*ΨJB: Junction to bottom surface center of PCB thermal characterization*

## 15.5. Thermal Performance of LQFP-128 on PCB Under Forced Convection

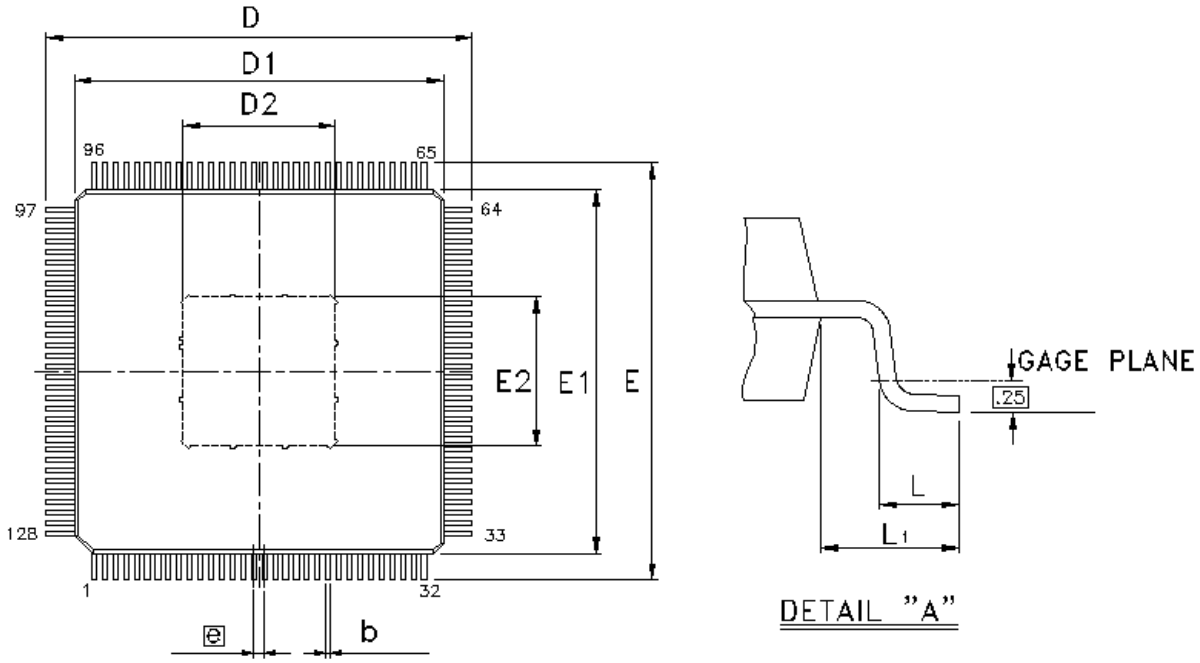
**Table 43. Thermal Performance of LQFP-128 on PCB Under Forced Convection**

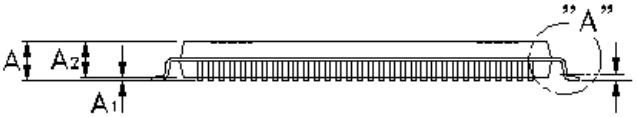
| | Air Flow (m/s) | 0 | 1 | 2 |
|---|---|---|---|---|
| 4L PCB | $\theta_{JA}$ | 20.5 | 18.6 | 18.1 |
| | $\Psi_{JB}$ | 14.2 | 14.1 | 14 |

*Note:*
*θJA: Junction to ambient thermal resistance*
*ΨJB: Junction to bottom surface center of PCB thermal characterization*

# 16. Mechanical Dimensions

*Thermal Enhance Low Profile Plastic Quad Flat Package 128 Leads 14x14mm$^2$ Outline*




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| $A_1$ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.09 |
| D/E | | 16.00 | | | 0.630 | |
| $D_1/E_1$ | | 14.00 | | | 0.551 | |
| $D_2/E_2$ | 7.49 | 8.00 | 8.50 | 0.295 | 0.315 | 0.335 |
| e | | 0.40 | | | 0.016 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MS-026.

# 17. Ordering Information

Table 44. Ordering Information

| Part Number | Package | Status |
|---|---|---|
| RTL9601-CG | Thermal Enhance Low Profile Plastic Quad Flat Package 128 Leads 'Green' Package | - |

*Note: See 6.2, page 8 for package identification information.*

## *17.1. Package Marking*

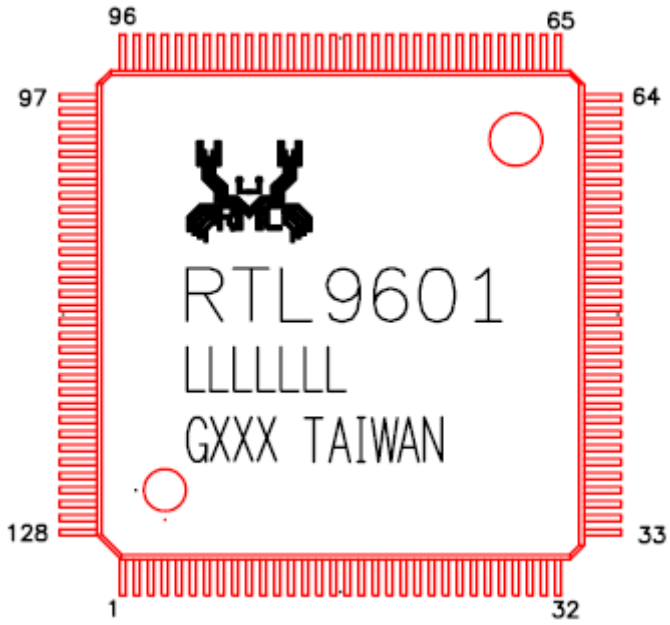



Figure 26. Package Marking Information

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