RTL9600
SINGLE-CHIP PON

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GPIO
Application Note
(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211 Fax: +886-3-577-6047
www.realtek.com

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REVISION HISTORY

Revision	Release Date	Summary
1.0.0	2013/06/21	First Release

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1. Overview

This application note introduces how to control RTL9600 GPIO function. RTL9600 provide GPIO function. Some MISC function share the same I/O pins with GPIO, such as LED, EJTAG, UART, NAND flash, I2C, MDIO, RGMII, VoIP … This Application will also introduce all I/O pins for each function.

2. GPIO PINs

System provides 52 GPIO pins. Here list all GPIO pins.

Table 1. GPIO Pins

Pin Name	Pin No.	Type	Description
GPIO0	57	I/O_{PD}	General Purpose Input/Output Interfaces IO0.
GPIO6	58	I/O	General Purpose Input/Output Interfaces IO6.
GPIO7	59	I/O_{PU}	General Purpose Input/Output Interfaces IO7.
GPIO8	61	I/O_{PU}	General Purpose Input/Output Interfaces IO8.
GPIO9	62	I/O	General Purpose Input/Output Interfaces IO9.
GPIO10	63	I/O_{PU}	General Purpose Input/Output Interfaces IO10.
GPIO11	65	I/O	General Purpose Input/Output Interfaces IO11.
GPIO15	66	I/O	General Purpose Input/Output Interfaces IO15.
GPIO16	67	I/O	General Purpose Input/Output Interfaces IO16.
GPIO17	68	I/O	General Purpose Input/Output Interfaces IO17.
GPIO18	69	I/O	General Purpose Input/Output Interfaces IO18.
GPIO19	70	I/O	General Purpose Input/Output Interfaces IO19.
GPIO20	71	I/O	General Purpose Input/Output Interfaces IO20.
GPIO1	73	I/O	General Purpose Input/Output Interfaces IO1.
GPIO31	74	I/O	General Purpose Input/Output Interfaces IO31.
GPO27	75	I/O_{PU}	General Purpose Output Interfaces O27.
GPO29	76	I/O_{PU}	General Purpose Output Interfaces O29.
GPIO28	77	I/O	General Purpose Input/Output Interfaces IO28.
GPO25	78	I/O_{PU}	General Purpose Output Interfaces O25.
GPO26	79	I/O_{PU}	General Purpose Output Interfaces O26.
GPO33	80	I/O_{PU}	General Purpose Output Interfaces O33.
GPIO32	81	I/O	General Purpose Input/Output Interfaces IO32.
GPIO30	82	I/O	General Purpose Input/Output Interfaces IO30.
GPIO21	83	I/O_{PU}	General Purpose Input/Output Interfaces IO21.
GPIO22	84	I/O	General Purpose Input/Output Interfaces IO22.
GPIO37	116	I/O	General Purpose Input/Output Interfaces IO37.
GPIO38	117	I/O	General Purpose Input/Output Interfaces IO38.
GPIO34	118	I/O	General Purpose Input/Output Interfaces IO34.
GPIO35	119	I/O	General Purpose Input/Output Interfaces IO35.
GPIO36	120	I/O	General Purpose Input/Output Interfaces IO36.
GPIO41	193	I/O	General Purpose Input/Output Interfaces IO41.

Pin Name	Pin No.	Type	Description
GPIO42	194	I/O	General Purpose Input/Output Interfaces IO42.
GPIO43	195	I/O	General Purpose Input/Output Interfaces IO43.
GPIO44	196	I/O	General Purpose Input/Output Interfaces IO44.
GPO50	203	I/O_{PU}	General Purpose Output Interfaces O50.
GPO51	204	I/O_{PU}	General Purpose Output Interfaces O51.
GPO53	207	I/O_{PU}	General Purpose Output Interfaces O53.
GPIO54	208	I/O	General Purpose Input/Output Interfaces IO54.
GPO58	209	I/O_{PU}	General Purpose Output Interfaces O58.
GPIO59	210	I/O_{PU}	General Purpose Input/Output Interfaces IO59.
GPO60	211	I/O_{PU}	General Purpose Output Interfaces O60.
GPIO61	212	I/O_{PU}	General Purpose Input/Output Interfaces IO61.
GPIO12	213	I/O_{PU}	General Purpose Input/Output Interfaces IO12.
GPO13	214	I/O_{PU}	General Purpose Output Interfaces O13.
GPIO23	215	I/O_{PU}	General Purpose Input/Output Interfaces IO23.
GPO24	216	I/O_{PU}	General Purpose Output Interfaces O24.
GPIO45	3	I/O_{PU}	General Purpose Input/Output Interfaces IO45.
GPO46	4	I/O_{PU}	General Purpose Output Interfaces O46.
GPIO47	5	I/O_{PU}	General Purpose Input/Output Interfaces IO47.
GPO48	6	I/O_{PU}	General Purpose Output Interfaces O48.
GPIO49	7	I/O_{PU}	General Purpose Input/Output Interfaces IO49.
GPO52	8	I/O_{PU}	General Purpose Output Interfaces O52.

3. Shared I/O pin Functions

Here list functions which share the I/O pin with GPIO function. GPIO and these functions can not be used simultaneously. Here list the register how to enable/disable these functions.

Table 2. LED IO Enable Register

REGISTER ADDRESS : 0xBB023014

Register	Description	Bit position
SERI_LED_EN	enable serial LED 0b0: disable serial LED IO 0b1: enable serial LED IO	17
LEDn_EN (n=0~16)	enable LEDn 0b0: disable LEDn IO 0b1: enable LEDn IO	0~16

Table 3. MISC IO Enable Register

REGISTER ADDRESS : 0xBB023018

Register	Description	Bit position
UART1_TX_EN	0b0: disable 0b1: enable	26
EXT_INTRPT_EN	0b0: disable 0b1: enable	21
OE_MODULE_TX_SD_EN	For PON OE module TX_SD input	19

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	0b0: disable 0b1: enable	
VOIP_SLIC_PCM_EN	0b0: disable 0b1: enable	18
VOIP_SLIC_SPI_EN	0b0: disable 0b1: enable	17
VOIP_SLIC_ZSI_EN	0b0: disable 0b1: enable	16
VOIP_SLIC_ISI_EN	0b0: disable 0b1: enable	15
I2C1_EN	0b0: disable 0b1: enable	14
I2C0_EN	0b0: disable 0b1: enable	13
INTRPT1_EN	0b0: disable 0b1: enable	12
INTRPT2_EN	0b0: disable 0b1: enable	11
MDX_M_EN	For mdc/mdio master 0b0: disable 0b1: enable	10:9
UART0_TX_EN	0b0: disable 0b1: enable	5
UART1_RX_EN	0b0: disable 0b1: enable	4
UART0_RX_EN	0b0: disable 0b1: enable	3

Table 4. EJTAG IO Enable Register

REGISTER ADDRESS : 0xBB000194

Register	Description	Bit position
DIS_JTAG	Enable / Disable JTAG interface 0: Enable JTAG 1: Disable JTAG	9

Table 5. RGMII IO Enable Register

REGISTER ADDRESS : 0xBB00014C

Register	Description	Bit position
MODE_EXT	0000:Disable 0001:EXT MAC with RGMII 0010:EXT MAC with MII MAC mode 0011:EXT MAC with MII PHY mode 0100:EXT MAC with TMII MAC mode 0101:EXT MAC with TMII PHY mode 0110:Disable (same as 0000) 0111:EXT MAC with RMII MAC mode 1000:EXT MAC with RMII PHY mode	3:0

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3.1. Strap PIN

The pin name which prefix is “GPO” are strap pins. The I/O pin using as trapping pin would only be using as “output PIN”.

3.2. Parallel LED

Parallel LED function may occupy some GPIO pins. Here list parallel led occupied pins.

Table 6. Parallel LED Pins

Pin Name	Description
LED0/ GPO52/ UTXD0	LED0 Output Signal. LED indicates information is defined by register.
LED1/ GPIO49/ URXD0	LED1 Output Signal. LED indicates information is defined by register.
LED2/ GPO48/ JTAG_nRST	LED2 Output Signal. LED2 indicates information is defined by register.
LED3/ GPIO47	LED3 Output Signal. LED3 indicates information is defined by register.
LED4/ GPO46/ JTAG_CK	LED4 Output Signal. LED4 indicates information is defined by register.
LED5/ GPIO45	LED5 Output Signal. LED5 indicates information is defined by register.
LED6/ GPO24/ URXD1/ DDR_TYPE_ FREQ[0]	LED6 Output Signal. LED6 indicates information is defined by register.
LED7/ GPIO23/ INT1	LED7 Output Signal. LED7 indicates information is defined by register.
LED8/ GPO13/ UTXD1/ BTUP_TYP	LED8 Output Signal. LED8 indicates information is defined by register.
LED9/ GPIO12/ INT0/ JTAG_TDI	LED9 Output Signal. LED9 indicates information is defined by register.
LED10/ GPIO61/ SDA1/ MDIO	LED Output Signal. LED indicates information is defined by register.

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Pin Name	Description
LED11/ GPO60/ SCK1/ MDC	LED9 Output Signal. LED9 indicates information is defined by register.
LED12/ GPIO59/ SLED_DA/ JTAG_TMS	LED12 Output Signal. LED12 indicates information is defined by register.
LED13/ GPO58/ SLED_CK/ JTAG_TDO/ DIS_JTAG	LED13 Output Signal. LED13 indicates information is defined by register.
LED15	LED15 Output Signal. LED15 indicates information is defined by register.
LED16	LED16 Output Signal. LED16 indicates information is defined by register.

3.3. Serial LED

Serial LED function may occupy some GPIO pins. Here list serial led occupied pins.

Table 7. Serial LED Pins

Pin Name	Description
SLED_CK/ GPO58/LED13/ JTAG_TDO/ DIS_JTAG	Serial LED Output Signal Clock.
SLED_DA/ GPIO59/ LED12/ JTAG_TMS	Serial LED Output Signal Data.

3.4. NAND Flash

The NAND flash I/O is decided by trapping. When NAND enabled some GPIO pins will be occupied by NAND flash. Here list NAND flash occupied pins.

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Table 8. NAND SPI Flash Control Pins

Pin Name	Description
nMCS/ SPIF_nCS/ NAFC_RC[1]	CHIP Select *The nMCS input is the device selection control. When the device is in the Busy state, CE high is ignored, and the device does not return to standby mode in program or erase operation.*
nFWE/ SPIF_CLK/ SPIF4BEN	WRITE ENABLE *The nFWE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse.*
ALE/ GPO50/ NAF_AC[0]	ADDRESS LATCH ENABLE *The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.*
CLE/ GPO51/ NAF_AC[1]	COMMAND LATCH ENABLE *The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.*
nFRE/ GPO53/ NAFC_RC[0]	READ ENABLE *The nFRE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one.*
RDY_BSY/ GPIO54	READY/BUSY OUTPUT The RDY_BSY output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. *R/B can simply wired-or together.*
SIO7/GPIO41 SIO6/GPIO42 SIO5/GPIO43 SIO4/GPIO44 SIO3/SPIF_D2 SIO2/SPIF_D1 SIO1/SPIF_D0 SIO0/SPIF_D3	DATA INPUTS/OUTPUTS *The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.*

3.5. UART

UART function may occupy some GPIO pins. Here list UART occupied pins.

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Table 9. UART Pins

Pin Name	Description
UTXD0/ GPO52/ LED0/ RESERVED	Data Transmit Serial Output of UART0.
URXD0/ GPIO49/ LED1	Data Receive Serial Input of UART0. Note: This pin must be pulled low via an external 4.7k ohm when the UART interface enabled.
UTXD1/ GPO13/ LED8/ BTUP_TYP	Data Transmit Serial Output of UART1.
URXD1/ GPO24/ LED6/ DDR_TYPE_FREQ[0]	Data Receive Serial Input of UART1. Note: This pin must be pulled low via an external 4.7k ohm when the UART interface enabled.

3.6. JTAG

JTAG function may occupy some GPIO pins. Here list JTAG occupied pins.

Table 10. JTAG Pins

Pin Name	Description
JTAG_CK/ GPO46/ LED4	JTAG Test Clock.
JTAG_TMS/ GPIO59/ LED12/ SLED_DA	JTAG Test Mode Select.
JTAG_TDO/ GPO58/ LED13/ SLED_CK/ DIS_JTAG	JTAG Test Data Output.
JTAG_TDI/ GPIO12/ LED9/ INT0	JTAG Test Data In.
JTAG_nRST/ GPO48/ LED2	JTAG Test Reset.

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3.7. VoIP

Table 11. VOIP Shared I/O Pin Mapping

GPIO	SPI+PCM	ZSI	ISI
GPIO31	SLICSPI_nCS1	-	-
GPO27	SLICPCM_CLK	ZPAPCK	-
GPO29	SLICSPI_MOSI	Z0MOSI	MSIF0_PSDO
GPIO28	SLICSPI_MISO	Z0MISO	MSIF0_PSDI
GPO25	SLICSPI_CLK	-	MSI_CLK24M
GPO26	SLICPCM_FS	Z0SYNC	-
GPO33	SLICPCM_TXD	Z1MOSI	MSIF1_PSDO
GPIO32	SLICPCM_RXD	Z1MISO	MSIF1_PSDI
GPIO30	SLICSPI_nCS0	Z1SYNC	-

3.8. MDC/MDIO

Table 12. MDIO I/O Pins

Pin Name	Description
GPO60	MDC
GPIO61	MDIO

3.9. PON OE Input

Table 13. PON OE Module Input I/O Pins

Pin Name	Description
GPIO35	PON OE module TX_SD

3.10. Interrupt PIN

Table 14. Interrupt I/O Pins

Pin Name	Description
GPIO12	Interrupt 0 input pin
GPIO23	Interrupt 1 input pin

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3.11. General Purpose Interfaces

The RTL9607 supports multi-function General Purpose Interfaces that can be configured as extra interfaces of Extension or other Digital I/O interfaces. The RTL9607 supports one extension interface for connecting with an external PHY, or MAC in specific applications. The extension interface support RGMII, (T)MII MAC mode, (T)MII PHY mode, RMII clock in mode, or RMII clock out mode via register configuration. The General Purpose Interface also could be configured to General Purpose Input/Output Interfaces when the GMII interface is disabled.

Table 15. General Purpose Interfaces Pin Definitions

GPIO	RGMII Mode	**(T)**MII MAC Mode	**(T)**MII PHY Mode	RMII Clock In mode	RMII Clock Out mode
GPIO11	RG_TXCLK (Output)	MM_TXCLK (Input)	MP_RXCLK (Output)	RMM_CLK (Input)	RMM_CLK (Output)
GPIO10	RG_TXCTL (Output)	MM_TXEN (Output)	MP_RXDV (Output)	RMM_TXEN (Output)	RMM_TXEN (Output)
GPIO6 GPIO7	RG_TXD [3:2] (Output)	MM_TXD [3:2] (Output)	MP_RXD [3:2] (Output)	-	-
GPIO8 GPIO9	RG_TXD [1:0] (Output)	MM_TXD [1:0] (Output)	MP_RXD [1:0] (Output)	RMM_TXD[1:0] (Output)	RMM_TXD[1:0] (Output)
GPIO15	RG_RXCLK (Input)	MM_RXCLK (Input)	MP_TXCLK (Input)	-	-
GPIO16	RG_RXCTL (Input)	MM_RXDV (Input)	MP_TXEN (Input)	RMM_CRS_DV (Input)	RMM_CRS_DV (Input)
GPIO20 GPIO19	RG_RXD [3:2] (Input)	MM_RXD [3:2] (Input)	MP_TXD [3:2] (Input)	-	-
GPIO18 GPIO17	RG_RXD [1:0] (Input)	MM_RXD [1:0] (Input)	MP_TXD [1:0] (Input)	RMM_RXD[1:0] (Input)	RMM_RXD[1:0] (Input)
GPIO0	-	MP_CRS	-	-	-

4. API

Realtek API provides a series of interface to let users setup the GPIO without writing register and table directly. This section will discuss these APIs.

4.1. Set GPIO Mode

The ***rtk_gpio_mode_set*** API will set GPIO mode. The GPIO mode would be GPIO_INPUT/ GPIO_OUTPUT.

Example:

```
/*
   Set GPIO10 to output mode
*/
int32 ret ;
if((ret= rtk_gpio_mode_set (10,GPIO_OUTPUT)) != RT_ERR_OK)
{
    return ret;
}
```

4.2. Enable GPIO PIN

The ***rtk _gpio_state_set*** API would enable GPIO function for given GPIO id.

Example:

```
/* Enable GPIO10 */
int32 ret;

if((ret= rtk _gpio_state_set (10,ENABLED)) != RT_ERR_OK)
    return ret;
```

4.3. Get GPIO Input Value

The ***rtk_gpio_databit_get*** API would get the gpio pin input value.

Example:

```
/*
  get input value from GPIO pin 10
*/

unit32 data;
int32 ret;

if((ret= rtk_gpio_databit_get (10, &data)) != RT_ERR_OK)
    return ret;
```

4.4. Get GPIO Output Value

The ***rtk_gpio_databit_set*** API would set the gpio pin output value.

Example:

```
/*
  Set GPIO pin 10 output value to 1
*/

unit32 data;
int32 ret;

Data =1;
if((ret= rtk_gpio_databit_set (10, data)) != RT_ERR_OK)
    return ret;
```

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Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com