RTL86907-CG

IEEE 10/100/1000M ETHERNET / PON ROUTER NETWORK PROCESSOR

PRELIMINARY DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek Ethernet/PON network router processor.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
Pre-0.9	2012/11/06	First release.

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1. General Description

The RTL86907 is an integrated System-on-a-Chip (SoC) Application Specific Integrated Circuit (ASIC) with dual core CPU that implements a L2 switch functions and Layer 3/4 hardware NAT/NAPT. The RTL86907 integrated an Realtek processor and the clock rate up to 700MHz. An VoIP processor is embedded and the clock rate 550MHz. A standard 5-signal P1149.1 compliant EJTAG test interface is supported for CPU testing and software development.

Via table configuration and look-up, the RTL86907 can perform hard-wired network traffic forwarding. The CPU may be used to handle upper layer functions, such as DHCP, HTTP, and some other protocols, and to operate with a hard-wired forwarding engine.

The RTL86907 integrated four Gigabit Ethernet physical layer transceivers for 10Base-T, 100Base-TX, and 1000Base-TX. One SerDes interface type to work with an external PON transceiver. One external MAC interface that could be an RGMII/RMII/TMII/MII interface type to work with an external MAC or PHY transceiver.

The RTL86907 supports flexible IEEE 802.3x full-duplex flow control and optional half-duplex backpressure control. For full-duplex, standard IEEE 803.3x flow control will enable pause ability only when both sides of UTP have auto-negotiation ability and have enabled pause ability. The RTL86907 also provides optional forced mode IEEE 802.3x full-duplex flow control. Based on optimized packet memory management, the RTL86907 is capable of Head-Of-Line blocking prevention.

Due to its powerful protocol parser, the RTL86907 can recognize and hard-wire-forward VLAN-tagged, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP and IGMP packets. Layer 2, 3, and 4 information is stored in look-up tables. For VLAN and PPPoE protocols, the RTL86907 can automatically encapsulate and decapsulate VLAN tagged frames and PPPoE headers.

The RTL86907 supports port-based, protocol-based, and tagged VLANs. Up to four thousand VLAN groups can be assigned. VLAN tags are inserted or removed based on the VLAN table configuration. The spanning tree protocol is supported and the states are divided into four types: Disabled, Blocking/Listening, Learning, and Forwarding.

For peripheral interfaces, two 16550-compatible UARTs are supported.

The RTL86907 requires only a single 25MHz crystal clock input for the system PLL. The RTL86907 also has six hardware timers and one watchdog timer to provide accurate timing and watchdog functionality. For extension and flexibility, the RTL86907 has up to 36 GPIO pins.

The RTL86907 is provided in a Low Profile Plastic Quad Flat Package, 216-Lead (LQFP216-E-PAD) package. It requires only a 3.3V and 1.0V external power supply.

2. Features

- **CPU**
  - Realtek 700MHz CPU
    - I-Cache: 64KB, 4-way set
    - D-Cache: 32KB, 4-way set
    - Virtually indexed, physically tagged
    - PREF instruction
  - Misc.
    - Power-down mode (Sleep instruction)
    - EJTAG support
    - Internal BIST
    - Internal real-time timer interrupts (Count/Compare registers)
    - 2 HW instruction breakpoint/1 HW data breakpoint.

- **DSP**
  - Realtek VoIP processor 550MHz DSP
    - I-Cache: 32KB, 2-way set
    - D-Cache: 16KB
    - Virtually indexed, physically tagged
    - PREF instruction
  - Misc.
    - Power-down mode (Sleep instruction)
    - EJTAG support
    - Internal BIST
    - 2 HW instruction break point/1 HW data break point.

- CPU Interface (NIC)
  - The NIC DMA support multiple-descriptor-ring architecture for QoS applications

- Memory Interfaces
  - Serial Flash (SPI Type)
    - Supports dual I/O channels for SPI Flash application
    - Each Flash bank could be configured as 256K/512K/1M/2M/4M/8M/16M/32M Bytes
    - Boot up from SPI flash is supported
  - NAND Flash
    - 8-bit parallel data width
    - Write-protection function
    - PIO and DMA data read/write operation
    - Configurable flash access timing
    - Boot up from NAND flash is supported
  - DDR1 SDRAM
    - Supports one DDR1 SDRAM bank that can be configured as 16M/32M/64M/128M bytes
    - 16-bit DDR1 SDRAM data bus supported. System totally supports up to 128Mbyte DDR1 SDRAM memory space
  - DDR2 SDRAM
    - Supports one DDR2 SDRAM bank that can be configured as 32M/64M/128M/256M bytes
    - 16-bit DDR2 SDRAM data bus supported. System totally supports up to 128Mbyte DDR2 SDRAM memory space
  - DDR3 SDRAM
    - Supports one DDR3 SDRAM bank that can be configured as 128M/256M bytes
    - 16-bit DDR3 SDRAM data bus supported. System totally supports up to 128Mbyte DDR3 SDRAM memory space

- Peripheral
  - Two USB 2.0 interfaces
  - Two PCI Express interfaces
  - Two 16550-compatible UARTs

- GPON
  - Compliant with ITU G.984.x
  - Bandwidth US: 1.24416G / DS: 2.48832G
  - Support 32 TCONT, 128 GEM
  - Support AES, key switching
  - Support upstream and downstream FEC
  - Support DBRu
  - HW dying gasp
- EPON
  - Compliance with IEEE 802.3 EPON MAC standard
  - Bandwidth US: 1.25G / DS: 1.25G
  - Support DS/US FEC
  - Triple-churning decryption of DS traffic
  - US scheduling
    - Per Queue rate control setting (CIR/PIR)
      - Support Strict Priority and Weight Fare Queue (WFQ) mode
  - Counter–Support RFC4837
  - HW dying gasp
- Layer 3/4 hardware NAT/NAPT
  - 8 Network interface tables
  - 8 External IP tables
  - 8 L3 Routing Tables
  - 512 ARP Tables
  - 16 Next Hop Tables
  - 8 PPPoE Tables
  - 2K NAPT Tables
  - 1K NAPTR Tables
- L2 Capabilities
  - Six Gigabit Ethernet MACs switch with four IEEE 802.3 10/100/1000Mbps physical layer transceivers
  - Non-blocking wire-speed reception and transmission and non-head-of-line-blocking/forwarding
  - Internal 2048 entry 4-way hash L2 look-up table
  - Supports source and destination MAC address filtering
- SupportsACL Rules
  - Supports MAC, IP, TCP/UDP, ICMP, IGMP, IPv6 Format
  - Supports mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, SVLAN assignment, interrupt, LLID, SID assignment and Extension forward portmask.
  - Supports 4 templates of user defined ACL rule format
  - Supports VID/IP/L4/Packet Length Port range check
  - Up to 16 user defined field selectors
- Support 512 PON Classification Rules
  - Supports SVLAN tagging/removing
  - Supports CVLAN tagging/removing
  - Supports indirect LLID/GEMPort assignment
  - Supports forced UNI ports forwarding and queueing priority assignment
  - VLAN translation/aggregation functions
- Supports GPON 128 GEM Port within 32 T-CONT
- Supports IEEE 802.1Q VLAN
  - Supports 4K VLAN and 32 Extra Enhanced VLAN

- Supports Untag definition in each VLAN
- Supports VLAN policing
- Supports Port Based and Port-and-Protocol-based VLAN

- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64/4096 SVLAN
  - Supports 8 L2/IPv4 Multicast mapping to SVLAN
  - Support 128 CLVAN to SVLAN
  - Support MAC-based customer CVID decision for 1:N VLAN

- Supports IVL, SVL and IVL/SVL
  - Supports 2K MAC Address Table
  - 4-way hash
  - Up to 16 L2/L3 Filtering Database as 16 MST instance

- Supports Spanning Tree
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree, up to 16 spanning tree

- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure

- Supports IEEE 802.1X access control protocol

- Supports Quality of Service (QoS)
  - Traffic classification based on IEEE 802.1P/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, SVLAN based priority and L4 NAT priority
  - 8 priority queues per port
  - Supports per port Ingress Bandwidth Control and Egress Bandwidth Control
  - Per queue flow control
  - Min-Max Scheduling
    - Strict Priority and Weighted Fair Queue (WFQ) to provide minimum bandwidth
    - One leaky bucket (APR) to constraint average rate of each queue

- Supports 32 shared meter with 8kpbs granularity

- Supports MIB Counters
  - MIB-II (RFC 1213)
  - Ethernet-like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
  - ITU G.984.4 OMCI ME MIBs
  - User defined Logging Counter

- Supports 8 Enhanced Filtering Database for Stacking VLAN and Port Isolation usage

- Port mirror with multicast monitored source ports to monitorring destination port.

- Supports IEEE 802.3ad Link aggregation port group, up to 4Gpbs bandwidth

- Support OAM and EEELLDP

- Support Loop Detection

- IGMP/MLD snooping trap function

- Green Ethernet Auto Fall-back

- Ethernet AV support with 802.1Qav and 802.1AS/1588v2 timing synchronization

- Storm Fileting Control for broadcast, multicast, unknown unicast, ARP, DHCP and ICMP with 8Kpbs granularity rate.
- DOS attacks prevention
- LQFP216-E-PAD package
- Supports Green Ethernet
  - Cable length power saving
  - Power down power saving
- Supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation and 10Base-T in full/half duplex mode
- Other Add-on-Value Features
  - Supports Link Down Power Saving in Ethernet PHYceivers
  - Supports six hardware timers and one watchdog timer
  - Per-port configurable auto-crossover function
  - Built-in regulator controller
    - DDR1 SDRAM to transform 3.3V to 2.5V via an external BJT transistor
    - DDR2 SDRAM to transform 3.3V to 1.8V via an external BJT transistor
    - DDR3 SDRAM to transform 3.3V to 1.5V via an external BJT transistor
  - Single 25MHz crystal clock input

3. System Applications

- 4+1-Port 1000Base-T / PON router with with dual VOIP channels, dual PCIEs, and dual USBs.

4. Application Examples

4.1. 4+1-Port 1000Base-T / PON router with dual VOIP channels, dual PCIEs, and dual USBs.

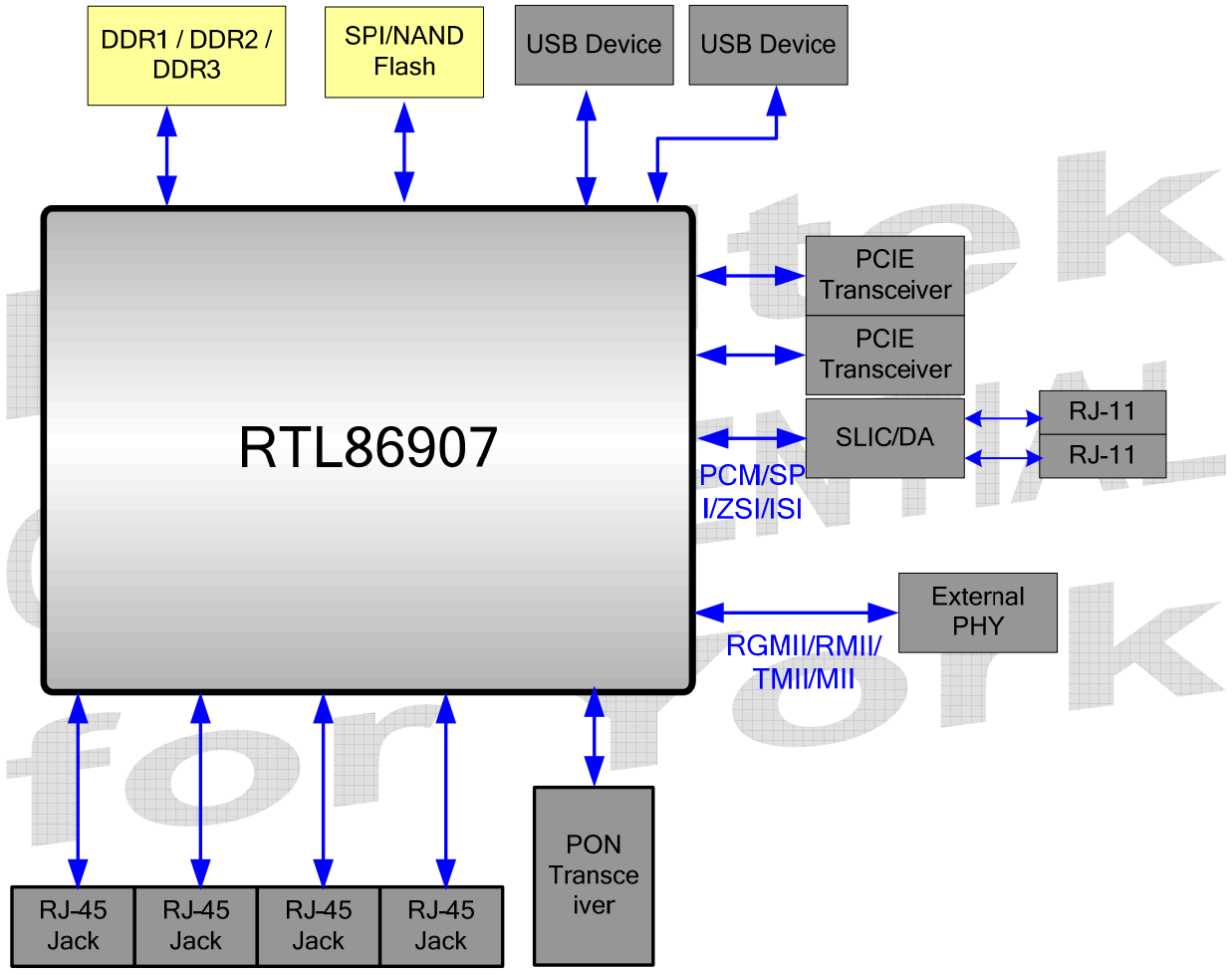


Figure 1. 4+1-Port 1000Base-T / PON router with dual VOIP channels, dual PCIEs, and dual USBs.

5. Block Diagram

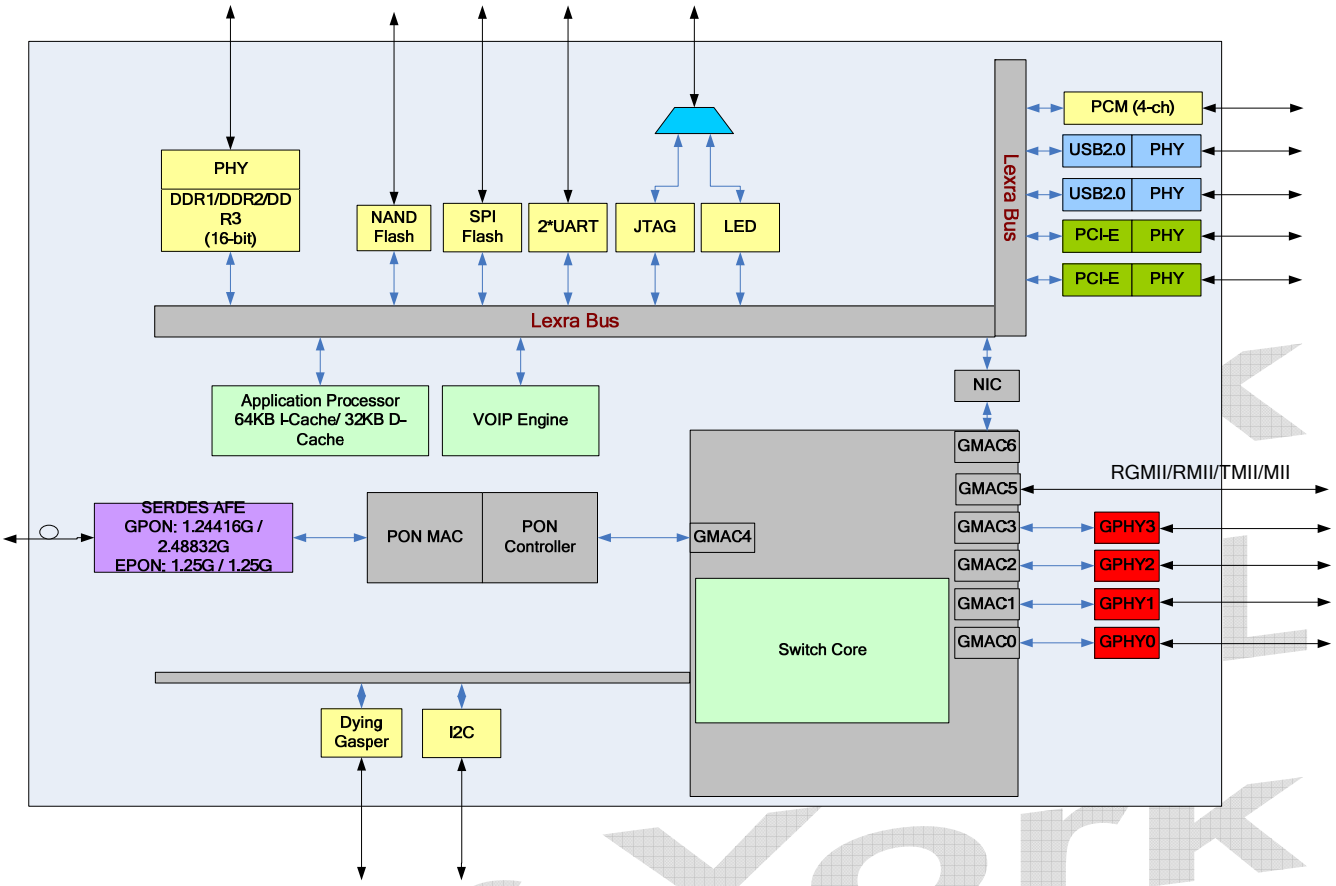


Figure 2. Block Diagram

6. Pin Assignments

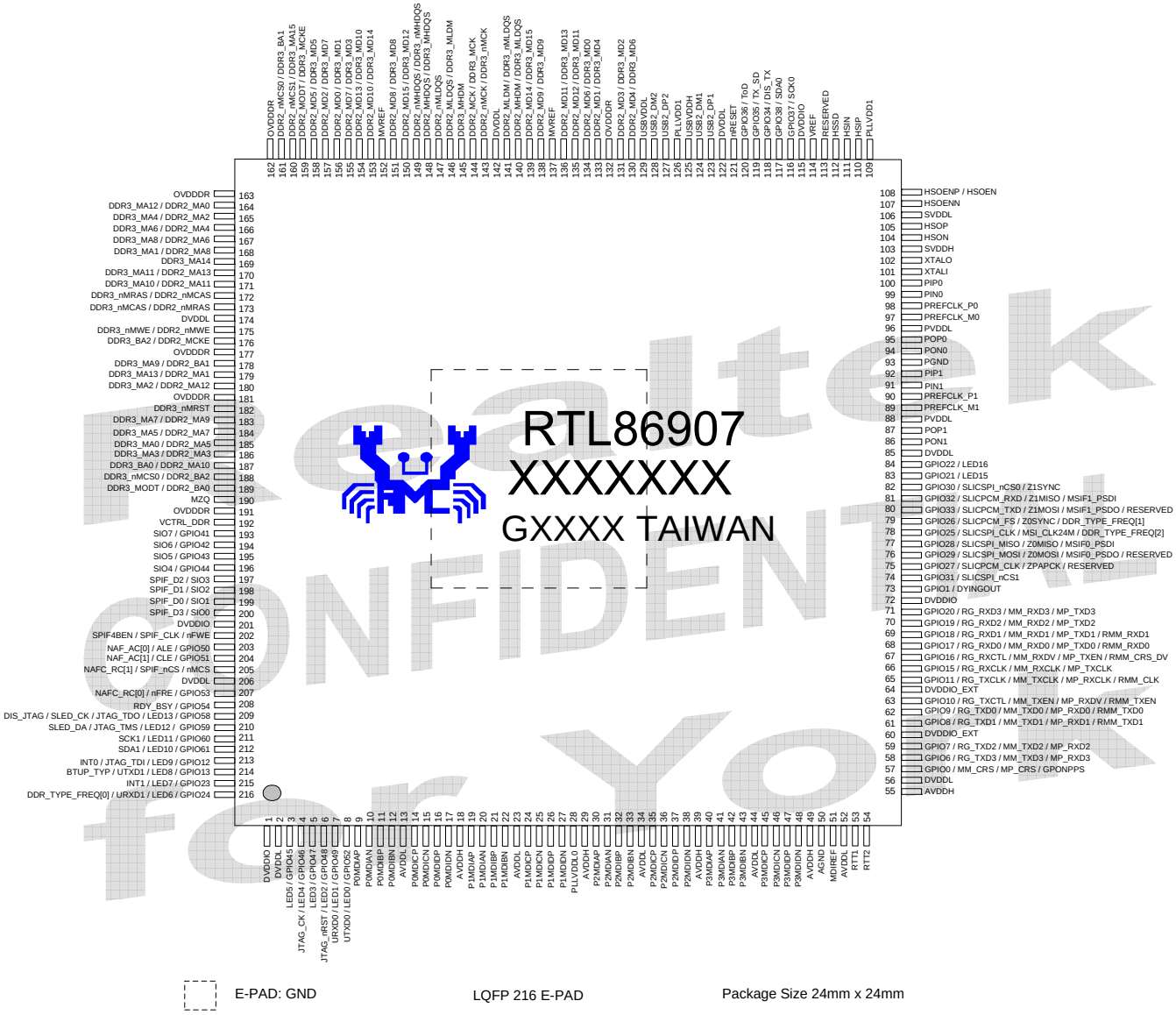


Figure 3. Pin Assignments

6.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 3).

6.2. Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I/O_{PU}: Input Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

I/O_{PD}: Input Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

I_S: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

I/O_{PU}: Output Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

I/O_{PD}: Output Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type
DVDDIO	1	P
DVDDL	2	P
GPIO45 / LED5	3	I/O_{PU}
GPIO46 / LED4 / JTAG_CK	4	I/O_{PU}
GPIO47 / LED3	5	I/O_{PU}
GPIO48 / LED2 / JTAG_nRST	6	I/O_{PU}
GPIO49 / LED1 / URXD0	7	I/O_{PU}
GPIO52 / LED0 / UTXD0	8	I/O_{PU}
P0MDIAP	9	AI/O
P0MDIAN	10	AI/O
P0MDIBP	11	AI/O
P0MDIBN	12	AI/O
AVDDL	13	AP
P0MDICP	14	AI/O
P0MDICN	15	AI/O
P0MDIDP	16	AI/O
P0MDIDN	17	AI/O
AVDDH	18	P
P1MDIAP	19	AI/O
P1MDIAN	20	AI/O
P1MDIBP	21	AI/O
P1MDIBN	22	AI/O
AVDDL	23	AP

Name	Pin No.	Type
P1MDICP	24	AI/O
P1MDICN	25	AI/O
P1MDIDP	26	AI/O
P1MDIDN	27	AI/O
PLLVDDL0	28	AP
AVDDH	29	AP
P2MDIAP	30	AI/O
P2MDIAN	31	AI/O
P2MDIBP	32	AI/O
P2MDIBN	33	AI/O
AVDDL	34	AP
P2MDICP	35	AI/O
P2MDICN	36	AI/O
P2MDIDP	37	AI/O
P2MDIDN	38	AI/O
AVDDH	39	AP
P3MDIAP	40	AI/O
P3MDIAN	41	AI/O
P3MDIBP	42	AI/O
P3MDIBN	43	AI/O
AVDDL	44	AP
P3MDICP	45	AI/O
P3MDICN	46	AI/O

Name	Pin No.	Type
P3MDIDP	47	AI/O
P3MDIDN	48	AI/O
AVDDH	49	AP
AGND	50	AG
MDIREF	51	AO
AVDDL	52	AP
RTT1	53	AO
RTT2	54	AO
AVDDH	55	AP
DVDDL	56	P
GPIO0 / MM_CRS / MP_CRS / GPONPPS	57	I/O_{PD}
GPIO6 / RG_TXD3 / MM_TXD3 / MP_RXD3	58	I/O
GPIO7 / RG_TXD2 / MM_TXD2 / MP_RXD2	59	I/O_{PU}
DVDDIO_EXT	60	P
GPIO8 / RG_TXD1 / MM_TXD1 / MP_RXD1 / RMM_TXD1	61	I/O_{PU}
GPIO9 / RG_TXD0 / MM_TXD0 / MP_RXD0 / RMM_TXD0	62	I/O
GPIO10 / RG_TXCTL / MM_TXEN / MP_RXDV / RMM_TXEN	63	I/O_{PU}
DVDDIO_EXT	64	P
GPIO11 / RG_TXCLK / MM_TXCLK / MP_RXCLK / RMM_CLK	65	I/O
GPIO15 / RG_RXCLK / MM_RXCLK / MP_TXCLK	66	I/O
GPIO16 / RG_RXCTL / MM_RXDV / MP_TXEN / RMM_CRS_DV	67	I/O
GPIO17 / RG_RXD0 / MM_RXD0 / MP_TXD0 / RMM_RXD0	68	I/O
GPIO18 / RG_RXD1 / MM_RXD1 / MP_TXD1 / RMM_RXD1	69	I/O
GPIO19 / RG_RXD2 / MM_RXD2 / MP_TXD2	70	I/O
GPIO20 / RG_RXD3 / MM_RXD3 / MP_TXD3	71	I/O
DVDDIO	72	P
GPIO1 / DYINGOUT	73	I/O
GPIO31 / SLICSPI_nCS1	74	I/O

Name	Pin No.	Type
GPIO27 / SLICPCM_CLK / ZPAPCK / RESERVED	75	I/O_{PU}
GPIO29 / SLICSPI_MOSI / Z0MOSI / MSIF0_PSDO / RESERVED	76	I/O_{PU}
GPIO28 / SLICSPI_MISO / Z0MISO / MSIF0_PSDI	77	I/O
GPIO25 / SLICSPI_CLK / MSI_CLK24M / DDR_TYPE_FREQ[2]	78	I/O_{PU}
GPIO26 / SLICPCM_FS / Z0SYNC / DDR_TYPE_FREQ[1]	79	I/O_{PU}
GPIO33 / SLICPCM_TXD / Z1MOSI / MSIF1_PSDO / RESERVED	80	I/O_{PU}
GPIO32 / SLICPCM_RXD / Z1MISO / MSIF1_PSDI	81	I/O
GPIO30 / SLICSPI_nCS0 / Z1SYNC	82	I/O
GPIO21 / LED15	83	I/O_{PU}
GPIO22 / LED16	84	I/O
DVDDL	85	P
PON1	86	AI/O
POP1	87	AI/O
PVDDL	88	AP
PREFCLKM1	89	AI/O
PREFCLKP1	90	AI/O
PIN1	91	AI/O
PIP1	92	AI/O
PGND	93	G
PON0	94	AI/O
POP0	95	AI/O
PVDDL	96	AP
PREFCLKM0	97	AI/O
PREFCLKP0	98	AI/O
PIN0	99	AI/O
PIP0	100	AI/O
XTALI	101	AI
XTALO	102	AO
SVDDH	103	AP
HSON	104	AO
HSOP	105	AO
SVDDL	106	AP
HSOENN	107	AO
HSOENP / HSOEN	108	AO

Name	Pin No.	Type
PLLVDD1	109	AP
HSIP	110	AI
HSIN	111	AI
HSSD	112	I
RESERVED	113	AI
VREF	114	AI
DVDDIO	115	P
GPIO37 / SCK0	116	I/O
GPIO38 / SDA0	117	I/O
GPIO34	118	I/O
GPIO35 / TX_SD	119	I/O
GPIO36 / RESERVED	120	I/O
nRESET	121	I_S
DVDDL	122	P
USB2_DP1	123	AI/O
USB2_DM1	124	AI/O
USBVDDH	125	AP
PLLVDD1	126	AP
USB2_DP2	127	AI/O
USB2_DM2	128	AI/O
USBVDDL	129	AP
DDR2_MD4 / DDR3_MD6	130	I/O
DDR2_MD3 / DDR3_MD2	131	I/O
OVDDDR	132	P
DDR2_MD1 / DDR3_MD4	133	I/O
DDR2_MD6 / DDR3_MD0	134	I/O
DDR2_MD12 / DDR3_MD11	135	I/O
DDR2_MD11 / DDR3_MD13	136	I/O
MVREF1	137	AO
DDR2_MD9 / DDR3_MD9	138	I/O
DDR2_MD14 / DDR3_MD15	139	I/O
DDR2_MHDM / DDR3_MLDQS	140	I/O
DDR2_MLDM / DDR3_nMLDQS	141	I/O
DVDDL	142	P
DDR2_nMCK / DDR3_nMCK	143	O
DDR2_MCK / DDR3_MCK	144	O
DDR3_MHDM	145	I/O
DDR2_MLDQS / DDR3_MLDM	146	I/O
DDR2_nMLDQS	147	I/O
DDR2_MHDQS / DDR3_MHDQS	148	I/O

Name	Pin No.	Type
DDR2_nMHDQS / DDR3_nMHDQS	149	I/O
DDR2_MD15 / /DDR3_MD12	150	I/O
DDR2_MD8 / DDR3_MD8	151	I/O
MVREF0	152	AO
DDR2_MD10 / DDR3_MD14	153	I/O
DDR2_MD13 / DDR3_MD10	154	I/O
DDR2_MD7 / DDR3_MD3	155	I/O
DDR2_MD0 / DDR3_MD1	156	I/O
DDR2_MD2 / DDR3_MD7	157	I/O
DDR2_MD5 / DDR3_MD5	158	I/O
DDR2_MODT / DDR3_MCKE	159	O
DDR2_nMCS1 / DDR3_MA15	160	O
DDR2_nMCS0 / DDR3_BA1	161	O
OVDDDR	162	P
OVDDDR	163	P
DDR2_MA0 / DDR3_MA12	164	O
DDR2_MA2 / DDR3_MA4	165	O
DDR2_MA4 / DDR3_MA6	166	O
DDR2_MA6 / DDR3_MA8	167	O
DDR2_MA8 / DDR3_MA1	168	O
DDR3_MA14	169	O
DDR2_MA13 / DDR3_MA11	170	O
DDR2_MA11 / DDR3_MA10	171	O
DDR2_nMCAS / DDR3_nMRAS	172	O
DDR2_nMRAS / DDR3_nMCAS	173	O
DVDDL	174	P
DDR2_nMWE / DDR3_nMWE	175	O
DDR2_MCKE / DDR3_BA2	176	O
OVDDDR	177	P
DDR2_BA1 / DDR3_MA9	178	O
DDR2_MA1 / DDR3_MA13	179	O
DDR2_MA12 / DDR3_MA2	180	O
OVDDDR	181	P
DDR3_nMRST	182	O
DDR2_MA9 / DDR3_MA7	183	O
DDR2_MA7 / DDR3_MA5	184	O
DDR2_MA5 / DDR3_MA0	185	O
DDR2_MA3 / DDR3_MA3	186	O
DDR2_MA10 / DDR3_BA0	187	O
DDR2_BA2 / DDR3_nMCS0	188	O
DDR2_BA0 / DDR3_MODT	189	O

Name	Pin No.	Type
MZQ	190	AO
OVDDDR	191	P
VCTRL_DDR	192	AO
GPIO41 / SIO7	193	I/O
GPIO42 / SIO6	194	I/O
GPIO43 / SIO5	195	I/O
GPIO44 / SIO4	196	I/O
SPIF_D2	197	I/O
SPIF_D1	198	I/O
SPIF_D0	199	I/O
SPIF_D3	200	I/O
DVDDIO	201	P
nFWE / SPIF_CLK / SPIF4BEN	202	I/O_{PU}
GPIO50 / ALE / NAF_AC[0]	203	I/O_{PU}
GPIO51 / CLE / NAF_AC[1]	204	I/O_{PU}
nMCS / SPIF_nCS / RESERVED	205	I/O

Name	Pin No.	Type
DVDDL	206	P
GPIO53 / nFRE / NAFC_RC([0]	207	I/O_{PU}
GPIO54 / RDY_BSY	208	I/O
GPIO58 / LED13 / SLED_CK/ JTAG_TDO / DIS_JTAG	209	I/O_{PU}
GPIO59 / LED12 / SLED_DA / JTAG_TMS	210	I/O_{PU}
GPIO60 / LED11 / SCK1	211	I/O_{PU}
GPIO61 / LED10 / SDA1	212	I/O_{PU}
GPIO12 / LED9 / INT0 / JTAG_TDI	213	I/O_{PU}
GPIO13 / LED8 / UTXD1 / BTUP_TYP	214	I/O_{PU}
GPIO23 / LED7 / INT1	215	I/O_{PU}
GPIO24 / LED6 / URXD1 / RESERVED	216	I/O_{PU}
GND	EPAD	G

7. Pin Descriptions

7.1. DDR2 (DDR) / DDR3 Shared I/O Pin Mapping

Table 2. DDR2 (DDR) / DDR3 Shared I/O Pin Mapping

Pin No.	DDR / DDR2	DDR3
130	DDR2_MD4	DDR3_MD6
131	DDR2_MD3	DDR3_MD2
133	DDR2_MD1	DDR3_MD4
134	DDR2_MD6	DDR3_MD0
135	DDR2_MD12	DDR3_MD11
136	DDR2_MD11	DDR3_MD13
138	DDR2_MD9	DDR3_MD9
139	DDR2_MD14	DDR3_MD15
140	DDR2_MHDM	DDR3_MLDQS
141	DDR2_MLDM	DDR3_nMLDQS
143	DDR2_nMCK	DDR3_nMCK
144	DDR2_MCK	DDR3_MCK
145	-	DDR3_MHDM
146	DDR2_MLDQS	DDR3_MLDM
147	DDR2_nMLDQS	-
148	DDR2_MHDQS	DDR3_MHDQS
149	DDR2_nMHDQS	DDR3_nMHDQS
150	DDR2_MD15	DDR3_MD12
151	DDR2_MD8	DDR3_MD8
153	DDR2_MD10	DDR3_MD14
154	DDR2_MD13	DDR3_MD10
155	DDR2_MD7	DDR3_MD3
156	DDR2_MD0	DDR3_MD1
157	DDR2_MD2	DDR3_MD7
158	DDR2_MD5	DDR3_MD5
159	DDR2_MODT	DDR3_MCKE
160	DDR2_nMCS1	DDR3_MA15
161	DDR2_nMCS0	DDR3_BA1
164	DDR2_MA0	DDR3_MA12
165	DDR2_MA2	DDR3_MA4
166	DDR2_MA4	DDR3_MA6
167	DDR2_MA6	DDR3_MA8
168	DDR2_MA8	DDR3_MA1
169	-	DDR3_MA14
170	DDR2_MA13	DDR3_MA11
171	DDR2_MA11	DDR3_MA10
172	DDR2_nMCAS	DDR3_nMRAS
173	DDR2_nMRAS	DDR3_nMCAS
175	DDR2_nMWE	DDR3_nMWE
176	DDR2_MCKE	DDR3_BA2
178	DDR2_BA1	DDR3_MA9
179	DDR2_MA1	DDR3_MA13
180	DDR2_MA12	DDR3_MA2
182	-	DDR3_nMRST
183	DDR2_MA9	DDR3_MA7
184	DDR2_MA7	DDR3_MA5

Pin No.	DDR / DDR2	DDR3
185	DDR2_MA5	DDR3_MA0
186	DDR2_MA3	DDR3_MA3
187	DDR2_MA10	DDR3_BA0
188	DDR2_BA2	DDR3_nMCS0
189	DDR2_BA0	DDR3_MODT

Table 3. DDR2 SDRAM Pins

Pin Name	Pin No.	Type	Description
DDR2_MCKE	176	O	DDR2 SDRAM clock enable
DDR2_MCK	144	O	DDR2 SDRAM differential clock signal 0
DDR2_nMCK	143	O	DDR2 SDRAM differential clock signal 1
DDR2_nMCS0	161	O	DDR2 SDRAM chip select 0
DDR2_nMCS1	160	O	DDR2 SDRAM chip select 1
DDR2_MODT	159	O	DDR2 on die termination
DDR2_nMWE	175	O	Write enable
DDR2_nMCAS	172	O	Column address strobe
DDR2_nMRAS	173	O	Row address strobe
DDR2_BA[2:0]	188, 178, 189	O	Bank address
DDR2_MLDM	141	O	Data mask for DQ[7:0]
DDR2_MHDM	140	O	Data mask for DQ[15:8]
DDR2_MLDQS	146	I/O	Data strobe for DQ[7:0]
DDR2_nMLDQS	147	I/O	Data strobe for DQ[7:0]
DDR2_MHDQS	148	I/O	Data strobe for DQ[15:8]
DDR2_nMHDQS	149	I/O	Data strobe for DQ[15:8]
DDR2_MA[13:0]	170, 180, 171, 187, 183, 168, 184, 167, 185, 166, 186, 165, 179, 164	O	Address for DDR2 SDRAM
DDR2_MD[15:0]	150, 139, 154, 135, 136, 153, 138, 151, 155, 134, 158, 130, 131, 157, 133, 156	I/O	Data for DDR2 SDRAM
MZQ	190	AO	Reference Pin for ZQ calibration.

Table 4. DDR3 SDRAM Pins

Pin Name	Pin No.	Type	Description
DDR3_MCKE	159	O	DDR3 SDRAM clock enable
DDR3_MCK	144	O	DDR3 SDRAM differential clock signal 0
DDR3_nMCK	143	O	DDR3 SDRAM differential clock signal 1
DDR3_nMCS0	188	O	DDR3 SDRAM chip select 0
DDR3_MODT	189	O	DDR3 on die termination
DDR3_nMWE	175	O	Write enable
DDR3_nMCAS	173	O	Column address strobe
DDR3_nMRAS	172	O	Row address strobe
DDR3_BA[2:0]	176, 161, 187	O	Bank address
DDR3_MLDM	146	O	Data mask for DQ[7:0]
DDR3_MHDM	145	O	Data mask for DQ[15:8]
DDR3_MLDQS	140	I/O	Data strobe for DQ[7:0]
DDR3_nMLDQS	141	I/O	Data strobe for DQ[7:0]
DDR3_MHDQS	148	I/O	Data strobe for DQ[15:8]
DDR3_nMHDQS	149	I/O	Data strobe for DQ[15:8]
DDR3_MA[15:0]	160, 169, 179, 164, 170, 171, 178, 167, 183, 166, 184, 165, 186, 180, 168, 185	O	Address for DDR3 SDRAM
DDR3_MD[15:0]	139, 153, 136, 150, 135, 154, 138, 151, 157, 130, 158, 133, 155, 131, 156, 134	I/O	Data for DDR3 SDRAM
MZQ	190	AO	Reference Pin for ZQ calibration.
DDR3_nMRST	182	O	Memory reset for DDR3 SDRAM.

7.2. Media Dependent Interface Pins

Table 5. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	9 10 11 12 14 15 16 17	AI/O	10	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	19 20 21 22 24 25 26 27	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	30 31 32 33 35 36 37 38	AI/O	10	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	40 41 42 43 45 46 47 48	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

7.3. Shared I/O Pin Mapping

The RTL86907 supports many types of digital interface Parallel LED, Serial LED, EJTAG, SMI, MIIM and UART.

Table 6. Shared I/O Pin Mapping

PIN No.	GPIO	Parallel LED	Serial LED	EJTAG	SPI FLASH	NAND FLASH	Others
83	GPIO21	LED15	-	-	-	-	-
84	GPIO22	LED16	-	-	-	-	-
116	GPIO37	-	-	-	-	-	SCK0
117	GPIO38	-	-	-	-	-	SDA0
118	GPIO34	-	-	-	-	-	-
119	GPIO35	-	-	-	-	-	TX_SD
120	GPIO36	-	-	-	-	-	-
193	GPIO41	-	-	-	-	SIO7	-
194	GPIO42	-	-	-	-	SIO6	-
195	GPIO43	-	-	-	-	SIO5	-
196	GPIO44	-	-	-	-	SIO4	-
197	-	-	-	-	SPIF_D2	SIO3	-
198	-	-	-	-	SPIF_D1	SIO2	-
199	-	-	-	-	SPIF_D0	SIO1	-
200	-	-	-	-	SPIF_D3	SIO0	-
202	-	-	-	-	SPIF_CLK	nFWE	-
203	GPIO50	-	-	-	-	ALE	-
204	GPIO51	-	-	-	-	CLE	-
205	-	-	-	-	SPIF_nCS	nMCS	-
207	GPIO53	-	-	-	-	nFRE	-
208	GPIO54	-	-	-	-	RDY_BSY	-
209	GPIO58	LED13	SLED_CK	JTAG_TDO	-	-	-
210	GPIO59	LED12	SLED_DA	JTAG_TMS	-	-	-
211	GPIO60	LED11	-	-	-	-	SCK1
212	GPIO61	LED10	-	-	-	-	SDA1
213	GPIO12	LED9	-	JTAG_TDI	-	-	INT0
214	GPIO13	LED8	-	-	-	-	UTXD1
215	GPIO23	LED7	-	-	-	-	INT1
216	GPIO24	LED6	-	-	-	-	URXD1
3	GPIO45	LED5	-	-	-	-	-
4	GPIO46	LED4	-	JTAG_CK	-	-	-
5	GPIO47	LED3	-	-	-	-	-
6	GPIO48	LED2	-	JTAG_nRST	-	-	-
7	GPIO49	LED1	-	-	-	-	URXD0
8	GPIO52	LED0	-	-	-	-	UTXD0

7.4. GPIO

Table 7. GPIO Pins

Pin Name	Pin No.	Type	Description
GPIO0	57	I/O_{PD}	General Purpose Input/Output Interfaces IO0.
GPIO6	58	I/O	General Purpose Input/Output Interfaces IO6.
GPIO8	61	I/O_{PU}	General Purpose Input/Output Interfaces IO8.
GPIO9	62	I/O	General Purpose Input/Output Interfaces IO9.
GPIO10	63	I/O_{PU}	General Purpose Input/Output Interfaces IO10.
GPIO11	65	I/O	General Purpose Input/Output Interfaces IO11.
GPIO15	66	I/O	General Purpose Input/Output Interfaces IO15.
GPIO16	67	I/O	General Purpose Input/Output Interfaces IO16.
GPIO17	68	I/O	General Purpose Input/Output Interfaces IO17.
GPIO18	69	I/O	General Purpose Input/Output Interfaces IO18.
GPIO19	70	I/O	General Purpose Input/Output Interfaces IO19.
GPIO20	71	I/O	General Purpose Input/Output Interfaces IO20.
GPIO1	73	I/O	General Purpose Input/Output Interfaces IO1.
GPIO31	74	I/O	General Purpose Input/Output Interfaces IO31.
GPIO27	75	I/O_{PU}	General Purpose Input/Output Interfaces IO27.
GPIO29	76	I/O_{PU}	General Purpose Input/Output Interfaces IO29.
GPIO28	77	I/O	General Purpose Input/Output Interfaces IO28.
GPIO25	78	I/O_{PU}	General Purpose Input/Output Interfaces IO25.
GPIO26	79	I/O_{PU}	General Purpose Input/Output Interfaces IO26.
GPIO33	80	I/O_{PU}	General Purpose Input/Output Interfaces IO33.
GPIO32	81	I/O	General Purpose Input/Output Interfaces IO32.
GPIO30	82	I/O	General Purpose Input/Output Interfaces IO30.
GPIO21	83	I/O_{PU}	General Purpose Input/Output Interfaces IO21.
GPIO22	84	I/O	General Purpose Input/Output Interfaces IO22.
GPIO37	116	I/O	General Purpose Input/Output Interfaces IO37.
GPIO38	117	I/O	General Purpose Input/Output Interfaces IO38.
GPIO34	118	I/O	General Purpose Input/Output Interfaces IO34.
GPIO35	119	I/O	General Purpose Input/Output Interfaces IO35.
GPIO36	120	I/O	General Purpose Input/Output Interfaces IO36.
GPIO41	193	I/O	General Purpose Input/Output Interfaces IO41.
GPIO42	194	I/O	General Purpose Input/Output Interfaces IO42.
GPIO43	195	I/O	General Purpose Input/Output Interfaces IO43.
GPIO44	196	I/O	General Purpose Input/Output Interfaces IO44.
GPIO58	209	I/O_{PU}	General Purpose Input/Output Interfaces IO58.
GPIO59	210	I/O_{PU}	General Purpose Input/Output Interfaces IO59.
GPIO60	211	I/O_{PU}	General Purpose Input/Output Interfaces IO60.
GPIO61	212	I/O_{PU}	General Purpose Input/Output Interfaces IO61.
GPIO12	213	I/O_{PU}	General Purpose Input/Output Interfaces IO12.
GPIO13	214	I/O_{PU}	General Purpose Input/Output Interfaces IO13.
GPIO23	215	I/O_{PU}	General Purpose Input/Output Interfaces IO23.

Pin Name	Pin No.	Type	Description
GPIO24.	216	I/O_{PU}	General Purpose Input/Output Interfaces IO24.
GPIO45	3	I/O_{PU}	General Purpose Input/Output Interfaces IO45.
GPIO46	4	I/O_{PU}	General Purpose Input/Output Interfaces IO46.
GPIO47	5	I/O_{PU}	General Purpose Input/Output Interfaces IO47.
GPIO48	6	I/O_{PU}	General Purpose Input/Output Interfaces IO48.
GPIO49	7	I/O_{PU}	General Purpose Input/Output Interfaces IO49.
GPIO52	8	I/O_{PU}	General Purpose Input/Output Interfaces IO52.

7.5. Parallel LED Pins

Table 8. Parallel LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED0	8	I/O_{PU}	-	LED0 Output Signal. LED indicates information is defined by register.
LED1	7	I/O_{PU}	-	LED1 Output Signal. LED indicates information is defined by register.
LED2	6	I/O_{PU}	-	LED2 Output Signal. LED2 indicates information is defined by register.
LED3	5	I/O_{PU}	-	LED3 Output Signal. LED3 indicates information is defined by register.
LED4	4	I/O_{PU}	-	LED4 Output Signal. LED4 indicates information is defined by register.
LED5	3	I/O_{PU}	-	LED5 Output Signal. LED5 indicates information is defined by register.
LED6	216	I/O_{PU}	-	LED6 Output Signal. LED6 indicates information is defined by register.
LED7	215	I/O_{PU}	-	LED7 Output Signal. LED7 indicates information is defined by register.
LED8	214	I/O_{PU}	-	LED8 Output Signal. LED8 indicates information is defined by register.
LED9	213	I/O_{PU}	-	LED9 Output Signal. LED9 indicates information is defined by register.
LED10	212	I/O_{PU}	-	LED Output Signal. LED indicates information is defined by register.
LED11	211	I/O_{PU}	-	LED9 Output Signal. LED9 indicates information is defined by register.
LED12	210	I/O_{PU}	-	LED12 Output Signal. LED12 indicates information is defined by register.
LED13	209	I/O_{PU}	-	LED13 Output Signal. LED13 indicates information is defined by register.

7.6. Serial LED Pins

Table 9. Serial LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SLED_CK	209	I/O_{PU}	-	Serial LED Output Signal Clock.
SLED_DA	210	I/O_{PU}	-	Serial LED Output Signal Data.

7.7. Serial SPI Flash Control

Table 10. Serial SPI Flash Control Pins

Pin Name	Pin No.	Type	Description
SPIF_nCS	205	I/O	SPI Serial Flash Chip Select.
SPIF_D[3:0]	200, 197, 198, 199	I/O	SPI Serial Flash Serial Data Input/Output.
SPIF_CLK	202	I/O_{PU}	SPI Serial Flash Serial Clock Output. The SF_SDI will be driven on the falling edge. The SF_SDO will be latched on the rising edge.

7.8. NAND Flash Control

Table 11. Serial SPI Flash Control Pins

Pin Name	Pin No.	Type	Description
nMCS0	205	O	CHIP Select *The nMCS0 input is the device selection control. When the device is in the Busy state, CE high is ignored, and the device does not return to standby mode in program or erase operation.*
nFWE	202	O_{PU}	WRITE ENABLE *The nFWE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse.*
ALE	203	O_{PU}	ADDRESS LATCH ENABLE *The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.*
CLE	204	O_{PU}	COMMAND LATCH ENABLE *The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.*
nFRE	207	O_{PU}	READ ENABLE *The nFRE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one.*

Pin Name	Pin No.	Type	Description
RDY_BSY	208	I_{PU}	READY/BUSY OUTPUT The RDY_BSY output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. *R/B can simply wired-or together.*
SIO[7:0]	193, 194, 195, 196, 197, 198, 199, 200	I/O	DATA INPUTS/OUTPUTS *The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.*

7.9. UART

Table 12. UART Pins

Pin Name	Pin No.	Type	Description
UTXD0	8	O_{PU}	Data Transmit Serial Output of UART0.
URXD0	6	I_{PU}	Data Receive Serial Input of UART0.
UTXD1	214	O_{PD}	Data Transmit Serial Output of UART1.
URXD1	216	I_{PU}	Data Receive Serial Input of UART1.

7.10. JTAG

Table 13. JTAG Pins

Pin Name	Pin No.	Type	Description
JTAG_CK	4	I_{PU}	JTAG Test Clock.
JTAG_TMS	210	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	209	O_{PU}	JTAG Test Data Output.
JTAG_TDI	213	I_{PU}	JTAG Test Data In.
JTAG_nRST	6	I_{PU}	JTAG Test Reset.

7.11. General Purpose Interfaces

The RTL86907 supports multi-function General Purpose Interfaces that can be configured as extra interfaces of Extension or other Digital I/O interfaces. The RTL86907 supports one extension interface for connecting with an external PHY, or MAC in specific applications. The extension interface support RGMII, (T)MII MAC mode, (T)MII PHY mode, RMII clock in mode, or RMII clock out mode via register configuration. The General Purpose Interface also could be configured to General Purpose Input/Output Interfaces when the GMII interface is disabled.

Table 14. RTL86907 General Purpose Interfaces Pin Definitions

Pin No.	GPIO	RGMII Mode	(T)MII MAC Mode	(T)MII PHY Mode	RMII Clock In mode	RMII Clock Out mode
65	GPIO11	RG_TXCLK (Output)	MM_TXCLK (Input)	MP_RXCLK (Output)	RMM_CLK (Input)	RMM_CLK (Output)
63	GPIO10	RG_TXCTL (Output)	MM_TXEN (Output)	MP_RXDV (Output)	RMM_TXEN (Output)	RMM_TXEN (Output)
58 59	GPIO6 GPIO7	RG_TXD [3:2] (Output)	MM_TXD [3:2] (Output)	MP_RXD [3:2] (Output)	-	-
61 62	GPIO8 GPIO9	RG_TXD [1:0] (Output)	MM_TXD [1:0] (Output)	MP_RXD [1:0] (Output)	RMM_TXD[1:0] (Output)	RMM_TXD[1:0] (Output)
66	GPIO15	RG_RXCLK (Input)	MM_RXCLK (Input)	MP_TXCLK (Input)	-	-
67	GPIO16	RG_RXCTL (Input)	MM_RXDV (Input)	MP_TXEN (Input)	RMM_CRS_DV (Input)	RMM_CRS_DV (Input)
71 70	GPIO20 GPIO19	RG_RXD [3:2] (Input)	MM_RXD [3:2] (Input)	MP_TXD [3:2] (Input)	-	-
69 68	GPIO18 GPIO17	RG_RXD [1:0] (Input)	MM_RXD [1:0] (Input)	MP_TXD [1:0] (Input)	RMM_RXD[1:0] (Input)	RMM_RXD[1:0] (Input)
57	GPIO0	-	MP_CRS	-	-	-

7.11.1. RGMII Pins

The Extension of the RTL86907 support one RGMII interfaces to connect with an external MAC or PHY device when register configuration is set to RGMII mode interface.

Table 15. Extension RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG_RXD3 RG_RXD2 RG_RXD1 RG_RXD0	71 70 69 68	I	-	RG_RXD[3:0] Extension RGMII Receive Data Input. Received data is received synchronously by RG_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.
RG_RXCTL	67	I	-	RG_RXCTL Extension RGMII Receive Control signal input. The RG_RXCTL indicates RX_DV at the rising of RG_RXCLK and RX_ER at the falling edge of RG_RXCLK. At RG_RXCLK falling edge, RG_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG_RXCLK	66	I	-	RG_RXCLK Extension RGMII Receive Clock Input. RG_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG_RXD[3:0] and RG_RXCTL synchronization at both RG_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No.	Type	Drive (mA)	Description
RG_TXCLK	65	O	-	RG_TXCLK Extension RGMII Transmit Clock Output. RG_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG_TXD[3:0] and RG_TXCTL synchronization at RG_TXCLK on both rising and falling edges.
RG_TXCTL	63	O_{PU}	-	RG_TXCTL Extension RGMII Transmit Control signal Output. The RG_TXCTL indicates TX_EN at the rising edge of RG_TXCLK, and TX_ER at the falling edge of RG_TXCLK. At the RG_TXCLK falling edge, RG_TXCTL= TX_EN (XOR) TX_ER. This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
RG_TXD0 RG_TXD1 RG_TXD2 RG_TXD3	58 59 61 62	I/O I/O_{PU} I/O_{PU} I/O	-	RG_TXD[3:0] Extension RGMII Transmit Data Output. Transmitted data is sent synchronously to RG_TXCLK.

7.11.2. (T)MII Pins

The Extension of the RTL86907 also support one (T)MII interfaces to connect with an external MAC or PHY device when register configuration is set to (T)MII mode interface. The (T)MII interface also can be configured as MII MAC mode or MII PHY mode by register.

Table 16. Extension MII Pins ((T)MII MAC Mode or (T)MII PHY Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
MM_CRS/ MP_CRS	57	I/O_{PD}	-	MM_CRS Extension (T)MII MAC Mode Carrier Sense Input when operating in 10/100 MII half duplex mode. MP_CRS Extension (T)MII MAC Mode Carrier Sense Output when operating in 10/100 (T)MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
MM_RXD3/ MP_TXD3 MM_RXD2/ MP_TXD2 MM_RXD1/ MP_TXD1 MM_RXD0/ MP_TXD0	71 70 69 68	I	-	MM_RXD[3:0] Extension (T)MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of MM_RXCLK. MP_TXD[3:0] Extension (T)MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of MP_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No.	Type	Drive (mA)	Description
MM_RXDV/ MP_TXEN	67	I	-	MM_RXDV Extension (T)MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of MM_RXCLK. MP_TXEN Extension (T)MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of MP_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
MM_RXCLK/ MP_TXCLK	66	I/O	-	MM_RXCLK Extension (T)MII MAC Mode Receive Clock Input. In MII 100Mbps, MM_RXCLK is 25MHz Clock Input. In MII 10Mbps, MM_RXCLK is 2.5MHz Clock Input. In TMII 200Mbps, MM_RXCLK is 50MHz Clock Input. In TMII 20Mbps, MM_RXCLK is 5MHz Clock Input. Used to synchronize MM_RXD[3:0], and MM_RXDV. MP_TXCLK (T)MII PHY Mode Transmit Clock Output. In MII 100Mbps, MP_TXCLK is 25MHz Clock Output. In MII 10Mbps, MP_TXCLK is 2.5MHz Clock Output. In TMII 200Mbps, MP_TXCLK is 50MHz Clock Output. In TMII 20Mbps, MP_TXCLK is 5MHz Clock Output. Used to synchronize MP_TXD[3:0], and MP_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
MM_TXCLK/ MP_RXCLK	65	I/O	-	MM_TXCLK Extension (T)MII MAC Mode Transmit Clock Input. In MII 100Mbps, MM_TXCLK is 25MHz Clock Input. In MII 10Mbps, MM_TXCLK is 2.5MHz Clock Input. In TMII 200Mbps, MM_TXCLK is 50MHz Clock Input. In TMII 20Mbps, MM_TXCLK is 5MHz Clock Input. Used to synchronize MM_TXD[3:0], and MM_TXEN. MP_RXCLK Extension MII PHY Mode Receive Clock Output. In MII 100Mbps, MP_RXCLK is 25MHz Clock Output. In MII 10Mbps, MP_RXCLK is 2.5MHz Clock Output. In TMII 200Mbps, MP_RXCLK is 50MHz Clock Output. In TMII 20Mbps, MP_RXCLK is 5MHz Clock Output. Used to synchronize MP_RXD[3:0], and MP_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No.	Type	Drive (mA)	Description
MM_TXEN/ MP_RXDV	63	O_{PU}	-	MM_TXEN Extension (T)MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of MM_TXCLK. MP_RXDV Extension (T)MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of MP_RXCLK. This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
MM_TXD0/ MP_RXD0 MM_TXD1/ MP_RXD1 MM_TXD2/ MP_RXD2 MM_TXD3/ MP_RXD3	62 61 59 58	I/O I/O_{PU} I/O_{PU} I/O	-	MM_TXD[3:0] Extension (T)MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of MM_TXCLK. MP_RXD[3:0] Extension (T)MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of MP_RXCLK.

7.11.3. RMII Pins

The Extension of the RTL86907 also support one RMII interfaces to connect with an external MAC or PHY device when register configuration is set to RMII mode interface. The RMII interface also can be configured as RMII clock in mode or MII clock out mode by register.

Table 17. Extension RMII Pins (RMII clock in Mode or RMII clock out Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
RMM_RXD1 RMM_RXD0	69 68	I	-	RMM_RXD[1:0] Extension MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of RMM_RXCLK.
RMM_CRS_DV	67	I	-	RMM_RXDV Extension MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of RMM_RXCLK.

Pin Name	Pin No.	Type	Drive (mA)	Description
RMM_CLK	65	I/O	-	RMM_CLK Extension MII MAC Mode Receive Clock Input in RMII clock in mode. RMM_CLK Extension MII MAC Mode Transmit Clock Output in RMII clock out mode. In RMII 100Mbps, RMM_CLK is 50MHz Clock Input / Output. In RMII 10Mbps, RMM_CLK is 5MHz Clock Input / Output. Used to synchronize RMM_TXD[1:0], and RMM_TXEN.
RMM_TXEN	63	O_{PU}	-	RMM_TXEN Extension MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of RMM_TXCLK. This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
RMM_TXD0 RMM_TXD1	62 61	I/O I/O_{PU}	-	RMM_TXD[1:0] Extension MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of RMM_TXCLK.

7.12. VOIP Interface

Table 18. VOIP Shared I/O Pin Mapping

PIN No.	GPIO	SPI+PCM	ZSI	ISI
74	GPIO31	SLICSPI_nCS1	-	-
75	GPIO27	SLICPCM_CLK	ZPAPCK	-
76	GPIO29	SLICSPI_MOSI	Z0MOSI	MSIF0_PSDO
77	GPIO28	SLICSPI_MISO	Z0MISO	MSIF0_PSDI
78	GPIO25	SLICSPI_CLK	-	MSI_CLK24M
79	GPIO26	SLICPCM_FS	Z0SYNC	-
80	GPIO33	SLICPCM_TXD	Z1MOSI	MSIF1_PSDO
81	GPIO32	SLICPCM_RXD	Z1MISO	MSIF1_PSDI
30	GPIO30	SLICSPI_nCS0	Z1SYNC	-

7.12.1. PCM Interface

Table 19. PCM Interface

Pin Name	Pin No.	Type	Description
SLICPCM_TXD	80	O	PCM transmit data
SLICPCM_RXD	81	I	PCM receive data
SLICPCM_CLK	75	O	PCM clock which frequency is 2.048Mhz

Pin Name	Pin No.	Type	Description
SLICPCM_FS	79	O	PCM transmit frame synchronization

7.12.2. SLIC SPI Interface

Table 20. SPI Interface

Pin Name	Pin No.	Type	Description
SLICSPI_nCS0	82	O	SPI chip select pin 0
SLICSPI_nCS1	74	O	SPI chip select pin 1
SLICSPI_CLK	78	O	SPI reference clock
SLICSPI_MOSI	76	O	SPI data out
SLICSPI_MISO	77	I	SPI data in

7.12.3. SLIC ZSI Interface

Table 21. ZSI Interface

Pin Name	Pin No.	Type	Description
ZPAPCK	75	O	ZSI clock
Z0MOSI	76	O	ZSI data out, port 0
Z0MISO	77	I	ZSI data in, port 0
Z0SYNC	79	O	ZSI sync, port 0
Z1MOSI	80	O	ZSI data out, port 1
Z1MISO	81	I	ZSI data in, port 1
Z1SYNC	82	O	ZSI sync, port 1

7.12.4. SLIC ISI Interface

Table 22. ISI Interface

Pin Name	Pin No.	Type	Description
MSIF0_PSDO	76	O	ISI data out, port 0
MSIF0_PSDI	77	I	ISI data in, port 0
MSI_CLK24M	78	O	ISI clock
MSIF1_PSDO	80	O	ISI data out, port 1
MSIF1_PSDI	81	I	ISI data in, port 1

7.13. PON SerDes Interface

Table 23. PON SerDes Interface

Pin Name	Pin No.	Type	Description
HSON	104	AO	Transmit Data Analog negative output signals. Internal pull high 50 ohm, CML or LVPECL signal, DC couple for ONU.
HSOP	105	AO	Transmit Data Analog positive output signals. Internal pull high 50 ohm, CML or LVPECL signal, DC couple for ONU.
HSIN	111	AI	Receiver Data Analog positive input signals. CML signal, internal pull high 50 ohm, AC couple for ONU.
HSIP	110	AI	Receiver Data Analog negative input signals. CML signal, internal pull high 50 ohm, AC couple for ONU.
HSOENN	107	AO	Differential negative burst fiber transceiver burst enable signal, internal pull high 50 ohm, CML signal.
HSOENP / HSOEN	108	AO	Differential positive fiber transceiver burst enable signal, internal pull high 50 ohm, CML signal. This signal can be set to single end LVTTL BEN signal via register.
HSSD	112	I	PON Optical Signal Detect, LVTTL signal. High: optical is present at receiver input. Low : No RX signal input
TX_SD	119	I	PON Optical TX Signal Detect, LVTTL signal. High: optical is present at transmitter output. Low : No TX signal output

7.14. USB 2.0

Table 24. USB 2.0 Pins

Pin Name	Pin No.	Type	Description
USB2_DP1	123	AI/O	USB0 USB 2.0 Analog positive signals.
USB2_DM1	124	AI/O	USB0 USB 2.0 Analog negative signals.
USB2_DP2	127	AI/O	USB1 USB 2.0 Analog positive signals.
USB2_DM2	128	AI/O	USB1 USB 2.0 Analog negative signals.

7.15. PCI Express Interface

Table 25. PCI Express Interface

Pin Name	Pin No.	Type	Description
PON1	86	AO	PCI Express 1 Transmit Data Analog negative output signals
POP1	87	AO	PCI Express 1 Transmit Data Analog positive output signals.
PREFCLKM1	89	AO	PCI Express 1 Reference Clock Differential Pair.
PREFCLKP1	90	AO	PCI Express 1 Reference Clock Differential Pair.

Pin Name	Pin No.	Type	Description
PIN1	91	AI	PCI Express 1 Transmit Data Analog negative input signals
PIP1	92	AI	PCI Express 1 Receiver Data Analog positive input signals.
PON0	94	AO	PCI Express 0 Receiver Data Analog negative output signals.
POP0	95	AO	PCI Express 0 Transmit Data Analog positive output signals.
PREFCLKM0	97	AO	PCI Express 0 Reference Clock Differential Pair.
PREFCLKP0	98	AO	PCI Express 0 Reference Clock Differential Pair.
PIN0	99	AI	PCI Express 0 Receiver Data Analog negative input signals.
PIP0	100	AI	PCI Express 0 Receiver Data Analog positive input signals.

7.16. Power & GND

Table 26. Power & GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO	1, 72, 115, 201,	P	Digital I/O High Voltage Power
DVDDL	2, 56, 85, 122, 142, 174, 206	P	Digital Low Voltage Power.
AVDDH	18, 29, 39, 49, 55	AP	Analog High Voltage Power.
AVDDL	13, 23, 34, 44, 52	AP	Analog Low Voltage Power.
PLLVDDL0	28	AP	PLL0 Low Voltage Power.
PLLVDDL1	109, 126	AP	PLL1 Low Voltage Power.
SVDDH	103	AP	SerDes Analog High Voltage Power.
SVDDL	106	AP	SerDes Analog Low Voltage Power.
USBVDDH	125	AP	USB Analog High Voltage Power.
USBVDDL	129	AP	USB Analog Low Voltage Power.
PVDDL	88, 96	AP	PCI Express Analog Low Voltage Power.
OVDDDR	132, 162, 163, 181, 191	P	DDR SDRAM I/O Power Supply DDR1 SDRAM I/O Power Supply 2.5V DDR2 SDRAM I/O Power Supply 1.8V DDR3 SDRAM I/O Power Supply 1.5V
MVREF	137, 152	AO	1/2 OVDDDR reference level
GND	EPAD	G	Digital GND.
AGND	50	AG	Analog GND.
PGND	93	AG	PCI Express Analog GND

7.17. Configuration Upon Power On Strapping

All mode configuration pins are internal pull high. The strap data will be latched after the system power-on and a delay of 300ms.

Table 27. Configuration Upon Power On Strapping

Pin Name	Pin No.	Type	Description
NAFC_RC[1:0]	205, 207	I/O	*NAFC_RC[1]:* Reserved for internal use. Must be pulled high. *NAFC_RC[0]:* Reserved for internal use. Must be left floating or pull high.
NAF_AC[1]	204, 203	I/O	Reserved for internal use. Must be left floating or pull high.
RESERVED	75	I/O_{PU}	Reserved for internal use. Must be pulled low.
RESERVED	76	I/O_{PU}	Reserved for internal use. Must be left floating or pull high.
DDR_TYPE_FREQ[2:0]	78, 79, 216	I/O_{PU}	Reserved for internal use. Must be pulled low.
RESERVED	80	I/O_{PU}	Reserved for internal use. Must be pulled low.
SPIF4BEN	202	I/O_{PU}	SPI flash address byte number 0: 3 Bytes 1: 4 Bytes
DIS_JTAG	209	I/O_{PU}	Enable / Disable JTAG interface 0: Enable JTAG 1: Disable JTAG
BTUP_TYP	214	I/O_{PU}	Boot up flash selection 0: SPI Flash 1: Nand Flash

7.18. Test Pins

Table 28. Test Pins

Pin Name	Pin No.	Type	Description
RTT1	53	AO	Reserved for Internal Use. Must be left floating.
RTT2	54	AO	Reserved for Internal Use. Must be left floating.

7.19. Miscellaneous Pins

Table 29. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
XTALI	101	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/-50ppm tolerance crystal reference or oscillator input.
XTALO	102	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.

Pin Name	Pin No.	Type	Description
MDIREF	51	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
VCTRL_DDR	192	AO	Linear Regulator Voltage Control. External 3.3V to 2.5V Transfer for DDR1 SDRAM External 3.3V to 1.8V Transfer for DDR2 SDRAM External 3.3V to 1.5V Transfer for DDR3 SDRAM
RESERVED	113	AI	*Reserved for Internal Use. Must be left floating.*
VREF	114	AI	Dying Gasp voltage detect input.
DYINGOUT	73	O	Dying Gasp voltage detect output.
INT0	213	I	CPU interrupt 0.
INT1	215	I	CPU interrupt 1.
SCK0	116	O	SMI Interface Clock 0.
SDA0	117	I/O	SMI Interface Data 0.
SCK1	211	O	SMI Interface Clock 1.
SDA1	212	I/O	SMI Interface Data 1.

8. Memory Controller

The RTL86907 integrates a memory control module to access external DDR SDRAM , DDR2 SDRAM, DDR3 SDRAM and Flash memory. The DDR SDRAM interface supports two chip (**nMCS0 and nMCS1**), and the memory size and timing is configurable in registers.

The RTL86907 also supports a flash memory chips. The interface supports SPI flash memory. When Flash is used, the system will boot from KSEG1 at virtual address 0xBFC0_0000 (physical address: 0x1FC0_0000). The flash size is configurable from 1M to 32M bytes for each chip. If flash size is set to 4M, 8M, 16M, or 32M byte, 0xBFC0_0000 still maps the first 4M bytes of flash, and there will be a new memory mapping from 0xBD00_0000 (0xBD00_0000 maps to chip 0 byte 0).

8.1. DDR1/DDR2 SDRAM Controller

8.1.1. Features

- Interface (Bus Width): 16-bit
- DDR1 Frequency: Up to 200MHz (DDR-400)
- DDR2 Frequency: Up to 400MHz (DDR2-800)
- Supports two Chip Selects (nMCS0 and nMCS1)
- Supports both DDR1 and DDR2 SDRAM
- Supported DDR SDRAM Chip Specification
  - Bank Counts: 4
  - Row Counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column Counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11), 4K (A0~A9, A11, A12)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

8.2. DDR3 SDRAM Controller

8.2.1. Feature lists

- Interface (Bus Width): 16 bit
- Targeted DDR3 Frequency: up to 400MHz (DDR3-800)
- Supports one Chip Select (nMCS0)
- Supported DDR3 SDRAM chip spec
  - Bank counts: 4,8
  - Row counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9,A11), 4K (A0~A9,A11,A12)
- Programmable timing parameters
  - tRAS, tRP, tRCD, tCL, tREFI,…
- Fixed DDR2 parameters.
  - AL = 0.
  - Some DDR2 SDRAM introduces tRPA timing parameter. We merge tRPA with tRP into one parameter.

- No tRTP. Need to check DDR2 Bus waveform to confirm there is no tRTP violation.

8.3. SPI Flash Controller

The SPI flash controller is a new design and incorporates new features.

8.3.1. Features

- SPI flash frequency: up to 62.5MHz
- Supports one chip
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

8.3.2. Pin Mode and Definition of Serial and Dual I/O

Modes supported on the SPI flash interface:

1. Serial I/O mode:
   - SI: flash chip input pin
   - SO: flash chip output pin
2. Dual I/O mode:
   - SPIF_D0 (SI): flash chip bi-directional pin. This is LSB.
   - SPIF_D1 (SO): flash chip bi-directional pin. This is MSB.
3. Quad I/O mode:
   - SPIF_D0 (SI): flash chip bi-directional pin. This is LSB.
   - SPIF_D1 (SO): flash chip bi-directional pin.
   - SPIF_D2 (WP#): flash chip bi-directional pin.
   - SPIF_D3 (HOLD#): flash chip bi-directional pin. This is MSB.

8.4. NAND Flash Controller

- 8-bit parallel data width
- Built-in intelligent hardware ECC circuits. Do ECC on the fly. (**4 bit** error correction by BCH codes, 6T/12T/24T)
  - 6T: M=13, T=6, N=8191, K=8113 (512B + 6B + 78bits)
  - 12T: M=13, T=12, N=8191, K=8035 (512B + 6B + 156bits)
  - 24T: M=14, T=24, N=16383, K=16047 (1024B + 4B + 336bits)
- Write-protection function
- PIO and DMA data read/write operation
- Configurable flash access timing
- Boot from NAND type flash

9. PON Interface

The RTL86907 supports GPON interface which compliant with ITU G.984. It supports upstream and downstream FEC, downstream AES and key switching, DBRu, H/W dying gasp, and etc.

The RTL86907 has 128 GEM ports and 32 TCONTs. It has 128 queues in PON port. For upstream direction, it supports multiple GEM mapping to one queue; and supports one queue mapping to multiple GEMs.

For scheduler function, each TCONT could scheduling upto 32 queues. Each queue could be configured for the scheduling type as strict priority (SP) and weighted fair queue (WFQ). It supports the mix mode of SP+WFQ in one scheduler (TCONT).

It supports per queue configurable commited information rate (CIR) and peak information rate (PIR), with the SP/WFQ/SP+WFQ work simultaneous. That is compliant with the traffic management option in ITU G.988.

The RTL86907 supports EPON interface which compliant with IEEE 802.3 EPON MAC standard.

- Point to Multi-point protocol with interoperability
- Single copy broadcast (SCB)
- Queue set report

It supports upstream and downstream FEC, downstream triple churning key decryption, queue set repoting, RFC4837 mib counter, H/W dying gasp, and etc.

For scheduler function, each queue could be configured for the scheduling type as strict priority (SP) and weighted fair queue (WFQ). It supports the mix mode of SP+WFQ.

It supports per queue configurable commited information rate (CIR) and peak information rate (PIR), with the SP/WFQ/SP+WFQ work simultaneous.

The PON Interface of the RTL86907 support CML and LVPEL mode in SerDes Tx side and CML mode in SerDes Rx side to a Fiber Transceiver.

9.1. PON TX

9.1.1. CML Mode

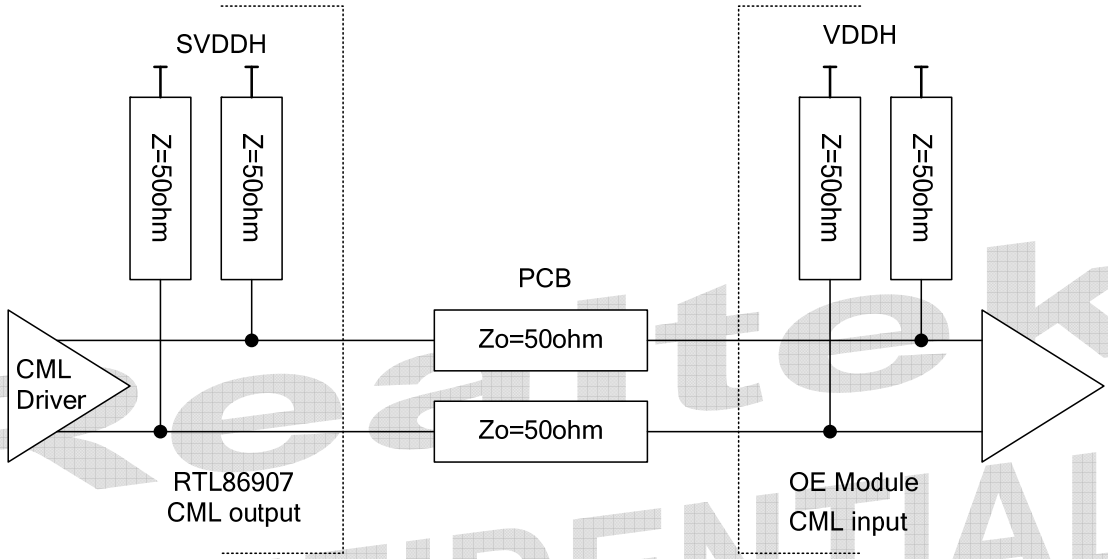


Figure 4. PON SerDes TX CML mode

9.1.2. LVPECL Mode

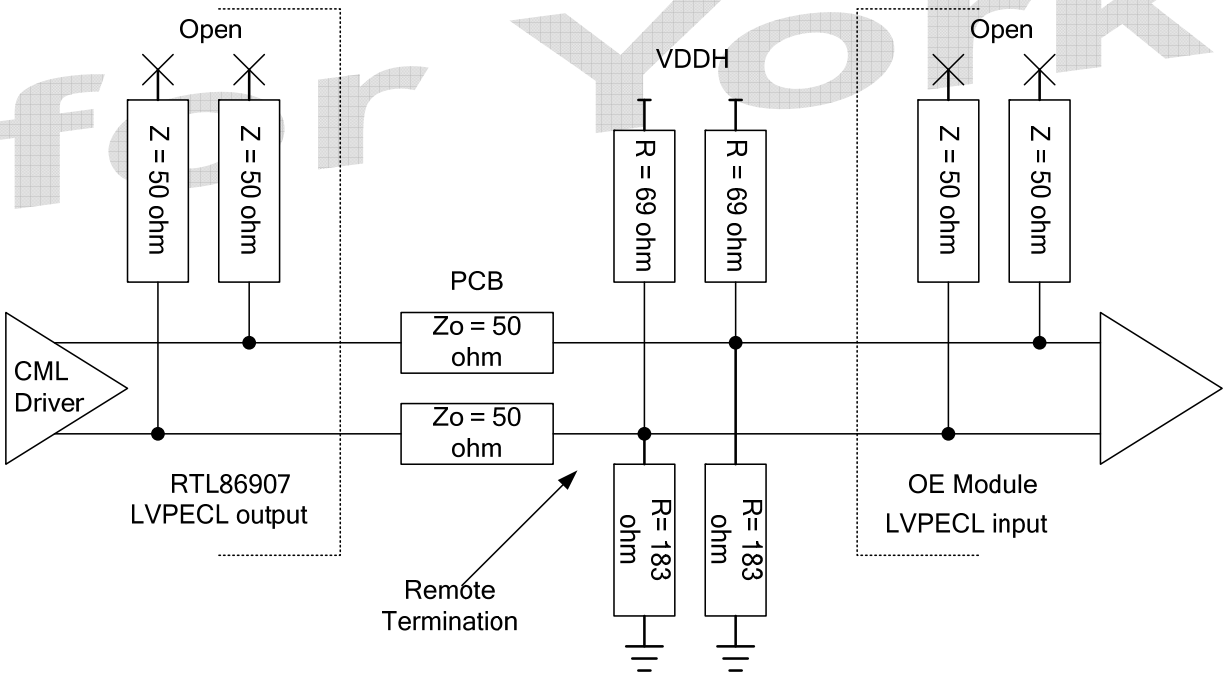


Figure 5. PON SerDes TX LVPECL mode

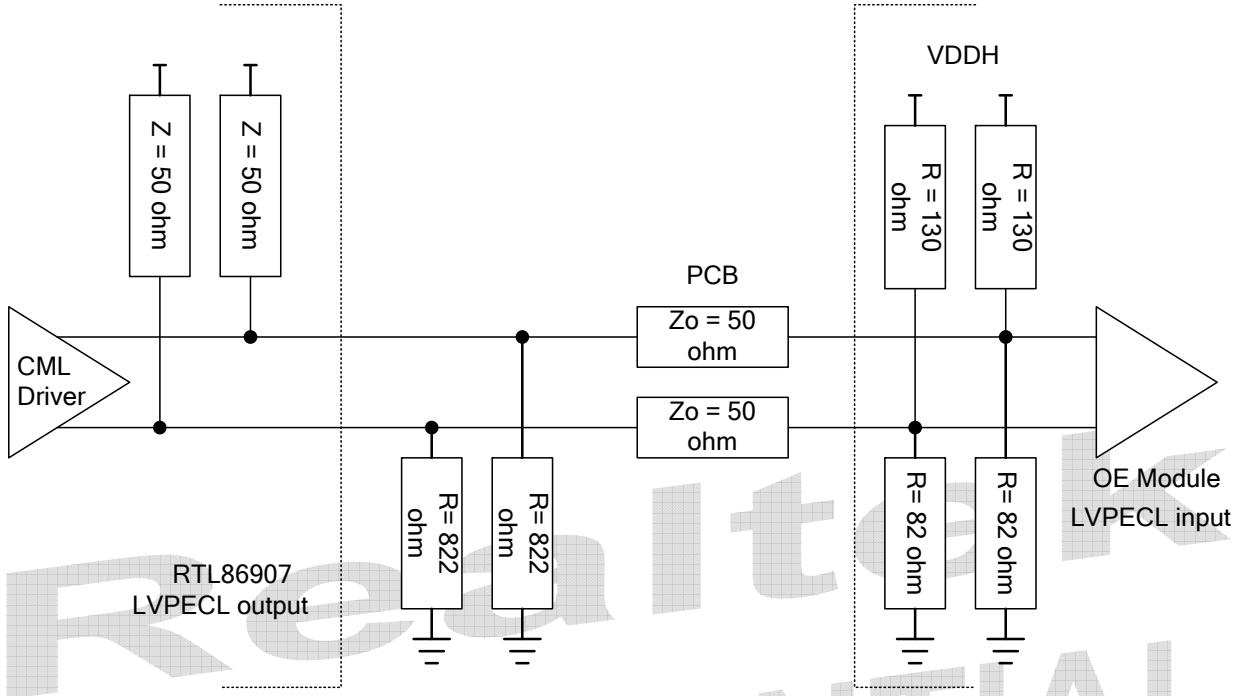


Figure 6. PON SerDes TX LVPECL mode

9.2. PON RX

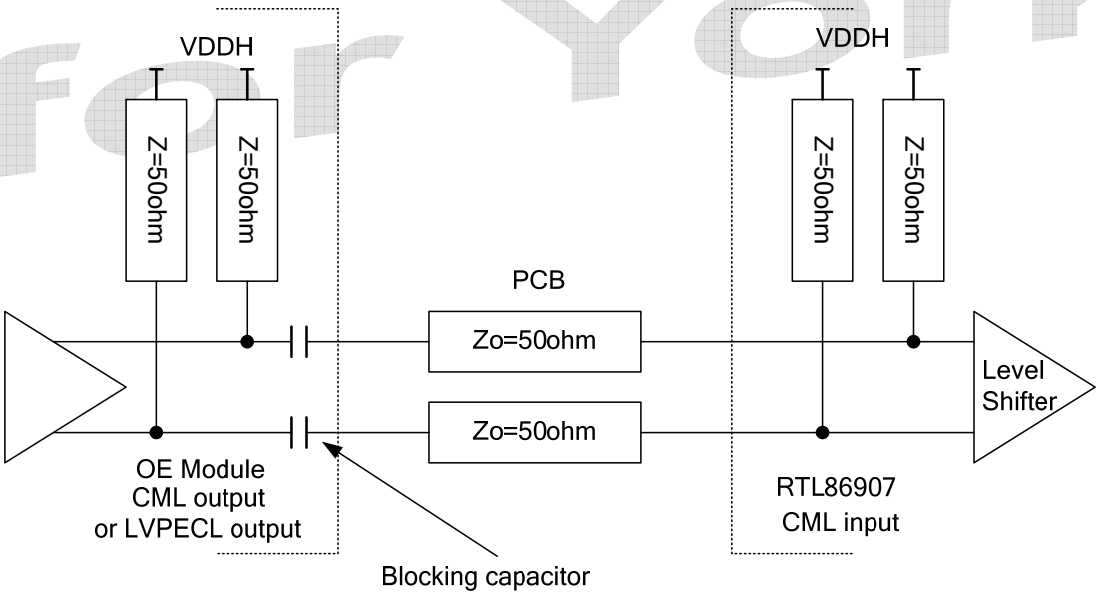


Figure 7. PON SerDes RX CML mode

10. Ethernet Physical Layer Functional Overview

10.1. MDI Interface

The RTL86907 embeds four 10/100/1000M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

10.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

10.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

10.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

10.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

10.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

10.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

10.8. Auto-Negotiation for UTP

The RTL86907 obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL86907 advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

10.9. Crossover Detection and Auto Correction

The RTL86907 automatically determines whether or not it needs to crossover between pairs (see Table 30) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL86907 automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 30. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

10.10. Polarity Correction

The RTL86907 automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

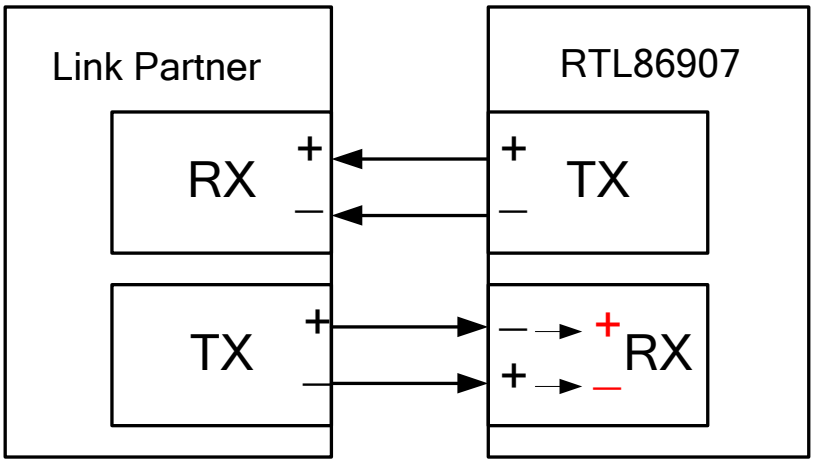


Figure 8. Conceptual Example of Polarity Correction

11. Interface Descriptions

11.1. General Purpose Interface

The RTL86907 shares one extension interfaces and GPIO pins with the General Purpose Interface. The interface function mux is summarized in Table 14. When the extension interface is configured as RGMII or MII mode.

11.1.1. Extension RGMII Mode (1Gbps)

The Extension port of the RTL86907 supports RGMII interfaces to an external device. The pin numbers and names are shown in Table 31. Figure 9 shows the signal diagram for Extension port in RGMII interfaces.

Table 31. Extension RGMII Pins

Pin No.	Type	RGMII
58, 59, 61, 62	O	RG_TXD[3:0]
63	O	RG_TXCTL
65	O	RG_TXCLK
66	I	RG_RXCLK
67	I	RG_RXCTL
71, 70, 69, 68	I	RG_RXD[0:3]

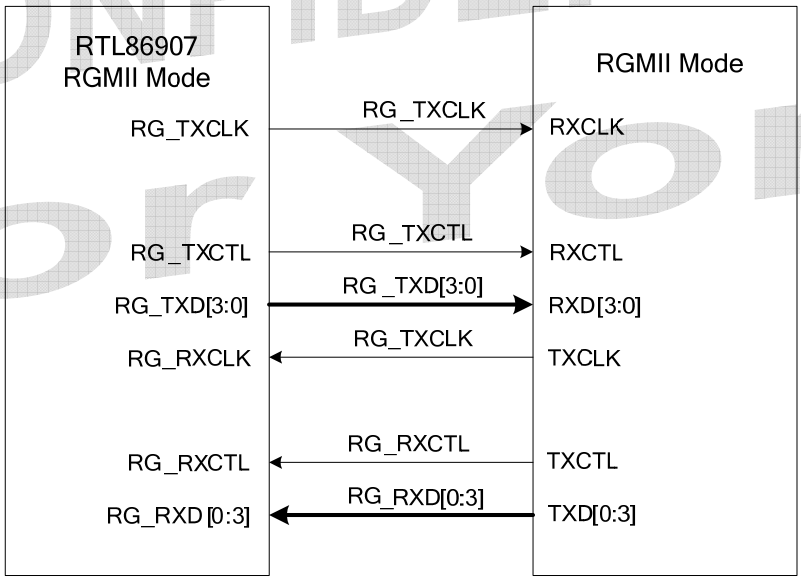


Figure 9. RGMII Mode Interface Signal Diagram

11.1.2. Extension (T)MII MAC/PHY Mode Interface (10/100Mbps)

The Extension of the RTL86907 support MII MAC/PHY mode interface to an external device. The pin numbers and names are shown in Table 32. Figure 10, page 42 shows the signal diagram for the MII PHY mode interface, and Figure 11, page 43 for the MII MAC mode interface.

The Extension of the RTL86907 is also can be configure to TMII MAC mode or TMII PHY mode interface to an external device. The throughput up to 200Mbps when configure to TMII MAC mode or TMII PHY mode. The TMII MAC mode interface operated with 50MHz clock provide by PHY mode side. The TMII PHY mode interface provided 50MHz clock to MAC mode side.

Table 32. Extension MII Pins

Pin No.	Type	MII MAC Mode	Type	MII PHY Mode
57	I	MM_CRS	O	MP_CRS
71, 70, 69, 68	I	MM_RXD[3:0]	I	MP_TXD[3:0]
67	I	MM_RXDV	I	MP_TXEN
66	I	MM_RXCLK	O	MP_TXCLK
65	I	MM_TXCLK	O	MP_RXCLK
63	O	MM_TXEN	O	MP_RXDV
58, 59, 61, 62	O	MM_TXD[3:0]	O	MP_RXD[3:0]

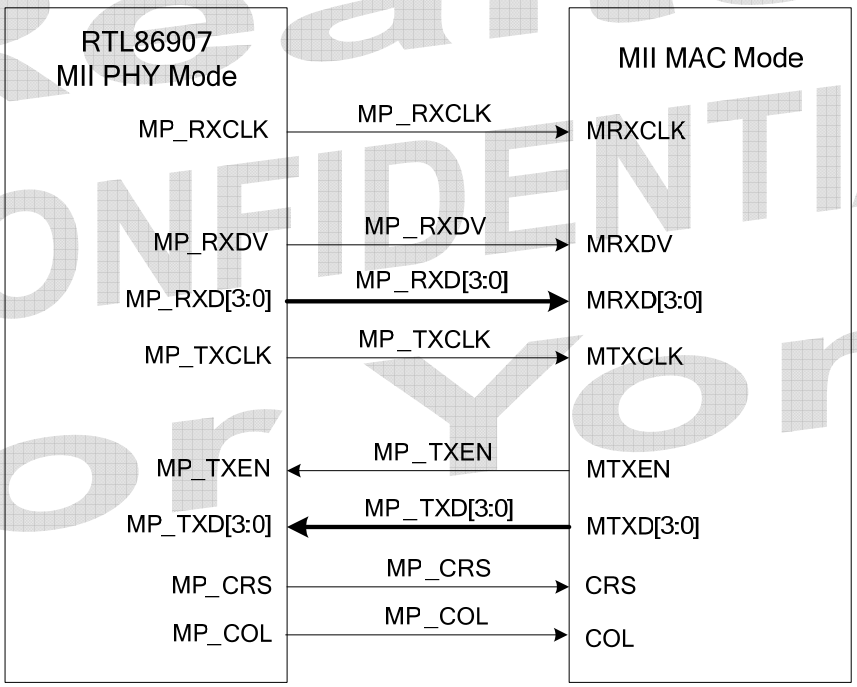


Figure 10. Signal Diagram of (T)MII PHY Mode Interface (100Mbps)

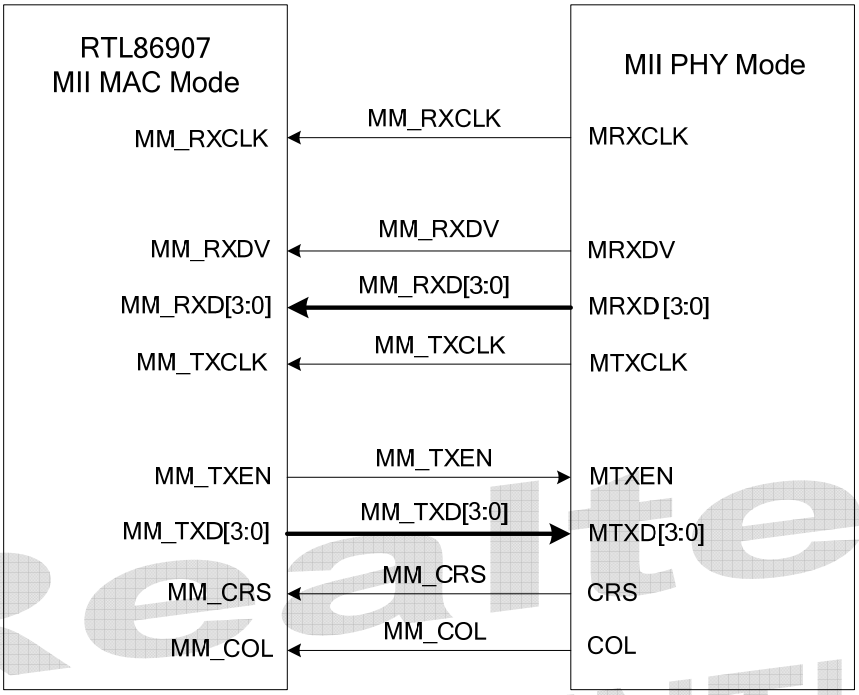


Figure 11. Signal Diagram of MII MAC Mode Interface (100Mbps)

11.2. Extension Ports RMII Mode (10/100Mbps)

The main advantage introduced by RMII is pin count reduction; e.g., it operates with only one 50MHz reference clock for both the TX and RX sides, without separate clocks needed for both paths, as with the MII interface. However, some hardware modification is needed for this change, the most important of which is the presence of an elastic buffer for absorption of the frequency difference between the 50MHz reference clock and the clocking information of the incoming data stream. Another change implemented is that the MII RXDV and Carrier_Sense are merged into one signal, CRS_DV, which is asserted high while detecting incoming packet data. When internal Carrier_Sense is de-asserted, CRS_DV is de-asserted when the first di-bit of a nibble is presented onto RXD[1:0] synchronously to REFCLK. If there is still data in the FIFO that has not yet been presented onto RXD[1:0], then, on the second di-bit of a nibble, CRS_DV reasserts. This pattern of assertion and de-assertion continues until all received data in the FIFO has been presented onto RXD[1:0].

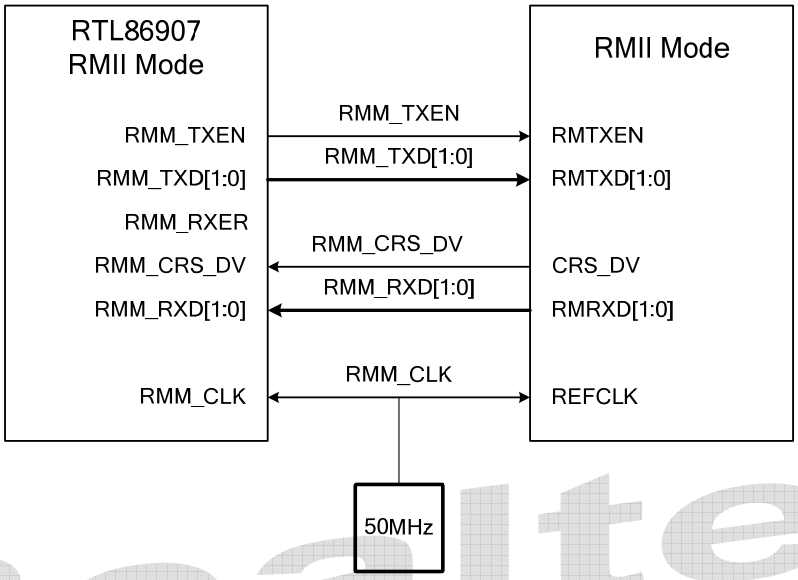


Figure 12. Signal Diagram of RMII Mode (Clock Input Mode)

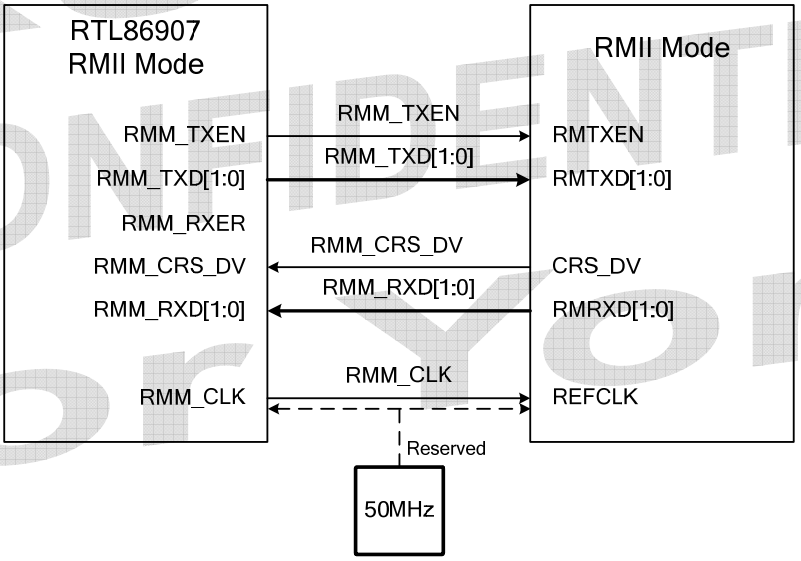


Figure 13. Signal Diagram of RMII Mode (Clock Output Mode)

Table 33. RTL86907 Extension RMII Pin Definitions

Pin No.	Type	RMII
69, 68	I	RM0M_RXD[1:0]
67	I	RM0M_CRS_DV
65	I/O	RM0M_CLK
63	O	RM0M_TXEN
61, 62	O	RM0M_TXD[1:0]

11.3. PCI Express Interface

The RTL86907 supports two PCI Express channels. The PCI Express clock rate is operates at 100 MHz.

11.4. USB Host Interface

For application extension purposes, the USB interface has become an essential interface. As a result, the RTL86907 provides two USB 2.0 host interface to give customers a wide range of value-added imagination space.

11.5. SMI Host Mode

The SMI interface of the RTL86907 uses the serial bus Serial Management Interface (SMI) to access SMI Slave device. The RTL86907 drives SCK and SDA to read or write the registers from the SMI Slave device.

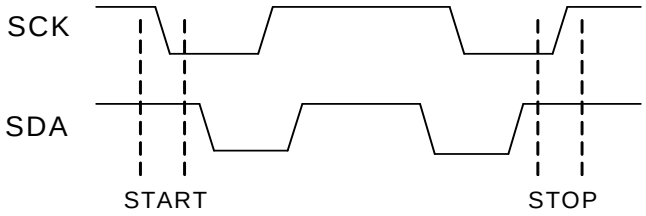


Figure 14. SMI Start and Stop Command

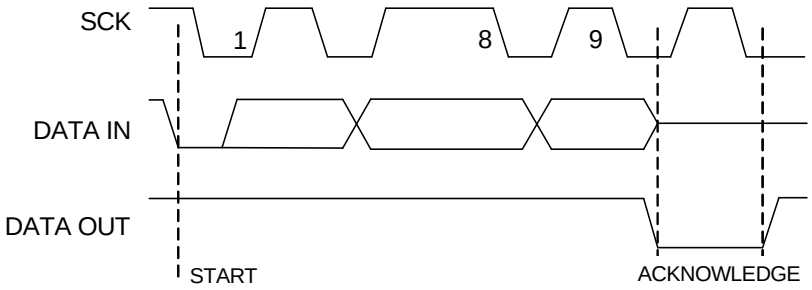


Figure 15. SMI Host to SMI Slave

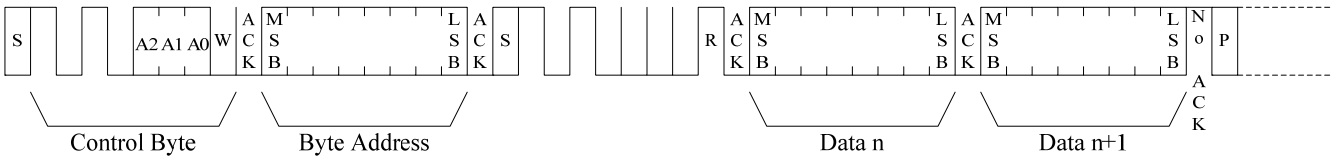


Figure 16. SMI Host Mode Frame

11.6. UART

The RTL86907 provides two 16450 compatible UARTs, which contains 16 byte FIFOs. The baud rate can be up to 1 Mbps and programmable baud rate generator allows division of any input reference clock

by 1 to (2^16-1) and generates an internal 16x clock. Berlin provides fully programmable serial interface, which can be configured to support 6,7,8 bit characters, even, odd, no parity generation and detection, and 1 or 2 stop bit generation. Last, fully prioritized interrupt control and loopback functionality for diagnostic capability are also provided.

12. General Function Description

12.1. Reset

12.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL86907 will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the boot code and system image from flash if flash is detected.
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the CPU.

12.1.2. Software Reset

The RTL86907 supports two software resets; a chip reset and a soft reset.

12.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and boot code, system image form flash.

2. Start embedded SRAM BIST (Built-In Self Test)

3. Clear all the Lookup and VLAN tables

4. Reset all registers to default values

5. Restart the auto-negotiation process

12.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list

2. Restart the auto-negotiation process

12.2. IEEE 802.3x Full Duplex Flow Control

The RTL86907 supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

12.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "Truncated Binary Exponential Backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL86907 is 9.

The half duplex back-off algorithm in the RTL86907 does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

12.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL86907 sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL86907 supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

12.4. Search and Learning

Search

When a packet is received, the RTL86907 has two kinds of search key. One is useing the destination MAC address, Filtering Identifier (FID) and enhanced Filtering Identifier (EFID) to search the 2K-entry look-up table. The other is using the destination MAC address, VID and EFID to search the look-up table. The 48-bit MAC address, 4-bit FID or 12-bit VID, and 3-bit EFID use a hash algorithm to calculate an 9-bit index value. The RTL86907 uses the index to compare the packet MAC address with the entries (MAC addresses) in the 4-way look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL86907 has two kinds of search key. It can use the source MAC address, FID, and EFID of the incoming packet or use the the source MAC address, VID, and EFID of the incoming packet to hash into a 9-bit index. It then compares the source MAC address with the data (MAC addresses) in this index of 4-way look-up table. If there is a match with one of the entries, the RTL86907 will update the entry with new information. If there is no match and the 4-way entries are not all occupied by other MAC addresses, the RTL86907 will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

If the look-up table is full, the source MAC address will not be learned in the RTL86907.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL86907 is can be set to 0.1 ~ 200, 000 seconds.

12.5. SVL and IVL/SVL

The RTL86907 supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. The RTL86907 also supports IVL mode for L2 search and learning. In IVL mode, the search key is MAC address, VID and EFID, the same source MAC address with different VIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

12.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL86907. The maximum packet length may be set to 16 ~ 16K bytes.

12.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL86907 supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 34 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 34. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
Provider Bridge Group Address	1-80-C2-00-00-08
Undefined 802.1 Address	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F
Provider Bridge MVRP Address	01-80-C2-00-00-0D
IEEE Std 802.1AB Link Layer Discovery Protocol Address	01-80-C2-00-00-0E
All LANs Bridge Management Group Address	01-80-C2-00-00-10
Load Server Generic Address	01-80-C2-00-00-11
Loadable Device Generic Address	01-80-C2-00-00-12
Undefined 802.1 Address	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F
Generic Address for All Manager Stations	01-80-C2-00-00-18
Generic Address for All Agent Stations	01-80-C2-00-00-1a
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F

12.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL86907 enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate, all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

12.9. Port Security Function

The RTL86907 supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

12.10. MIB Counters

The RTL86907 supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

12.11. Port Mirroring

The RTL86907 supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored to multiple mirror ports.

12.12. VLAN Function

The RTL86907 supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to 'Admit All' or 'Admit All Tagged'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL86907 will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL86907 also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL86907 supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL86907 also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

12.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached flash or UART interface. The 4K-entry VLAN Table designed into the RTL86907 provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

12.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL86907 supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL86907 uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL86907 compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is

reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL86907 performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL86907 performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL86907. One is the 'VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

12.12.3. Protocol-Based VLAN

The RTL86907 supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 17. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be 'Ethernet', and value to be '0x0800'. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

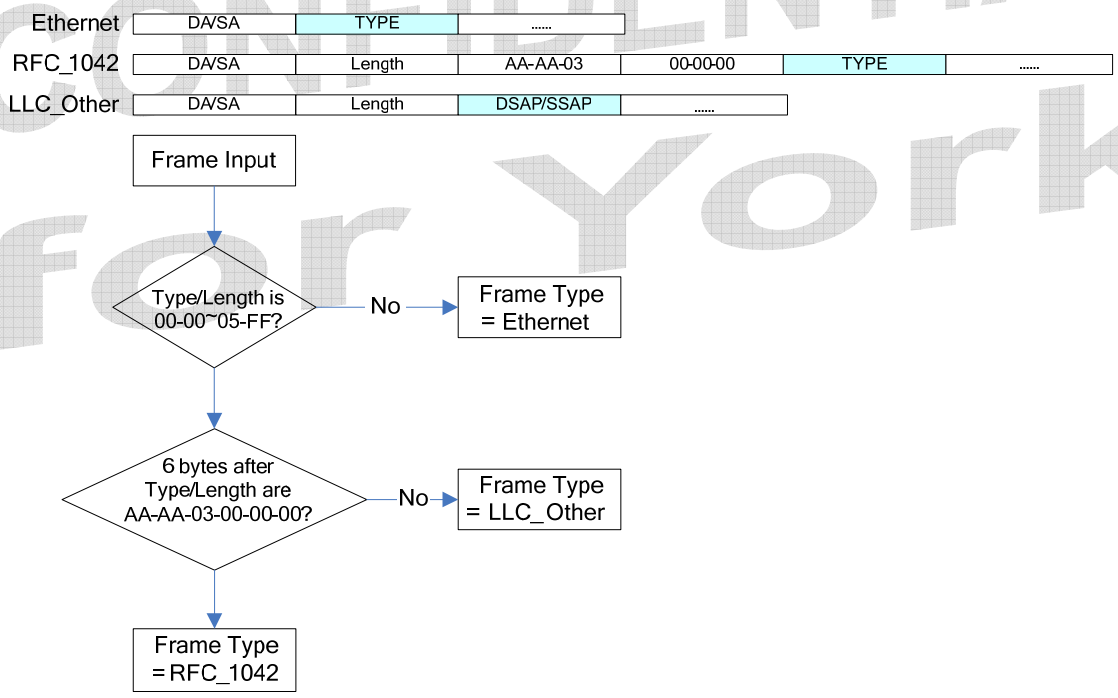


Figure 17. Protocol-Based VLAN Frame Format and Flow Chart

12.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL86907 supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL86907 will drop non-tagged packets and packets with an incorrect PVID.

12.13. QoS Function

The RTL86907 supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL86907, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

12.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

12.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL86907 can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL86907 identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

12.13.3. Priority Queue Scheduling

The RTL86907 supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- Average Packet Rate (APR) leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 18 shows the RTL86907 packet-scheduling diagram.

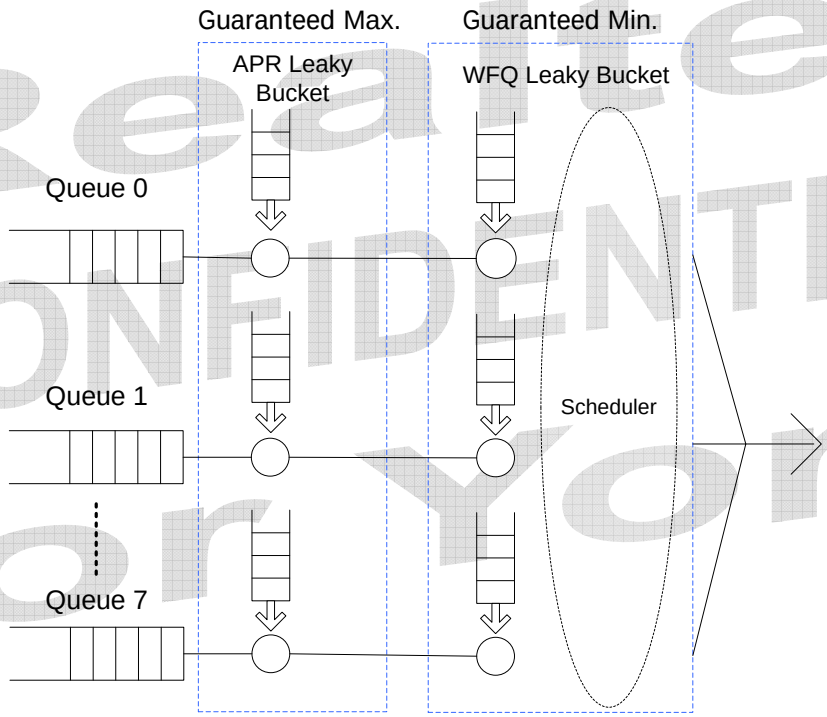


Figure 18. RTL86907 MAX-MIN Scheduling Diagram

12.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL86907 supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. Each output queue has a 3-bit 802.1p/Q, and a 6-bit IP DSCP value configuration register.

12.13.5. ACL-Based Priority

The RTL86907 supports 64-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

12.14. IEEE 802.1x Function

The RTL86907 supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior
- Guest VLAN

12.14.1. Port-Based Access Control

Each port of the RTL86907 can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

12.14.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

12.14.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

12.14.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

12.14.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction should be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

12.14.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

12.14.7. Guest VLAN

When the RTL86907 enables the Port-based or MAC-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, the RTL86907 will drop all packets from this port.

The RTL86907 also supports one Guest VLAN to allow unauthorized ports or packets to be forwarded to a limited VLAN domain. The user can configure one VLAN ID and member set for these unauthorized packets.

12.15. IEEE 802.1D Function

When using IEEE 802.1D, the RTL86907 supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL86907 also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

12.16. Classification

The RTL86907 supports 512-entry classification rules. When a packet is received, its physical port, ether type, VLAN, IP ToS, GPON stream ID, and internal priority are recorded and compared to classification entries.

If a received packet matches valid entries, the actions of the first matched entry will be applied. The action can be devided to upstream action and downstream action. For upstream action, it includs:

- S-tag action
- C-tag action
- User priority action
- GPON stream ID action
- DSCP remarking
- DROP action
- LOG action

For downstream action, it includes:

- S-tag action
- C-tag action
- User priority action
- Forwarding port mask
- DSCP remarking

12.17. Realtek Cable Test (RTCT)

The RTL86907 physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair.

12.18. LED Indicator

The RTL86907 supports parallel LED mode and serial LED mode. Eash LED can be configured for indicate any port, and compose the following basic elements (defined in Table 35) to archieve indicator information. for example: Indicator "Link", select "Spd1000", "Spd100", "Spd10"; Indicator "Link/Act", select "Spd1000", "Spd100", "Spd10","Spd1000 Act", "Spd100 Act", "Spd10 Act";

Table 35. LED Basic Elements

LED Statuses	Description
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Dup	Duplex Indicator. Low for full duplex, and high for half duplex mode.
Spd1000 Act	1000Mbps Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 Act	100Mbps Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10 Act	10Mbps Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Col	Collision Indicator. Blinking when collision occurs.

12.18.1. Parallel LED Indicator

The RTL86907 supports 14 parallel LEDs. Refer to section 7.5 Parallel LED Pins, page 19 for pin details.

Some of the LED pin also supports pin strapping configuration functions. Those LED pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is pulled high upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. For details refer to Figure 19, page 60, and Figure 20, page 60. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The LED pins also can be configurged as a Bi-color LED. But not any two LED pins can be connected as Bi-color mode, because one Bi-color LED pin should operate with the same polarity as other Bi-color LED pins. Two LED pins with strapping function are not recommended to connect as Bi-color mode, because two strapping pins are possible to configure with difference polarity.

For example:

- LED12 should pull up upon reset if LED12 is combined with LED13 as a Bi-color LED, and LED13 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- LED7 should pull down upon reset if LED7 is combined with LED6 as a Bi-color LED, and LED6 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

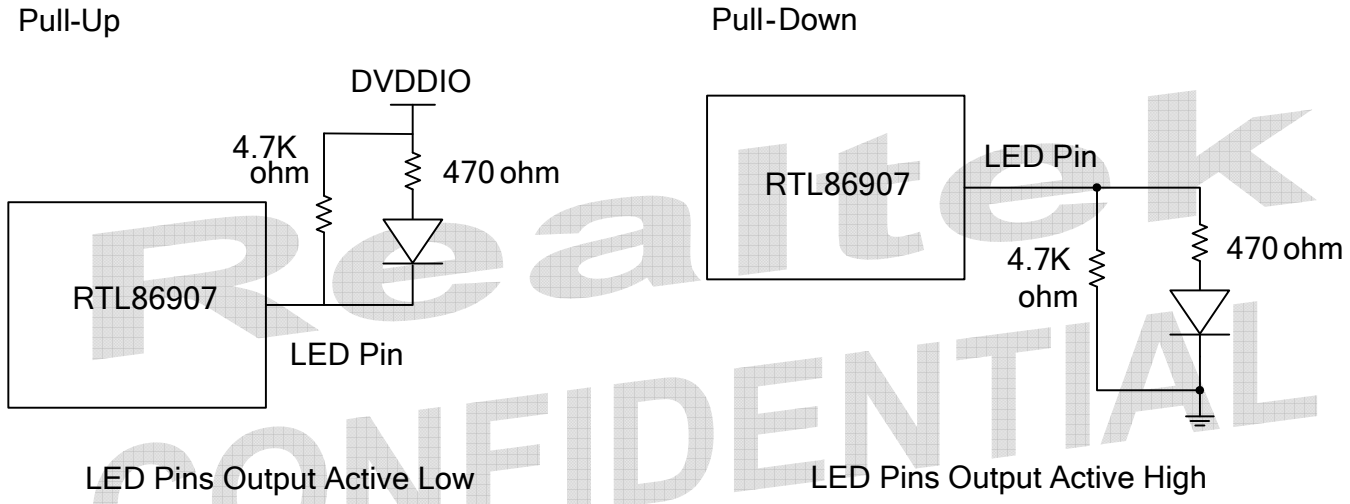


Figure 19. Pull-Up and Pull-Down of LED Pins for Single-Color LED

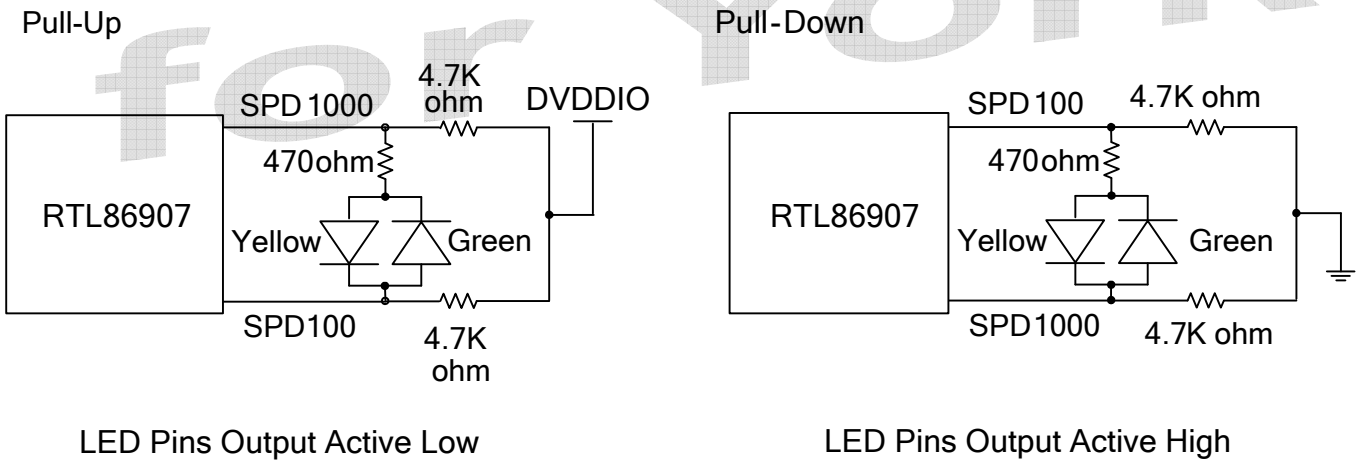


Figure 20. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

12.18.2. Serial LED Indicator

The RTL86907 also supports 32 serial LEDs. The serial LED mode use 2 pins SLED_CK/SLED_DA to connect a shift logic circuit, ex:RTL8231 or 74164. the output sequence as show in Figure 21. Refer to section 7.6 Serial LED Pins, page 20 for pin details.

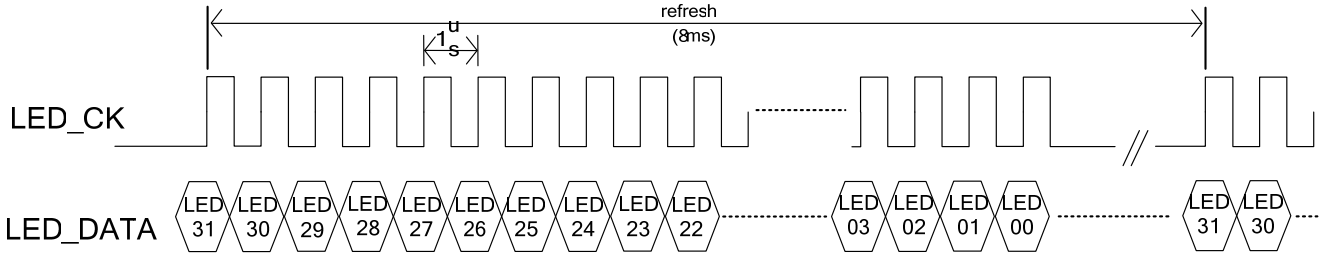


Figure 21. Serial LED output signal

12.19. Green Ethernet

12.19.1. Link-On and Cable Length Power Saving

The RTL86907 provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

12.19.2. Link-Down Power Saving

The RTL86907 implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

12.20. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL86907 support IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL86907 MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

12.21. L34 Function

The RTL86907 support the HW acceleration ability for L3/L4 traffic with IPv4 and IPv6 packets. It includes:

- L3 Routing for IPv4 and IPv6
- L4 NAT/NATR for IPv4
- L4 NAPT/NAPTR for IPv4 and support NAPT type as below:
- Full cone NAPT

- Restrict cone NAPT
- Port Restrict cone NATP
- WAN and Port Binding function
- Traffic indicator for againg time out
- PPPoE interface and pass through

Below show the supported entry number on each table for L34 function.

Table Name	Description	Entry no
NETIF	Network interface table	8
EXTERNAL_IP	External IP table	8
L3_ROUTING	L3 Routing Table	8
ARP	ARP Table	512
NEXT_HOP	Next Hop Table	16
PPPoE	PPPoE Table	8
NAPT	NAPT Table	2K
NAPTR	NAPTR Table	1K
IPV6_ROUTING	Routing Table for IPv6	4
IPV6_NEIGHBOR	Neighbor Table for IPv6	128
BINDING	Binding Table	32
WAN TYPE	WAN Type Table for binding	8

13. DC Specifications

13.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 36. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, AVDDH, SVDDH, USBVDDH Supply Referenced to GND and AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1, SVDDL, USBVDDL, Supply Referenced to GND, AGND.	GND-0.3	+1.1	V
OVDDDR Supply Referenced to GND, AGND.	GND-0.3	+2.75	V
Digital Input Voltage	GND-0.3	DVDDIO+0.3	V

13.2. Operating Conditions

Table 37. Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
Ta	Ambient Operating Temperature	0	-	70	°C
DVDDIO	Digital I/O High Voltage Power	3.135	3.3	3.465	V
DVDDL	Digital Low Voltage Power.	0.95	1.0	1.05	V
AVDDH	Analog High Voltage Power.	3.135	3.3	3.465	V
AVDDL	Analog Low Voltage Power.	0.95	1.0	1.05	V
PLLVDDL0	PLL0 Low Voltage Power.	0.95	1.0	1.05	V
PLLVDDL1	PLL1 Low Voltage Power.	0.95	1.0	1.05	V
DVDDIO_EXT	Extension Interface I/O Power Supply For Power Supply 3.3V For Power Supply 2.5V.	 3.135 2.4	 3.3 2.5	 3.465 2.7	V
PCIEVDDL	PCI Express Analog Low Voltage Power.	0.95	1.0	1.05	V
SVDDH	SerDes Analog High Voltage Power.	3.135	3.3	3.465	V
SVDDL	SerDes Analog Low Voltage Power.	0.95	1.0	1.05	V
USBVDDH	Analog High Voltage Power.	3.135	3.3	3.465	V
USBVDDL	Analog Low Voltage Power.	0.95	1.0	1.05	V
OVDDDR	DDR SDRAM I/O Power Supply DDR1 SDRAM I/O Power Supply 2.5V DDR2 SDRAM I/O Power Supply 1.8V DDR3 SDRAM I/O Power Supply 1.5V	 2.4 1.7 TBD	 2.5 1.8 1.5	 2.7 1.9 TBD	V
MVREF	DDR1/DDR2/DDR3 Reference Voltage	0.49* OVDDDR	0.5* OVDDDR	0.51* OVDDDR	V

13.3. Total Power Consumption

Table 38. Total Power Consumption

SYM	Conditions	Min	Typ.	Max	Units
PS	All LAN Ports Idle and CPU Suspended	-	TBD	-	Watt
	All LAN Ports Idle	-	TBD	-	
	LAN Full Load Active for Link at 10Base-T	-	TBD	-	
	LAN Full Load Active for Link at 100Base-TX	-	TBD	-	
	LAN Full Load Active for Link at 1000Base-TX	-	TBD	-	

Note: Power consumption is measured at full load of the chip system.

13.4. DDR SDRAM Bus DC Parameters

Table 39. DDR SDRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	SSTL_2	MVREF+0.15	-	MVREF+0.3	V
V_{IL}	Input-Low Voltage	SSTL_2	-0.3	-	MVREF-0.15	V
V_{TT}	I/O Termination Voltage	-	MVREF-0.04	-	MVREF+0.04	V
I_{IL}	Input-Leakage Current	V_{IN}=MVREF or 0	-10	±1	10	µA
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA

13.5. Flash Bus DC Parameters

Table 40. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshot: VIH (MAX)=VDDH + 2V for a pulse width ≤ 3ns.

Note 2: V_{IL} undershot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤ 3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

13.6. USB v1.1 DC Parameters

Table 41. USB v1.1 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	2.0	-	-	V	2
V_{IL}	Input-Low Voltage	-	-	-	0.8	V	2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{OH}	Output-High Voltage	-	2.4	-	-	V	2
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	2
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.
Note 2: For additional information, see the USB v1.1 Specification.

13.7. USB v2.0 DC Parameters

Table 42. USB v2.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	200	-	-	mV	2
V_{IL}	Input-Low Voltage	-	-	-	10	mV	2
V_{OH}	Output-High Voltage	-	300	-	500	mV	2
V_{OL}	Output-Low Voltage	-	-10	-	10	mV	2
I_{IL}	Input-Leakage Current	-	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.
Note 2: For additional information, see the USB v2.0 Specification.

13.8. UART DC Parameters

Table 43. UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for UART related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.9. GPIO DC Parameters

Table 44. GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GPIO related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.10. JTAG DC Parameters

Table 45. JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	$\|I_{OH}\|$=2~16mA	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	$\|I_{OL}\|$=2~16mA	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 4mA for JTAG related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.11. MII, TMII and RMII DC Parameters

Table 46. MII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for MII related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.12. RGMII DC Parameters

Table 47. RGMII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	3.3V/2.5V	2.0/1.7	-	-	V	-
V_{IL}	Input-Low Voltage	3.3V/2.5V	-	-	0.8/0.7	V	-
V_{OH}	Output-High Voltage	3.3V/2.5V	2.4/2.0	-	-	V	1
V_{OL}	Output-Low Voltage	3.3V/2.5V	-	-	0.4/0.4	V	1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for RGMII related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.13. PON SerDes DC Parameters

Table 48. Reset DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	

13.14. Reset DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V

13.15. LED DC Parameters

Table 49. LED DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OHED}	Output-High Voltage	-	2.4	-	-	V
V_{OLLED}	Output-Low Voltage	-	-	-	0.4	V

Note: The output current buffer for LED signals is 8mA.

14. AC Specifications

14.1. Clock Signal Timing

14.1.1. 25MHz System Clock Timing

Table 50. 25MHz System Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	-	-	0.8	V	-
$T_{FREQUENCY}$	Clock Frequency for RTL86907 Crystal or Oscillator	-	25	-	MHz	1

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$\Delta_{FREQUENCY}$	Clock Tolerance Over 0ºC to 50ºC	-50	-	50	ppm	-
C_{SHUNT}	Crystal Parameter (Sometimes Referred to as the Holder Capacitance)	-	-	7	pF	-
C_1	Load Capacitance	-	-	TBD	pF	2
C_2	Load Capacitance	-	-	TBD	pF	2
T_{DC}	Duty Cycle	-	50	-	%	-

Note 1: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.

Note 2: The RTL86907 PLL circuit requires an external 25MHz crystal with shunt capacitors. These shunt capacitors cannot be over 30pF due to chip design requirements.

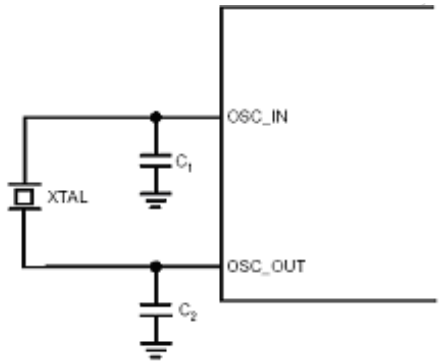


Figure 22. Typical Connection to a Crystal

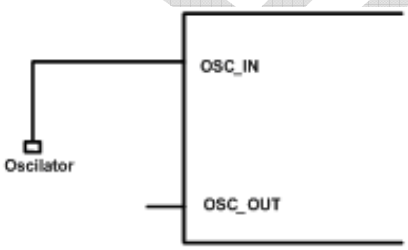


Figure 23. Typical Connection to an Oscillator

14.2. Bus Signal Timing

14.2.1. DDR SDRAM Bus

14.2.1.1 DDR SDRAM Input Timing

Table 51. DDR SDRAM Input Timing

Symbol	Parameter	Units	Notes
T_{SETUP}	Input Setup Prior to Rising Edge of Clock. Inputs included in this timing are D[31: 0] (during a read operation)	ns	1

Symbol	Parameter	Units	Notes
T_{HOLD}	Input Hold Time after the Rising Edge of Clock. Inputs included in this timing are D[31:0] (during a read operation)	ns	1

Note1: The RTL86907 integrates some timing control registers on the interface.

14.2.1.2 DDR SDRAM Output Timing

Table 52. DDR SDRAM Output Timing

Symbol	Parameter	Units	Notes
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output. Outputs include this timing are D[31: 0], CS0#, CS1#, RAS#, CAS#, LDQM, UDQM, WE#, LDQS, UDQS (during a write operation)	ns	1
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock. Outputs included in this timing are D[31: 0] (during a write operation)	ns	1

Note1: The RTL86907 integrates some timing control registers on the interface.

14.2.1.3 DDR SDRAM Access Control Timing

Table 53. DDR SDRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing. Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active. Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

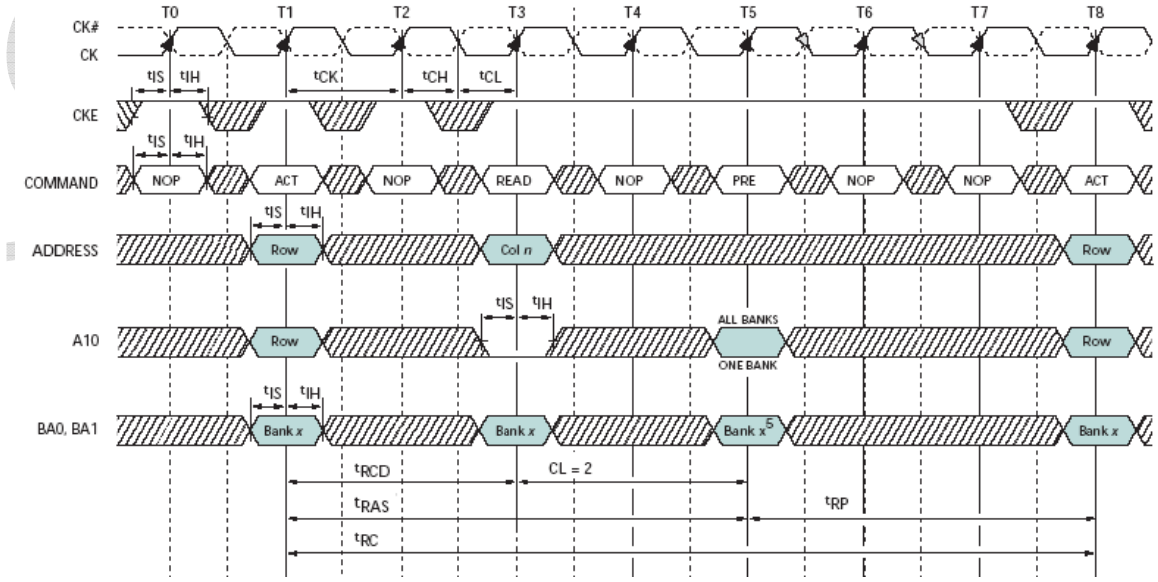


Figure 24. DDR SDRAM Access Control Timing

14.2.2. Serial Flash Interface

14.2.2.1 Serial Flash Interface Output Timing

Table 54. Serial Flash Interface Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SLCH}	The Timing Interval from Chip-Select Activated to the First Clock Rising Edge	$0.5*T_{SFCK}$ - 1	-	$0.5*T_{SFCK}$	ns
T_{CHSH}	The Timing Interval from the Last Clock Rising Edge to Chip-Select De-Activated	T_{SFCK} + 7	-	T_{SFCK} + 9	ns
T_{CLQV}	The Timing Interval from the Last Clock Falling Edge to Data-Out Validated	-	-	1	ns
T_{CLQX}	The Timing Interval from the Next Clock Falling Edge to Data-Out Invalidated	-1	-	-	ns

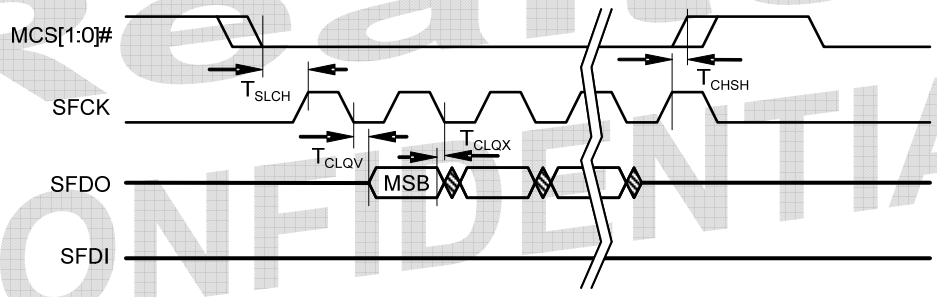


Figure 25. Serial Flash Interface Output Timing

14.2.2.2 Serial Flash Interface Intput Timing

Table 55. Serial Flash Interface Intput Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{DVCH}	The Timing Interval from Data-Input Ready to the Clock Rising Edge	0	-	-	ns
T_{CHDX}	The Timing Interval from the Clock Rising Edge to Data-Input Invalidated	$0.5*T_{SFCK}$	-	-	ns

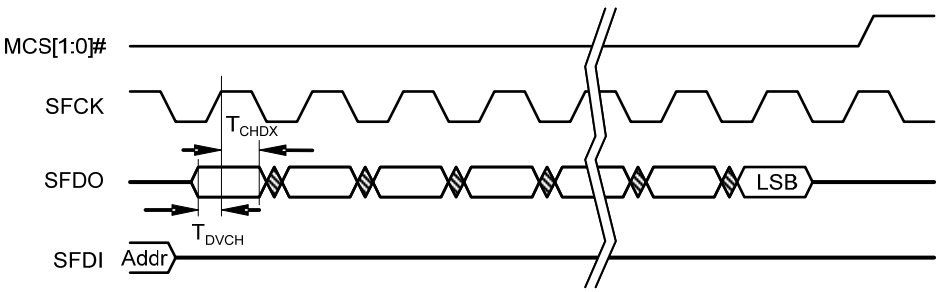


Figure 26. Serial Flash Interface Intput Timing

14.2.3. JTAG Boundary Scan

Table 56. JTAG Boundary Scan Interface Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{bscl}	JTAG Clock Low Time	50	-	-	ns	1
T_{bsch}	JTAG Clock High Time	50	-	-	ns	1
T_{bsis}	TDI, TMS Setup Time to Rising Edge of TCK	10	-	-	ns	-
T_{bsih}	TDI, TMS Hold Time from Rising Edge of TCK	10	-	-	ns	-
T_{bsoh}	TDO Hold Time after Falling Edge of TCK	1.5	-	-	ns	-
T_{bsod}	TDO Output from Falling Edge of TCK	-	-	40	ns	-
T_{bsr}	JTAG Reset Period	30	-	-	ns	-
T_{bsrs}	TMS Setup Time to Rising Edge of JTAG Reset	10	-	-	ns	-
T_{bsrh}	TMS Hold Time from Rising Edge of JTAG Reset	10	-	-	ns	-

Note 1: JTAG clock TCK may be stopped indefinitely in either the low or high phase.

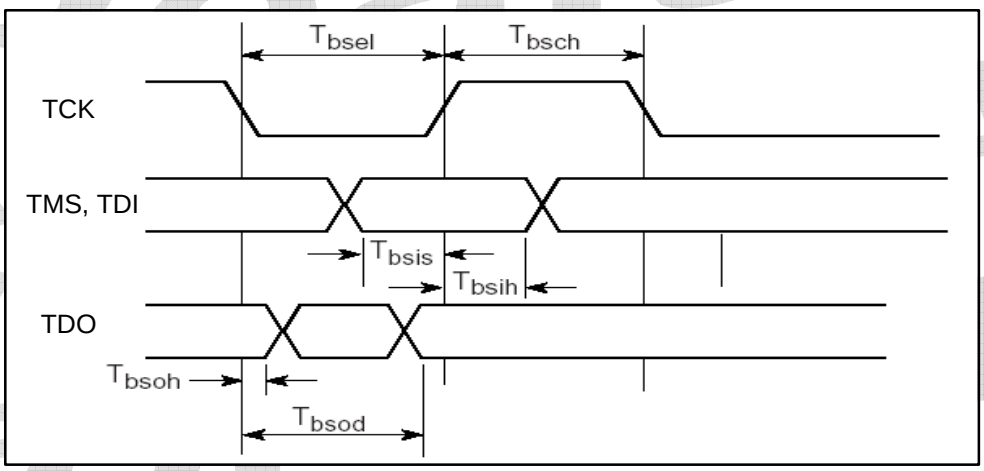


Figure 27. Boundary-Scan General Timing

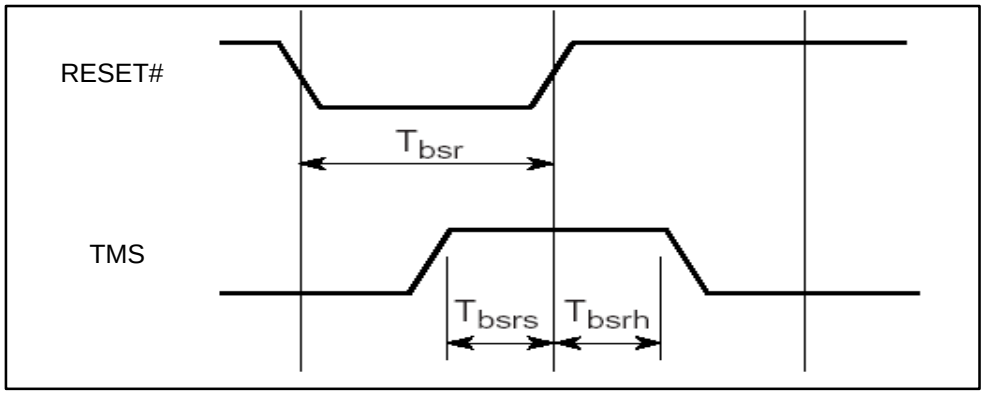


Figure 28. Boundary-Scan Reset Timing

14.2.4. MII MAC Mode Timing

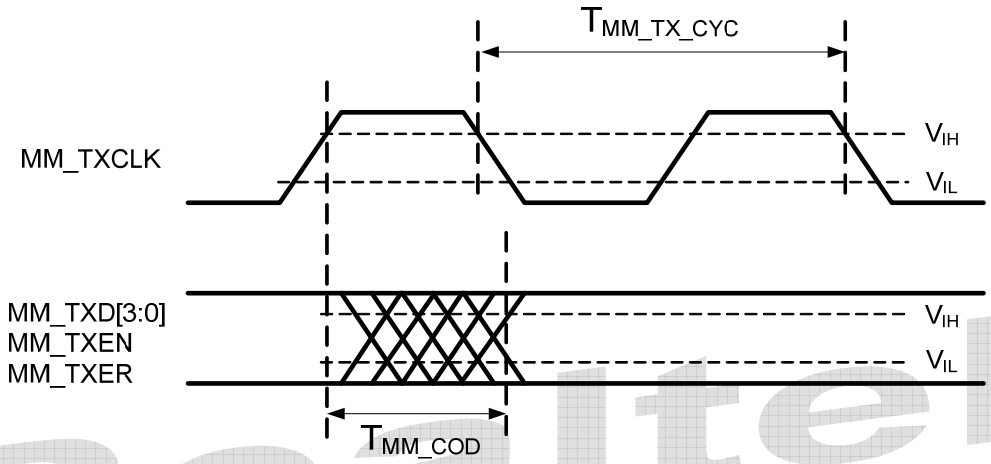


Figure 29. MII MAC Mode Clock to Data Output Delay Timing

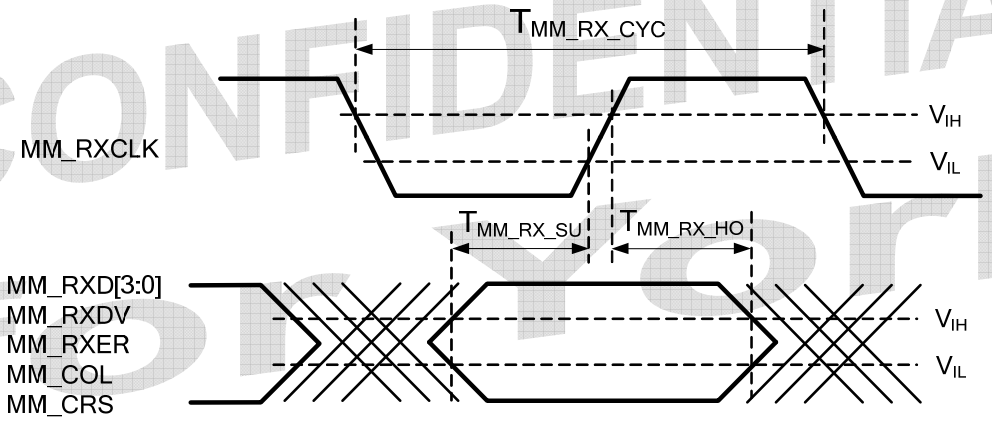


Figure 30. MII MAC Mode Input Timing

Table 57. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-T MM_TXCLK and MM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	25MHz Clock Input.	I	-	40	-	ns
10Base-T MM_TXCLK and MM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz Clock Input.	I	-	400	-	ns
MM_TXCLK to MM_TXD[3:0], MM_TXEN, and MM_TXER Output Delay Time	T_{MM_COD}	-	O	-	TBD	-	ns
MM_RXD[3:0], MM_RXDV, MM_RXER, MM_COL, and MM_CRS Input Setup Time	$T_{MM\_RX\_SU}$	-	I	10	-	-	ns

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MM_RXD[3:0], MM_RXDV, MM_RXER, MM_COL, and MM_CRS Input Hold Time	$T_{MM\_RX\_HO}$	-	I	10	-	-	ns

14.2.5. TMII MAC Mode Timing

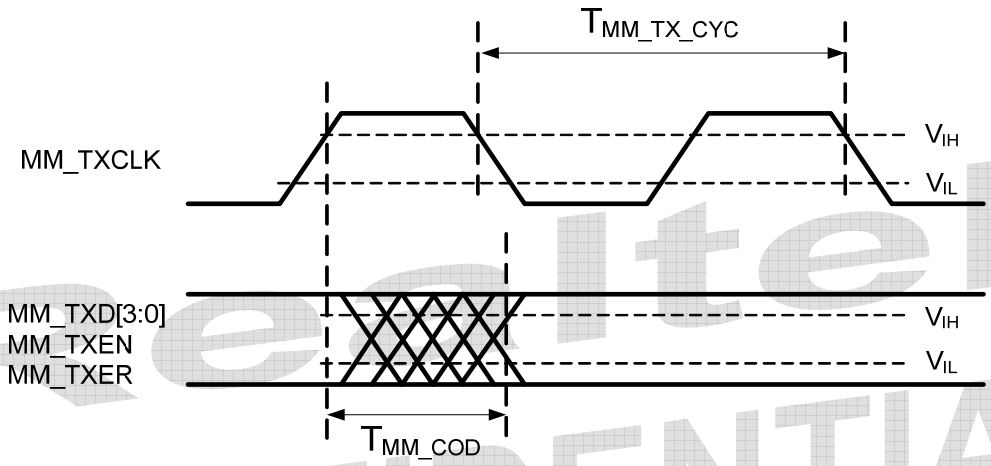


Figure 31. TMII MAC Mode Clock to Data Output Delay Timing

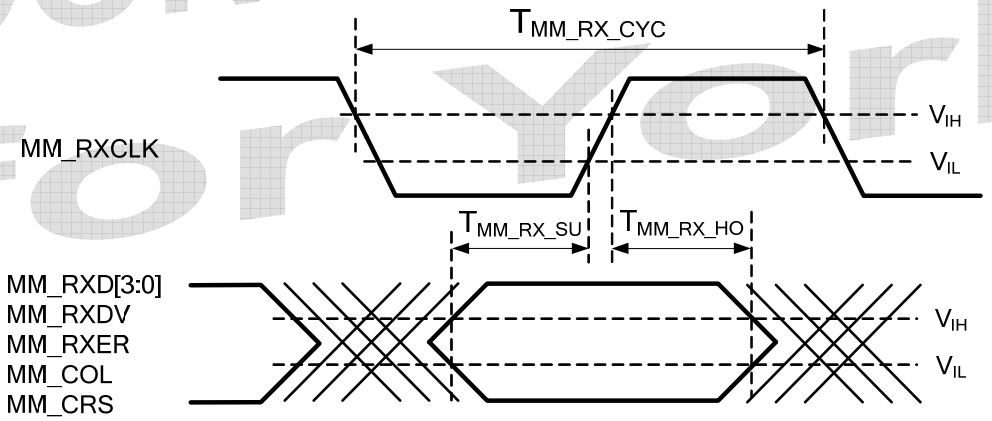


Figure 32. TMII MAC Mode Input Timing

Table 58. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-T MM_TXCLK and MM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	25MHz Clock Input.	I	-	20	-	ns
10Base-T MM_TXCLK and MM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz Clock Input.	I	-	200	-	ns

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MM_TXCLK to MM_TXD[3:0], MM_TXEN, and MM_TXER Output Delay Time	T_{MM_COD}	-	O	-	TBD	-	ns
MM_RXD[3:0], MM_RXDV, MM_RXER, MM_COL, and MM_CRS Input Setup Time	$T_{MM\_RX\_SU}$	-	I	5	-	-	ns
MM_RXD[3:0], MM_RXDV, MM_RXER, MM_COL, and MM_CRS Input Hold Time	$T_{MM\_RX\_HO}$	-	I	5	-	-	ns

14.2.6. MII PHY Mode Timing

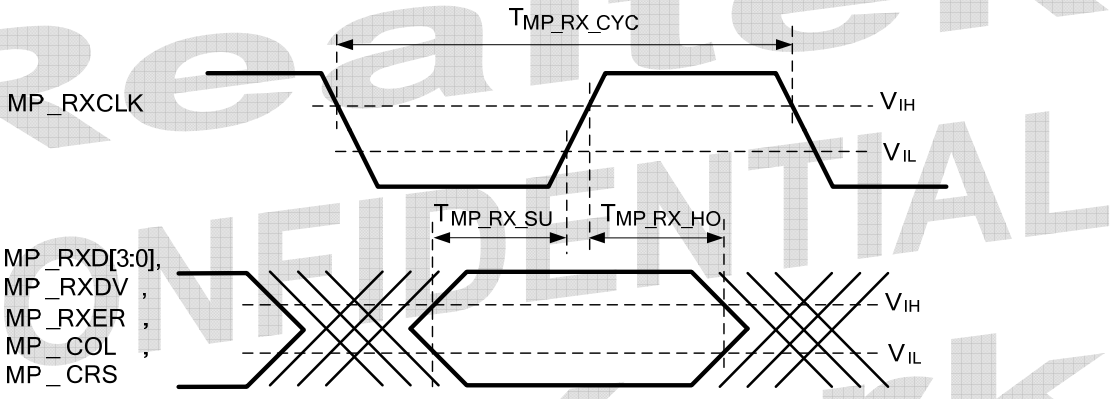


Figure 33. MII PHY Mode Output Timing

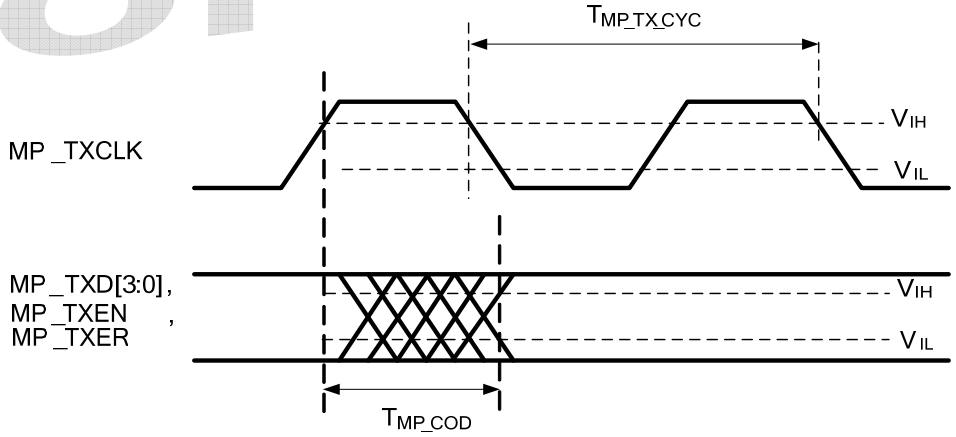


Figure 34. MII PHY Mode Clock Output to Data Input Delay Timing

Table 59. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MP_RXCLK and MP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10M MP_RXCLK and MP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns
100M MP_RXD[3:0], MP_RXDV, MP_RXER, MP_COL, and MP_CRS to MP_RXCLK Output Setup Time	$T_{MP\_RX\_SU}$	-	O	-	TBD	-	ns
100M MP_RXD[3:0], MP_RXDV, MP_RXER, MP_COL, and MP_CRS to MP_RXCLK Output Hold Time	$T_{MP\_RX\_HO}$	-	O	-	TBD	-	ns
100M MP_TXCLK Clock Output to MP_TXD[3:0], MP_TXEN and MP_TXER Input Delay Time	T_{MP_COD}	-	I	0	-	25	ns

14.2.7. TMII PHY Mode Timing

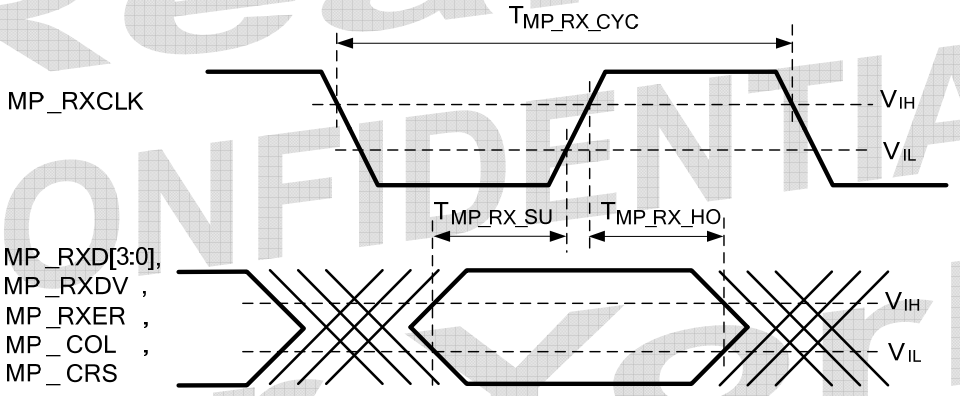


Figure 35. TMII PHY Mode Output Timing

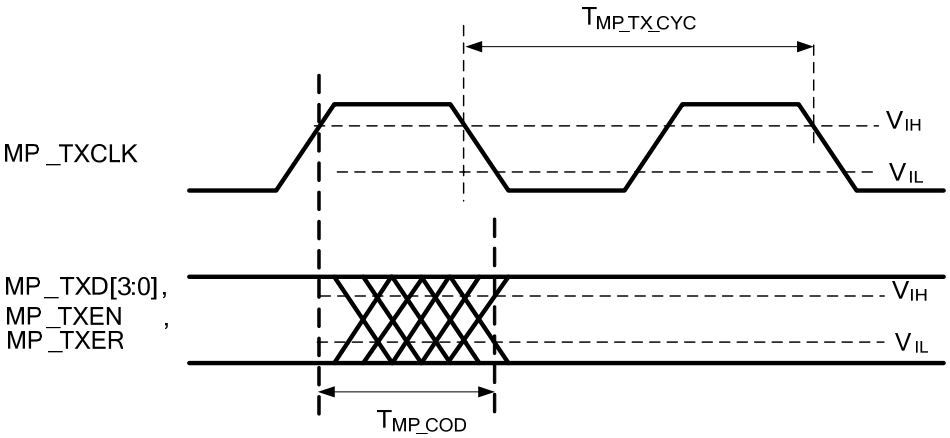


Figure 36. TMII PHY Mode Clock Output to Data Input Delay Timing

Table 60. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MP_RXCLK and MP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10M MP_RXCLK and MP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns
100M MP_RXD[3:0], MP_RXDV, MP_RXER, MP_COL, and MP_CRS to MP_RXCLK Output Setup Time	$T_{MP\_RX\_SU}$	-	O	-	TBD	-	ns
100M MP_RXD[3:0], MP_RXDV, MP_RXER, MP_COL, and MP_CRS to MP_RXCLK Output Hold Time	$T_{MP\_RX\_HO}$	-	O	-	TBD	-	ns
100M MP_TXCLK Clock Output to MP_TXD[3:0], MP_TXEN and MP_TXER Input Delay Time	T_{MP_COD}	-	I	0	-	25	ns

14.2.8. RGMII Timing Characteristics

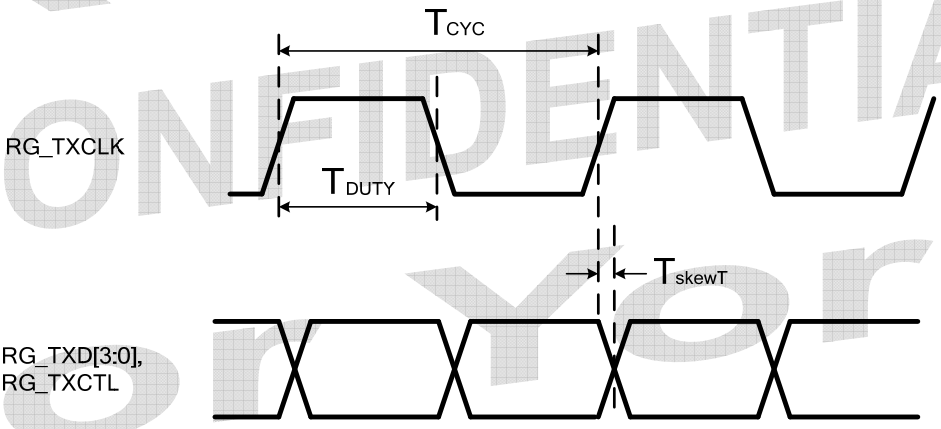


Figure 37. RGMII Output Timing Characteristics (RG_TXCLK_DELAY=0)

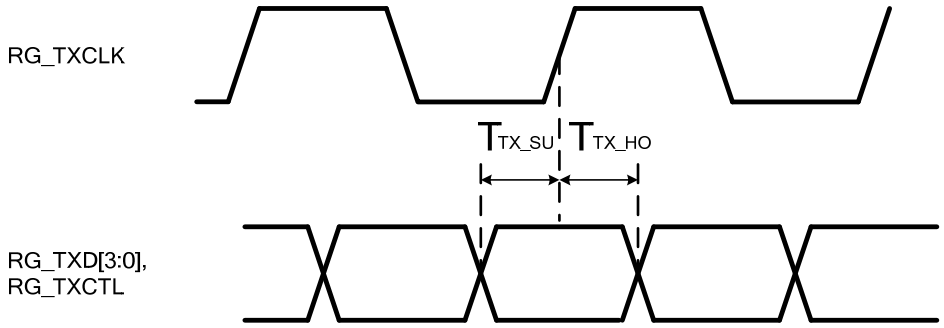


Figure 38. RGMII Output Timing Characteristics (RG_TXCLK_DELAY=2ns)

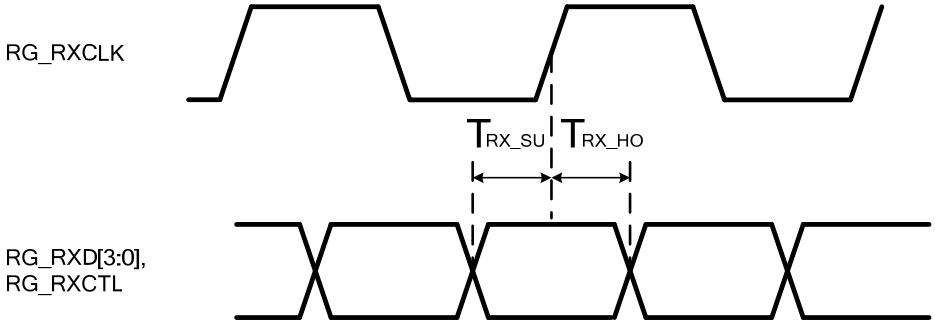


Figure 39. RGMII Input Timing Characteristics (RG_RXCLK_DELAY=0)

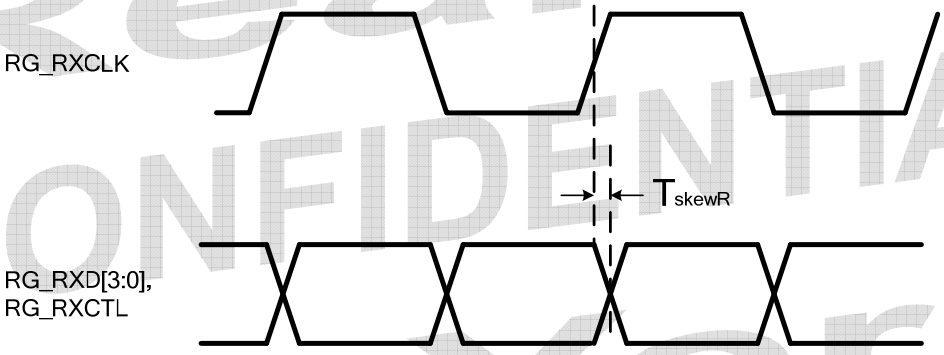


Figure 40. RGMII Input Timing Characteristics (RG_RXCLK_DELAY=2ns)

Table 61. RGMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000M RG_TXCLKc Output Cycle Time	T_{TX_CYC}	125MHz Clock Output. Refer to Figure 37, page 78.	O	TBD	8	TBD	ns
100M RG_TXCLK Output Cycle Time	T_{TX_CYC}	25MHz Clock Output. Refer to Figure 37, page 78.	O	TBD	40	TBD	ns
10M RG_TXCLK Output Cycle Time	T_{TX_CYC}	2.5MHz Clock Output. Refer to Figure 37, page 78.	O	TBD	400	TBD	ns
RG_TXD[3:0] and RG_TXCTL to RG_TXCLK Output Skew	T_{skewT}	Disable Output Clock Delay. (RG_TXCLK_DELAY=0). Refer to Figure 37, page 78.	O	TBD	TBD	TBD	ps
RG_TXD[3:0] and RG_TXCTL to RG_TXCLK Output Setup Time	T_{TX_SU}	Enable Output Clock Delay. (RG_TXCLK_DELAY=1). Refer to Figure 38, page 78.	O	TBD	TBD	-	ns

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
RG_TXD[3:0] and RG_TXCTL to RG_TXCLK Output Hold Time	T_{TX_HO}	Enable Output Clock Delay. (RG_TXCLK_DELAY=1). Refer to Figure 38, page 78.	O	TBD	TBD	-	ns
RG_RXD[3:0] and RG_RXCTL to RG_RXCLK Input Setup Time	T_{RX_SU}	Disable Input Clock Delay. (RG_RXCLK_DELAY=0). Refer to Figure 39, page 79.	I	TBD	-	-	ns
RG_RXD[3:0] and RG_RXCTL to RG_RXCLK Input Hold Time	T_{RX_HO}	Disable Input Clock Delay. (RG_RXCLK_DELAY=0). Refer to Figure 39, page 79.	I	TBD	-	-	ns
RG_RXD[3:0] and RG_RXCTL to RG_RXCLK Input Skew	T_{skewR}	Enable Input Clock Delay. (RG_RXCLK_DELAY=1). Refer to Figure 40, page 79.	I	TBD	-	TBD	ps

14.2.9. Power Sequence

Table 62. Power-Up Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	3.3V Stable to 1.0V	1	-	-	ms

Note 1: The 3.3V(I/O) must be powered up before 1.0V (core) and 1.0V (analog) voltage.

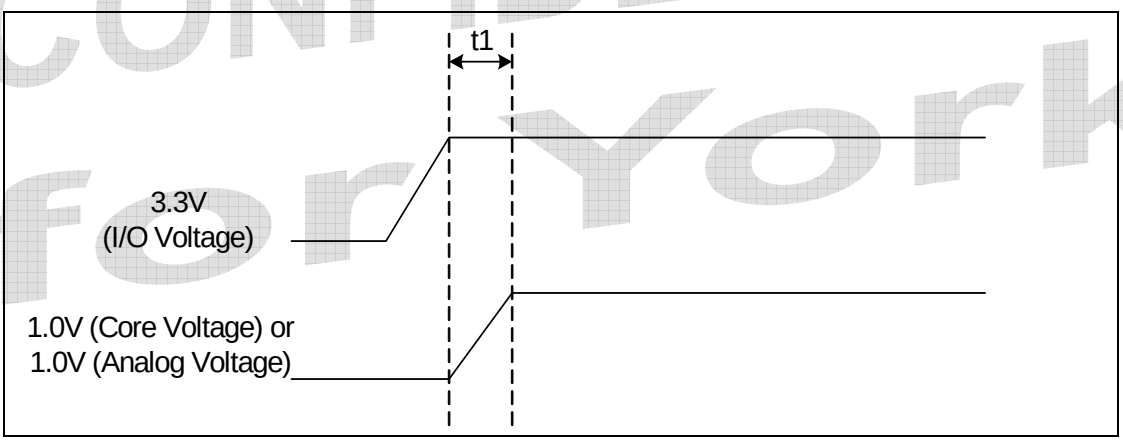


Figure 41. Power Up Sequence Timing Diagram

14.2.10. Power Configuration Timing

Power up configuration only relates to internal timing. The external hardware pin reset is unconcerned with power up configuration. The Hardware reset pin is valid when an internal reset ends the active state.

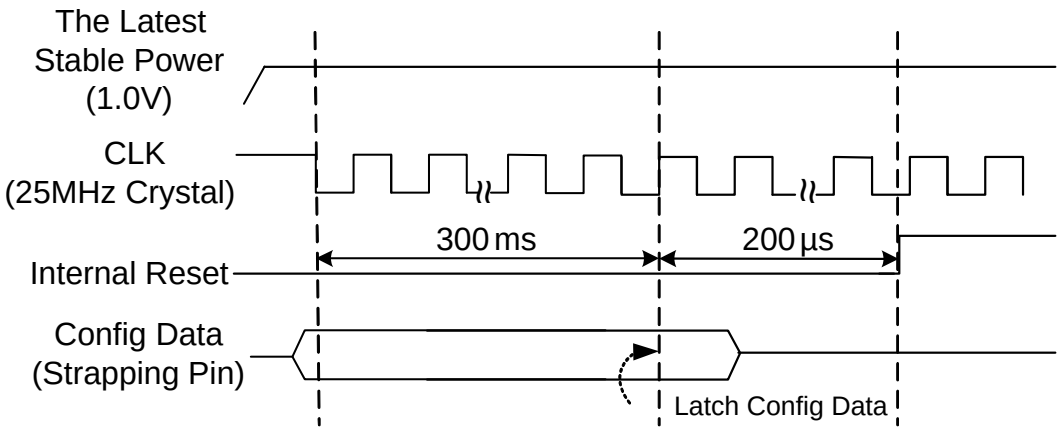


Figure 42. Power Up Configuration Timing

14.3. PCI Express Bus Parameters

14.3.1. Differential Transmitter Parameters

Table 63. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum Tx Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN- to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE- IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE- DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE- SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI

Symbol	Parameter	Min	Typical	Max	Units
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid Tx Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

14.3.2. Differential Receiver Parameters

Table 64. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

14.3.3. REFCLK Parameters

Table 65. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single-ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 46, page 85.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 43, page 84.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 43, page 84.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 45, page 84.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 43, page 84.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 43, page 84.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 43, page 84.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 49, page 86. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note12: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range. See Figure 48, page 86.

*Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 44, page 84.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

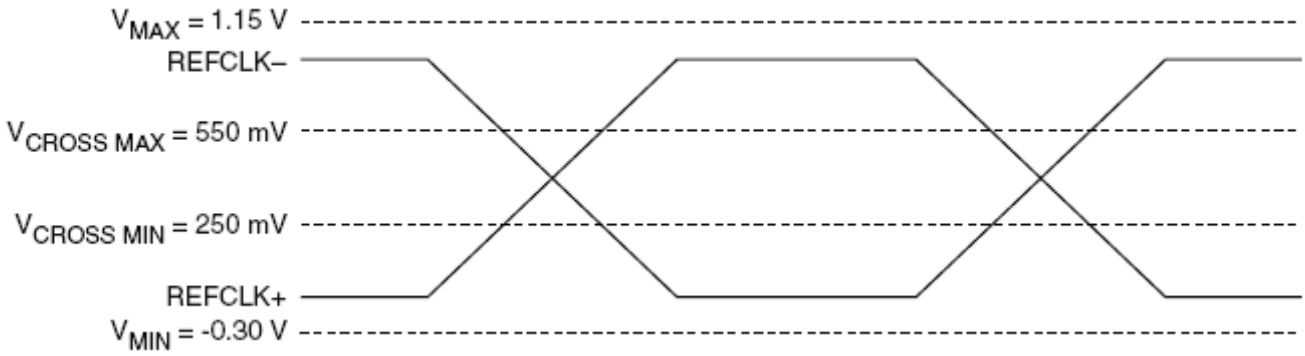


Figure 43. Single-Ended Measurement Points for Absolute Cross Point and Swing

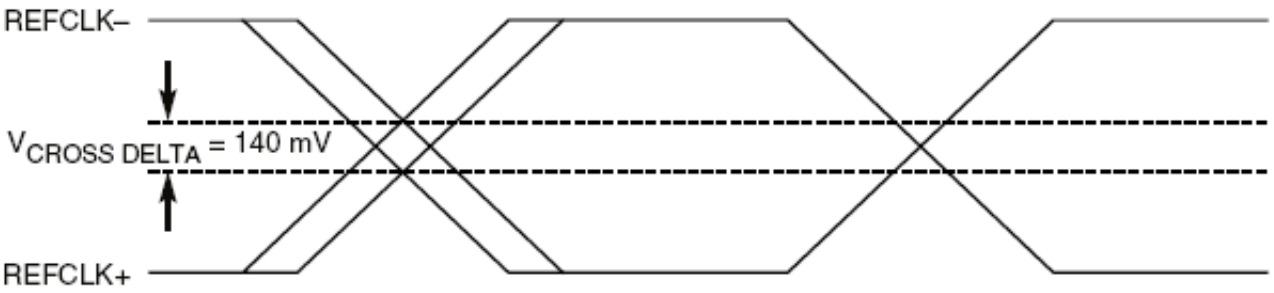


Figure 44. Single-Ended Measurement Points for Delta Cross Point

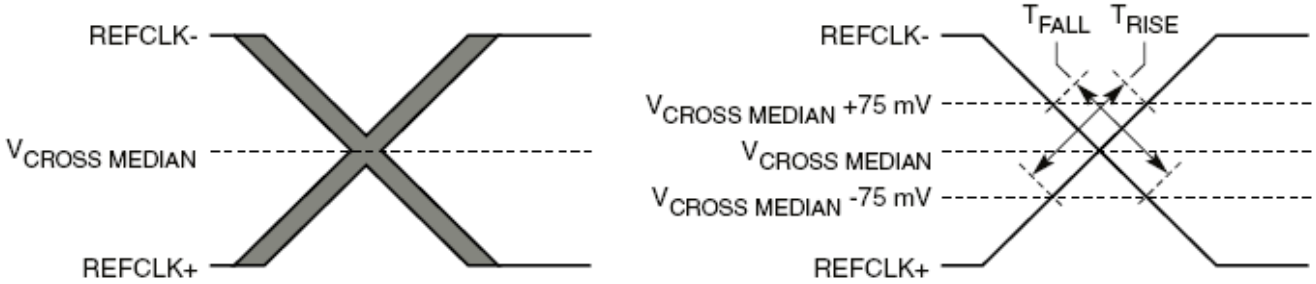


Figure 45. Single-Ended Measurement Points for Rise and Fall Time Matching

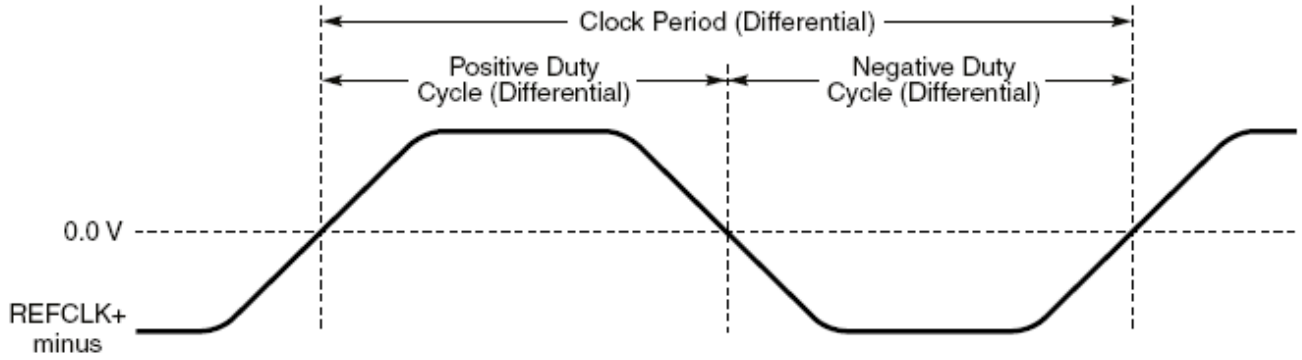


Figure 46. Differential Measurement Points for Duty Cycle and Period

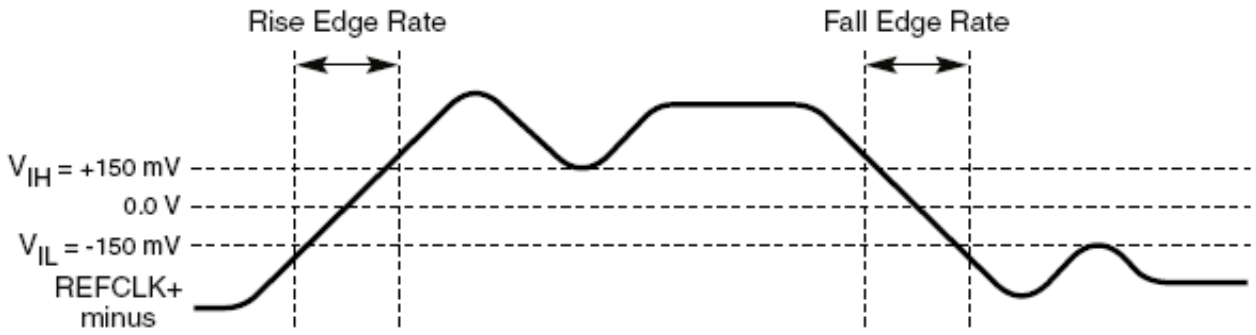


Figure 47. Differential Measurement Points for Rise and Fall Time

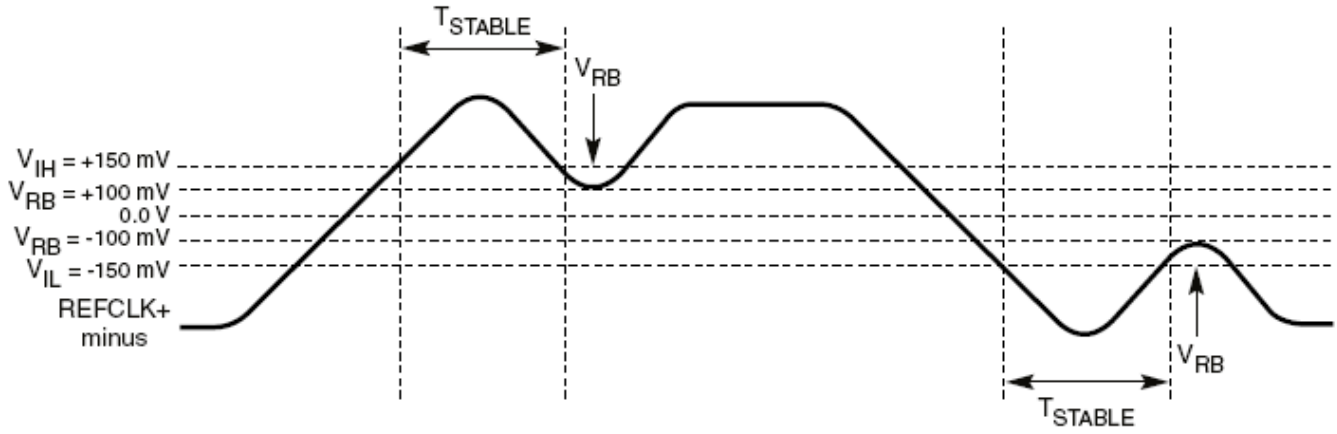


Figure 48. Differential Measurement Points for Ringback

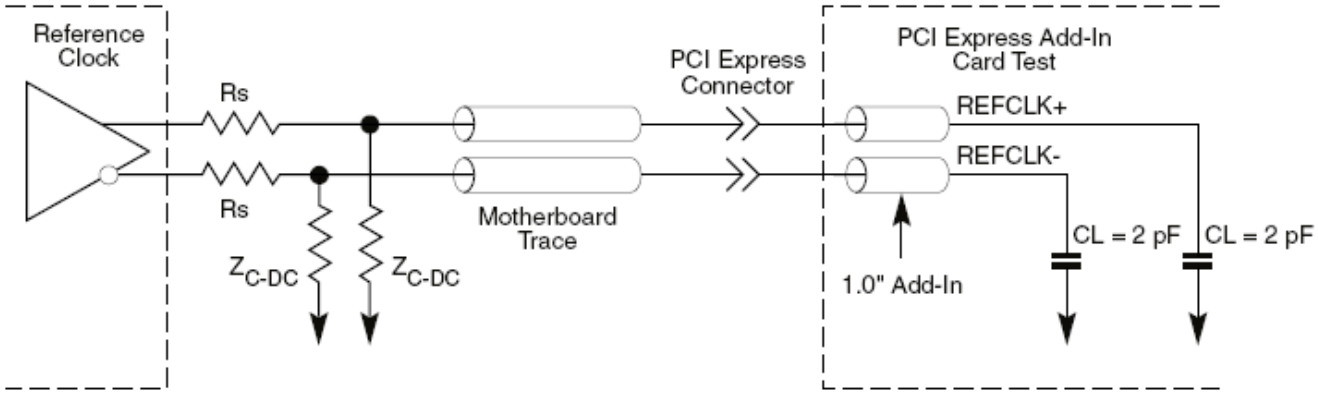


Figure 49. Reference Clock System Measurement Point and Loading

15. Thermal Characteristics

15.1. Assembly Description

Table 66. Assembly Description

	Type	**E-Pad LQFP-216**
Package	**Dimension (L x W)**	**24 x 24mm**
	Thickness	**1.4mm**
PCB	**PCB Dimension (L x W)**	**125 x 175mm2**
	PCB Thickness	**1.6mm**
	Number of Cu Layer-PCB	**2 layers (2S):** **-Top layer: 20% coverage of Cu** **-Bottom layer: 75% coverage of Cu**

15.2. Material Properties

Table 67. Material Properties

Item		**Material**	**Thermal Conductivity K (W/m-k)**
Package	Die	Si	147
	Silver Paste	1033BF	1.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.92
PCB		Cu	400
		FR4	0.2

15.3. Simulation Conditions

Table 68. Simulation Conditions

Input Power	**3.1 W**
Test Board (PCB)	**2L (2S)**
Control Condition	**Air Flow = 0, 1, 2, 3 m/s**

15.4. Thermal Performance of E-Pad LQFP-216 on PCB Under Still Air Convection

Table 69. Thermal Performance of E-Pad LQFP-216 on PCB Under Still Air Convection

	θ_{JA}	θ_{JB}	Ψ_{JT}
2L PCB	16.7	9.67	0.68

15.5. Thermal Performance of E-Pad LQFP-216 on PCB Under Forced Convection

Table 70. Thermal Performance of E-Pad LQFP-216 on PCB Under Forced Convection

	Air Flow (m/s)	0	1	2	3
4L PCB	θ_{JA}	17.3	13.9	12.9	12.2
	Ψ_{JT}	3.38	0.76	0.87	0.98

Note:

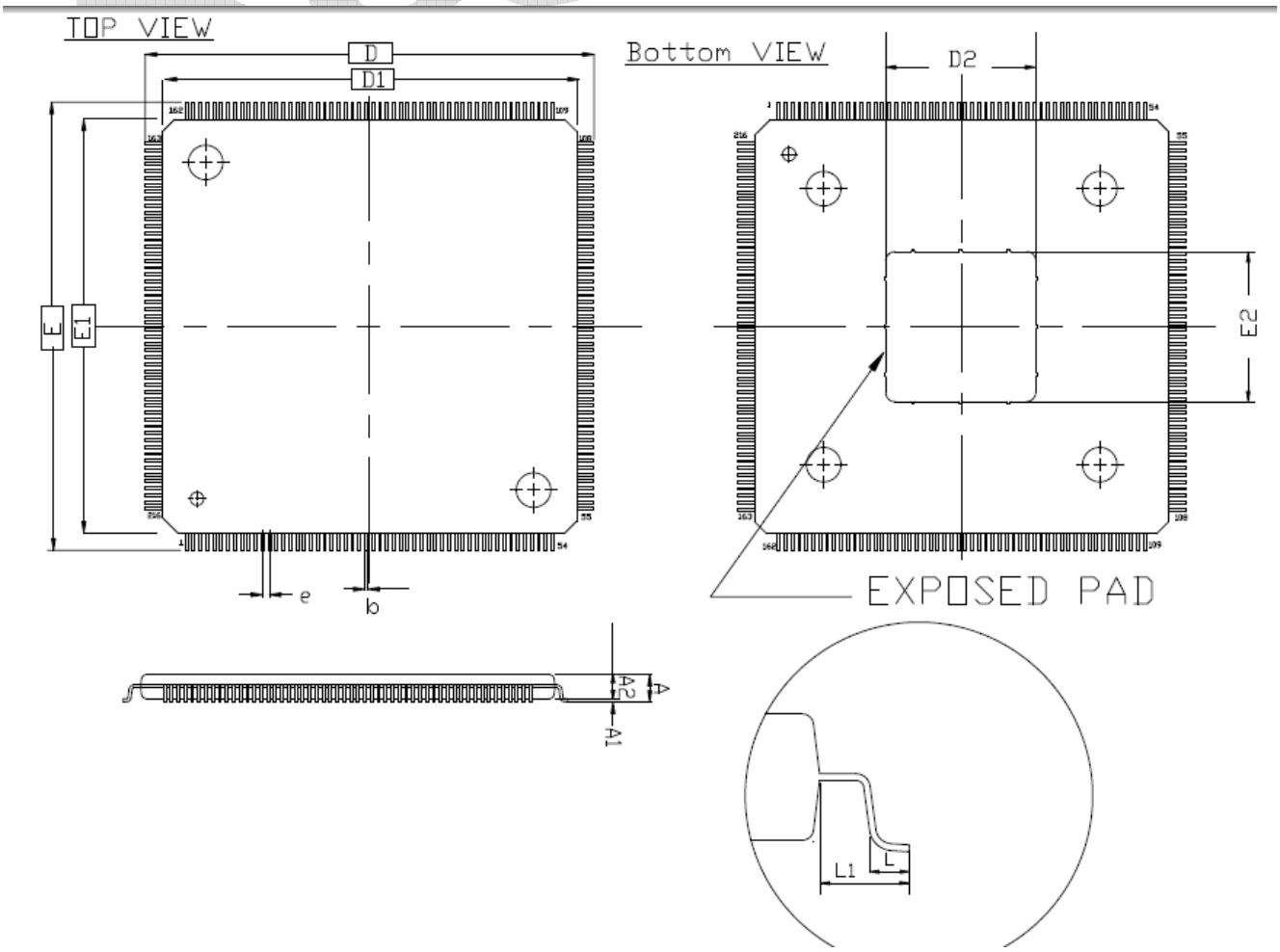
θ_{JA}: Junction to ambient thermal resistance

θ_{JB}: Junction to board thermal resistance

Ψ_{JT}: Junction to top center of package thermal characterization

16. Mechanical Dimensions

Low Profile Plastic Quad Flat Package 216 Leads 24x24mm^2 Outline.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
D/E	26.00 BSC			1.024 BSC		
D_1/E_1	24.00 BSC			0.945 BSC		
D_2/E_2	8.45	8.70	8.95	0.332	0.342	0.352
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MS-026.

17. Ordering Information

Table 71. Ordering Information

Part Number	Package	Status
RTL86907-CG	Low Profile Plastic Quad Flat Package 216-Lead E-PAD ‘Green’ Package	-

Note: See page 8 for ‘Green’ package identification information.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: +886-3-5780211 Fax: +886-3-5776047
www.realtek.com