IAS0600 LAB REPORT 2

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Introduction

This lab dealt with getting more knowledge and practical skills about structural design in particular and obviously by the end of the lab students were expected to get more insights about VHDL, Vivado tools and FPGA. The lab was performed during lab time and lasted approximately 3 and half hours. The lab was performed in presence of the lab assistant who was in charge of helping students both technically and theoretically.

Background

For this practical lab, the background sources I benefitted from are listed and detailed below:

-Lecture 6 Explanation and Slides: I relied on and used lecture 6 slides and explanations to understand more the notion of structural design;

-Lab Sheet: The explanations in the lab sheet was a guide for the completion of the tasks;

-The cumulated knowledge gained in previous lab work and first trainings practical classes about VHDL and Vivado were of great use.

Workflow

This lab was about implementing structural design of a 2bit adder using 1bit full adder and 1bit half adder as components in top level module. The lab included two tasks:

-implementation of the 2bit adder in VHDL top-level file

-implementation of the 2bit adder in Block Design top-level file.

In the first task, it was required to implement the 2bit adder using VHDL top level module. The top-level file would use a half adder and a full adder and the full adder itself would use 3 half adders as components. In that way the top module file representing the 2bit adder circuit can be described in the following tree.

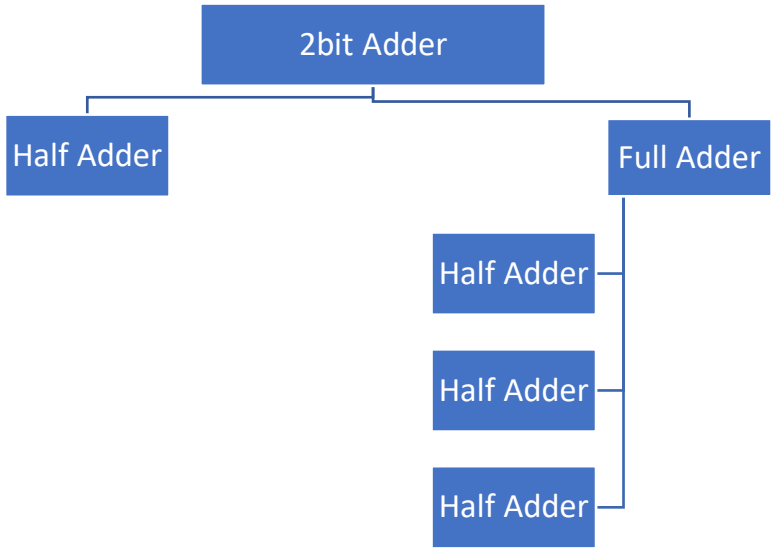

Figure1: 2bit Adder Components Tree

The half adder component was implemented in a separate VHDL source file as an entity. The full adder uses the previously implemented half adder entity as component and declare 3 different half adder components in its architecture. I used indirect instantiation to instantiate the half adder components serving as placeholders for the half adder design unit. I used explicit named association *port map* to map the inputs/outputs of half adders' components to signals, inputs/outputs in the full adder file.

In the second task, the same operation was performed as in the first task but using Vivado Block Design. There are two options here: one could use VHDL description of both half adder and full adder as packages into IP and could be instantiated from the list of IPs as mentioned in Vivado Tutorial, the other option is to use VHDL source file directly in the block design as RTL module. As suggested in the lab sheet, I used the second option. To do that, I just had to highlight any VHDL source file I want to use as component and drag it into the block design. I did that to add a half adder and a full adder into the block design and used wires to connect them to each other and connections to make external I/O pins. The following picture is a screenshot of the block design of the 2bit adder.

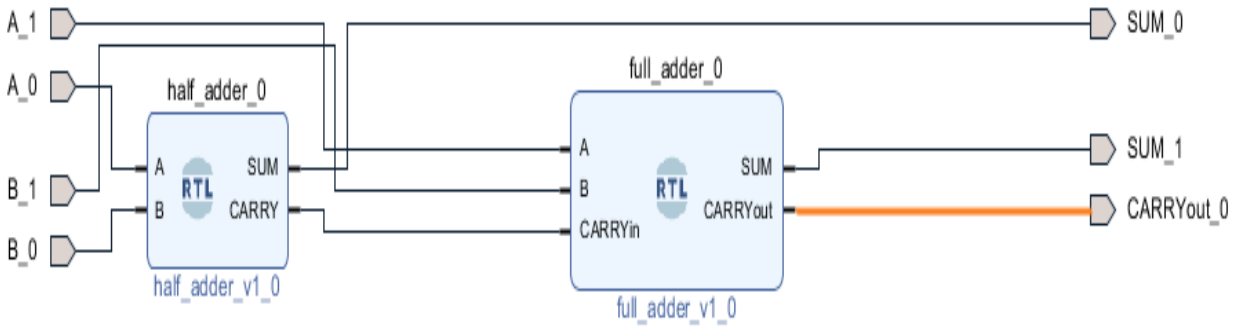

Figure 2: 2bit Adder block Design in Vivado

In order to test the correctness of the circuits, I used testbench simulation for both tasks and each testbench simulation file included 16 different inputs combinations. Note a block design can't be set as top module file directly, instead a source file has to be generated and updated using the block design. The generated source wrapper file can then be set as top module.

For each task, the implemented task was run on FPGA board and the results were visually defended during the lab session. Inputs A0, A1, B0, and B1 were connected to switches S0, S1, S2 and S3 respectively and outputs SUM0, SUM1 and Carry to LED0, LED1, LED2 respectively.

Results and Discussion

The simulation results for the two tasks were all the same. We obtained the desired outputs for all combinations of inputs. A screenshot of one of the simulations is included below.

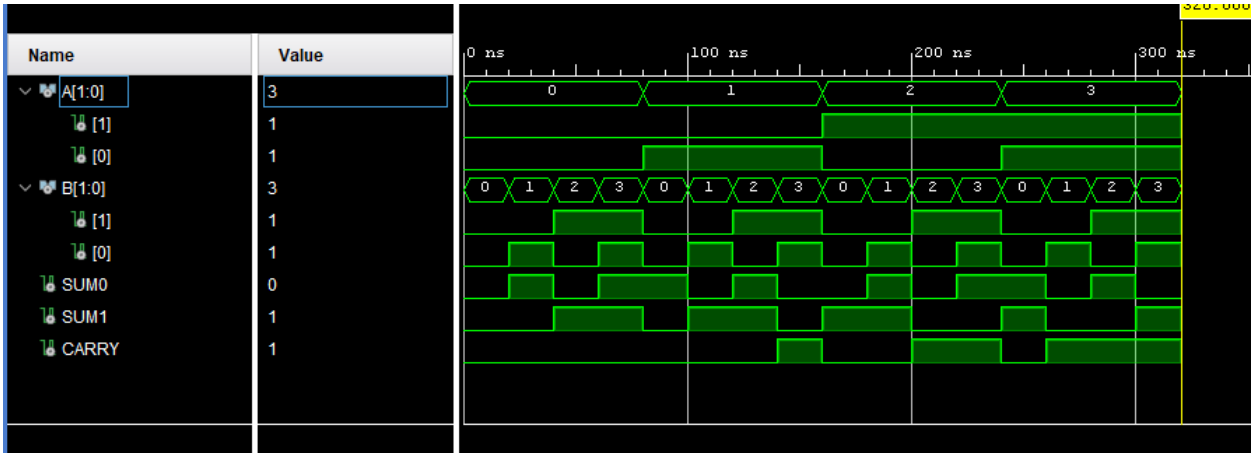

Figure3: Simulation Result

The results are understandable in the way that after generating source file for the block design file, the wrapper VHDL source file obtained is similar to the first task's top level VHDL file; only some signal names have changed. Both VHDL source or Block design are different ways of describing the same circuit, furthermore block design is easier to understand and implement as it features visual programming concept that has been shown to be much easier.

Conclusion

To summarize, in this lab I learned how to use structural design to describe a circuit using both VHDL source file and block design tool in Vivado. I followed the steps in the lab sheet one by one and asked questions when needed to successfully complete the expected outcomes. From now on, I am very sure I can design the implementation workflow of a complicated circuit using structural design style and implement this using VHDL or Block Design. As suggestion, I think if possible we could use block design only and connect the required part and gates without using any VHDL package or source file as another task for the lab. Also, maybe students should be the ones imagining and figuring out what components to use and how to use it. This means, in the lab description, less information about the internal architecture of the 2bit adder is provided so that students can try to figure out what they have to use as components themselves. In that way, the lab tests not only our ability to use structural design but also to understand a given case and interpret this into electronic design as it maybe in real world practical cases.