به نام خدا

حافظه‌ها

نگاشت حافظه

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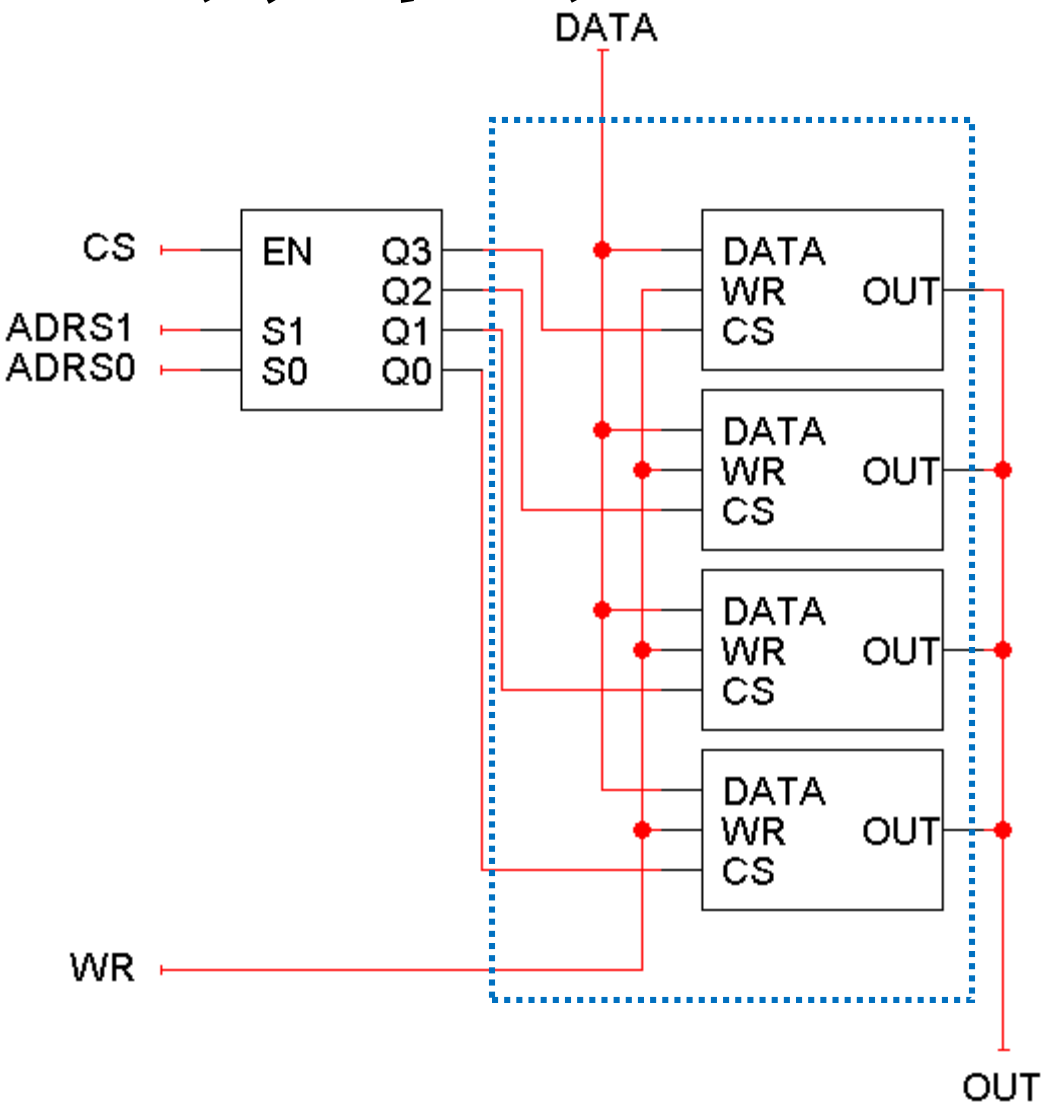
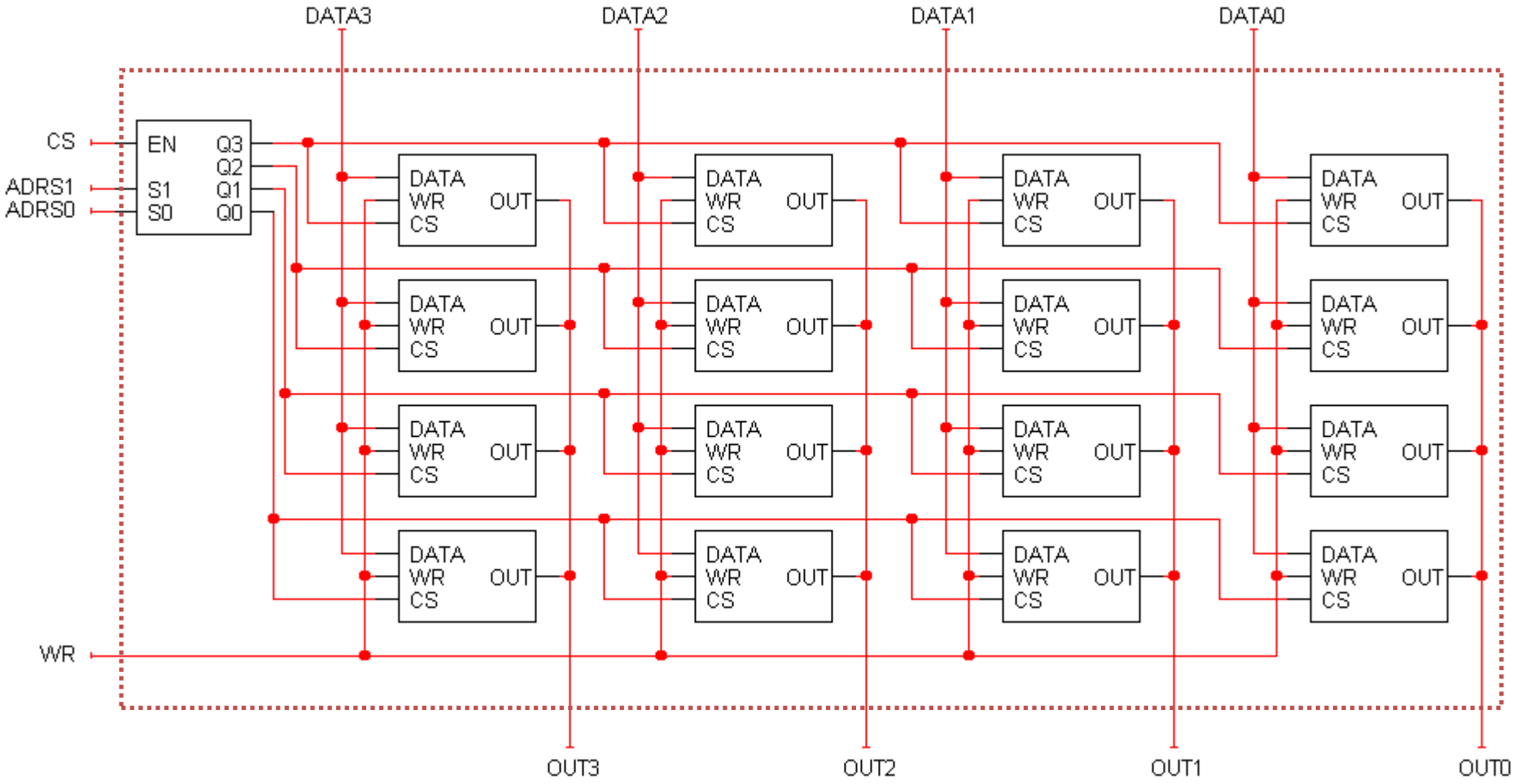
کنار هم قرار دادن سلول‌های حافظه

- Here is the 4 x 1 RAM once again.
- How can we make a “wider” memory with more bits per word, like maybe a 4 x 4 RAM?
- Duplicate the stuff in the blue box!



A 4 x 4 RAM

DATA and OUT are now each *four* bits long, so you can read and write four-bit words.



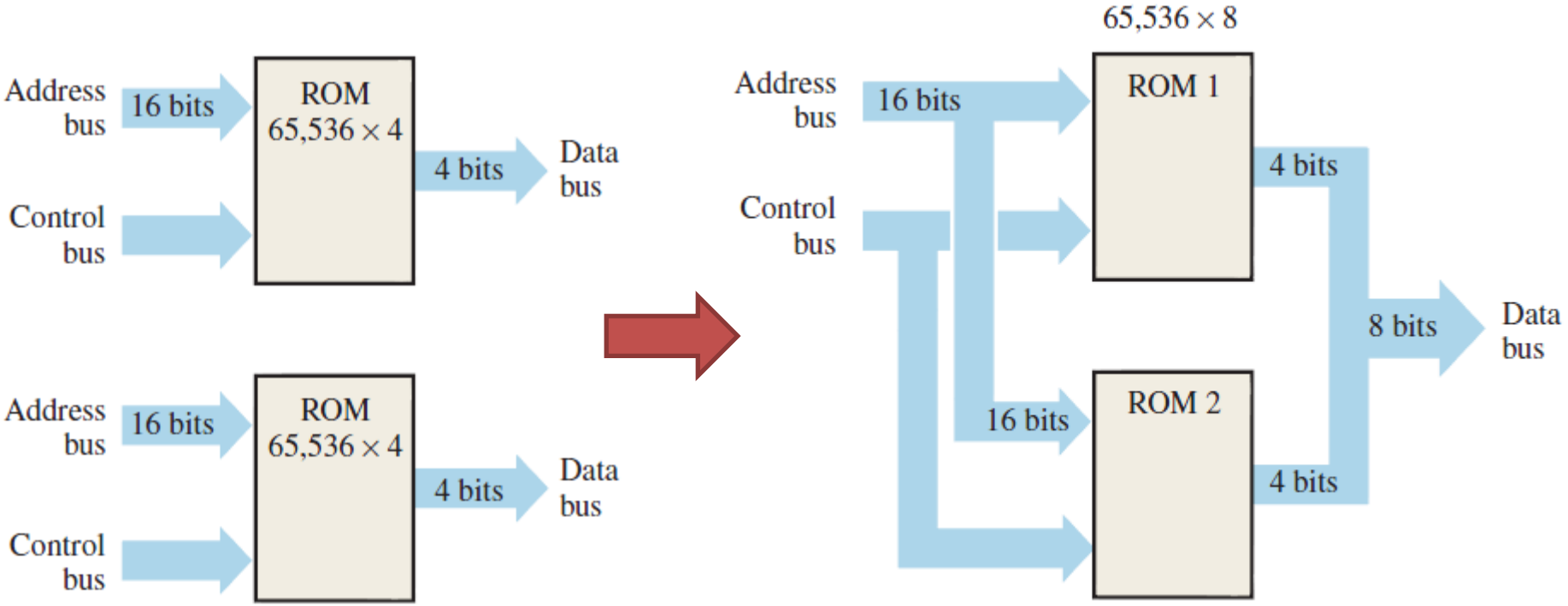
توسعه حافظه

- Available memory can be expanded
  - To increase the word length
    - Number of bits in each address
  - To increase the word capacity
    - Number of different addresses

- Memory expansion is accomplished by
  - Adding an appropriate number of memory chips to
    - Address buses
    - Data buses
    - Control buses

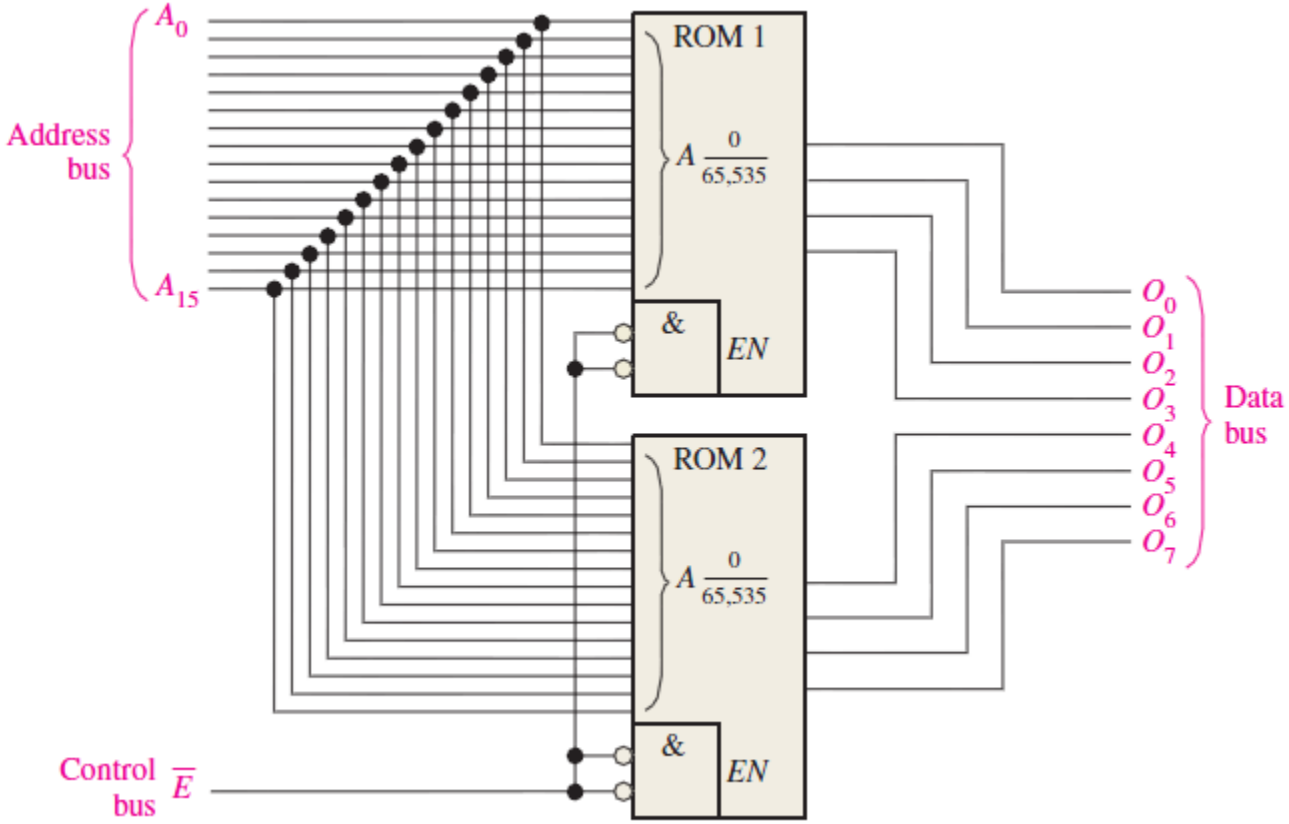
Increase the Word Length

- Number of bits in data bus must be increased
- For example
  - 8-bit word length can be achieved by using two memories, each with 4-bit words



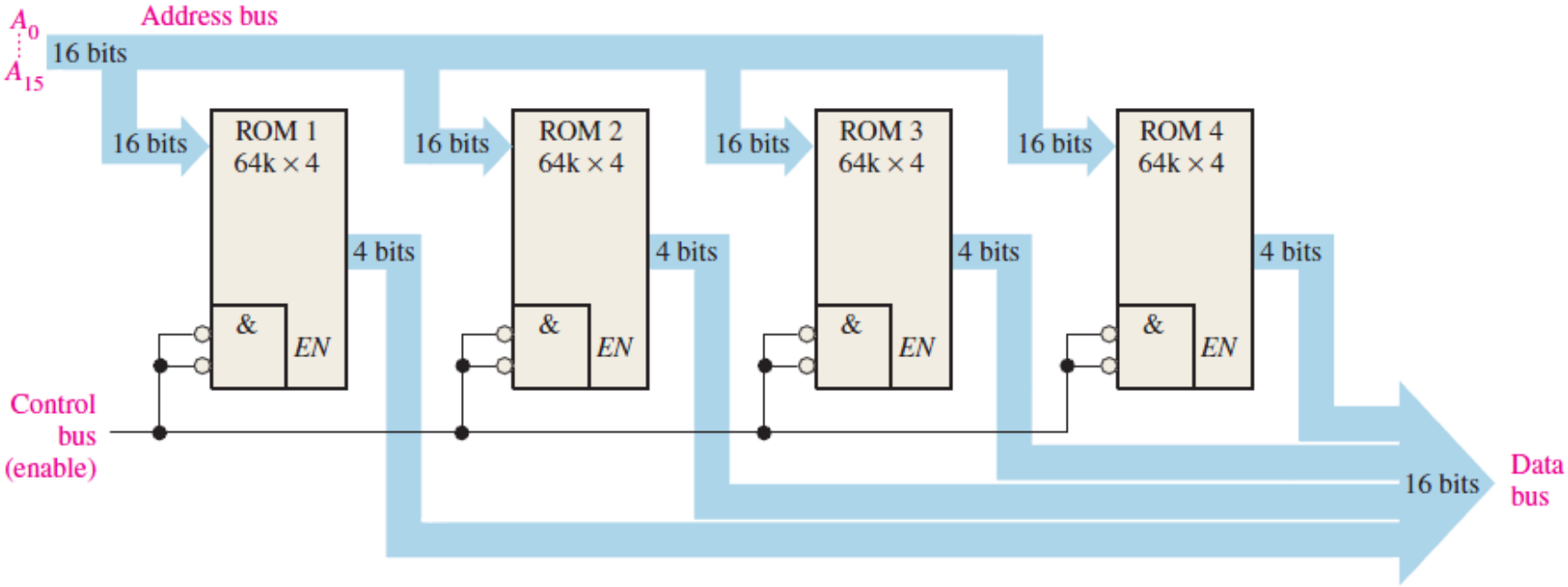
مثال

توسعه دو حافظه ROM 64k×4 برای تشکیل یک حافظه ROM 64k×8



مثال

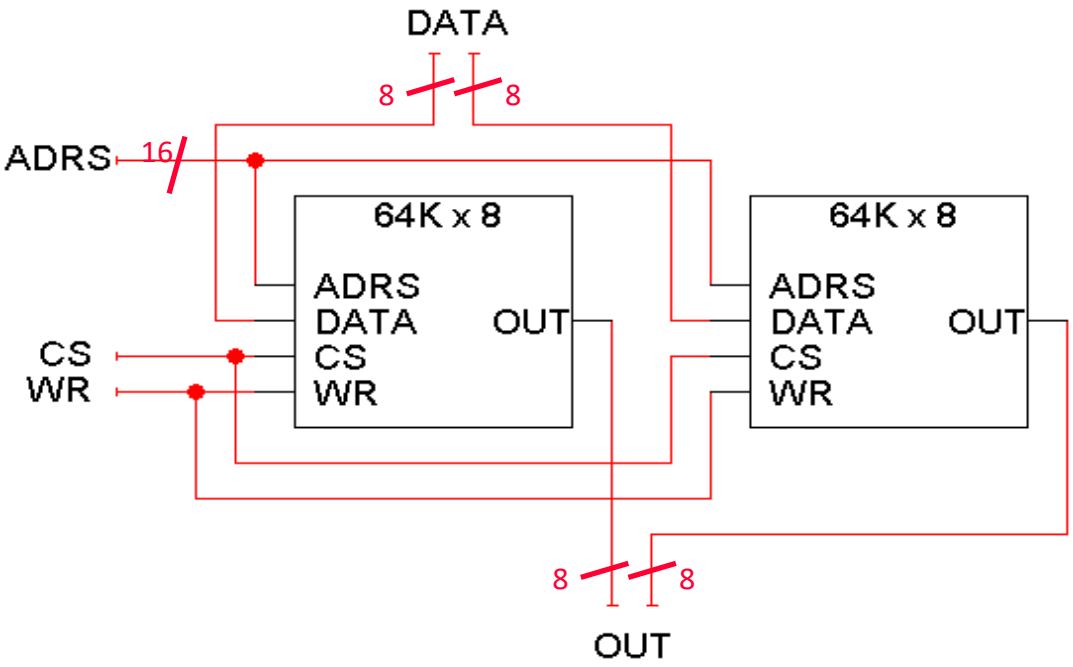
تشکیل یک حافظه ROM 64k×16 با استفاده از چهار حافظه ROM 64k×4



Word-length Expansion in a RAM

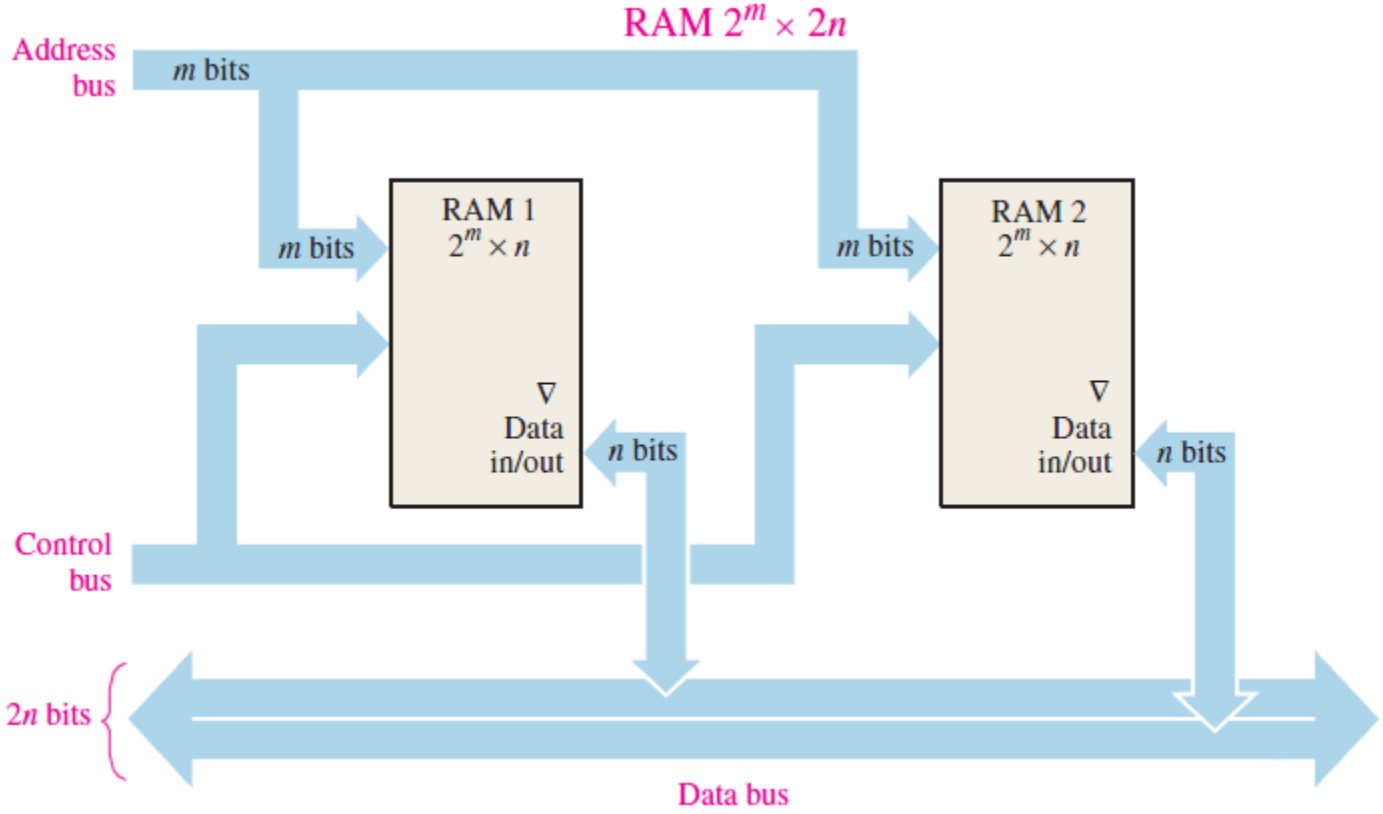
Design a 64K x 16 RAM, using two 64K x 8 chips.

- The left chip contains the most significant 8 bits of the data.
- The right chip contains the lower 8 bits of the data.



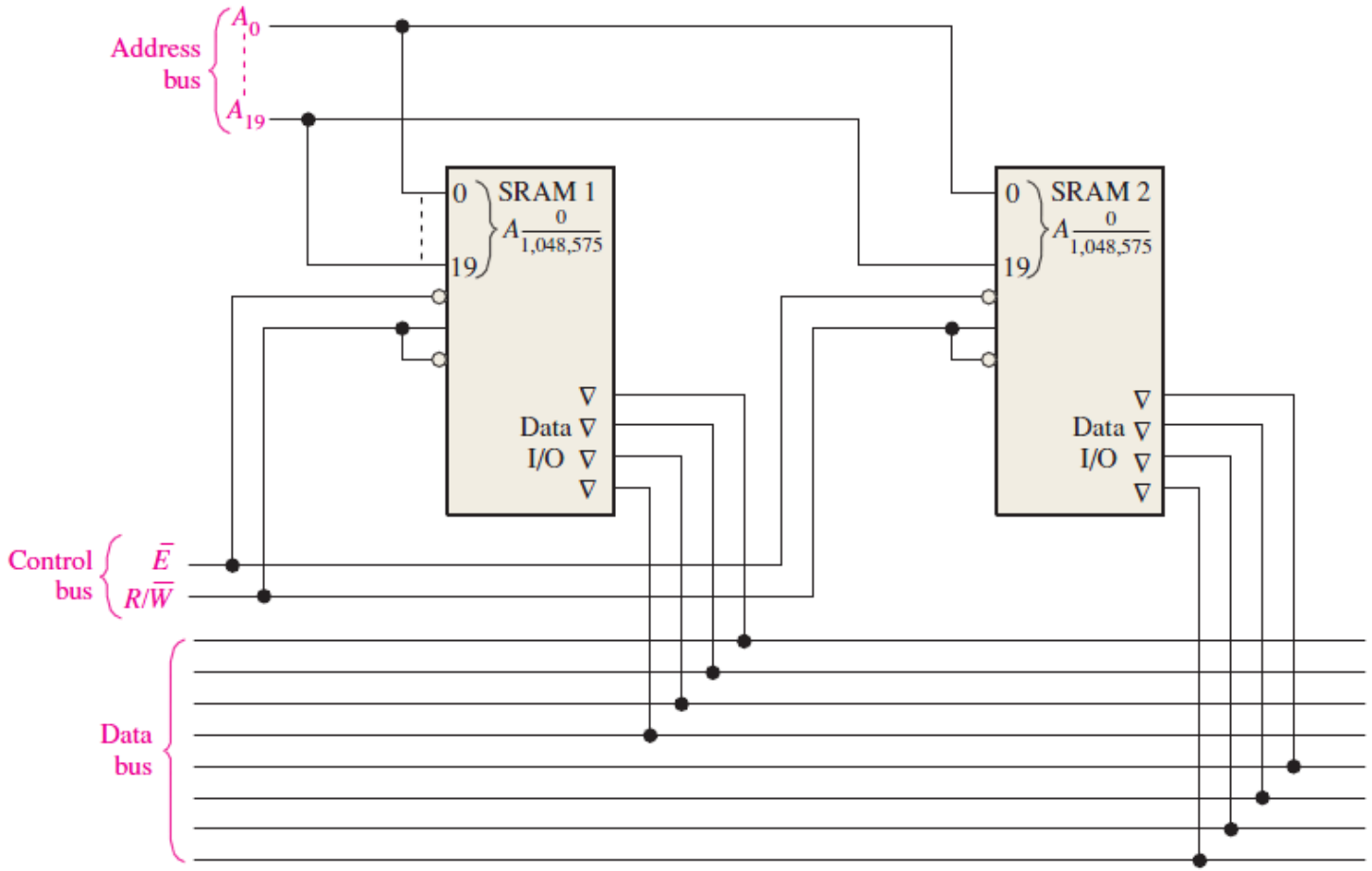
Word-length Expansion in a RAM

Tri-state buffers are required



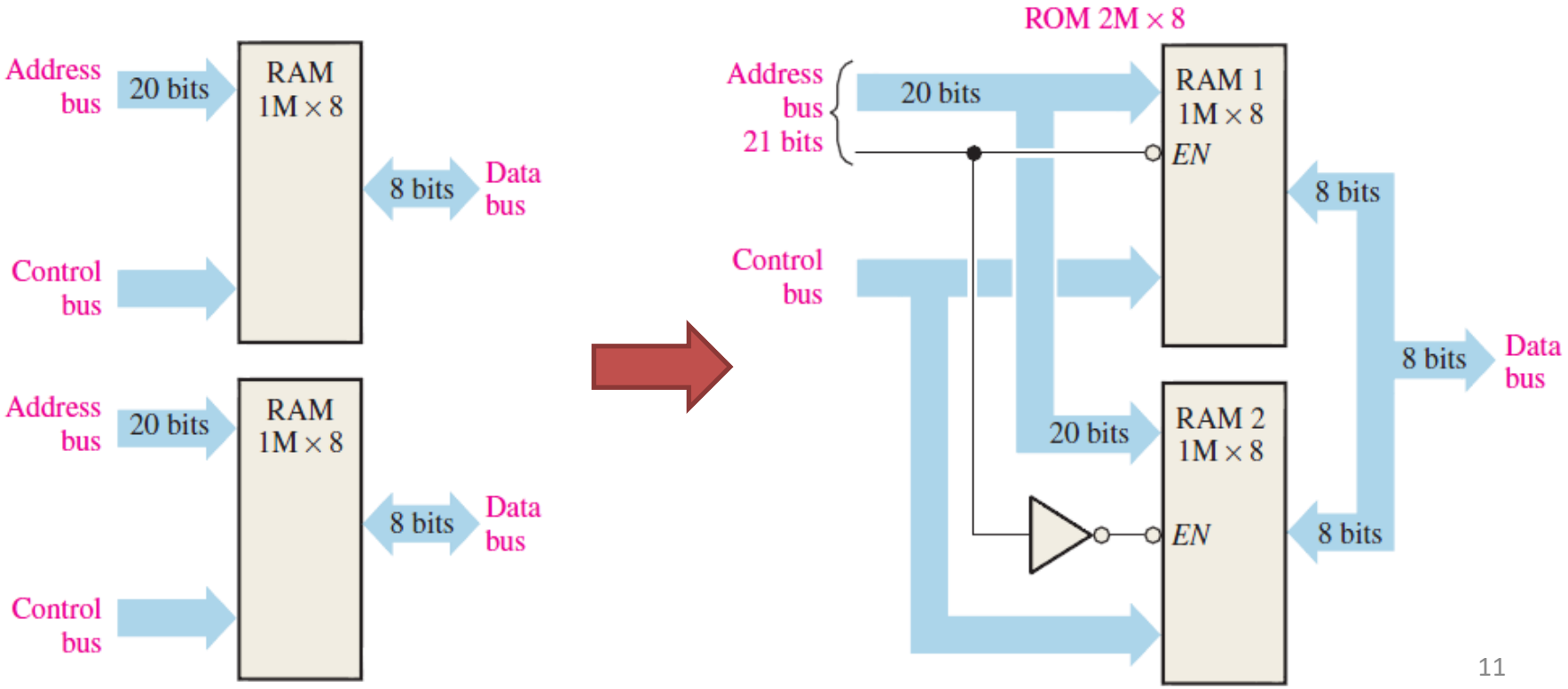
مثال

1M × 4 SRAMs to create a 1M × 8 SRAM



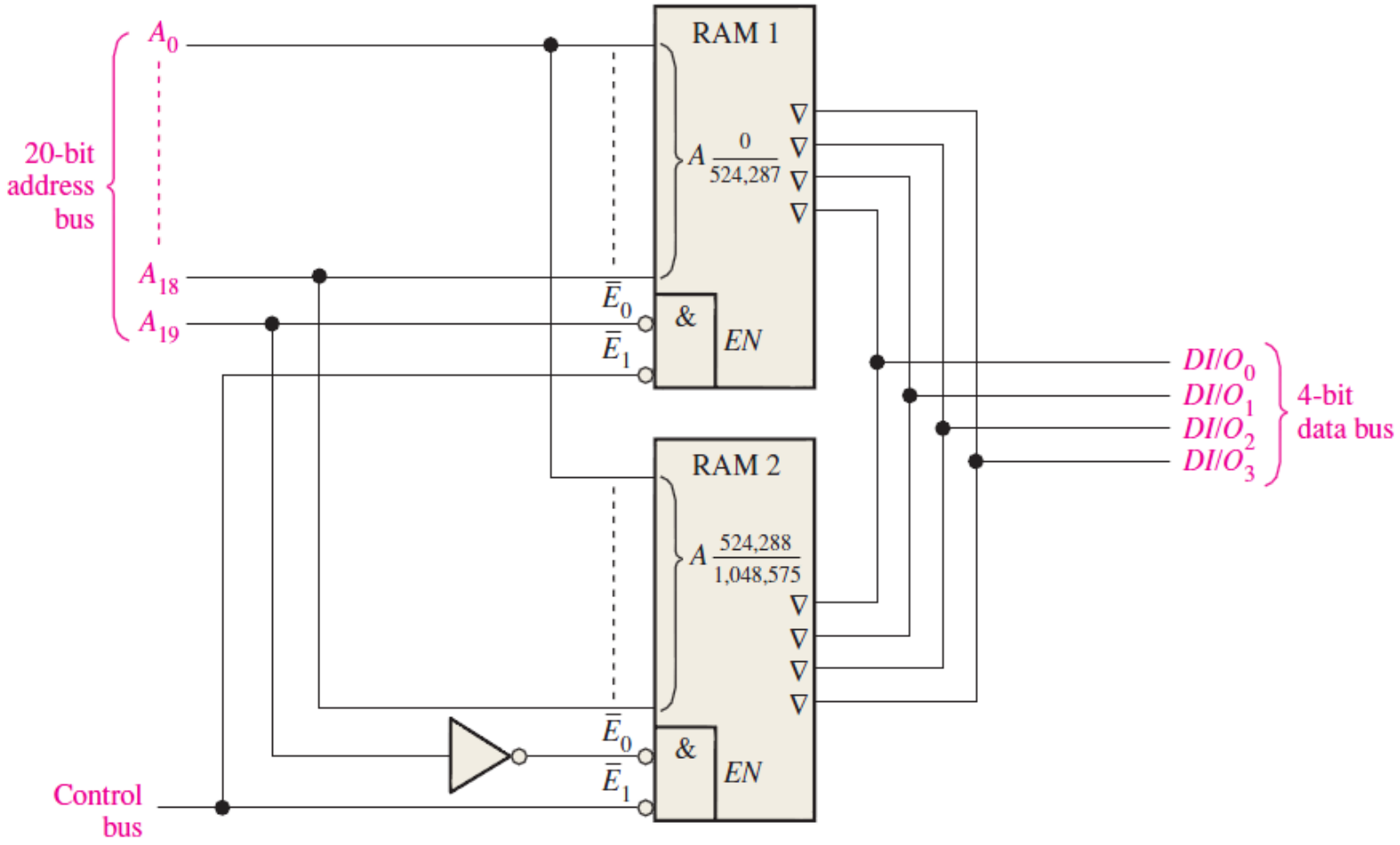
Word-Capacity Expansion

- Number of address bits must be increased
- For example
  - Two 1M × 8 RAMs are expanded to form a 2M × 8 memory



مثال

512k × 4 RAMs to implement a 1M × 4 memory



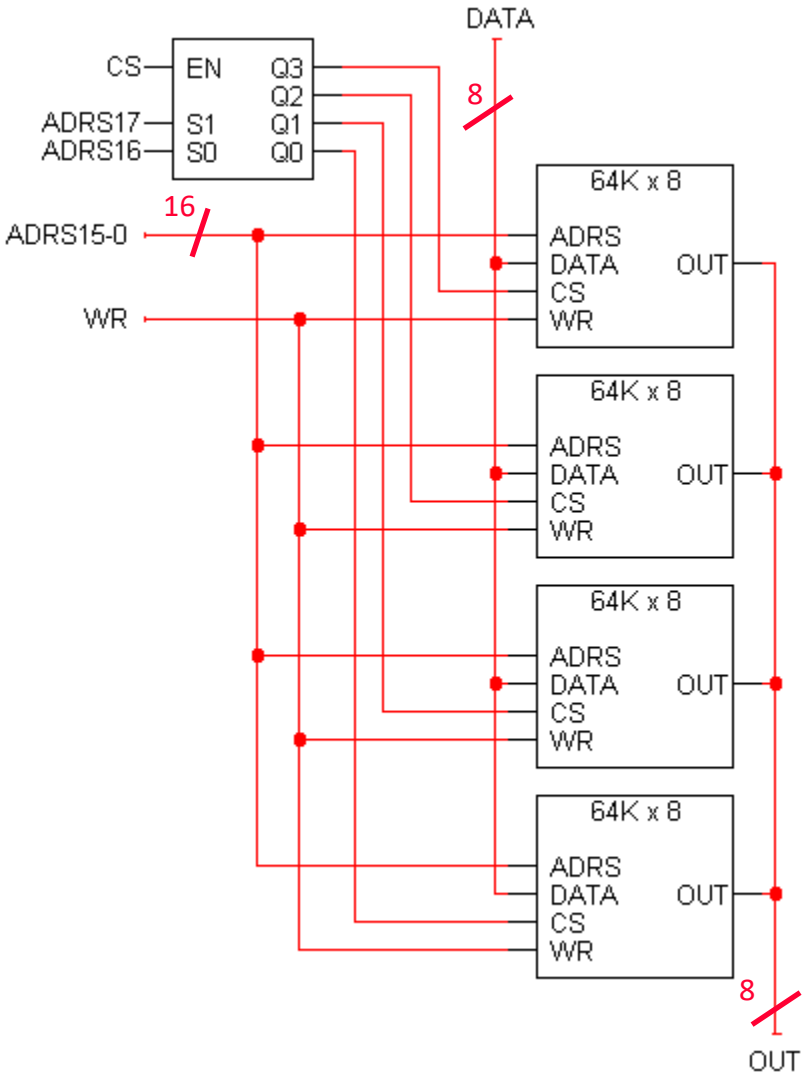
Making a larger memory

Example

Design a 256K x 8 memory, given that you have 64K x 8 chips

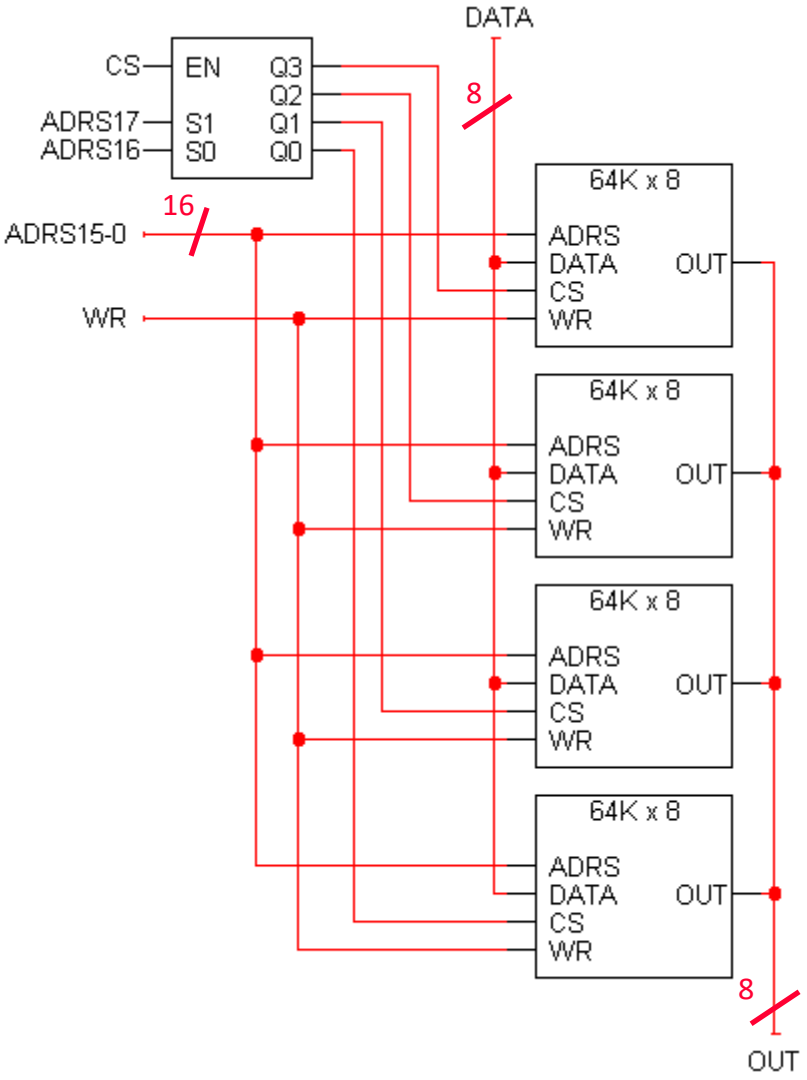
Solution

- For 256K words, we need 18 address lines.
  - The two most significant address lines go to the decoder, which selects one of the four 64K x 8 RAM chips.
  - The other 16 address lines are shared by the 64K x 8 chips.
- The 64K x 8 chips also share WR and DATA inputs.
- This assumes the 64K x 8 chips have three-state outputs.

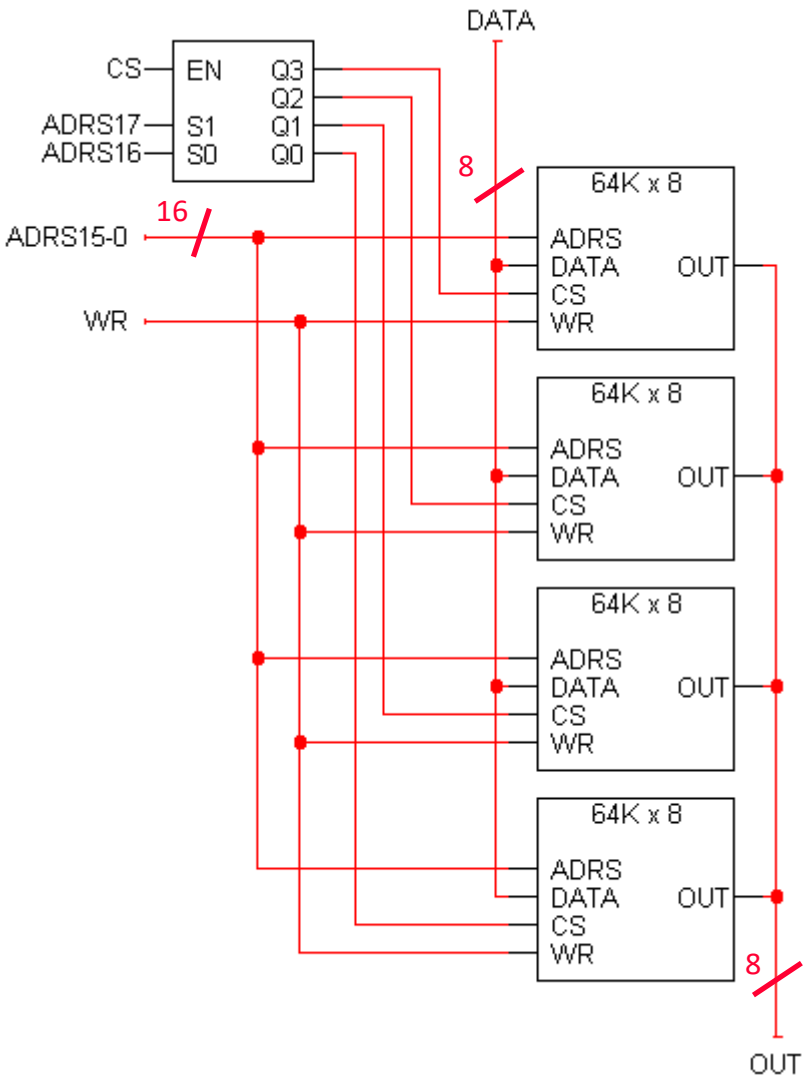


Analyzing the 256K x 8 RAM

- There are 256K words of memory, spread out among the four smaller 64K x 8 RAM chips.
- When the two most significant bits of the address are 00, the bottom RAM chip is selected. It holds data for the first 64K addresses.
- The next chip up is enabled when the address starts with 01. It holds data for the second 64K addresses.
- The third chip up holds data for the next 64K addresses.
- The final chip contains the data of the final 64K addresses.



Address ranges




```
11 1111 1111 1111 1111 (0x3ffff)
                to
11 0000 0000 0000 0000 (0x30000)

10 1111 1111 1111 1111 (0x2ffff)
                to
10 0000 0000 0000 0000 (0x20000)

01 1111 1111 1111 1111 (0x1ffff)
                to
01 0000 0000 0000 0000 (0x10000)

00 1111 1111 1111 1111 (0x0ffff)
                to
00 0000 0000 0000 0000 (0x00000)
```

ماژول‌های حافظه

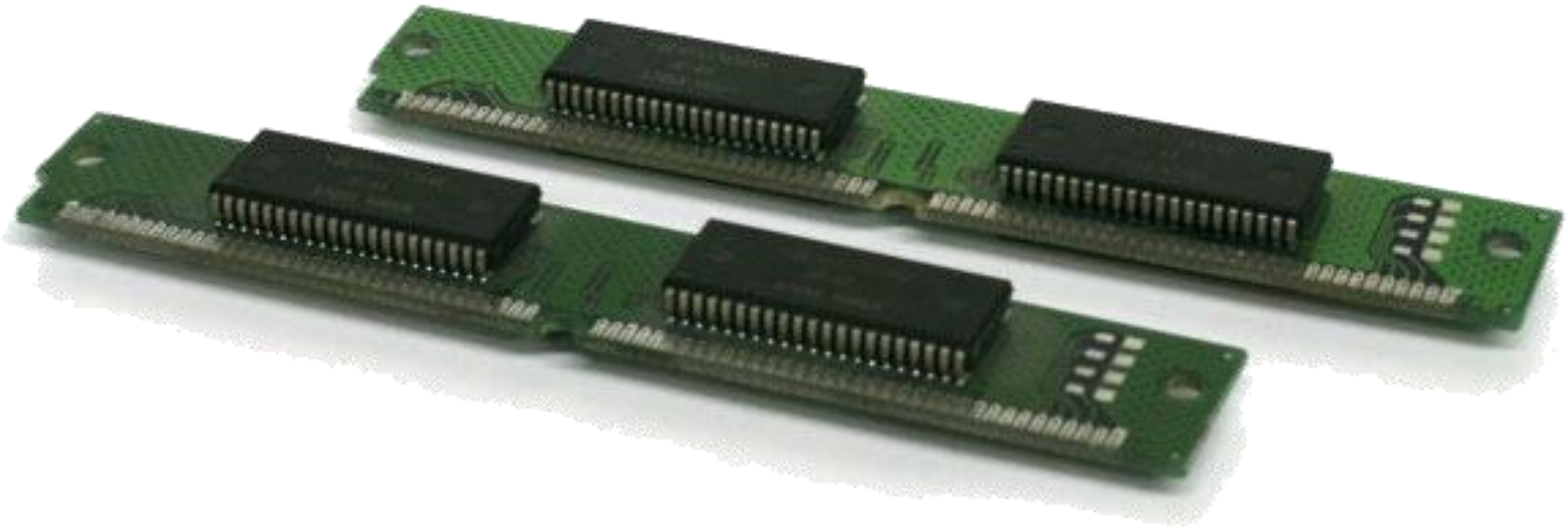
- Memory module
  - A narrow printed circuit board that holds memory chips
- Memory module types

  - Single In-Line Memory Module (SIMM)
    - Widely used from the late 1980s to 1990s
    - Typically had 32-bit data bus
      - Available in two physical types—30- and 72-pin

  - Dual In-Line Memory Module (DIMM)
    - "Dual in-line" refers to pins on both sides of the modules
    - Originally had a 168-pin connector supporting 64-bit data bus
      - which is twice the data width of SIMMs

SIMM

- 72-pin SIMM - use a data path of 32 bits

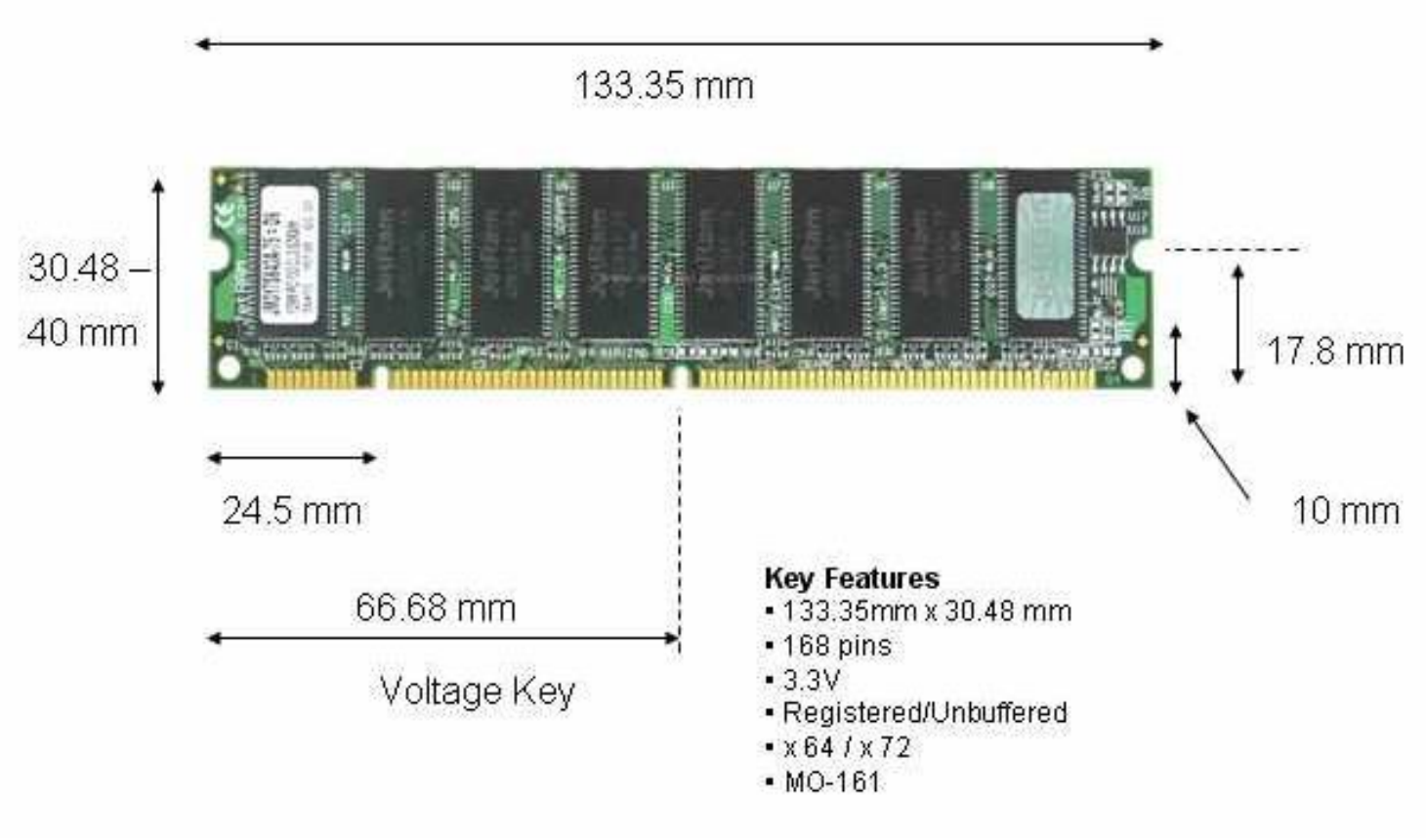


SIMM

- 30-pin SIMM- use a 16-bit address bus

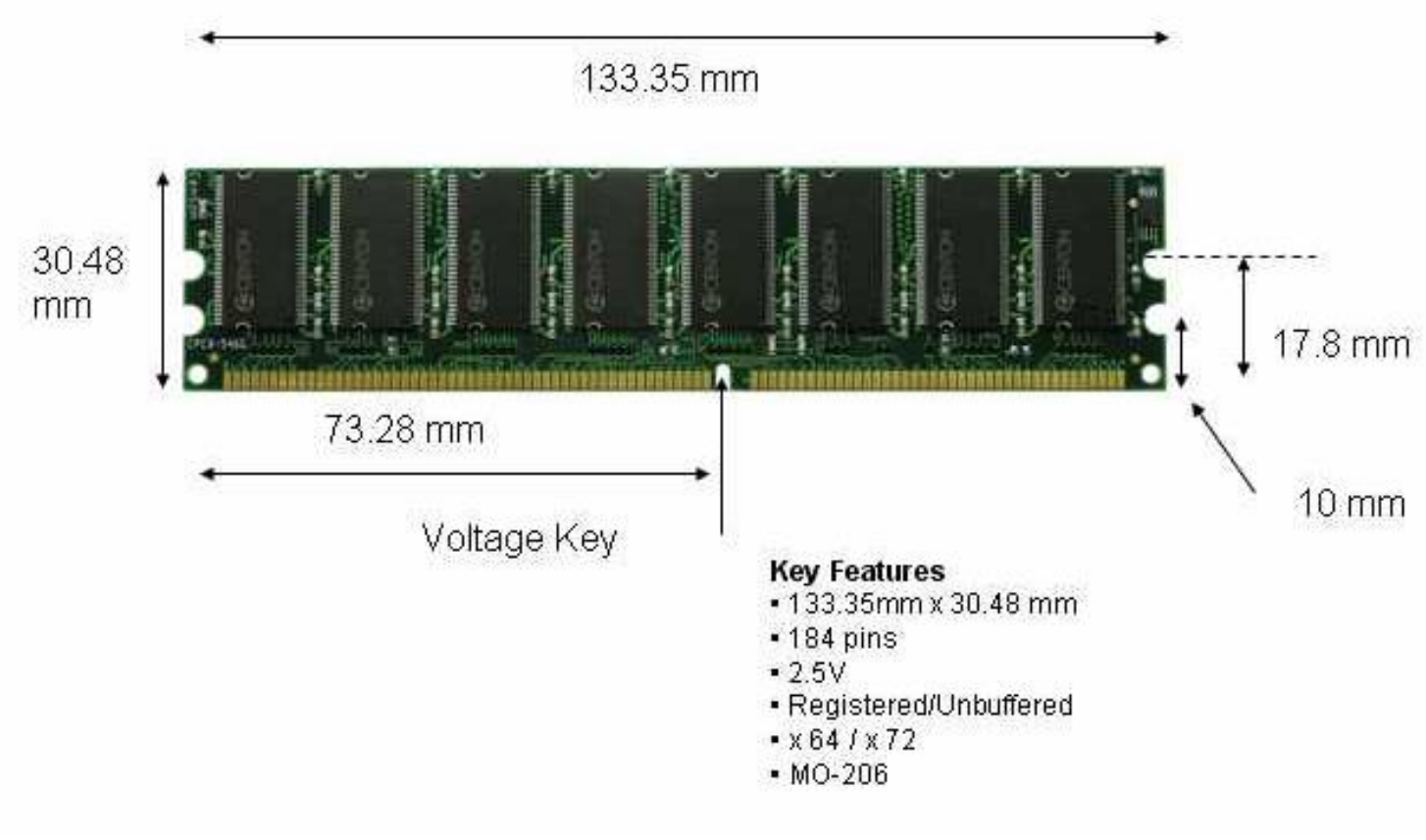
DIMM

- 168-pin SDRAM DIMM



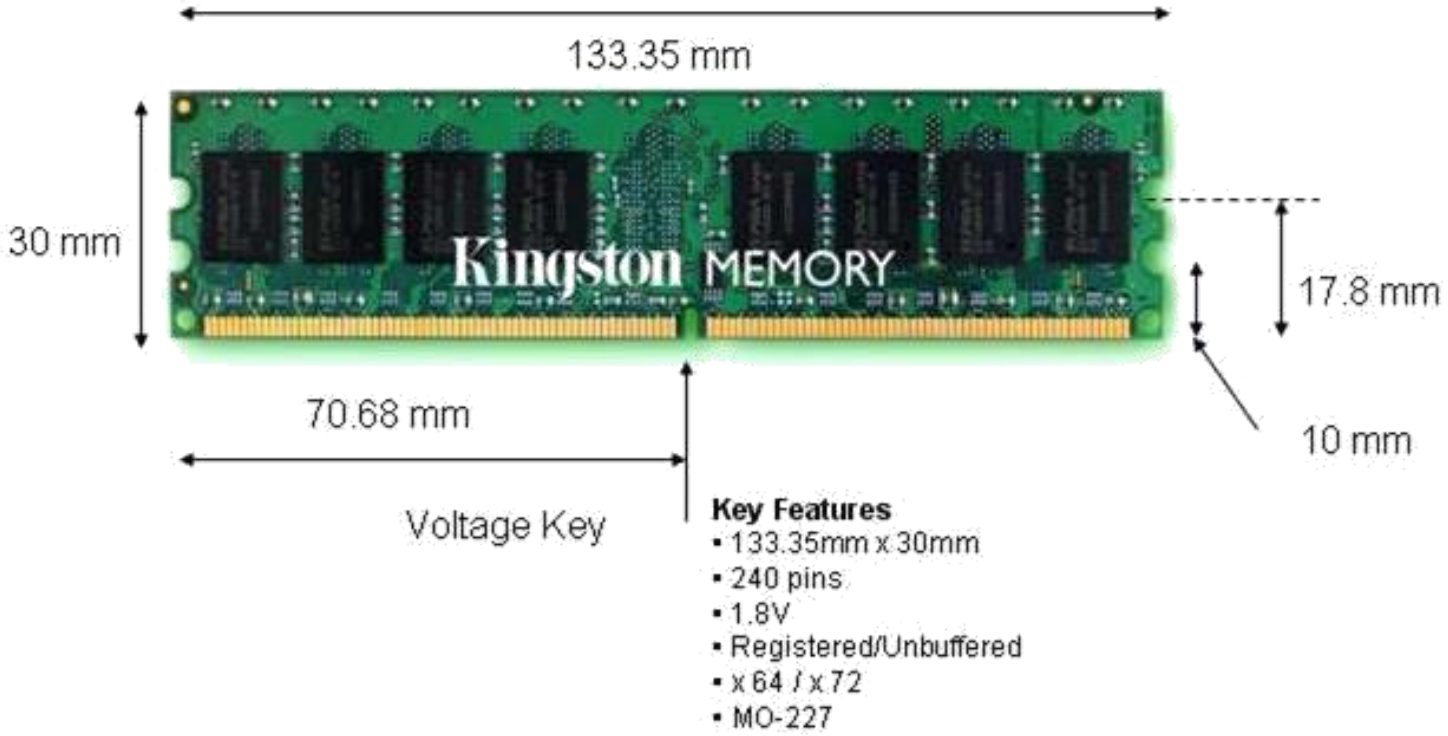
DIMM

- 184-pin DDR DIMM
  - DDR SDRAM performs two transfers per clock cycle



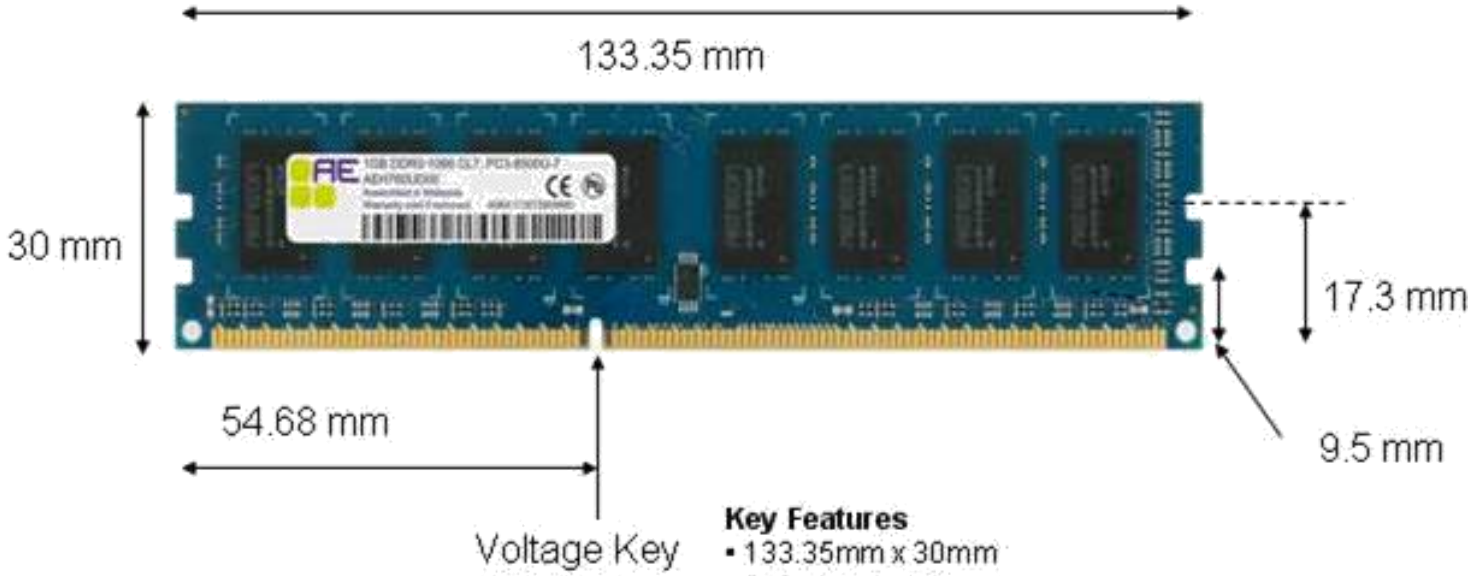
DIMM

- 240-pin DDR2 DIMM
  - Successor to DDR SDRAM
  - Features a four-bit prefetch buffer
  - Enabling faster performance, however has greater latency than DDR SDRAM



DIMM

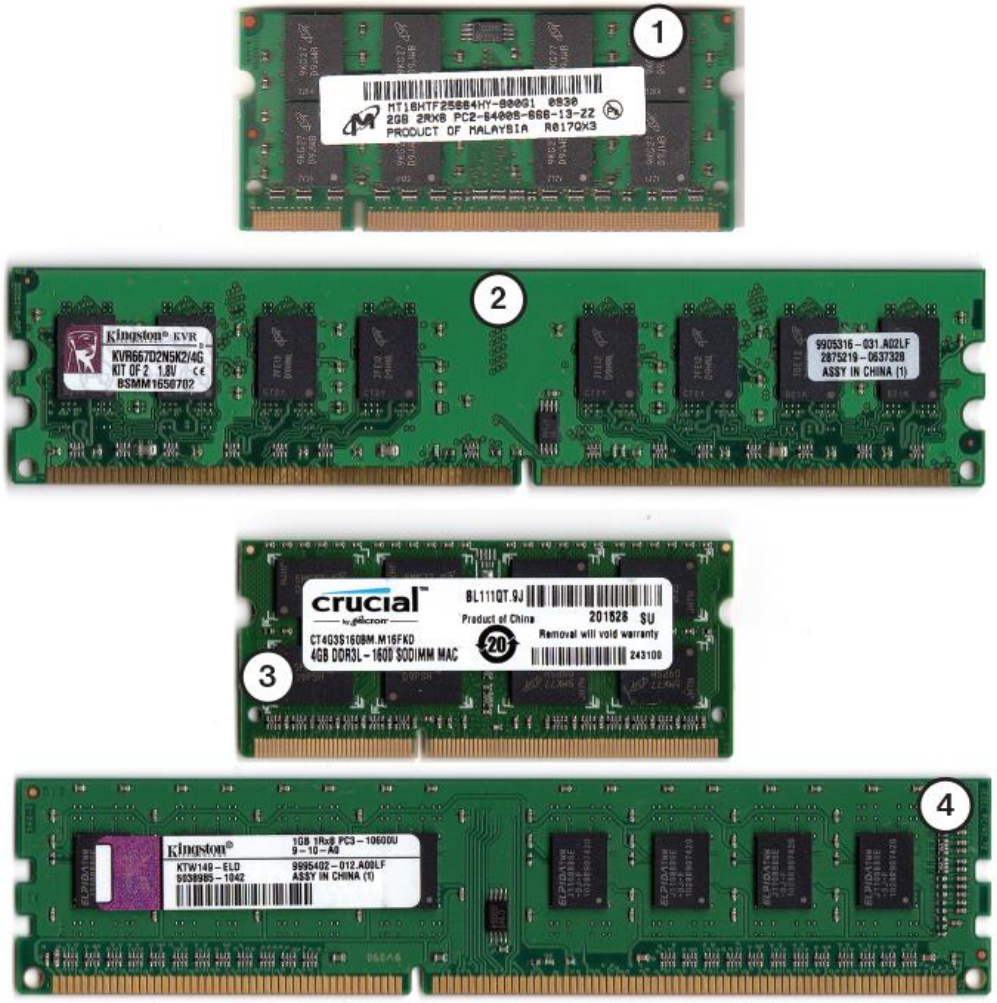
- 240-pin DDR3 DIMM
  - Compared to DDR2, DDR3 runs at lower voltages
  - Most versions run at faster speeds than DDR2
  - Has an eight-bit prefetch bus
  - As with DDR2 versus DDR, DDR3 has greater latency than DDR2



DIMM

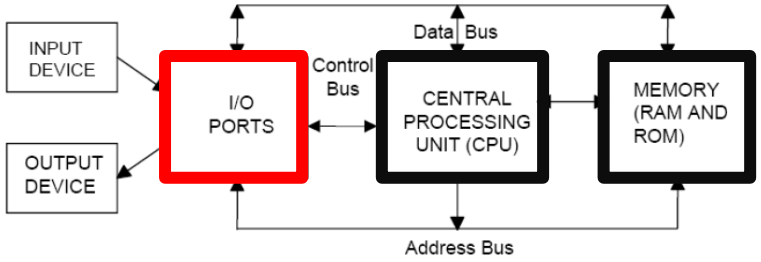
Reduced-size memory modules known as small outline DIMMs (SO-DIMMs or SODIMMS)

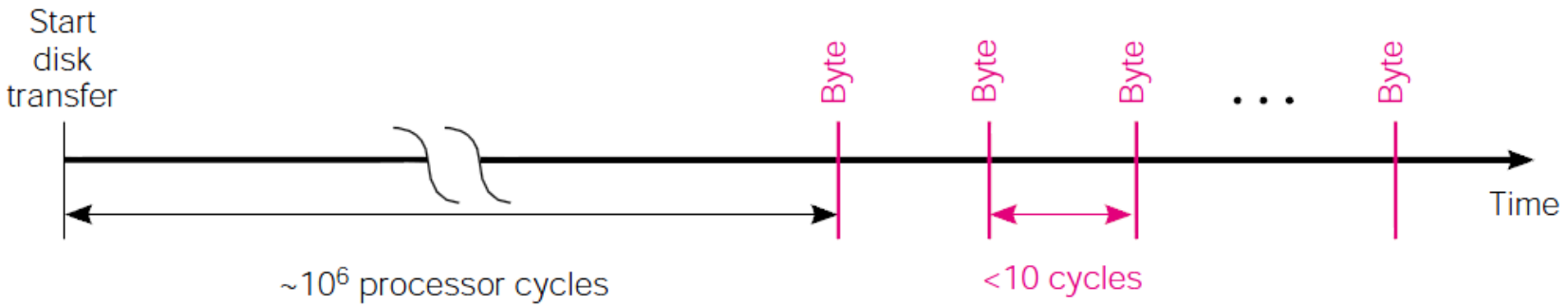
1.DDR2 SO-DIMM
2.DDR2 DIMM
3.DDR3 SO-DIMM
4.DDR3 DIMM



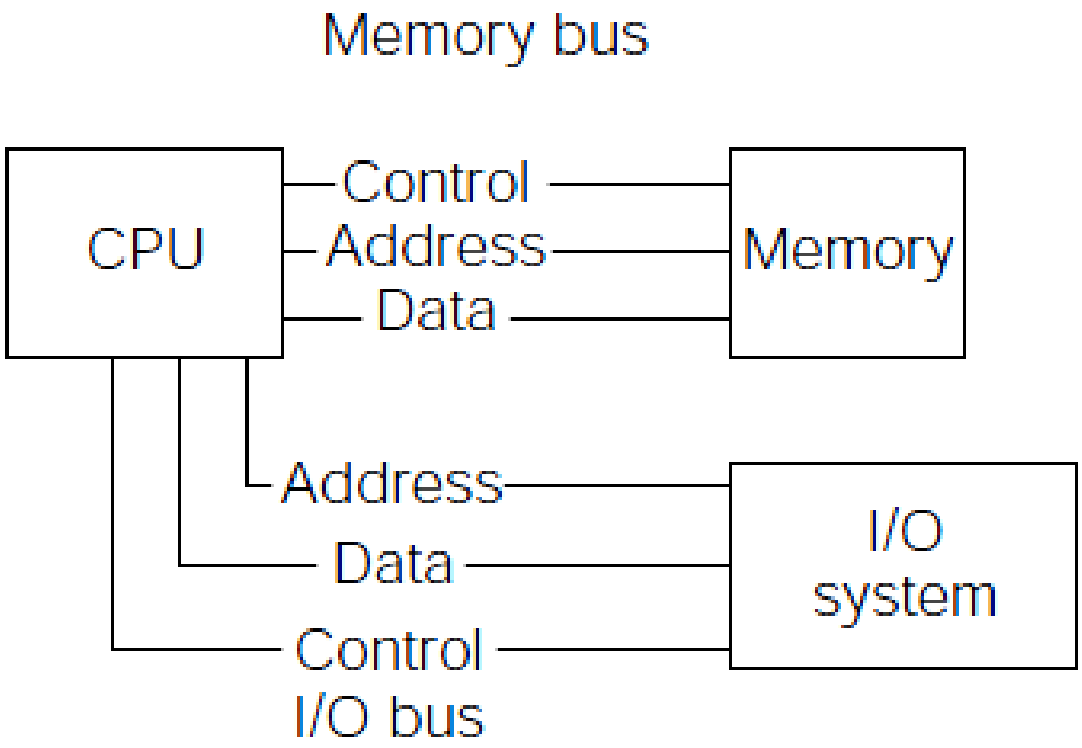
I/O Subsystem

- Provides the mechanism for communication between CPU and outside world
- Manages communications
  - Asynchronous with respect the CPU
  - Have widely ranging data rates





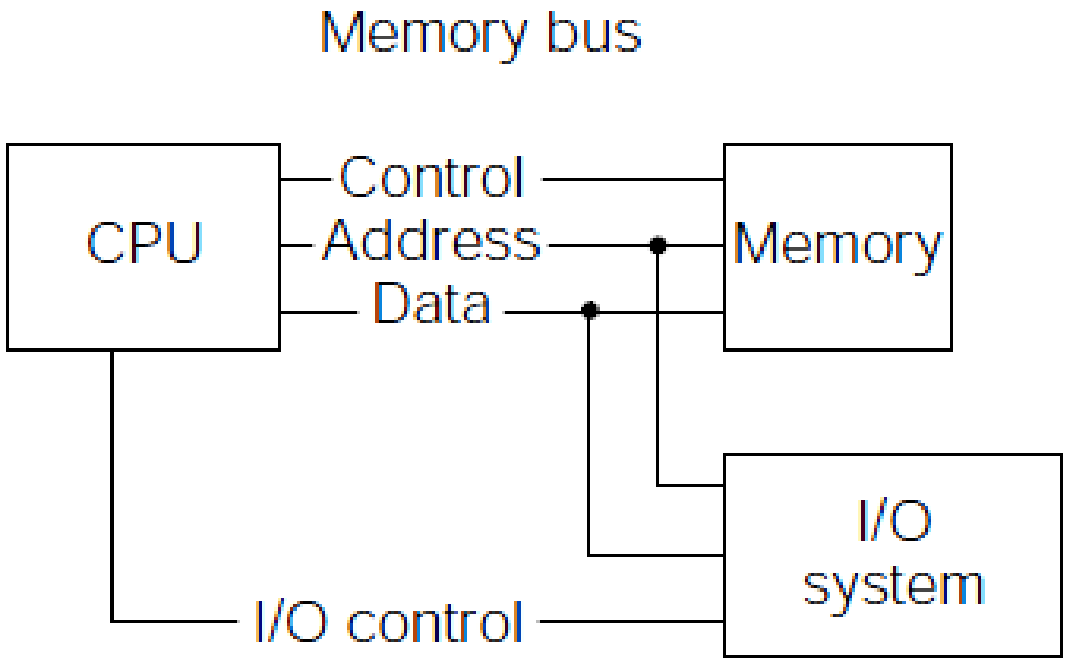
ساختار گذرگاه I/O



Separate memory and I/O buses

Isolated I/O

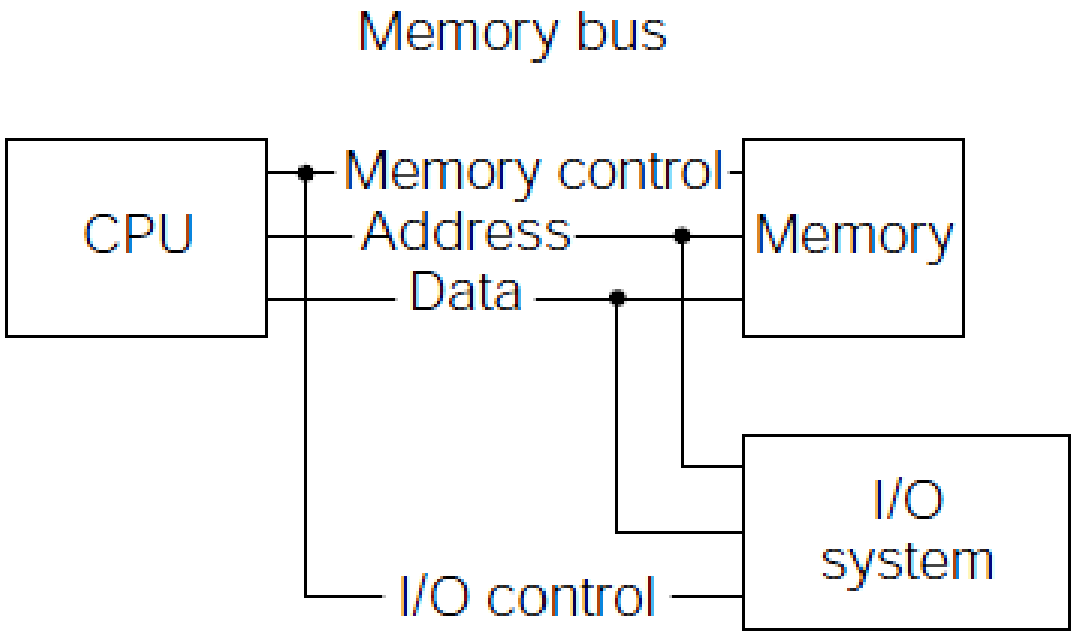
ساختار گذرگاه I/O



Shared address and data lines

Shared I/O

ساختار گذرگاه I/O

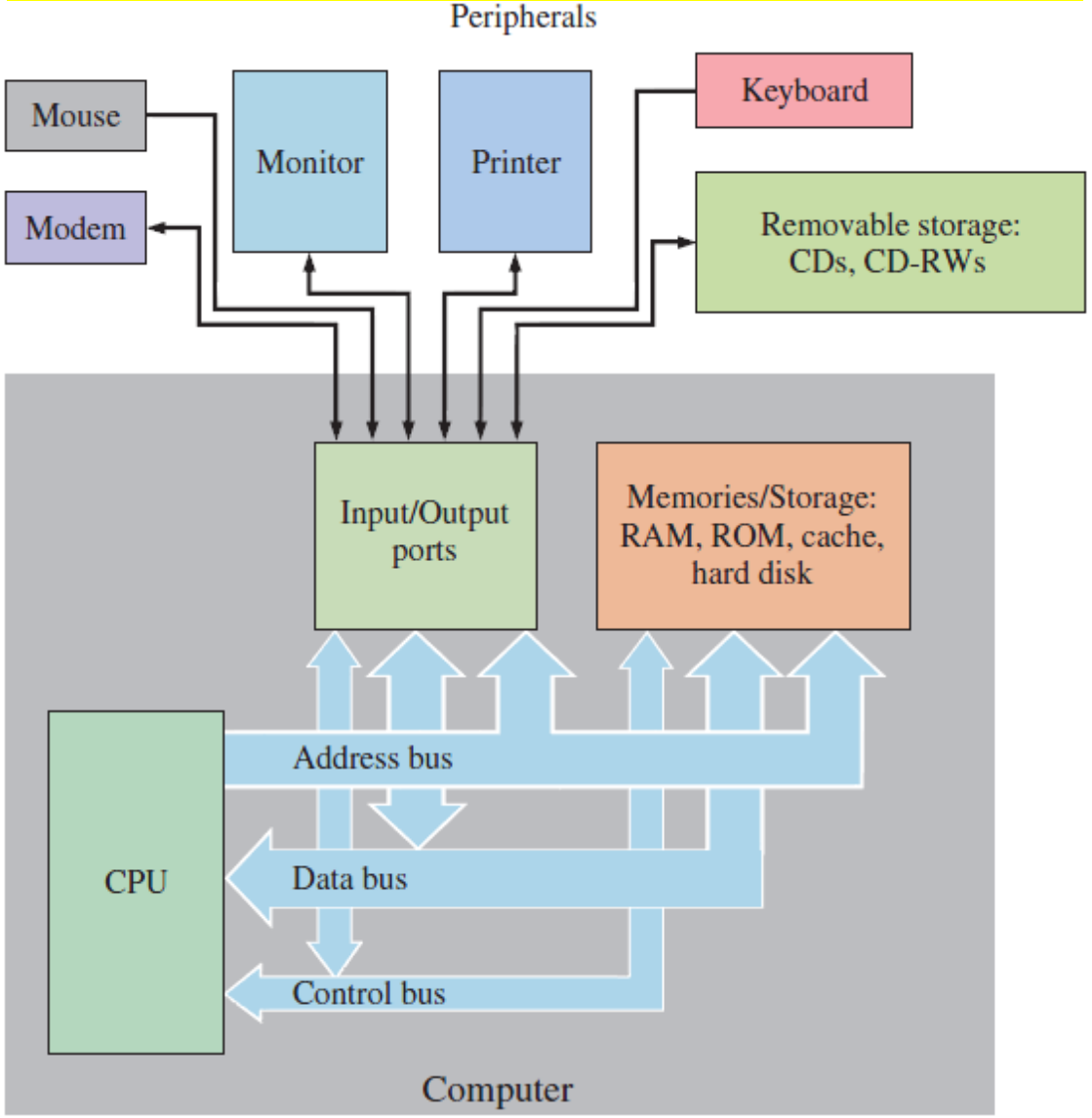


Shared address, data, and control lines → memory-mapped I/O

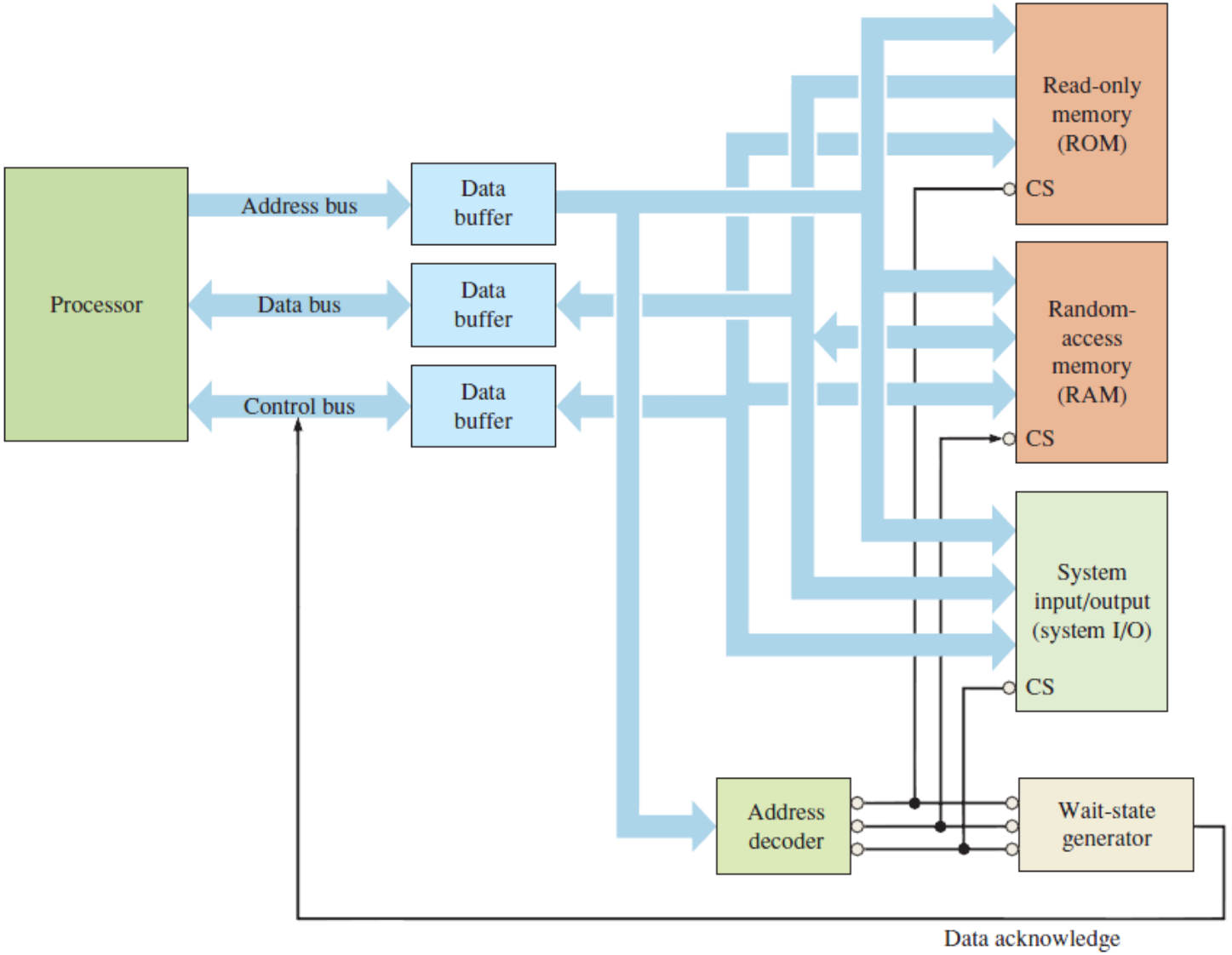
Memory Mapped I/O

- Combine memory control and I/O control lines to make one unified bus for memory and I/O
- This makes addresses of I/O device registers appear to the processor as memory addresses
- Reduces the number of connections to the processor chip
- Standardizes data transfer to and from the processor

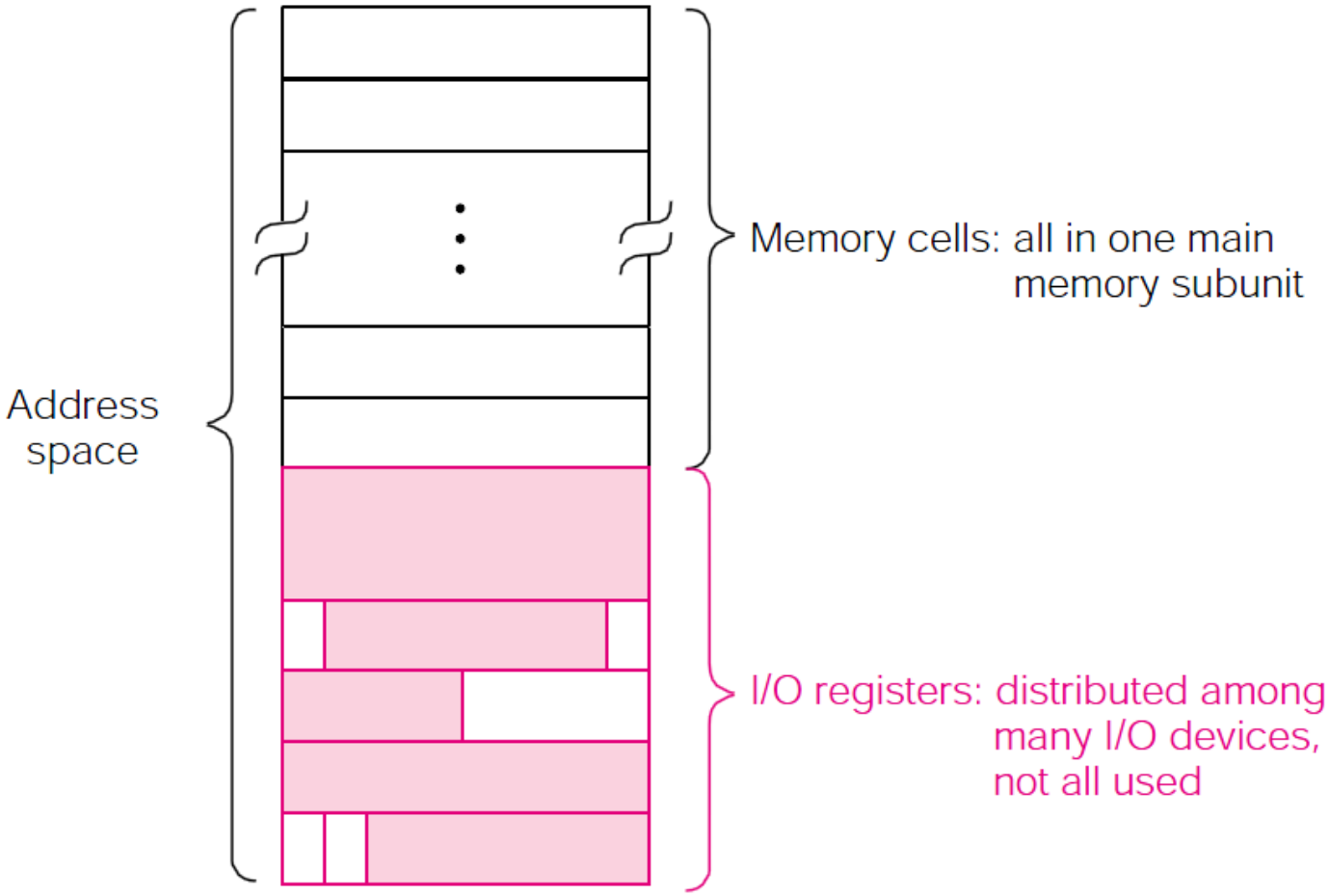
Memory Mapped I/O



Memory Mapped I/O



Address Space (using Memory Mapped I/O)

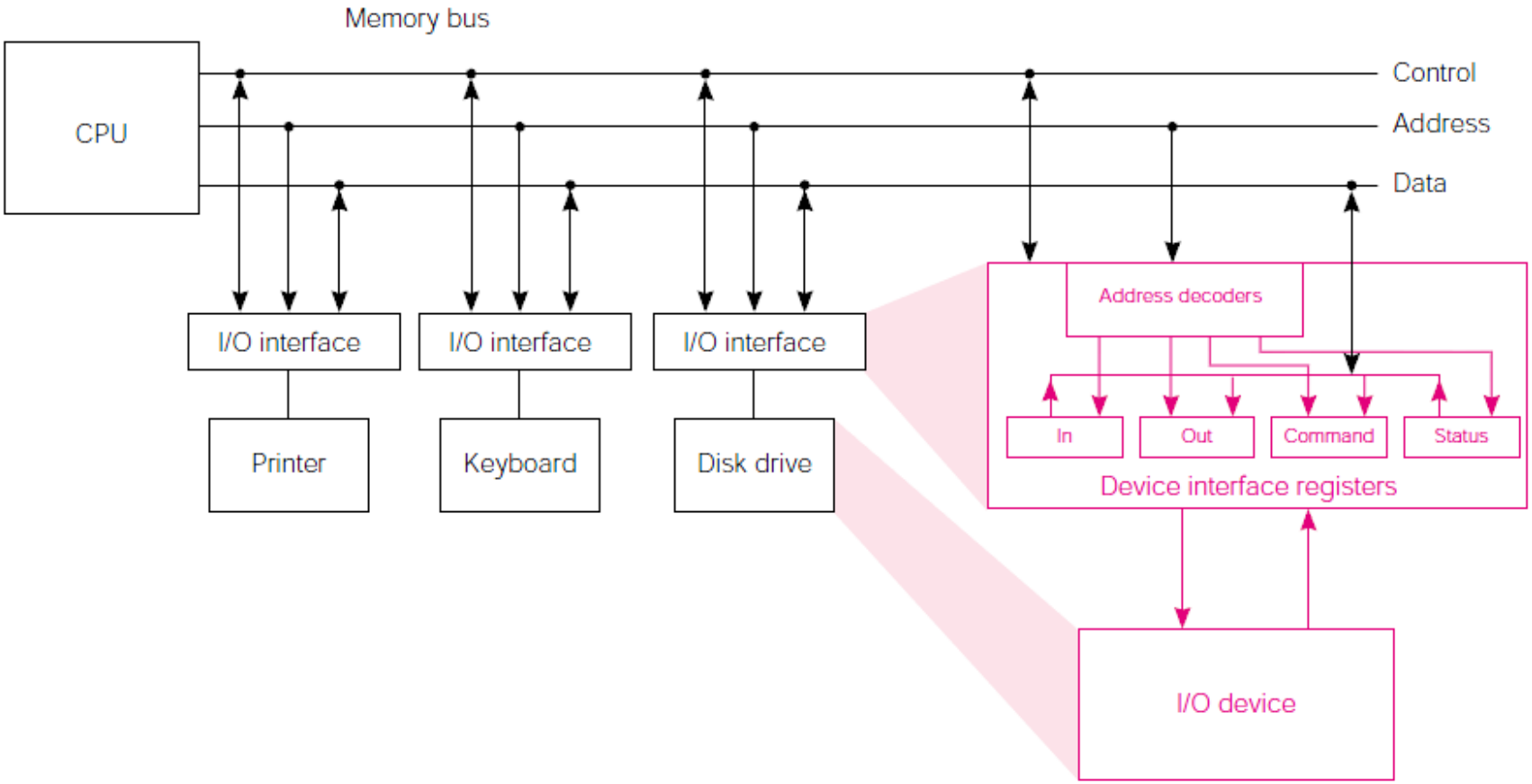


Programmed I/O Device Interface Structure

- Processor must know when output device can accept new data
- Processor must know when input device is ready to supply new data
- Synchronization can be done by processor reading device status bits
  - Data available signal from input device
  - Ready to accept output data from output device
- Example status bits:
  - Input data ready
  - Output device busy or off-line
- Example control bits:
  - Reset device
  - Start read or start write

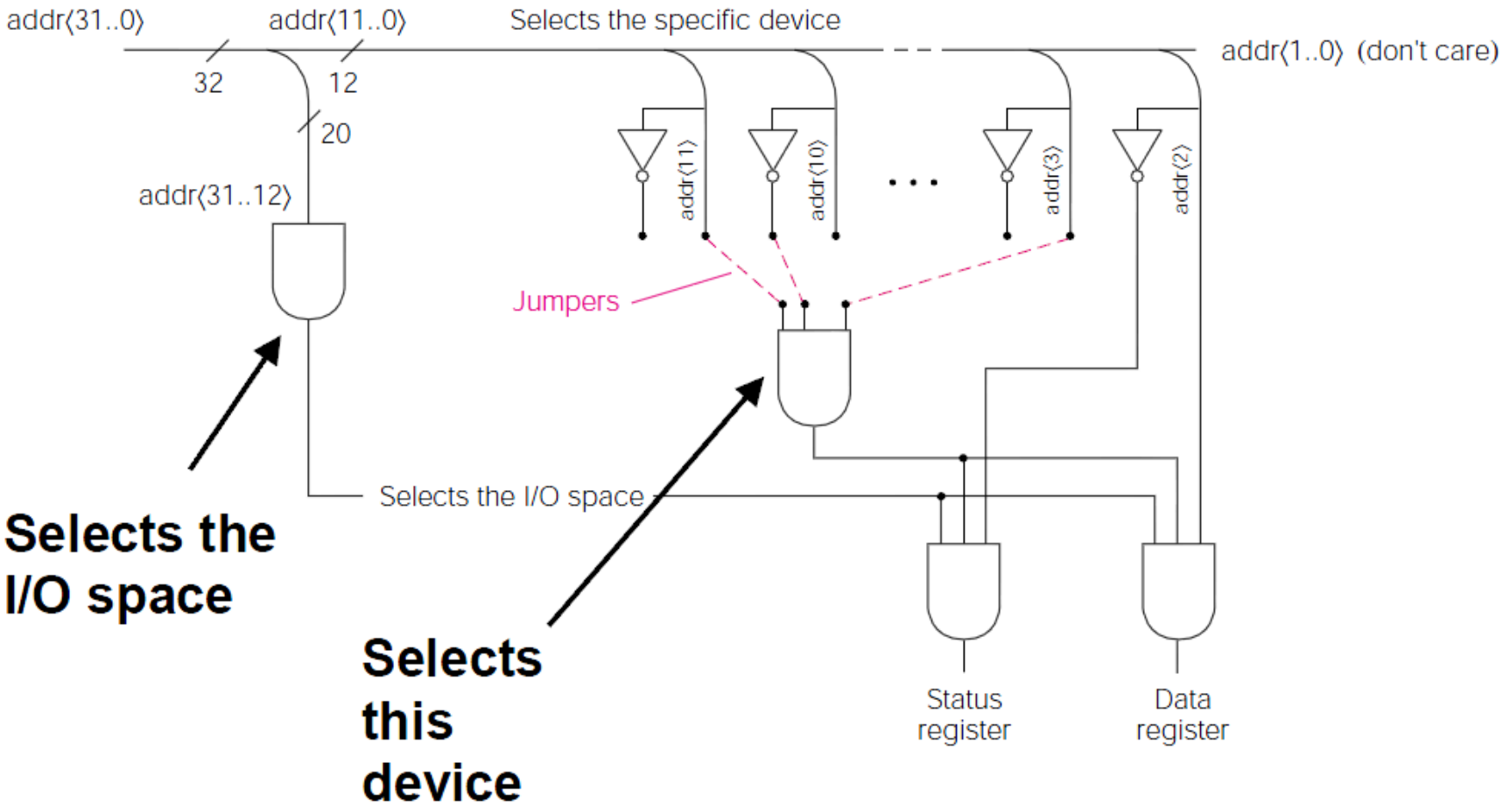
Programmed I/O

Device Interface Structure



Programmed I/O

Device Interface Structure



پایان

موفق و پیروز باشید