به نام خدا

حافظه‌ها

انواع حافظه و کارکردن با تراشه‌های مختلف حافظه

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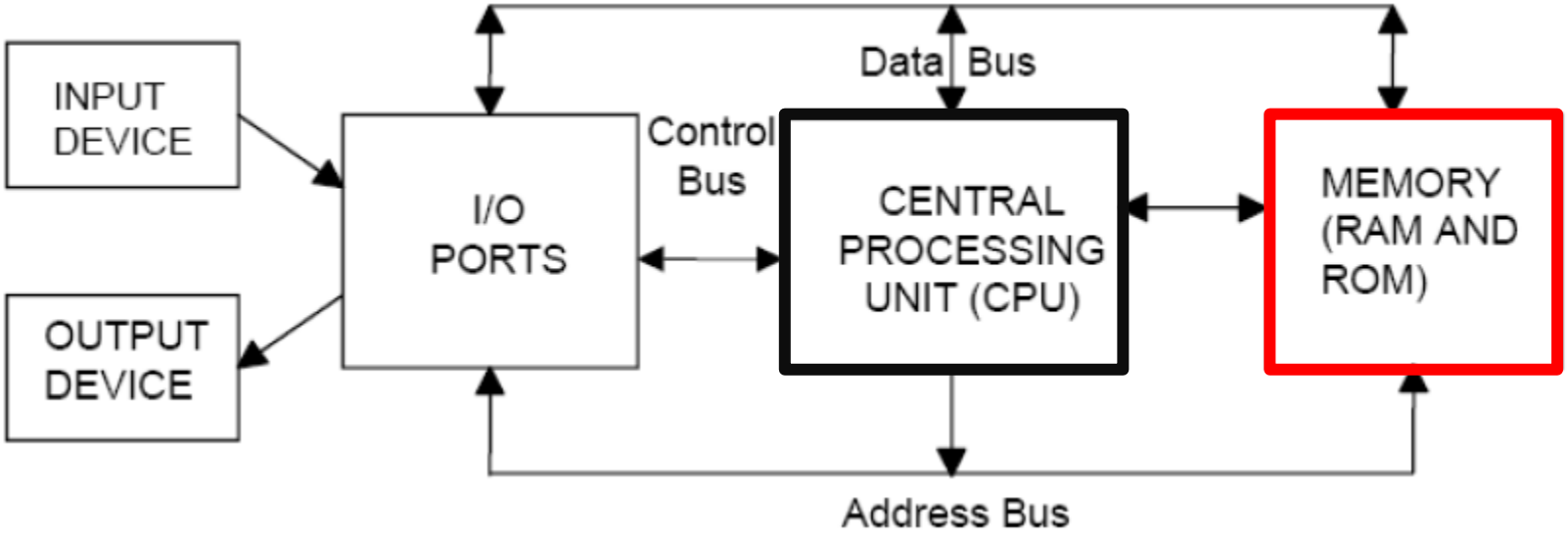
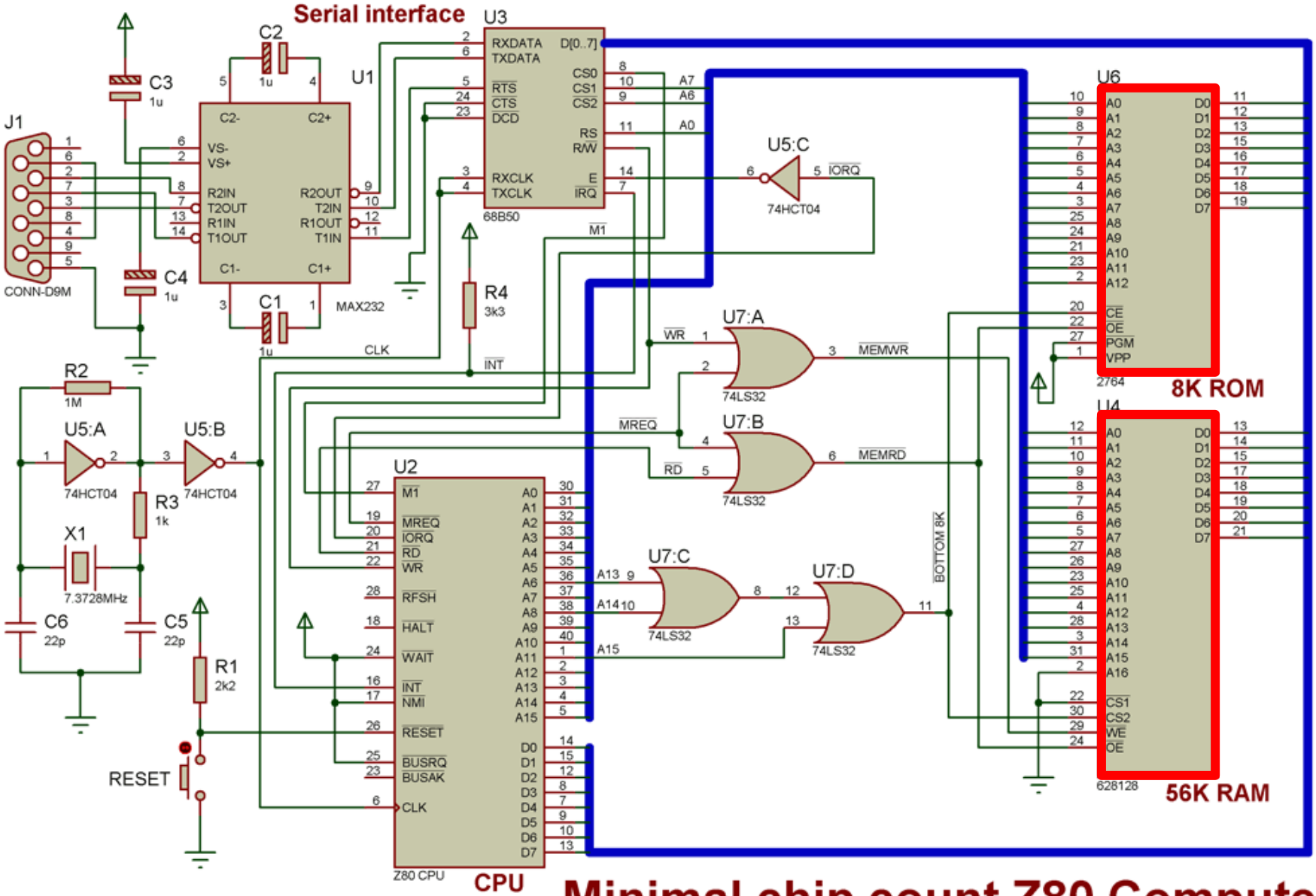
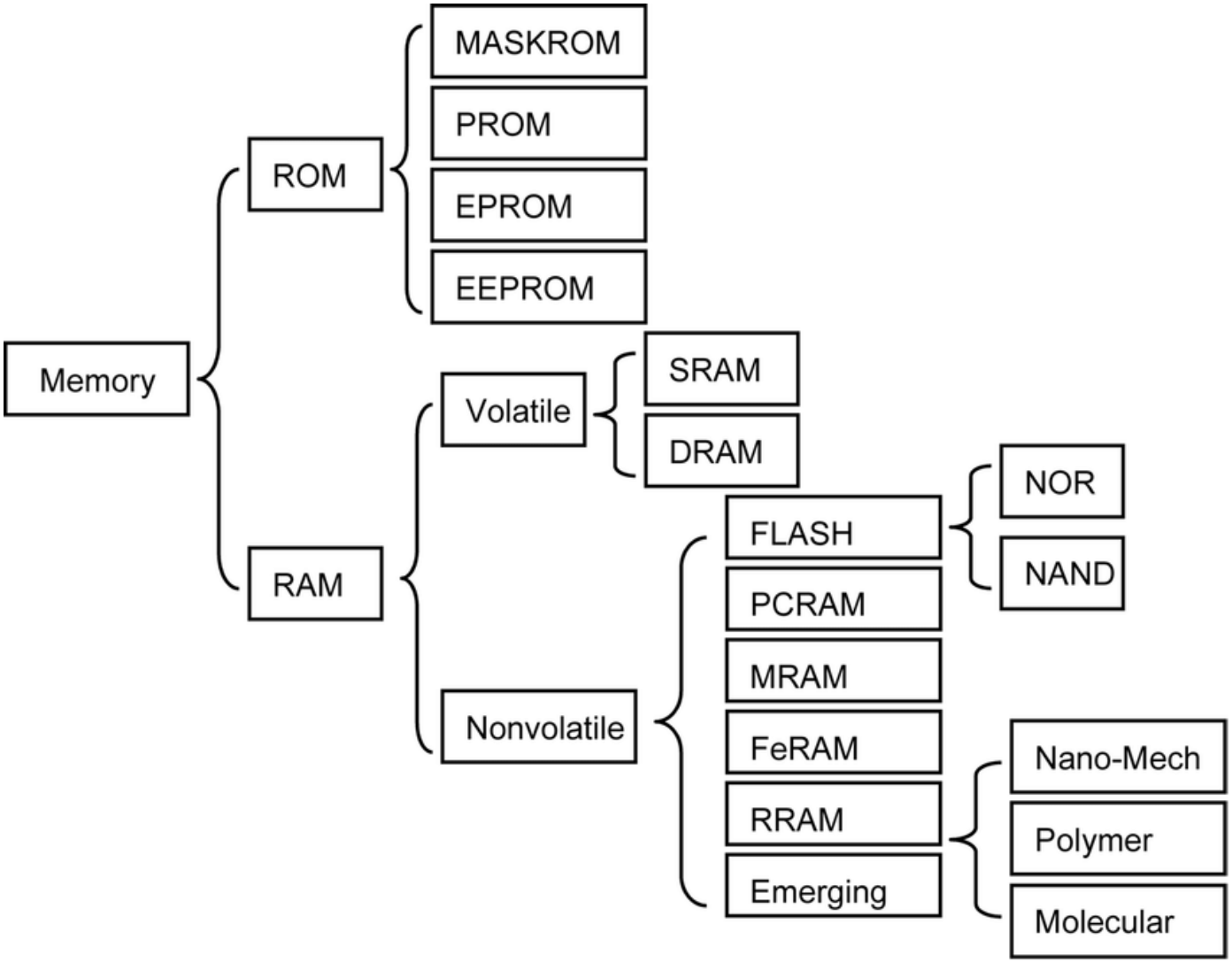
ساختار یک سیستم کامپیوتری





Minimal chip count Z80 Computer

دسته‌بندی حافظه‌ها

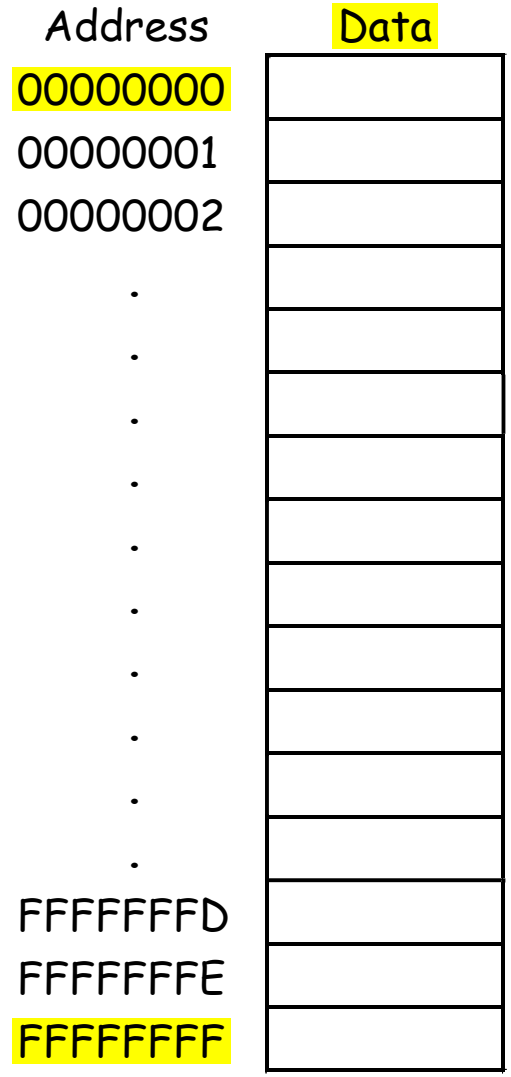


RAM

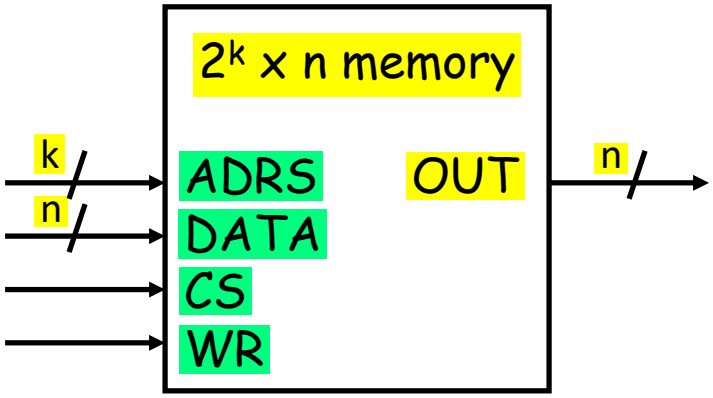
- Random-access memory, or RAM
  - provides large quantities of **temporary** storage in a computer system.
- Remember the basic capabilities of a memory:
  - **store a value**.
  - **read the value** that was saved.
  - **change** the stored value.
- A **RAM** can **store *many* values**.
  - An address will specify which memory value we're interested in.
  - Each value can be a multiple-bit word (e.g., 32 bits).

Picture of memory

- You can think of computer memory as being one big array of data.
  - The address serves as an array index.
  - Each address refers to one word of data.
- You can read or modify the data at any given memory address, just like you can read or modify the contents of an array at any given index.



Block diagram of RAM

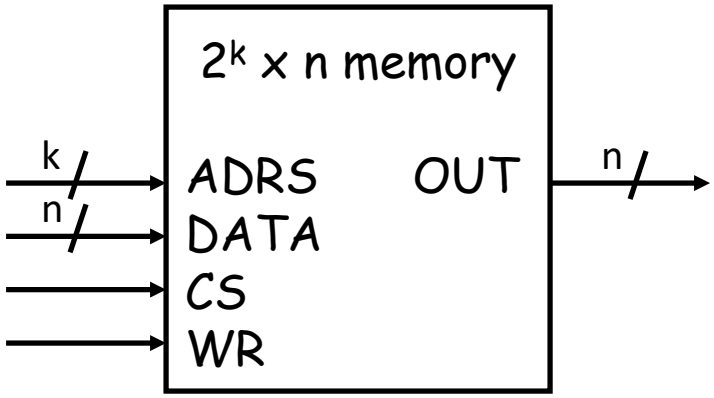


CS	WR	Memory operation
0	x	None
1	0	Read selected word
1	1	Write selected word

- This block diagram introduces the main interface to RAM.
  - A Chip Select, CS, enables or disables the RAM.
  - ADRS specifies the address or location to read from or write to.
  - WR selects between reading from or writing to the memory.
    - To read from memory, WR should be set to 0.
      OUT will be the n-bit value stored at ADRS.
    - To write to memory, we set WR = 1.
      DATA is the n-bit value to save in memory.
- This interface makes it easy to combine RAMs together, as we'll see.

اندازه حافظه

- We refer to this as a 2^k x n memory.
  - There are k *address lines*, which can specify one of 2^k addresses.
  - Each address contains an n-bit word.



- For example

  a 2^{24} x 16 RAM contains 2^{24} = 16M words, each 16 bits long.
  - The RAM would need 24 address lines.
  - The total storage capacity is 2^{24} x 16 = 2^{28} bits.

اندازه حافظه

- Memory sizes are usually specified in numbers of bytes (8 bits).
- The 2^{28}-bit memory on the previous page translates into:

2^{28} bits / 8 bits per byte = 2^{25} bytes

- With the abbreviations below, this is equivalent to 32 megabytes.

	Prefix	Base 2	Base 10
K	Kilo	2^{10} = 1,024	10^3 = 1,000
M	Mega	2^{20} = 1,048,576	10^6 = 1,000,000
G	Giga	2^{30} = 1,073,741,824	10^9 = 1,000,000,000

Big-Endian & Little-Endian Storage

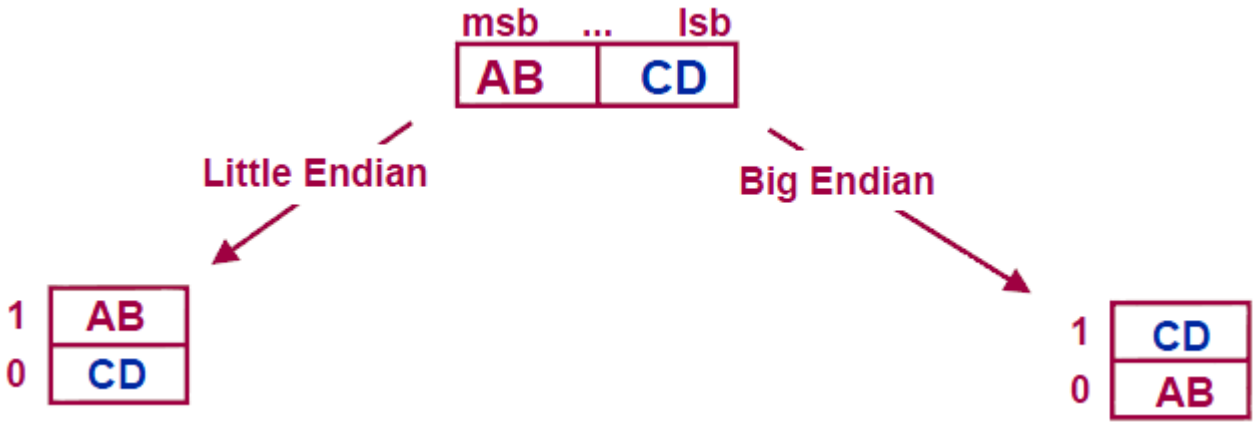
- When data types having a word size larger than the smallest addressable unit are stored in memory the question arises,

  Is the least significant part of the word stored at the lowest address (*little Endian, little end first*)

  or

  is the most significant part of the word stored at the lowest address (*big Endian, big end first*)?

Example: The hexadecimal 16-bit number ABCDH, stored at address 0:



The CPU–Main Memory Interface

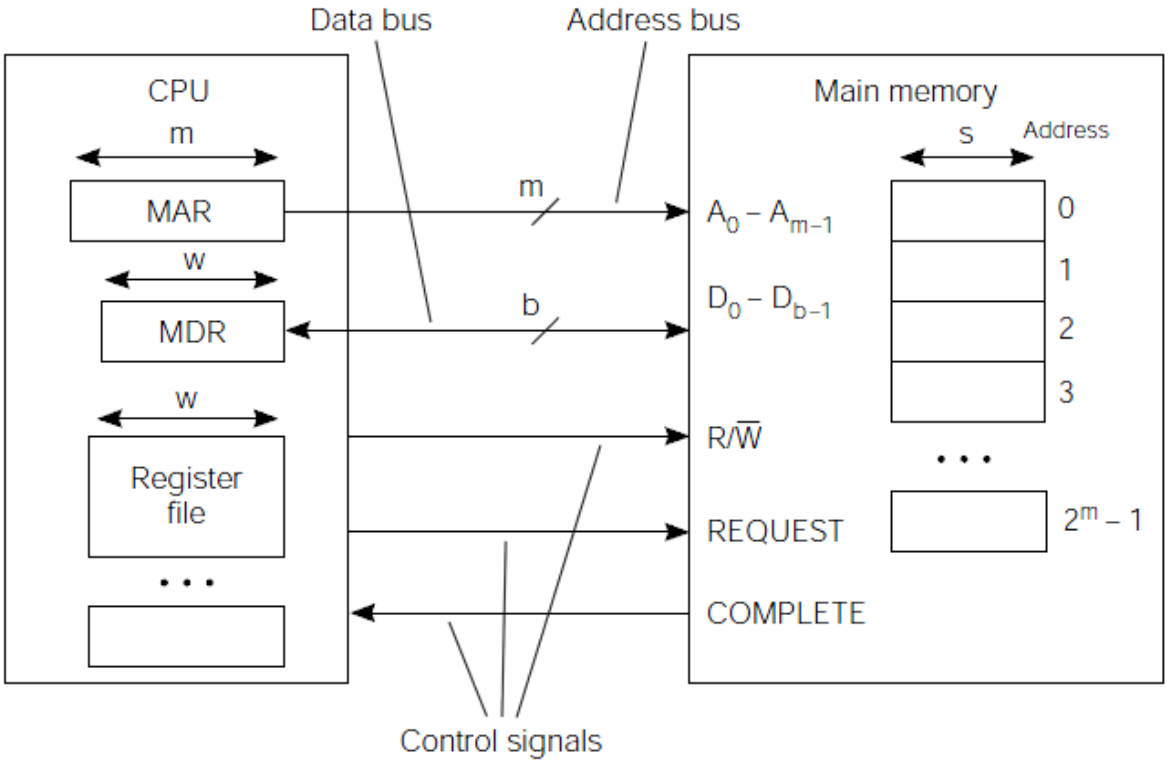
Sequence of events:

•Read:

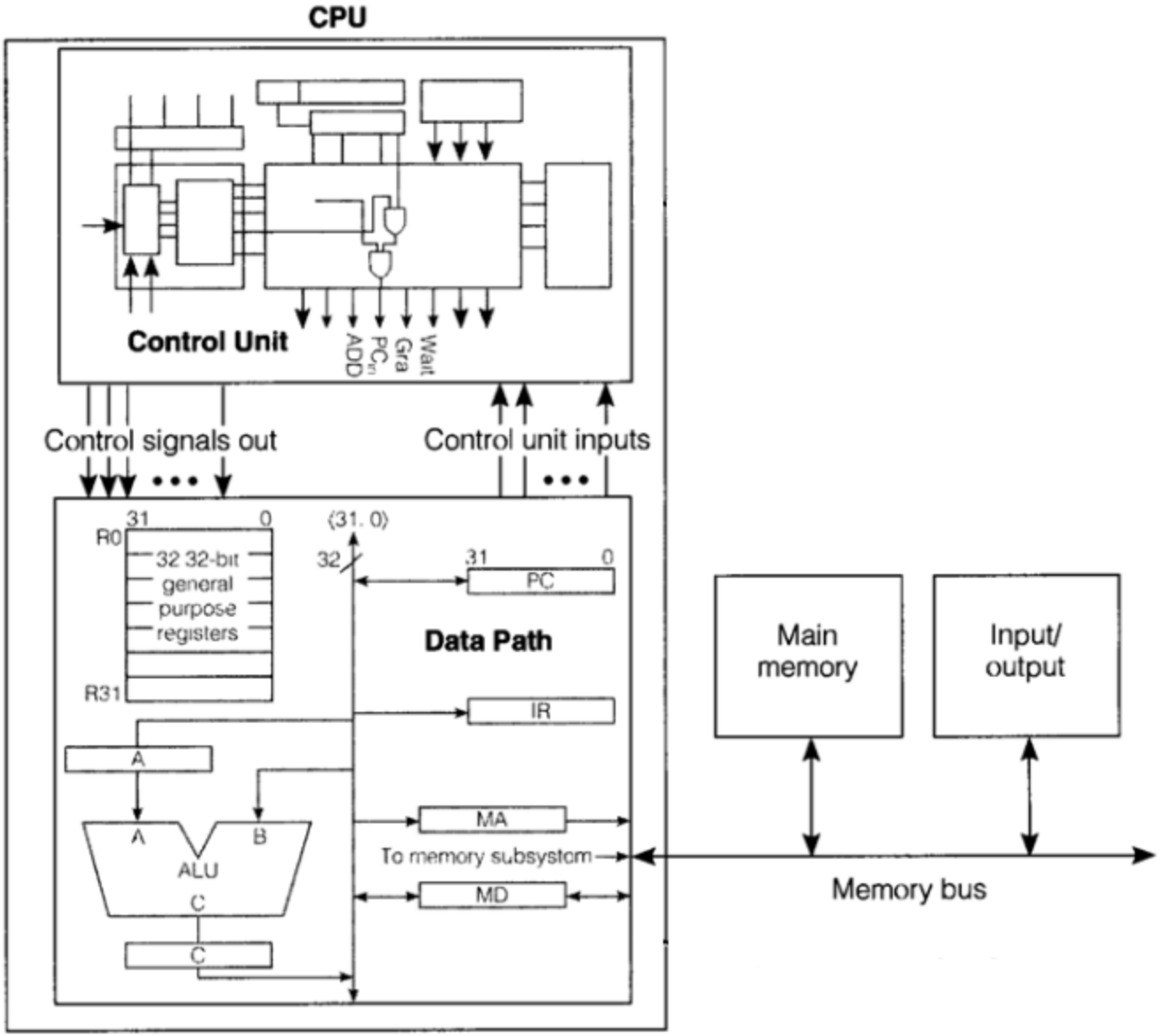
1. CPU loads MAR, issues Read, and REQUEST
2. Main Memory transmits words to MDR
3. Main Memory asserts COMPLETE.

•Write:

1. CPU loads MAR and MDR, asserts Write, and REQUEST
2. Value in MDR is written into address in MAR.
3. Main Memory asserts COMPLETE.

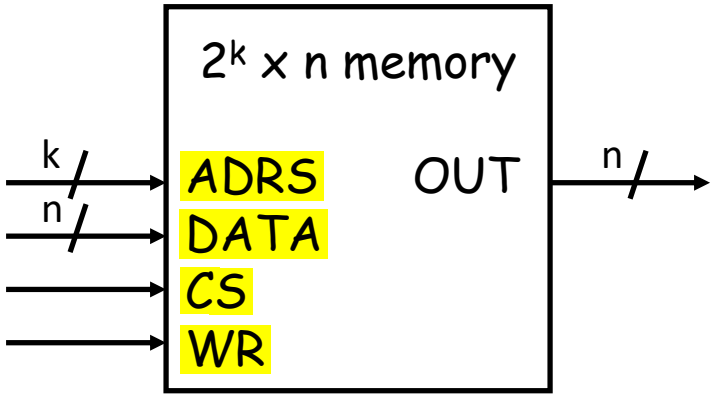


The CPU–Main Memory Interface



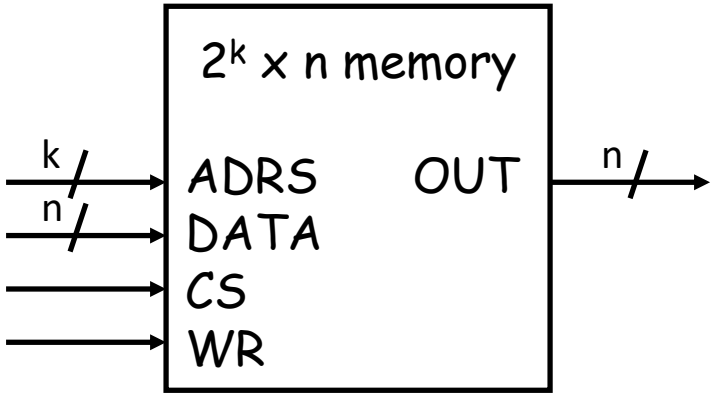
Reading RAM

- To *read* from this RAM, the controlling circuit must:
  - Enable the chip by ensuring CS = 1.
  - Select the read operation, by setting WR = 0.
  - Send the desired address to the ADRS input.
  - The contents of that address appear on OUT after a little while.
- Notice that the DATA input is unused for read operations.



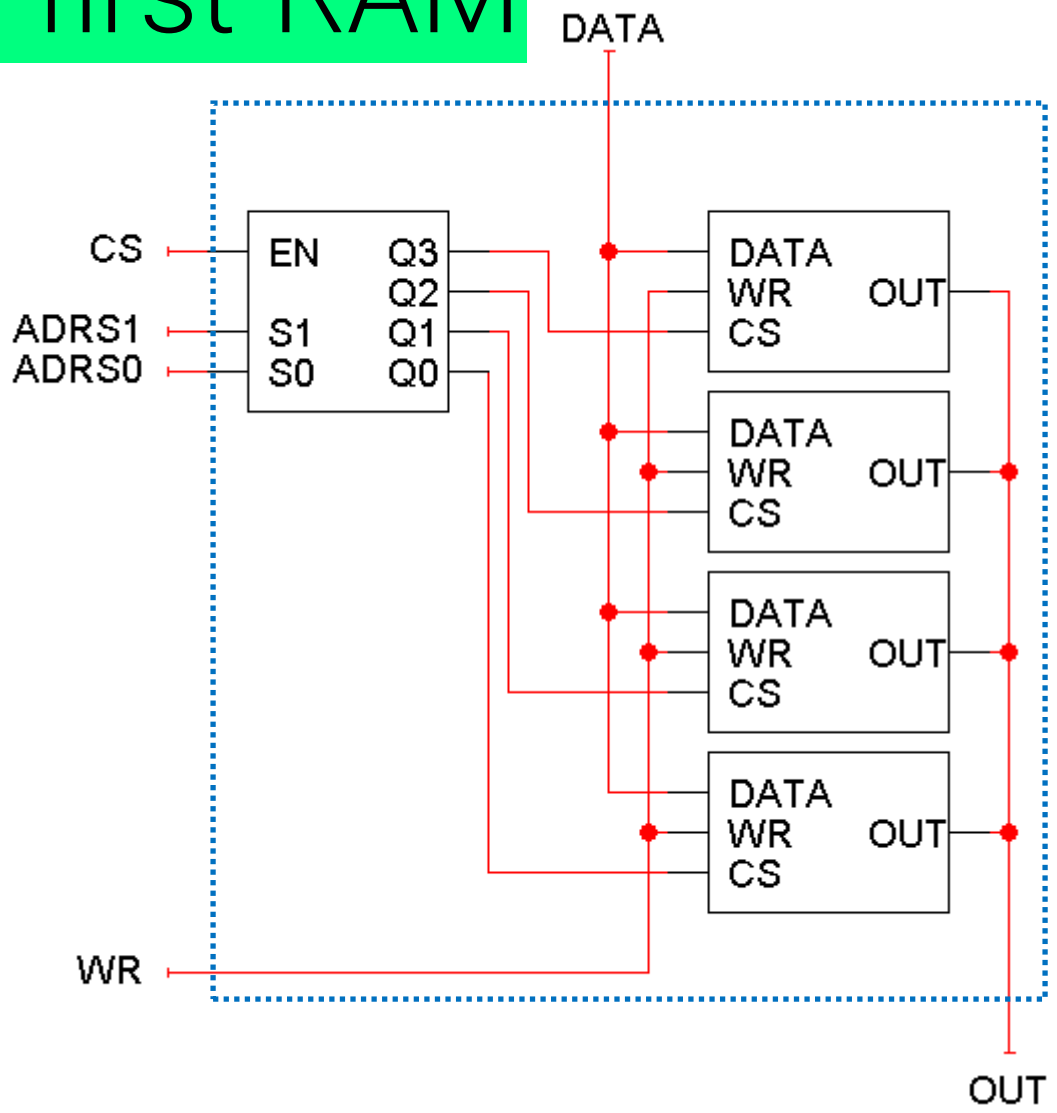
Writing RAM

- To *write* to this RAM, you need to:
  - Enable the chip by setting CS = 1.
  - Select the write operation, by setting WR = 1.
  - Send the desired address to the ADRS input.
  - Send the word to store to the DATA input.
- The output OUT is not needed for memory write operations.



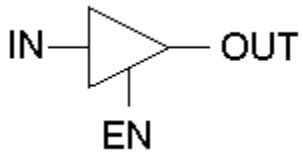
My first RAM

- We can use these cells to make a 4 x 1 RAM.
- Since there are four words, ADRS is two bits.
- Each word is only one bit, so DATA and OUT are one bit each.
- Word selection is done with a decoder attached to the CS inputs of the RAM cells. Only one cell can be read or written at a time.
- Notice that the outputs are connected together with a *single* line!



خروجی باس داده

- The triangle represents a three-state buffer.
- Unlike regular logic gates, the output can be one of *three* different possibilities, as shown in the table.

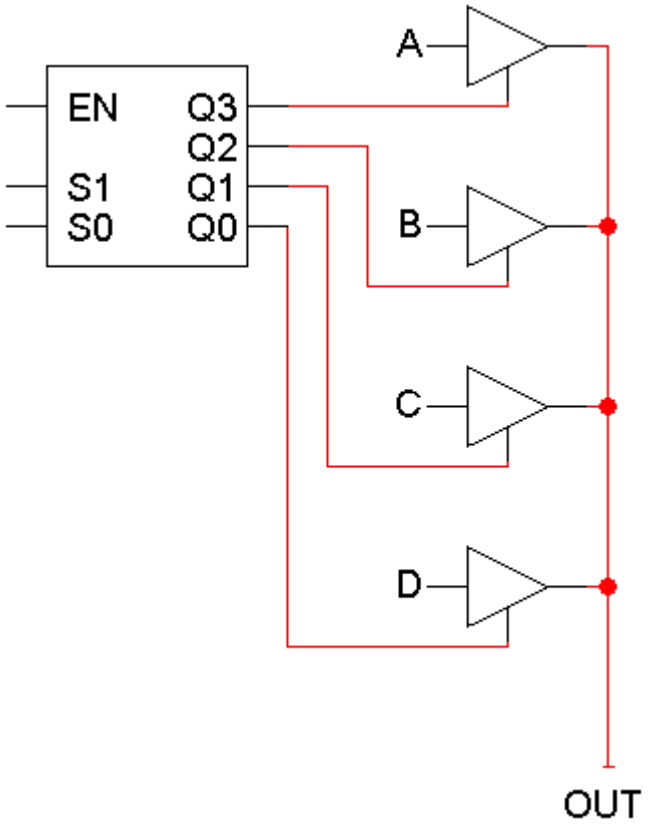


EN	IN	OUT
0	x	Disconnected
1	0	0
1	1	1

- "Disconnected" means no output appears at all, in which case it's safe to connect OUT to another output signal.
- The disconnected value is also sometimes called high impedance or Hi-Z.

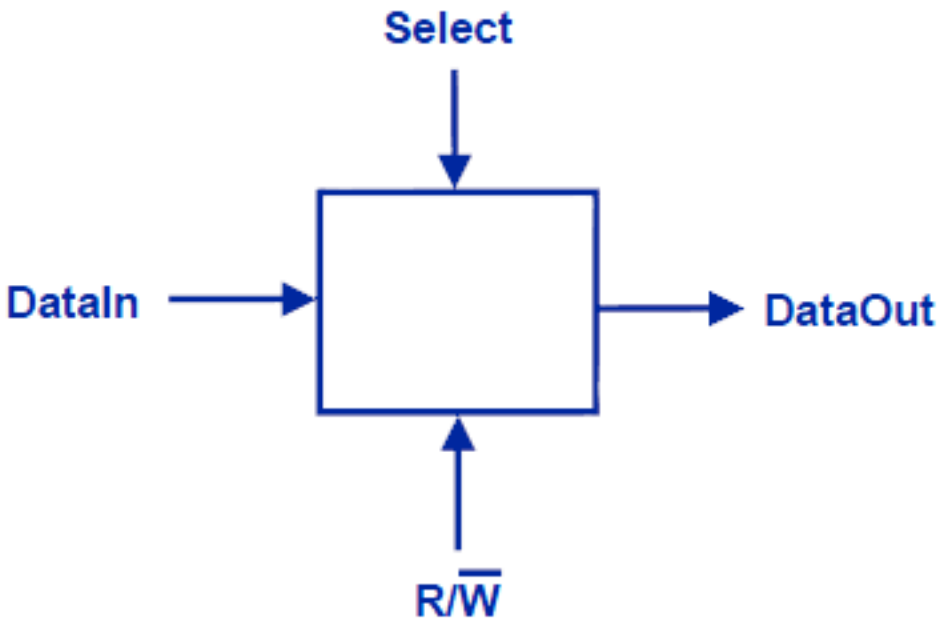
Connecting three-state buffers together

- You can connect several three-state buffer outputs together if you can *guarantee* that only one of them is enabled at any time.
- The easiest way to do this is to use a **decoder**!
- If the decoder is disabled, then all the three-state buffers will appear to be disconnected, and OUT will also appear disconnected.
- If the decoder is enabled, then exactly one of its outputs will be true, so only one of the tri-state buffers will be connected and produce an output.
- The net result is we can save some wire and gate costs. We also get a little more flexibility in putting circuits together.

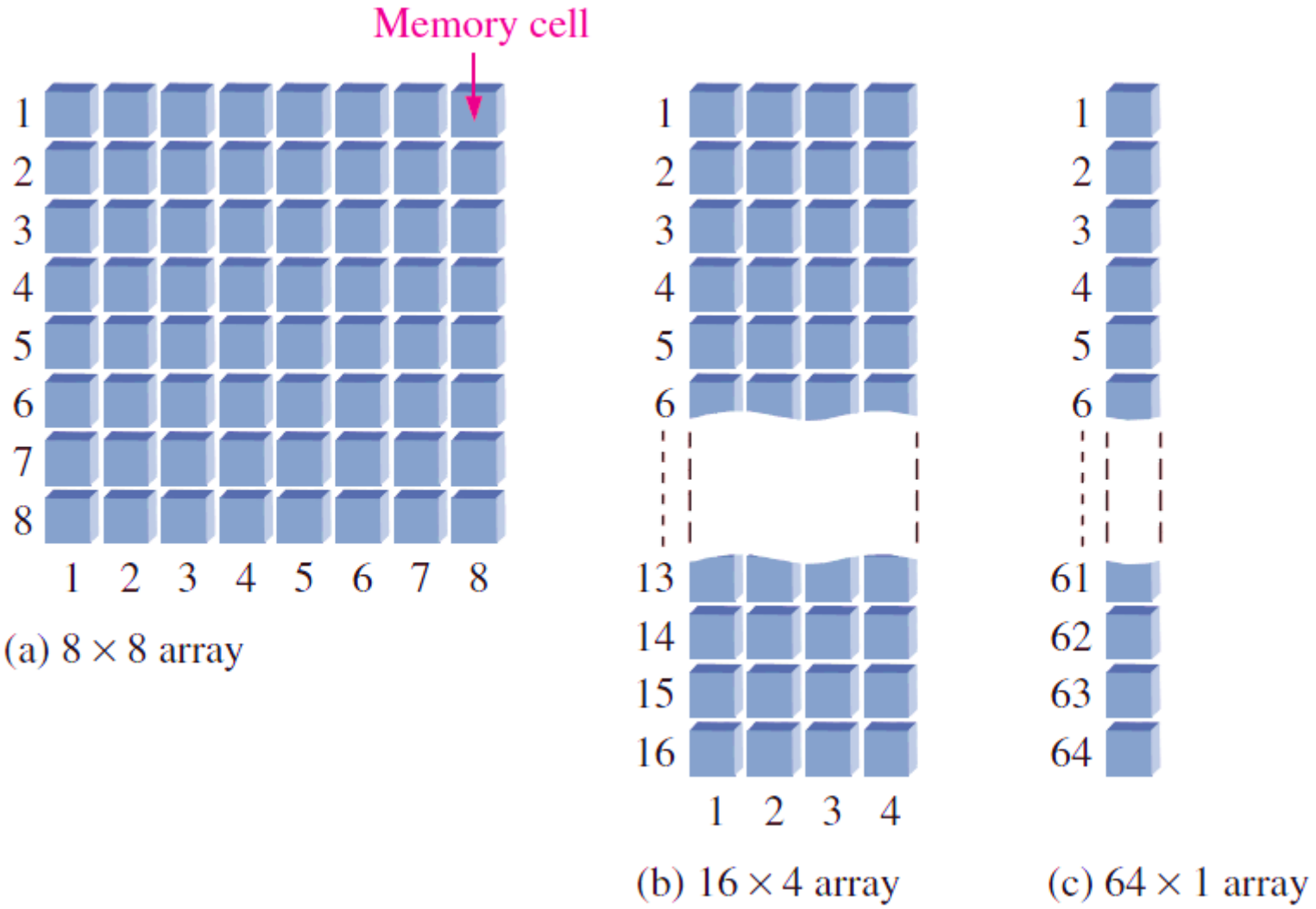


Memory Cells

- Regardless of the technology, all RAM memory cells provide
  - Select
  - DataIn
  - DataOut
  - R/W



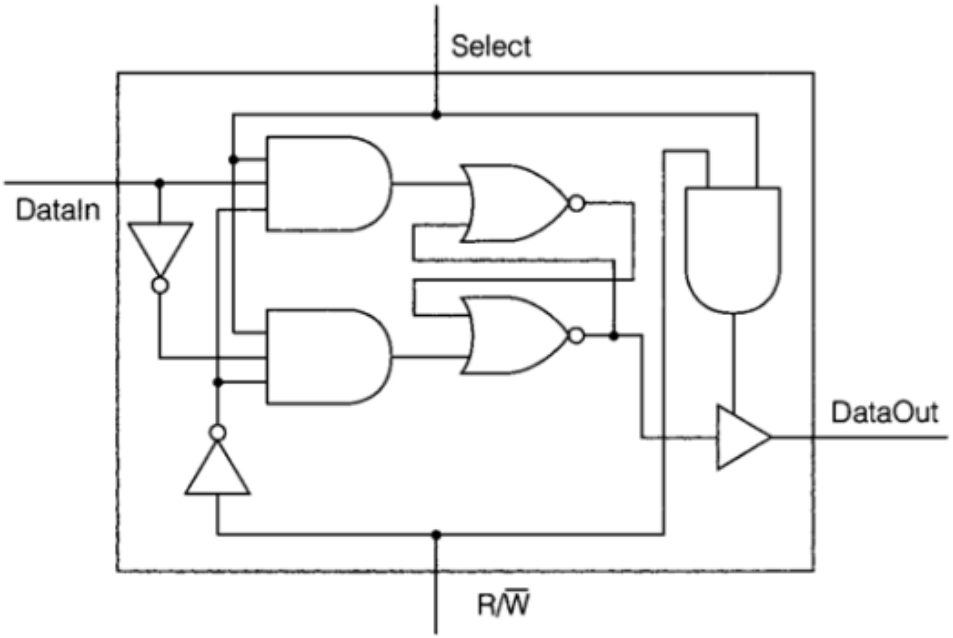
چینش خانه‌های حافظه

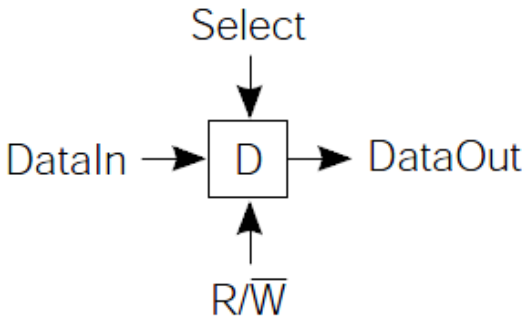


[**Book**]: Digital Fundamentals, by Thomas L. Floyd

Static RAM

D latch with added controls for selecting, reading and writing to the cell





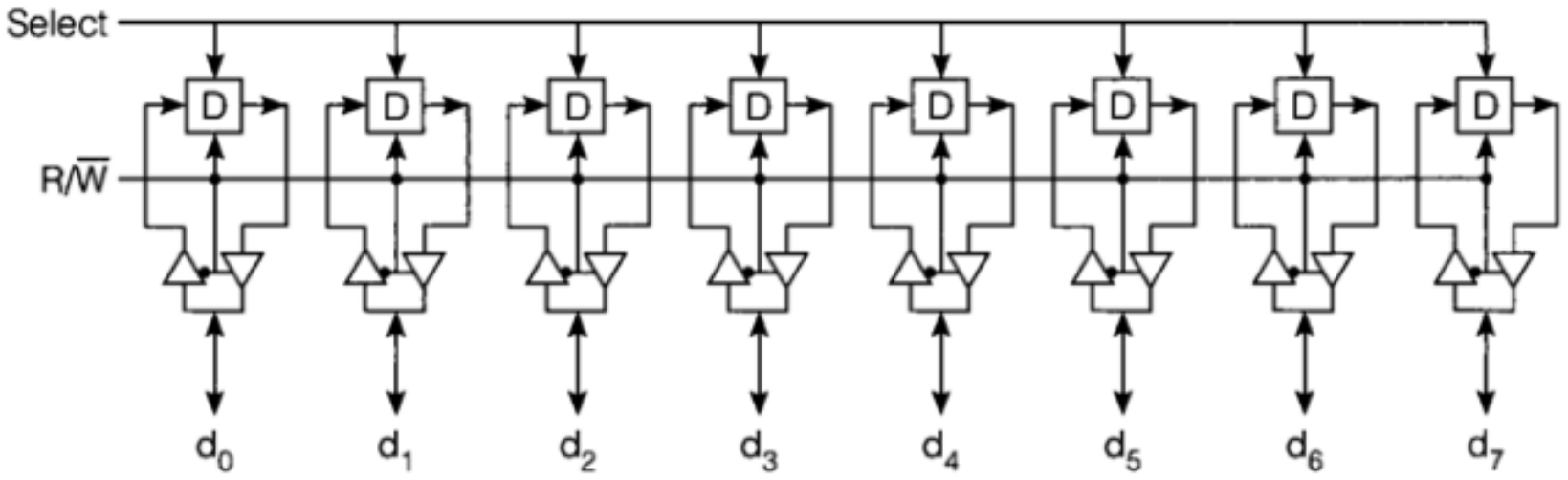
2 NOR gates for storage
5 gates for control
Cost of control exceeds cost of storage!!

This “static” RAM cell is unrealistic in practice, but it is functionally correct. We will discuss more practical designs later.

[**Book**]: Computer systems design and architecture, Vincent P. Heuring, Harry F. Jordan

8-bit register (1D RAM array)

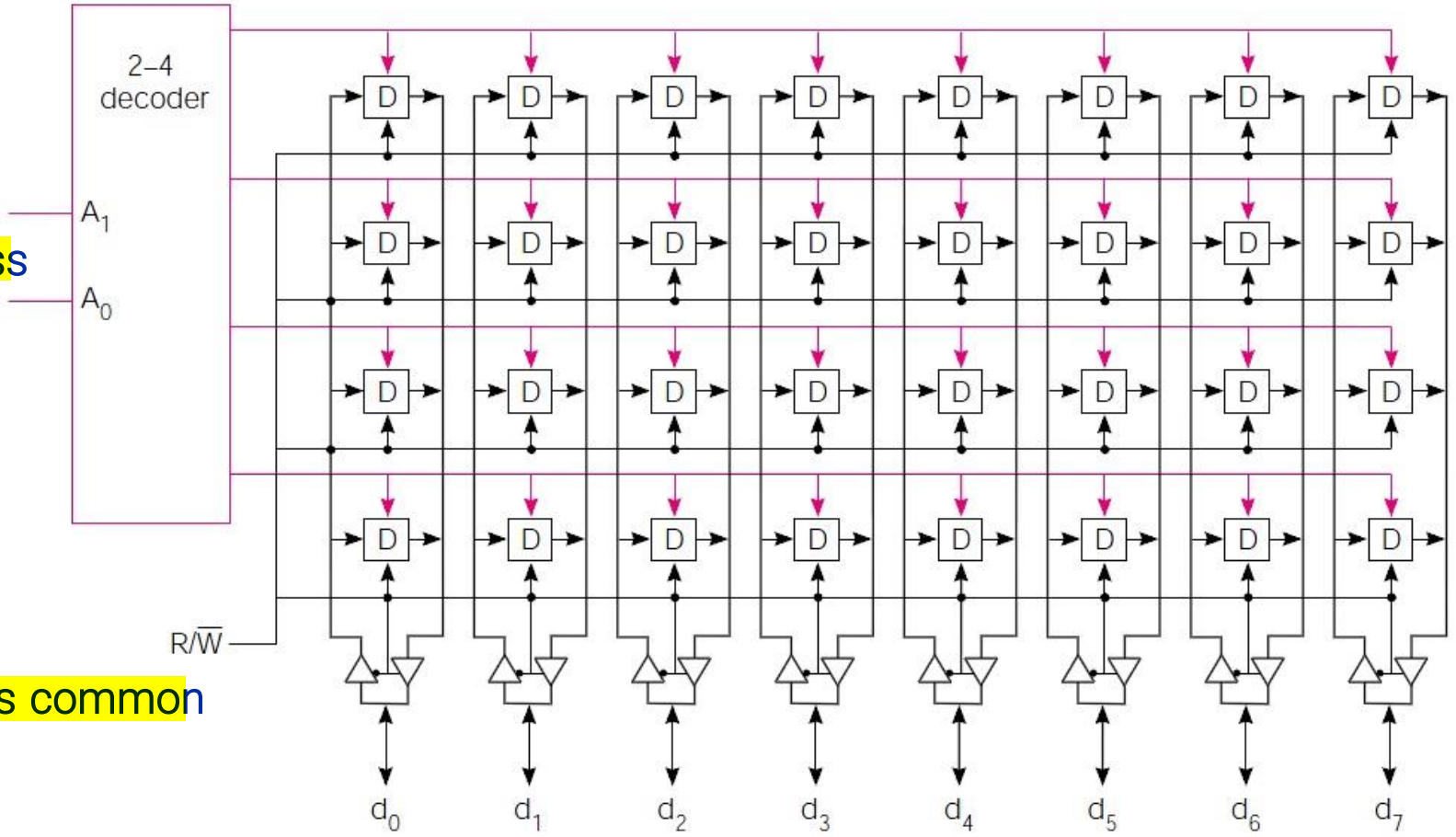
The entire register is selected with one select line, and uses one R/W line



Data bus is bi-directional, and buffered

4x8-bit (2D Memory cell array)

2-4 line decoder selects one of the four 8-bit arrays

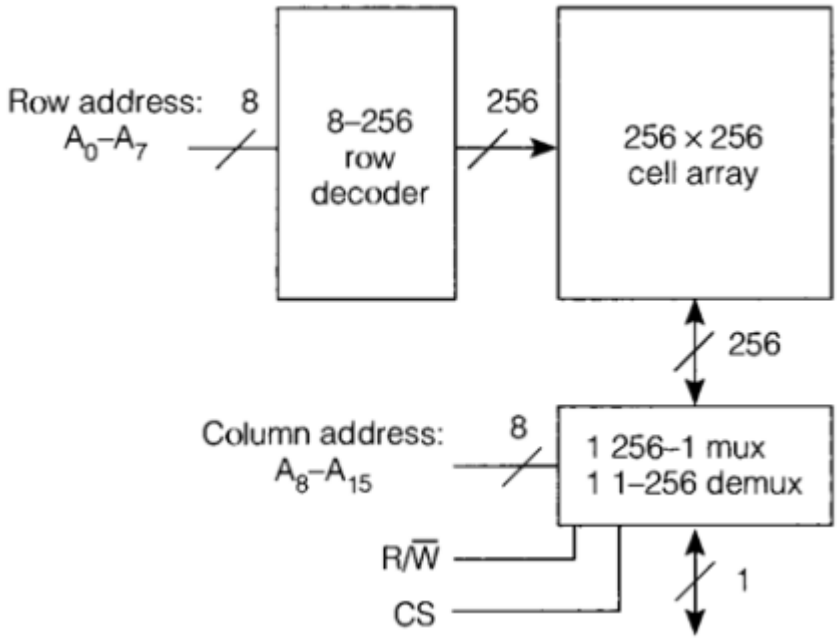


2-bit address

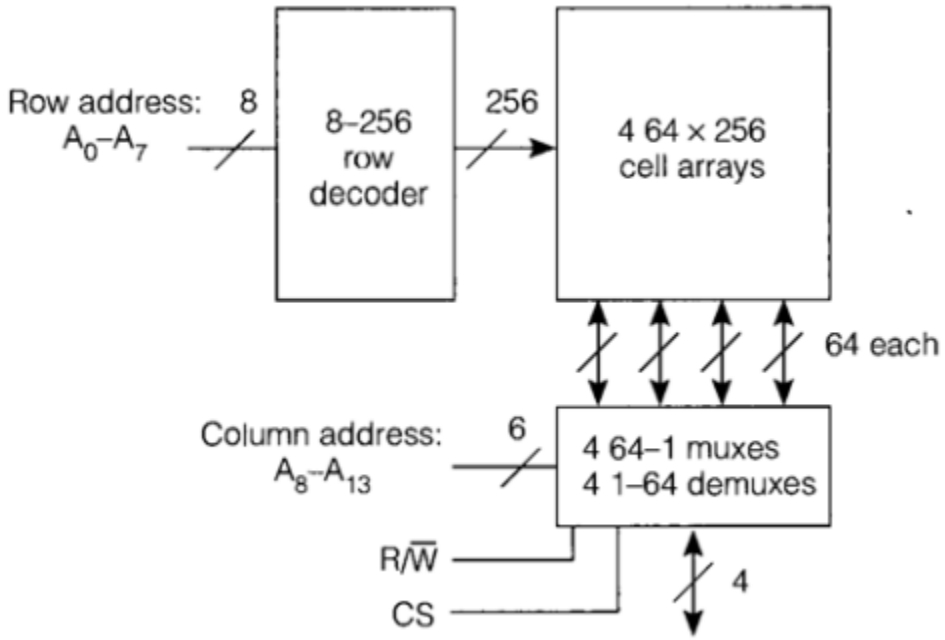
R/W is common to all

Bi-directional 8-bit buffered data bus

64k x 1 SRAM

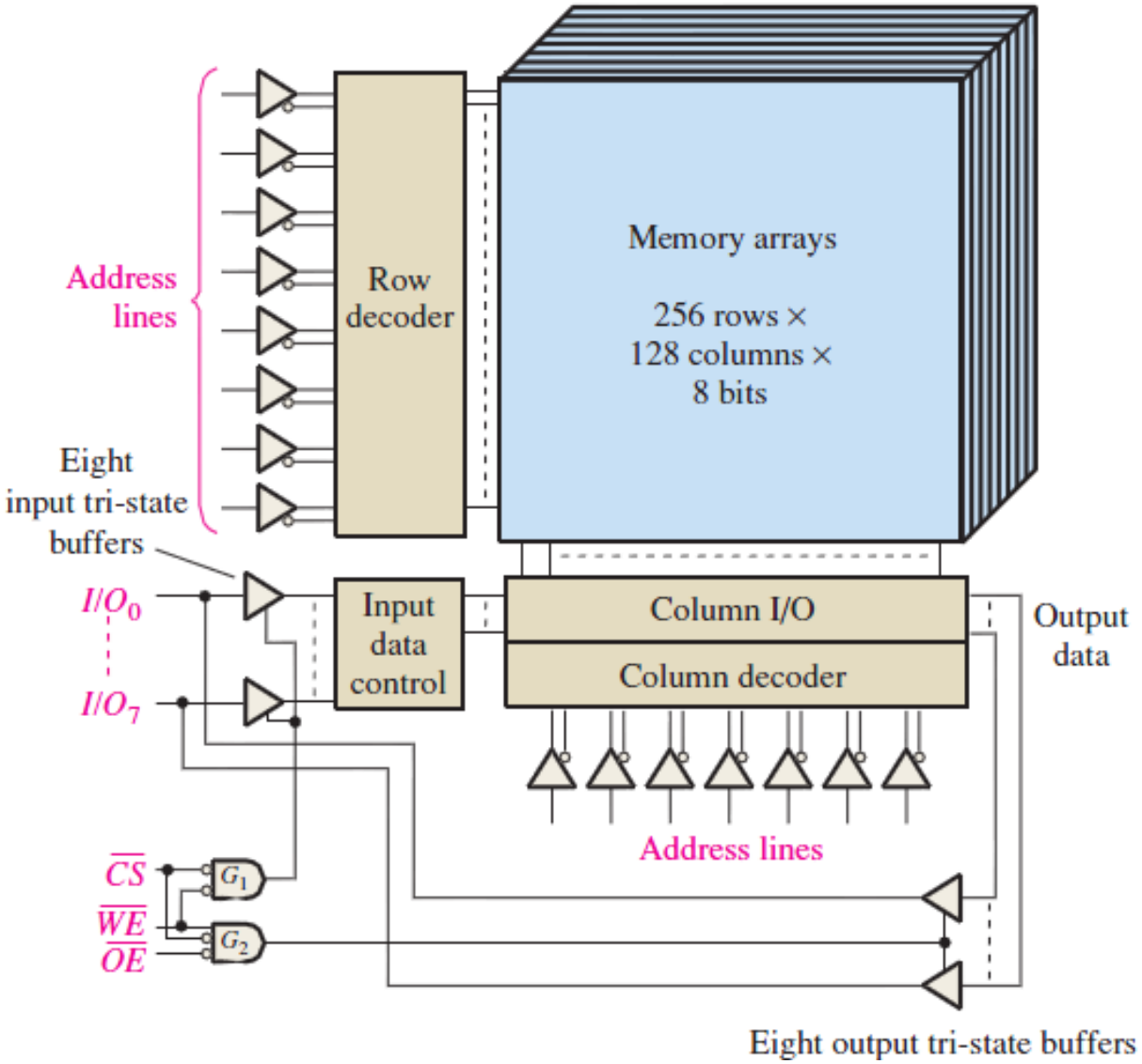


64 k x 1

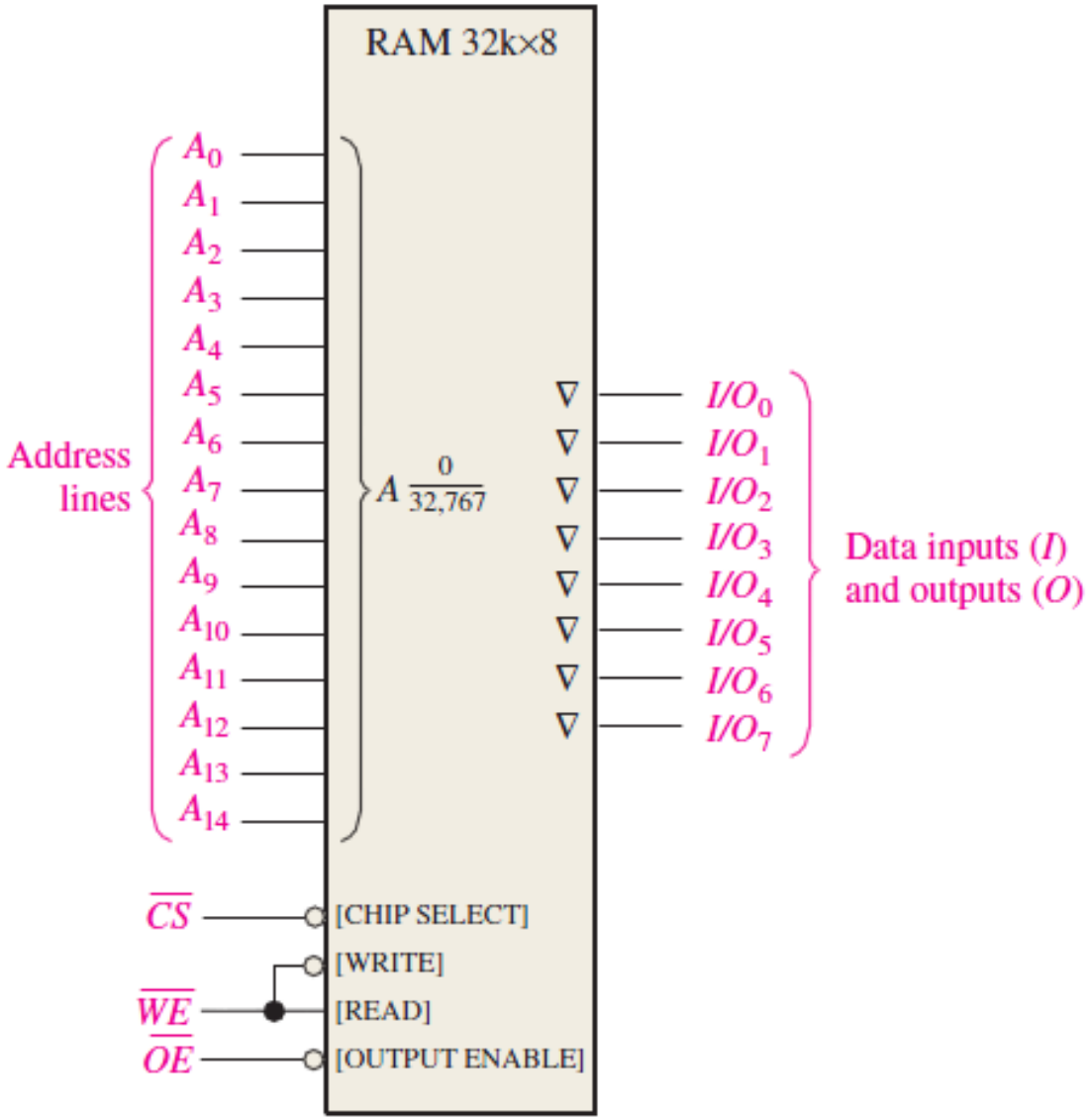


16 k x 4

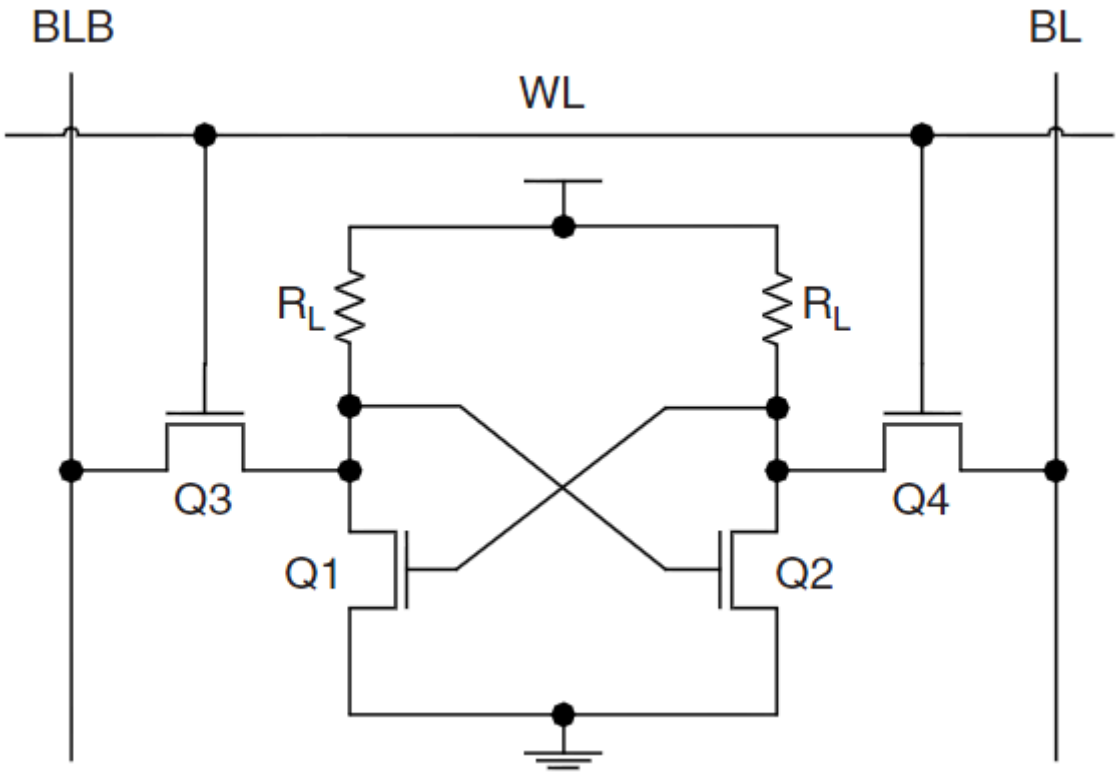
32k x 8 SRAM


Address lines
Row decoder
Memory arrays
256 rows ×
128 columns ×
8 bits
Eight input tri-state buffers
I/O_0
I/O_7
Input data control
Column I/O
Column decoder
Output data
Address lines
$\overline{CS}$
$\overline{WE}$
$\overline{OE}$
G_1
G_2
Eight output tri-state buffers

32k x 8 SRAM

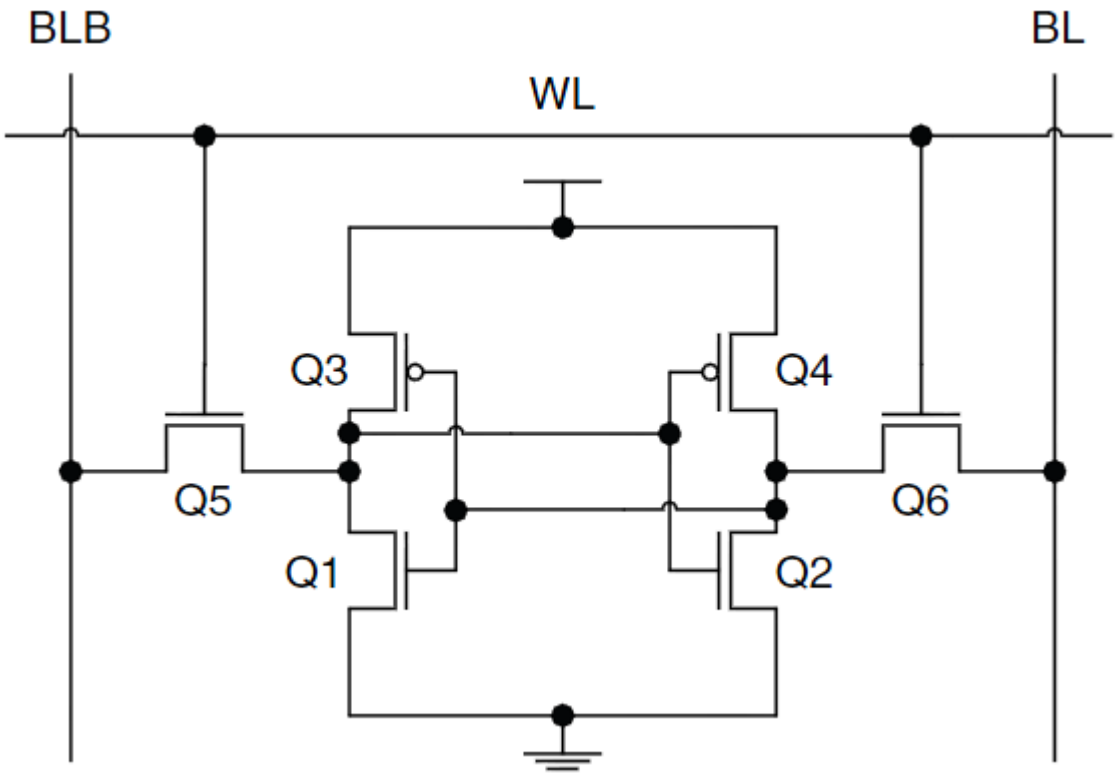

RAM 32k×8
Address lines
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
A_{10}
A_{11}
A_{12}
A_{13}
A_{14}
$A \frac{0}{32,767}$
I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7
Data inputs (I) and outputs (O)
$\overline{CS}$
[CHIP SELECT]
[WRITE]
$\overline{WE}$
[READ]
$\overline{OE}$
[OUTPUT ENABLE]

Four-transistor (4T) SRAM cell



[**Book**]: CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies

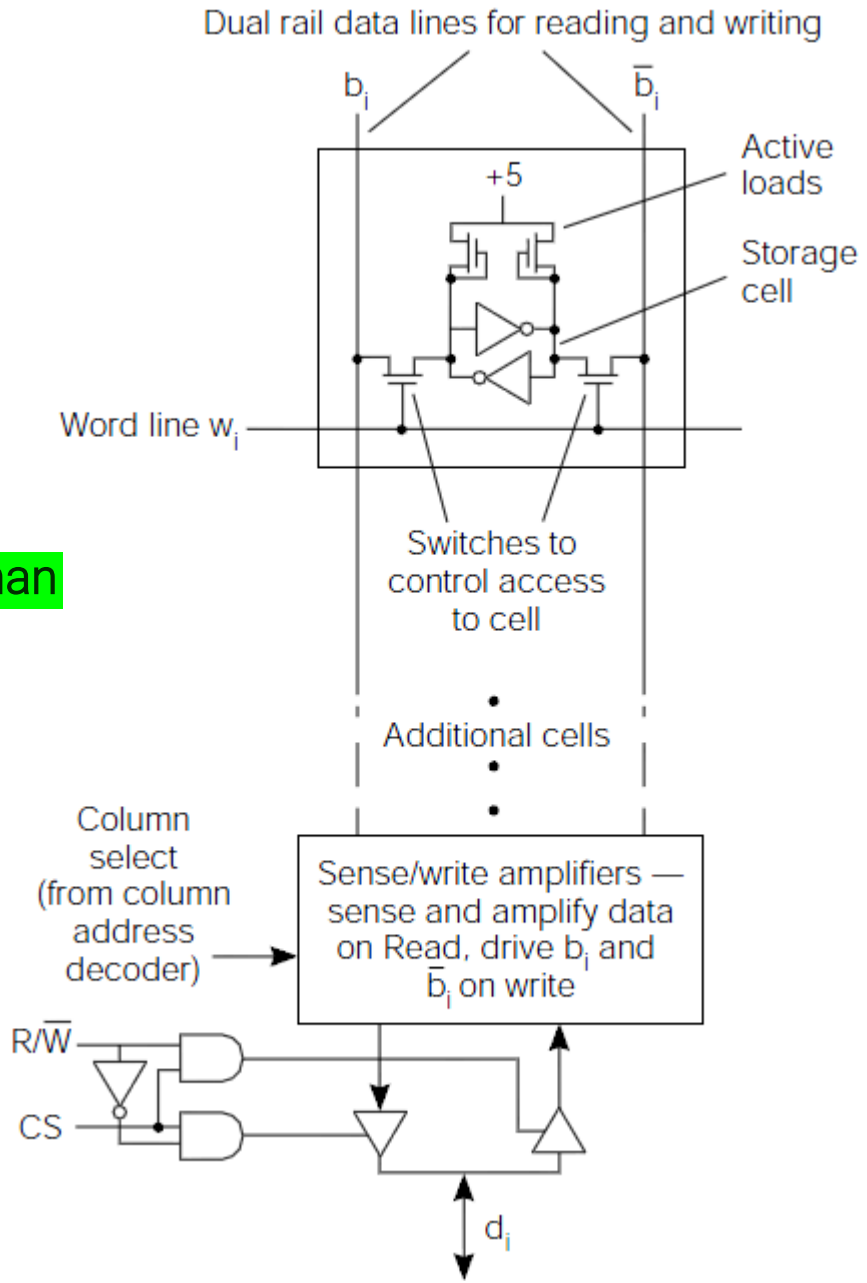
Six-transistor (6T) SRAM cell



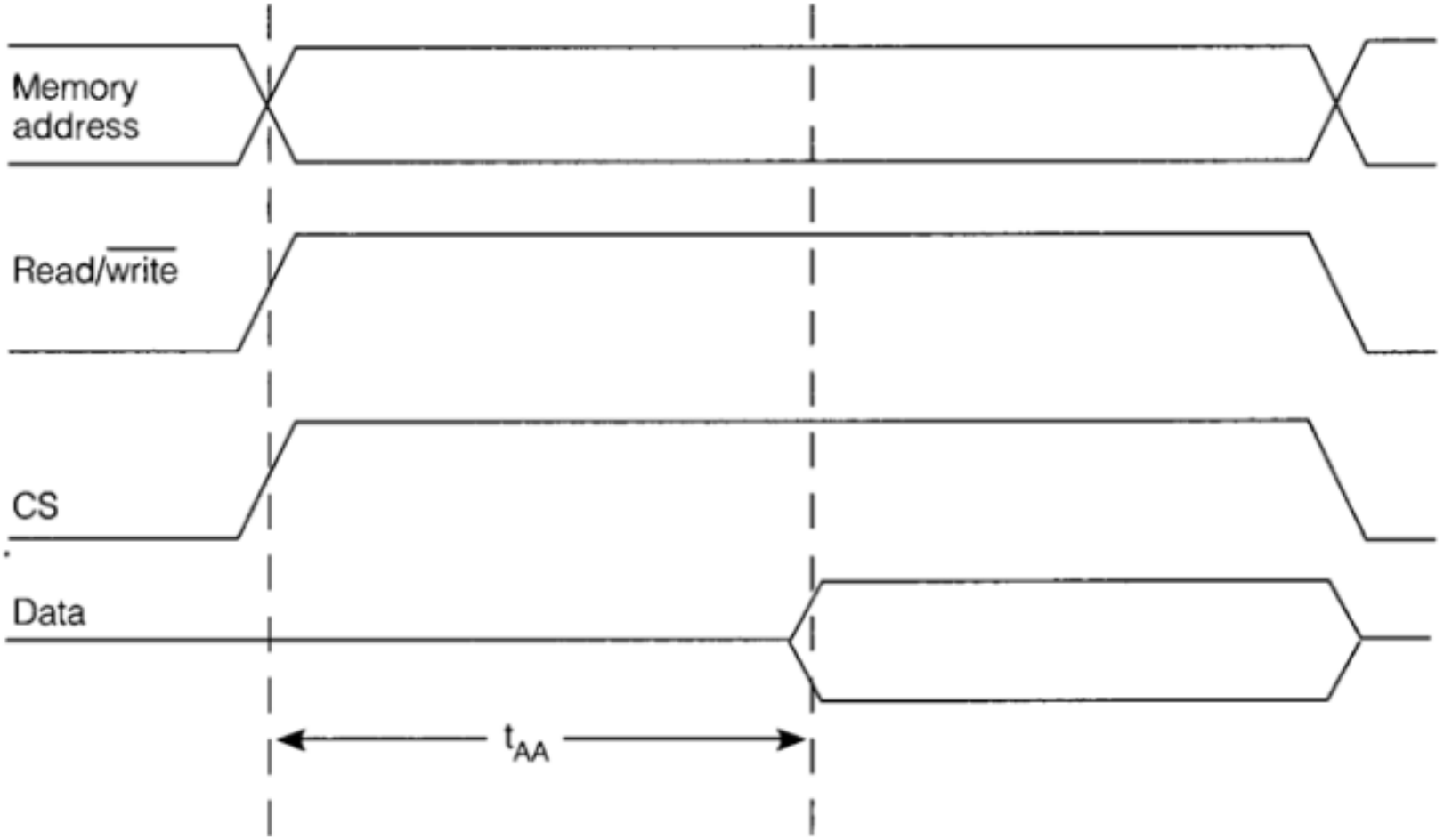
[**Book**]: CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies

6T SRAM cell

This is a more practical design than the 8-gate design.

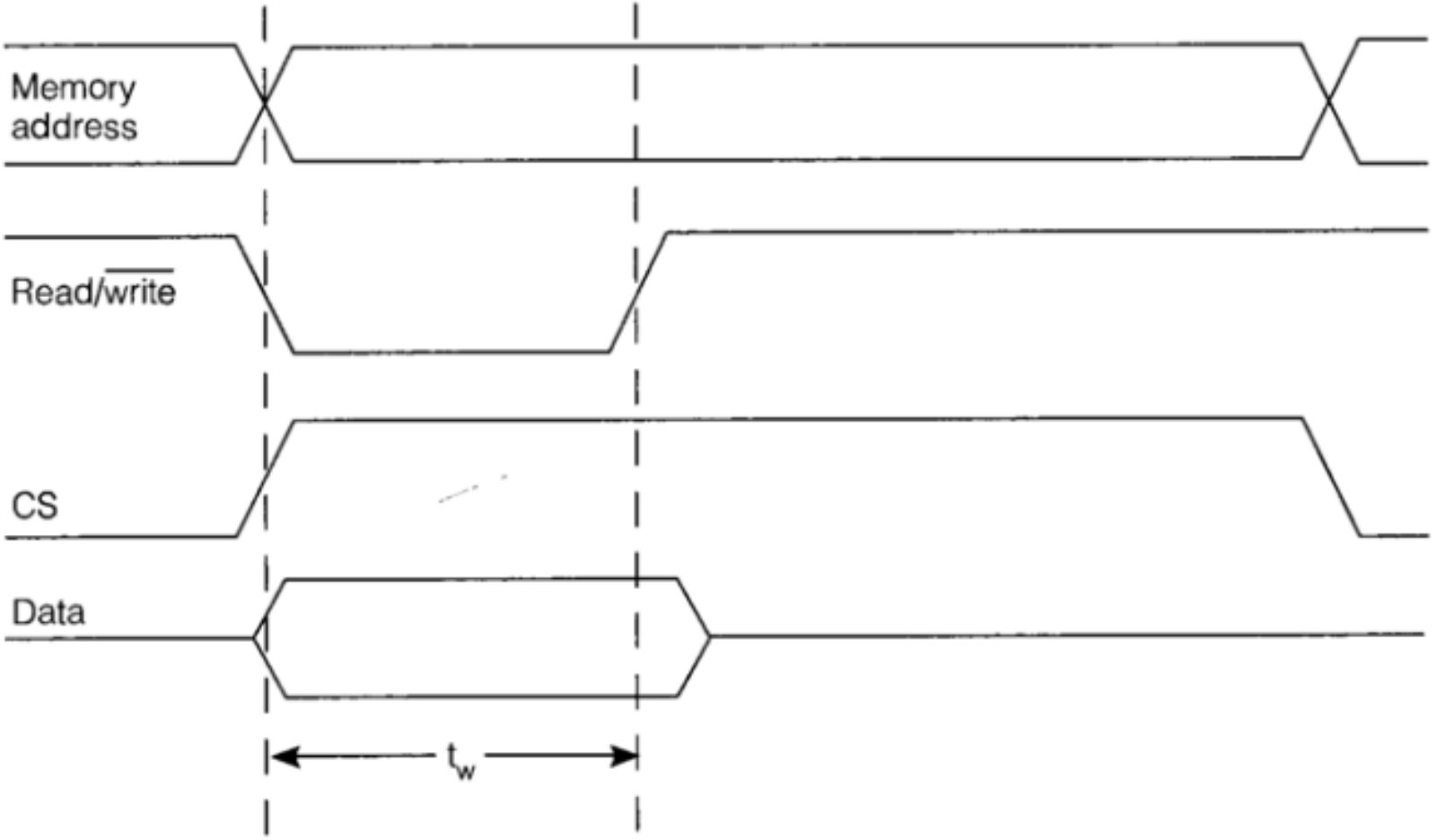


Static RAM Read Timing



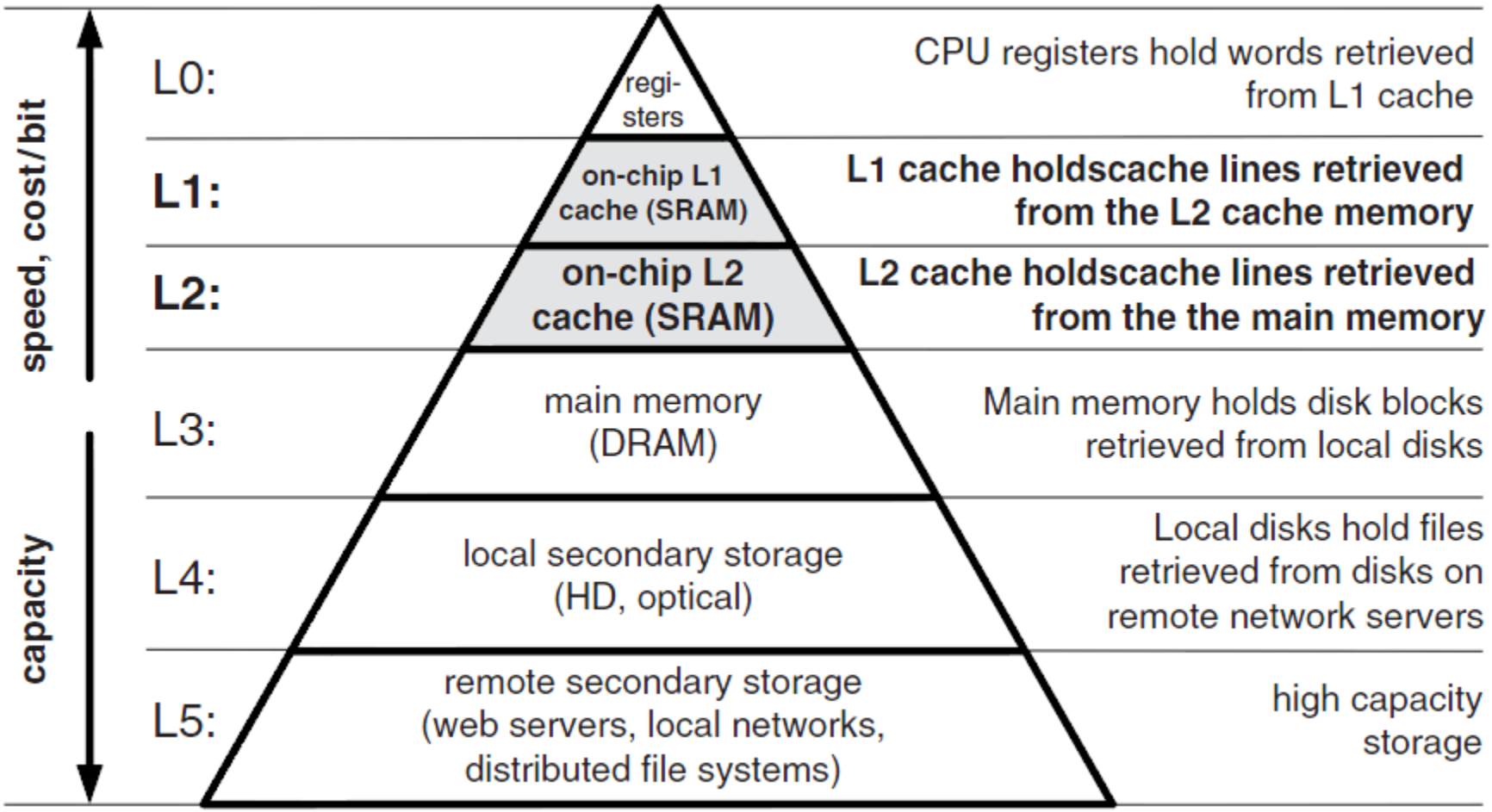
Access time from Address– the time required of the RAM array to decode the address and provide value to the data bus.

Static RAM Write Timing



Write time–the time the data must be held valid in order to decode address and store value in memory cells.

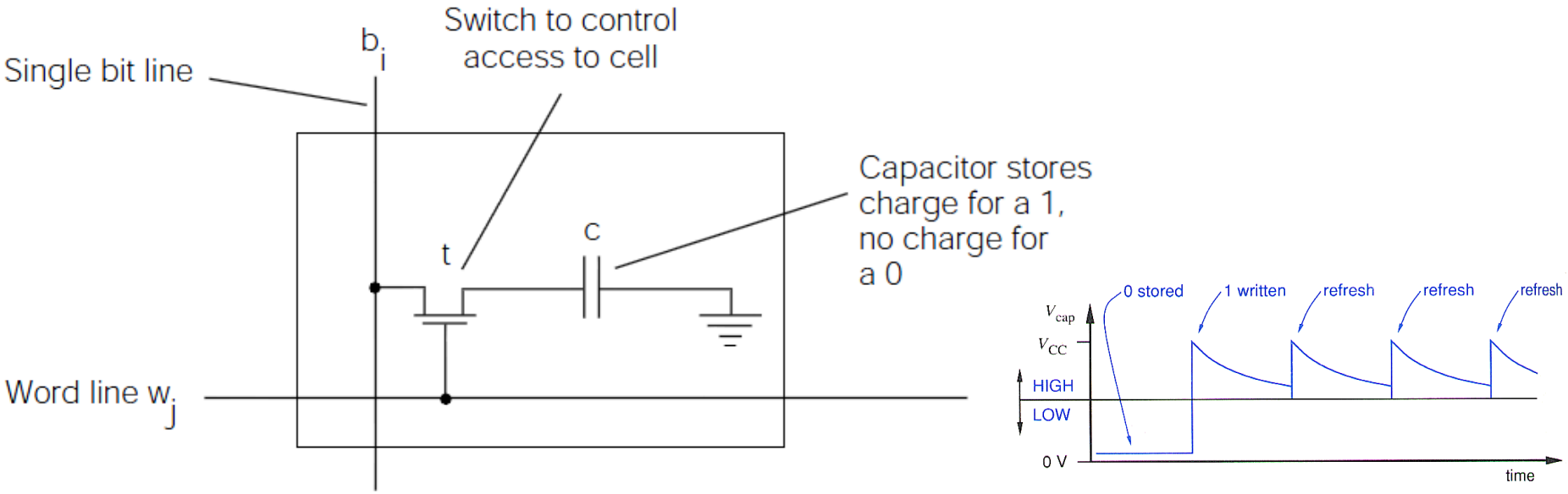
Static RAM



[**Book**]: CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies

Dynamic memory

- Dynamic memory is built with capacitors.
  - A stored charge on the capacitor represents a logical 1.
  - No charge represents a logic 0.
  - However, capacitors lose their charge after a few milliseconds.
    - The memory requires constant refreshing to recharge the capacitors.

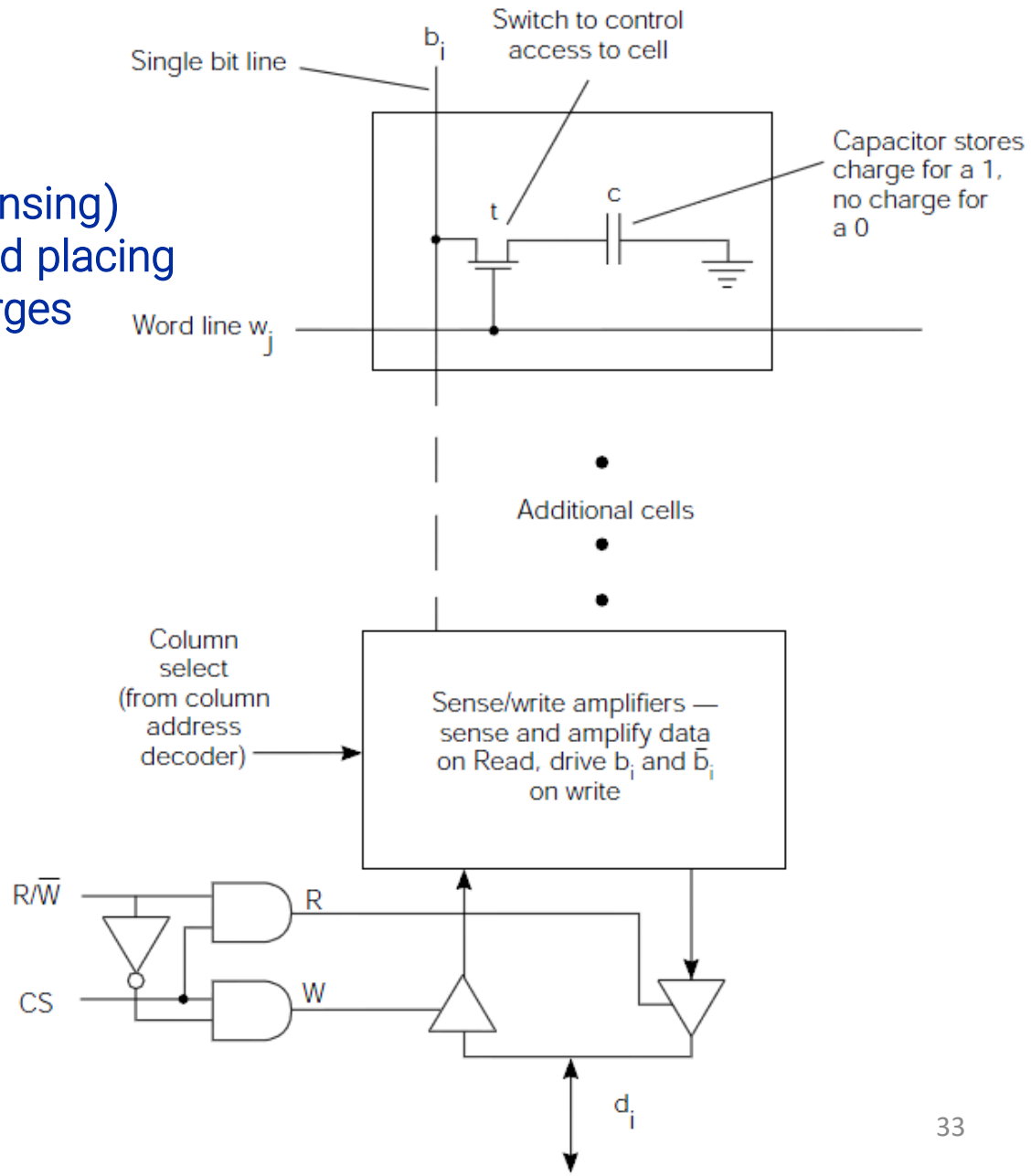


[**Book**]: DRAM circuit design a tutorial by Brent Keeth R Jacob Baker

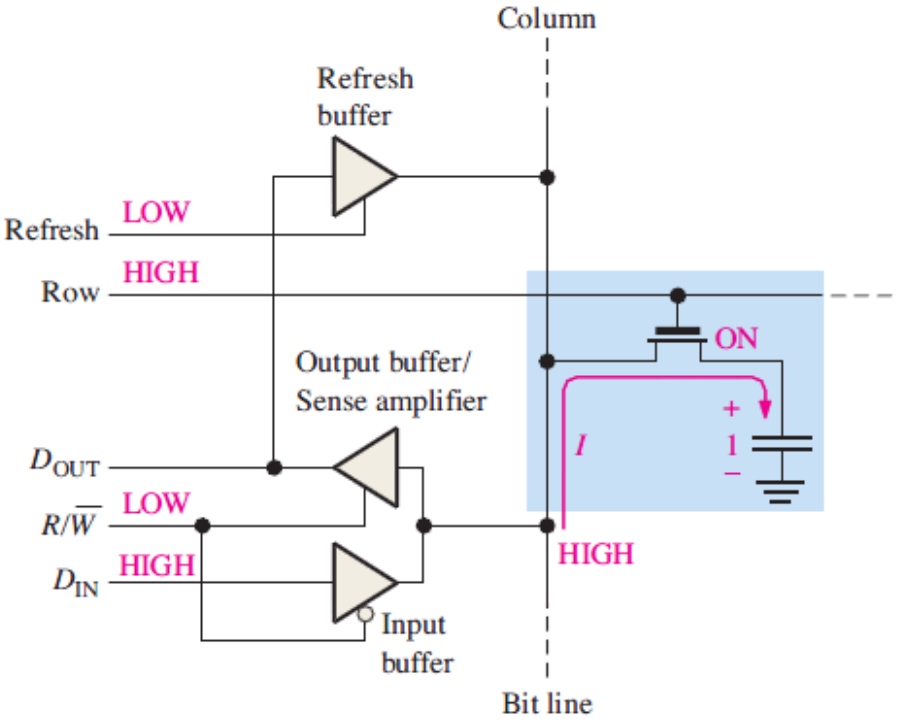
Dynamic memory

Refresh capacitor by reading (sensing) value on bit line, amplifying it, and placing it back on bit line where it recharges capacitor.

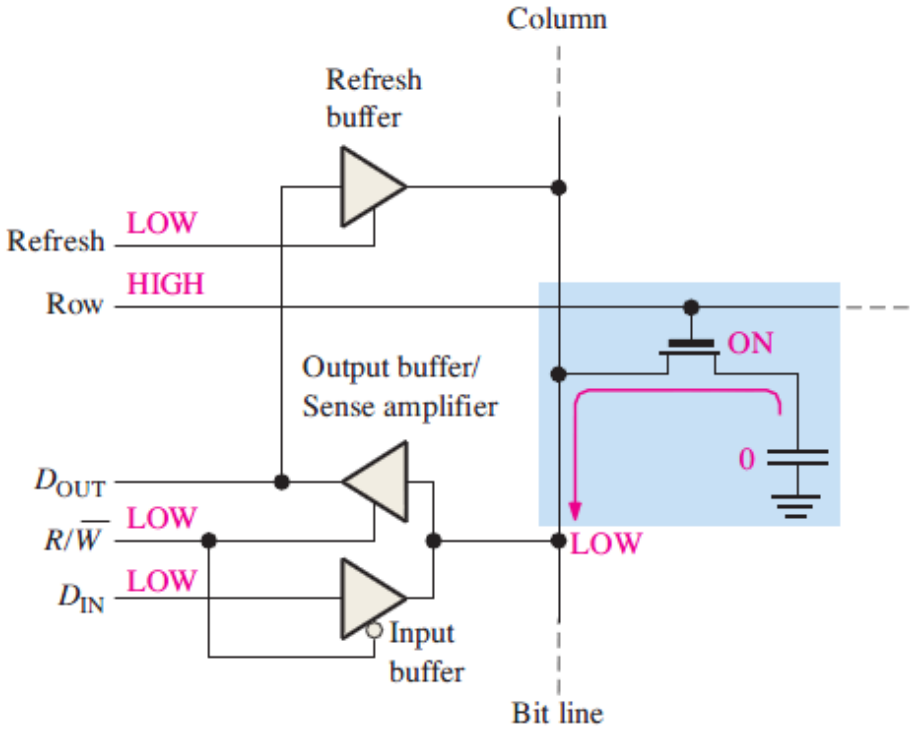
Write: place value on bit line and assert word line.
Read: precharge bit line, assert word line, sense value on bit line with sense/amp.



Basic operation of a DRAM cell

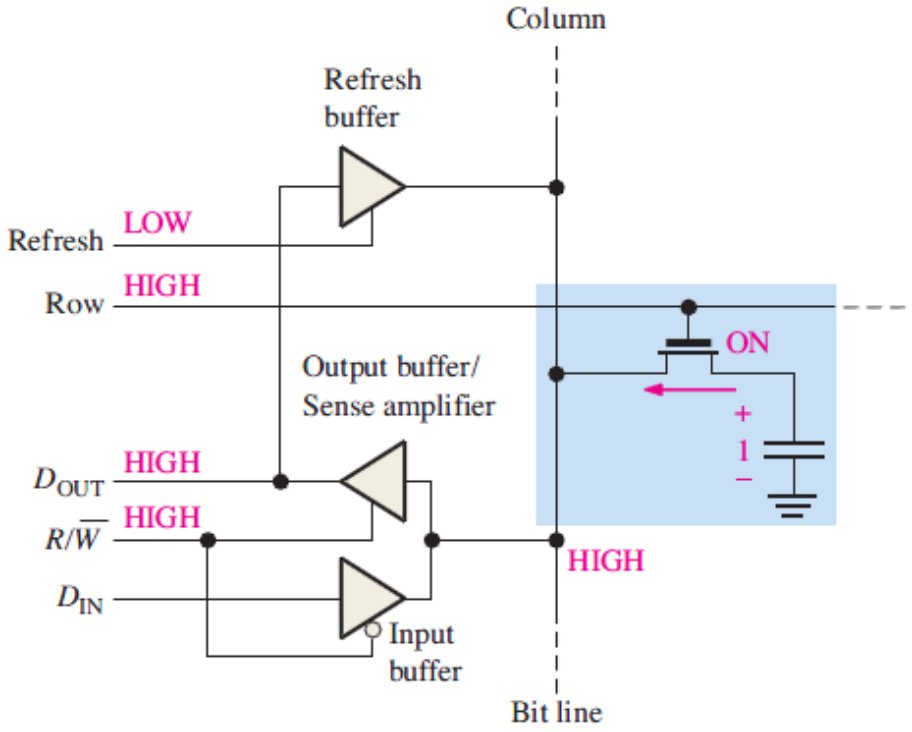


Writing a 1 into the memory cell

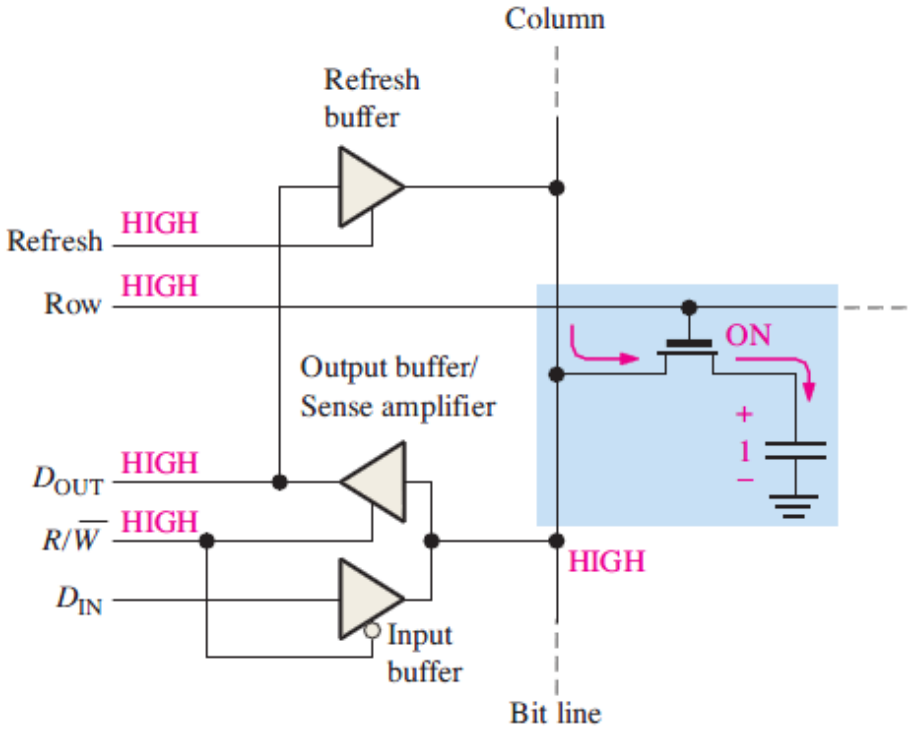


Writing a 0 into the memory cell

Basic operation of a DRAM cell



Reading a 1 from the memory cell



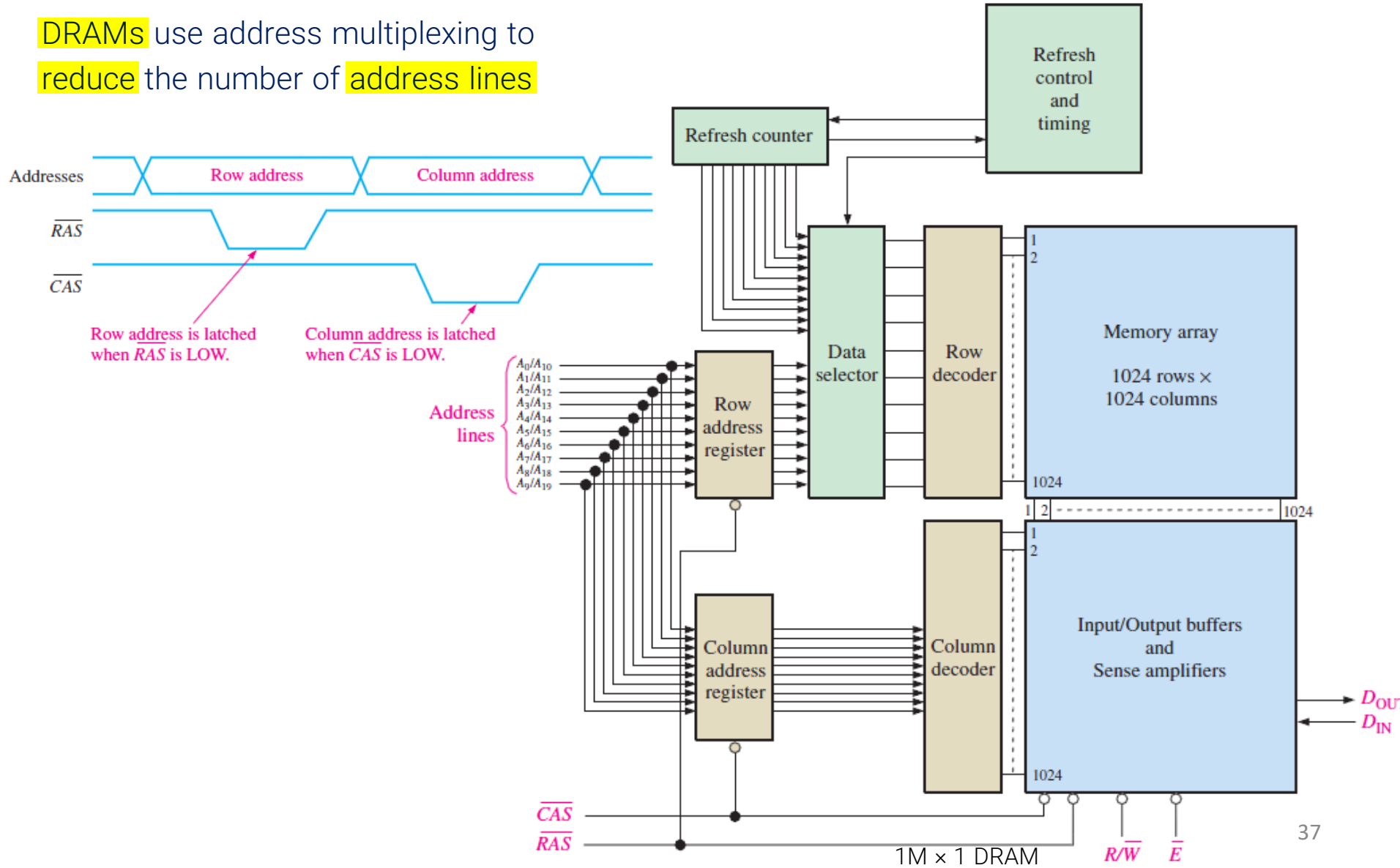
Refreshing a stored 1

Dynamic vs. static memory

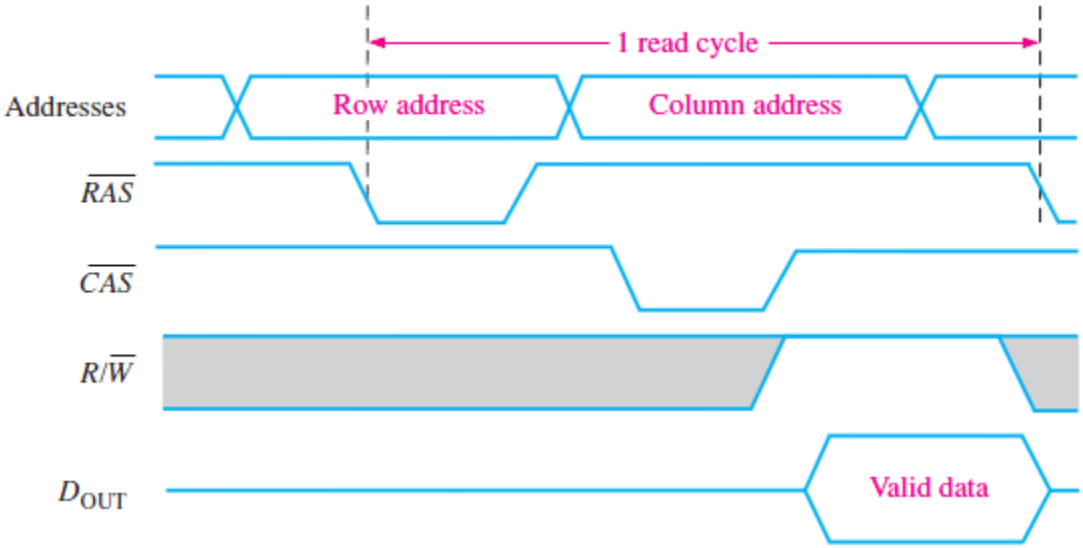
- Dynamic RAMs tend to be physically smaller than static RAMs.
  - A single bit of data can be stored with just one capacitor and one transistor, while static RAM cells typically require 4-6 transistors.
  - This means dynamic RAM is cheaper and denser—more bits can be stored in the same physical area.
- Dynamic RAM is used for a computer's main memory
  - it's cheap and you can pack a lot of storage into a small space.
- Disadvantage of dynamic RAM is its speed.
  - Transfer rates are 800MHz at best, which can be much slower than the processor itself.
  - You also have to consider latency, or the time it takes data to travel from RAM to the processor.
- Real systems augment dynamic memory with small fast sections of static memory called caches.

Address Multiplexing

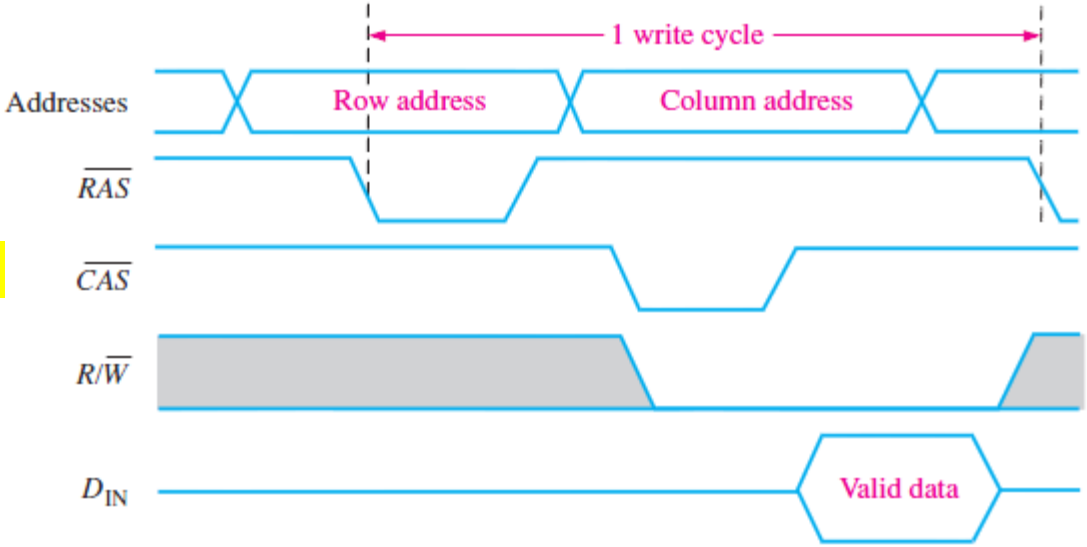
DRAMs use address multiplexing to reduce the number of address lines



Basic timing for address multiplexing



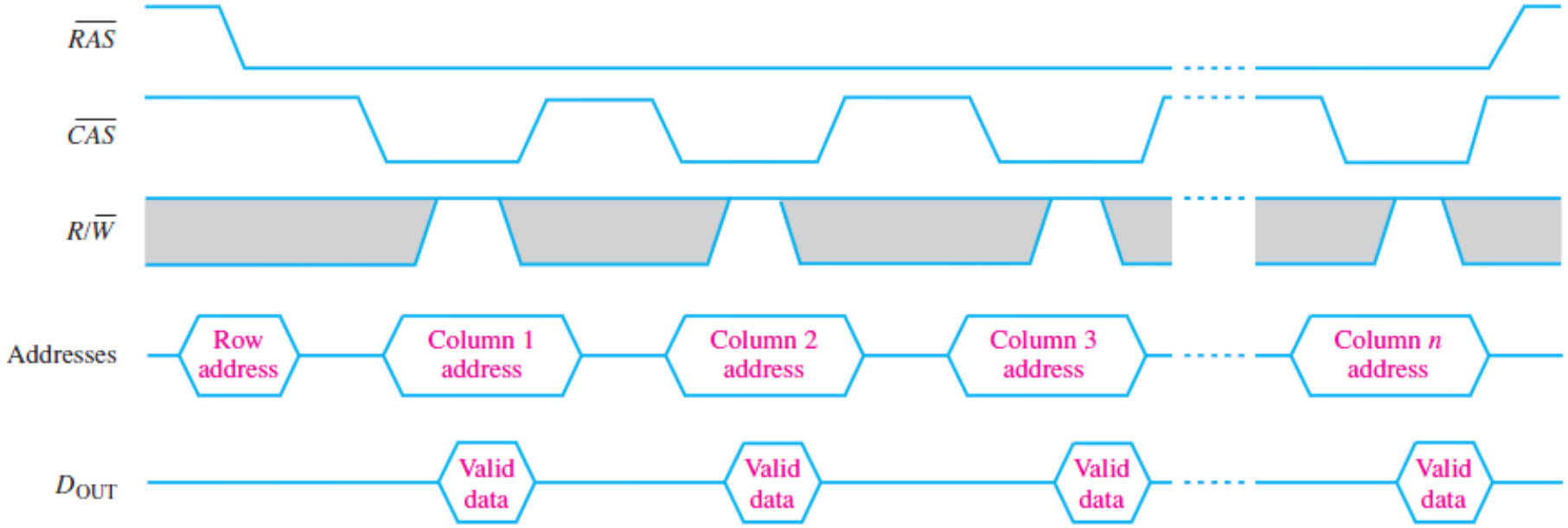
Read cycle



Write cycle

Fast Page Mode

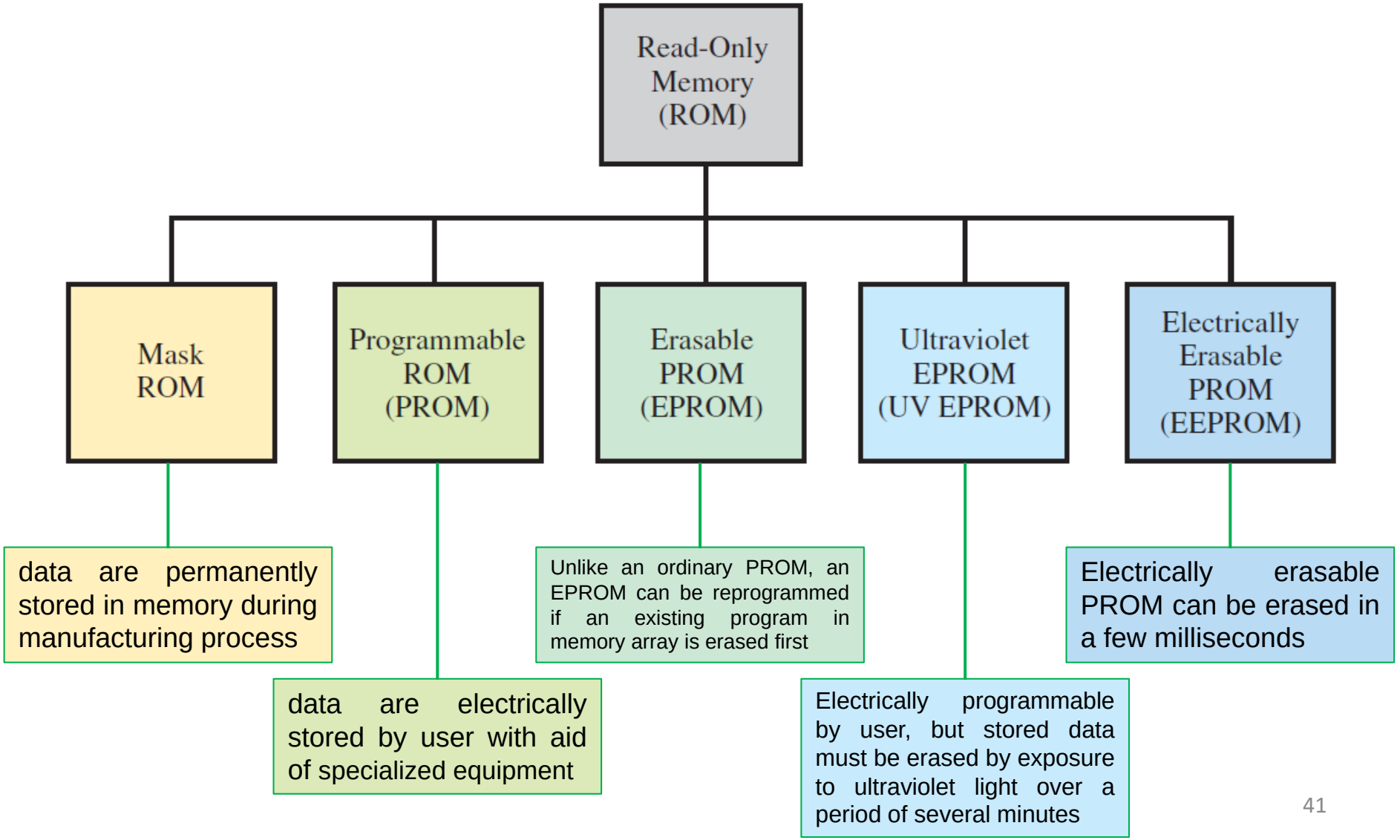
allows fast successive read or write operations at each column address in a selected row



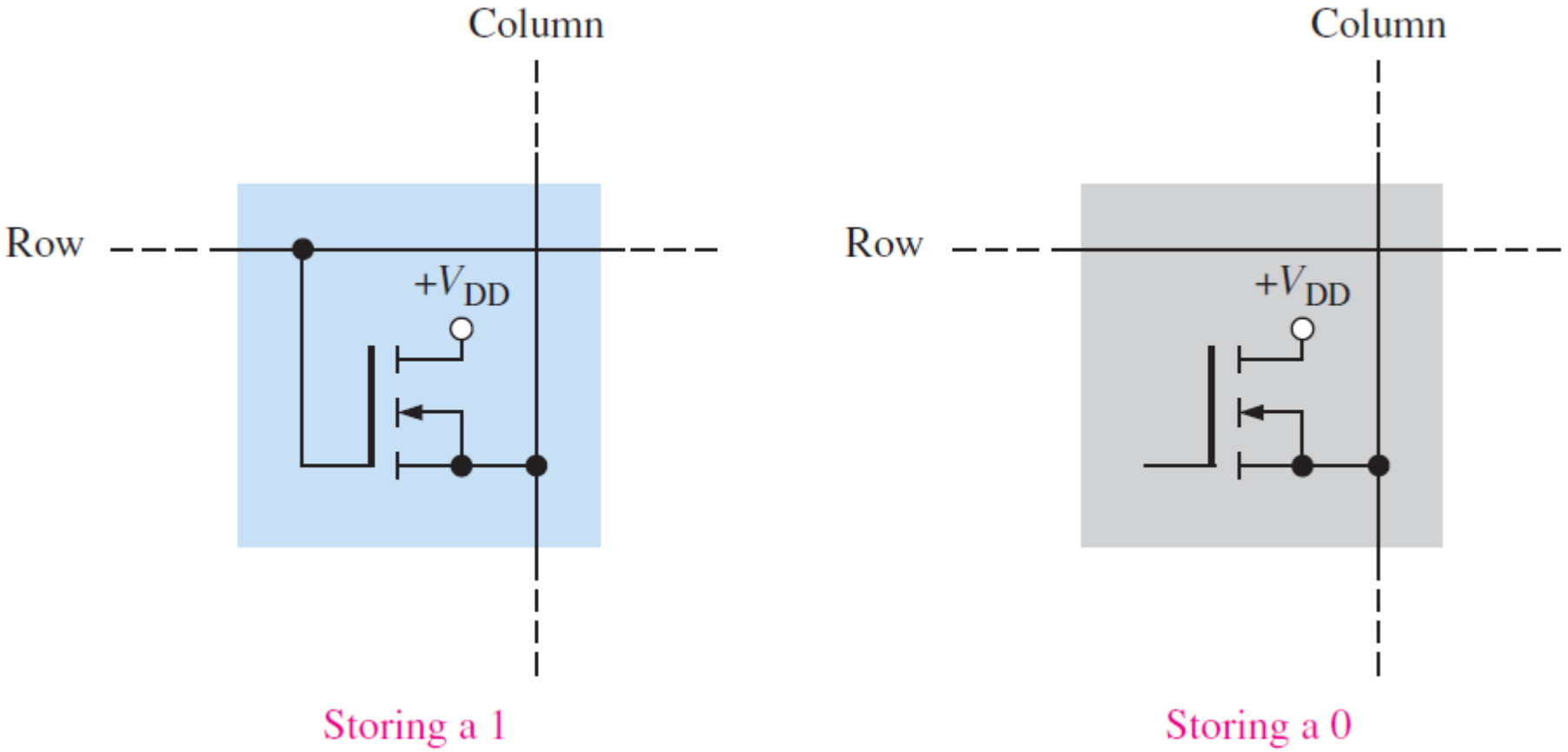
Read-Only Memory (ROM)

- ROM contains permanently or semipermanently stored data
  - cannot be changed at all
  - cannot be changed without specialized equipment
- ROM stores data that are used repeatedly in system applications
  - Tables, conversions, or programmed instructions for system initialization and operation
- ROMs retain stored data when the power is off and are therefore nonvolatile memories

انواع ROM

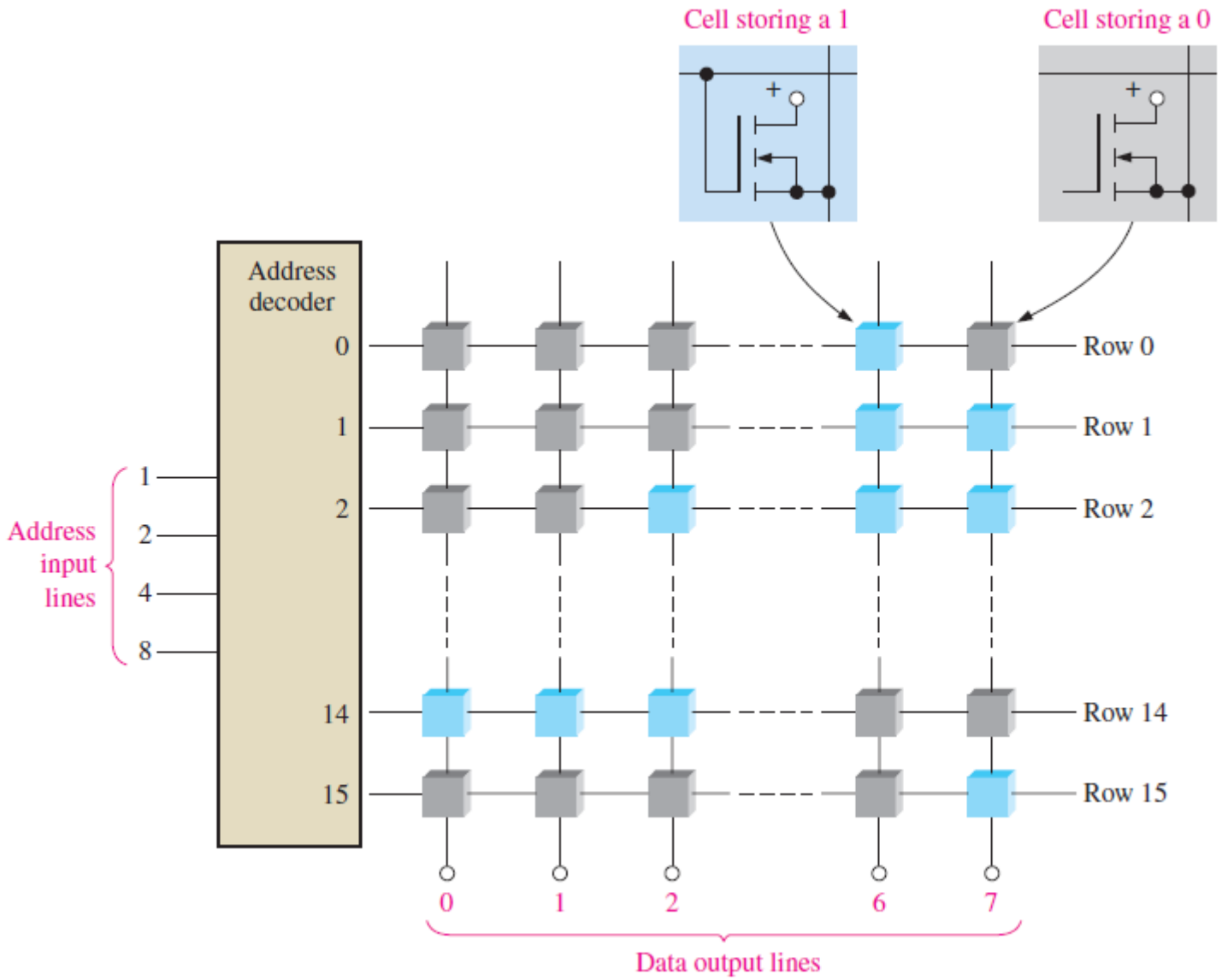

Read-Only Memory (ROM)
Mask ROM
Programmable ROM (PROM)
Erasable PROM (EPROM)
Ultraviolet EPROM (UV EPROM)
Electrically Erasable PROM (EEPROM)
data are permanently stored in memory during manufacturing process
data are electrically stored by user with aid of specialized equipment
Unlike an ordinary PROM, an EPROM can be reprogrammed if an existing program in memory array is erased first
Electrically programmable by user, but stored data must be erased by exposure to ultraviolet light over a period of several minutes
Electrically erasable PROM can be erased in a few milliseconds

Mask ROM

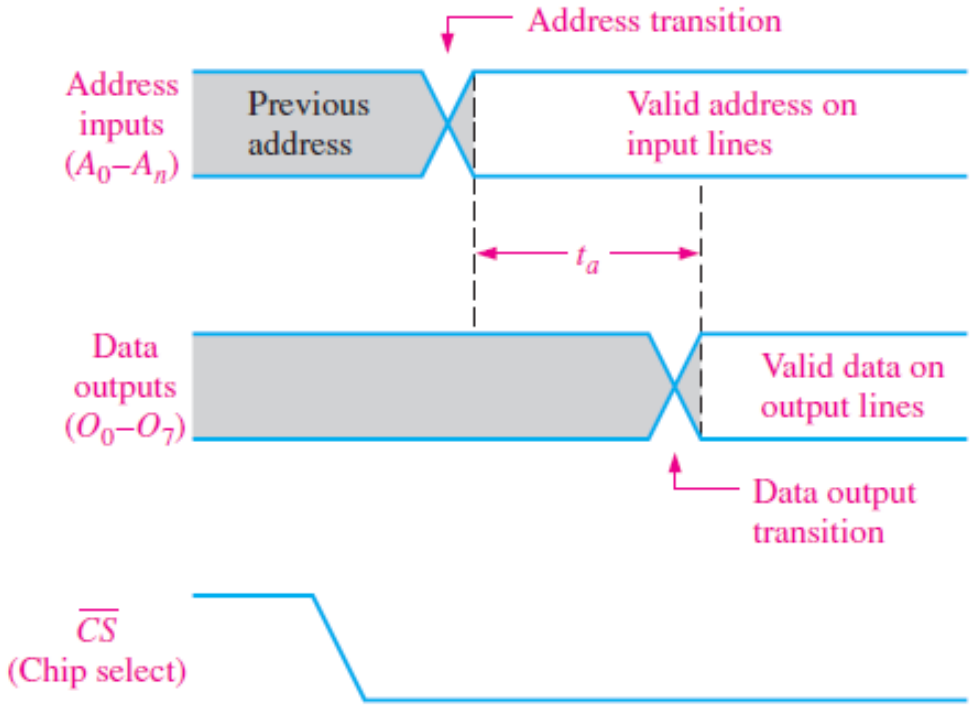


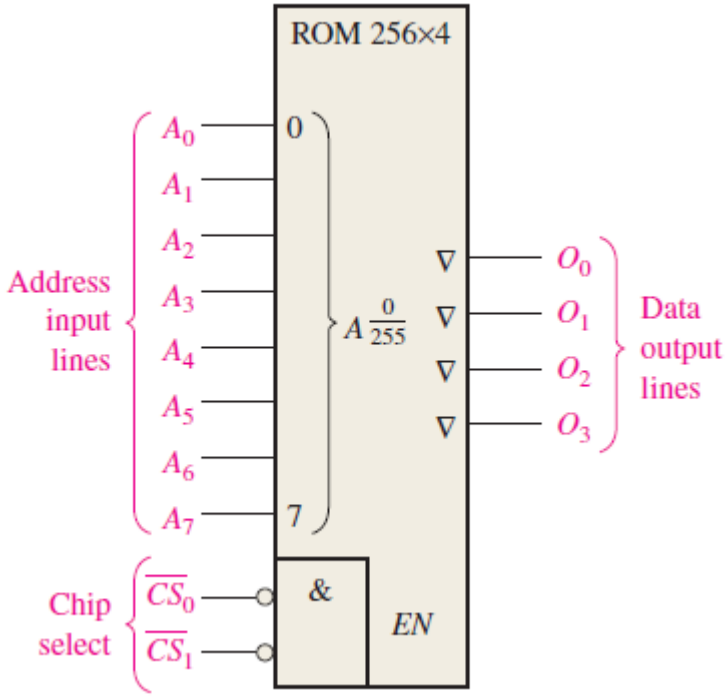
Once the memory is programmed, it cannot be changed

Mask ROM

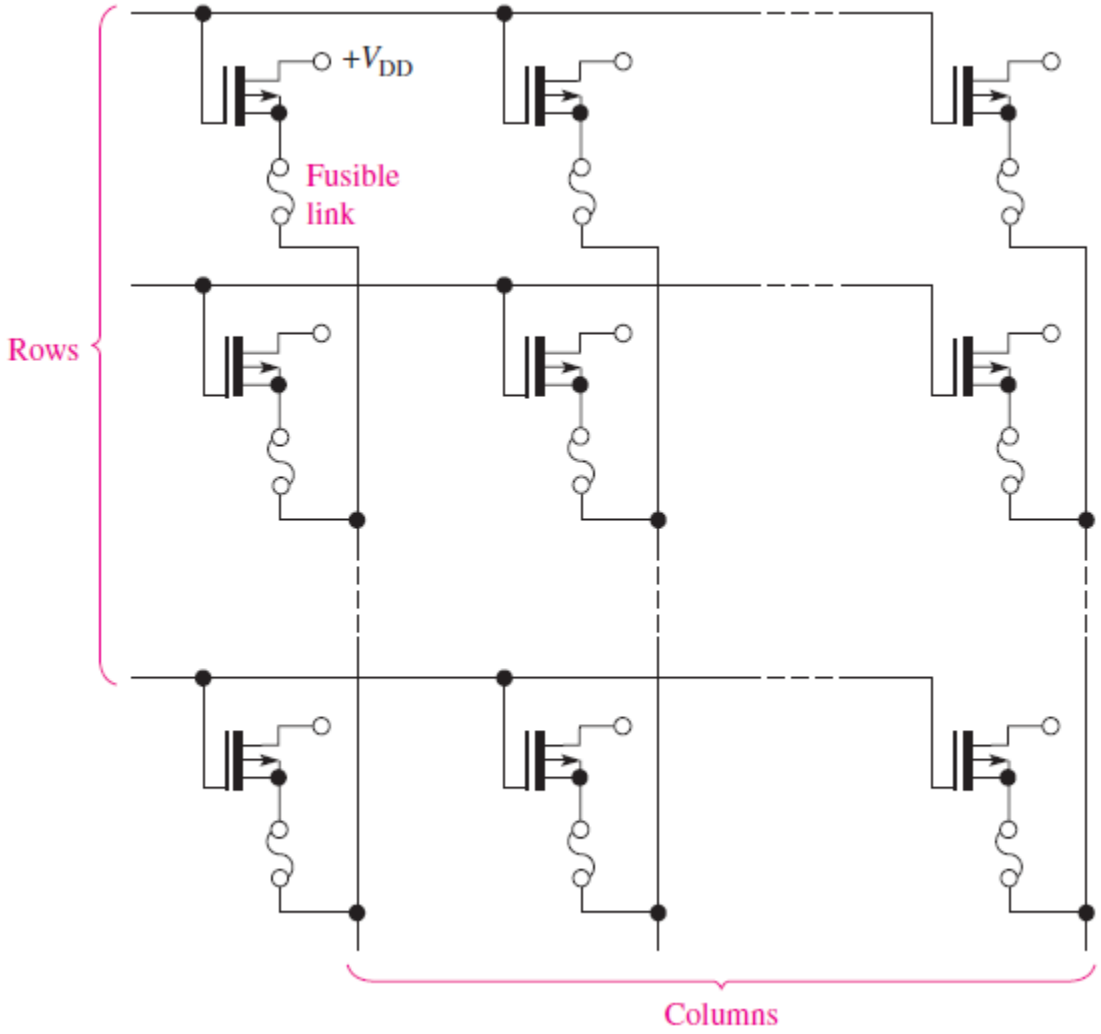

Cell storing a 1
Cell storing a 0
Address decoder
0
1
2
14
15
Row 0
Row 1
Row 2
Row 14
Row 15
Address input lines
1
2
4
8
0
1
2
6
7
Data output lines

ROM access time



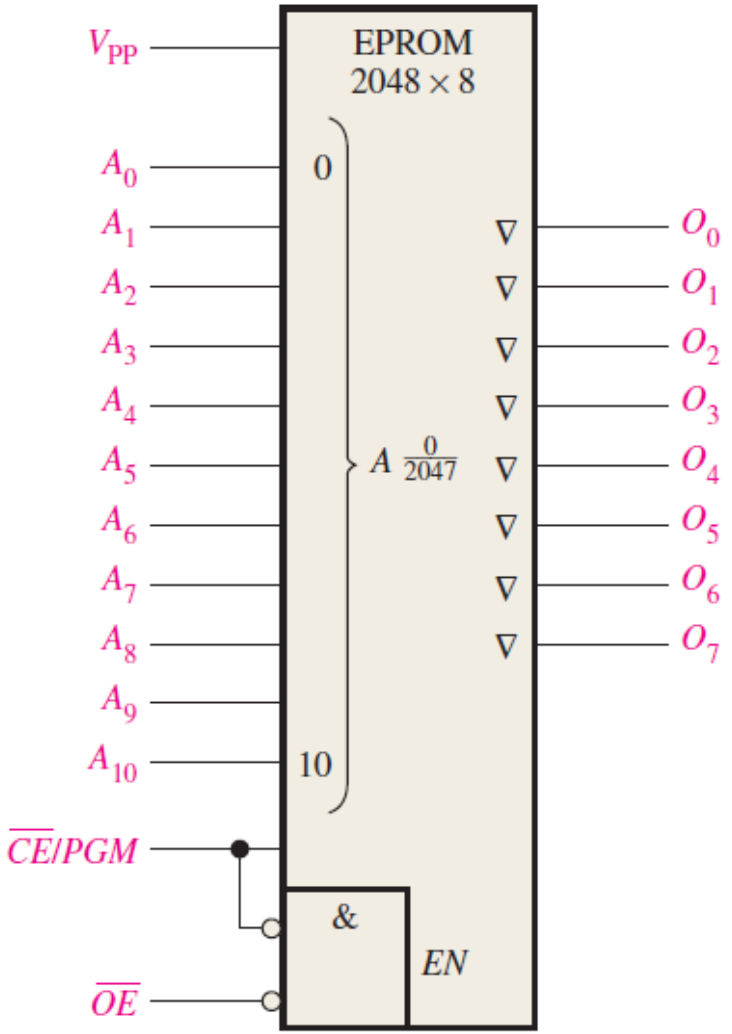


Programmable ROMs (PROMs)



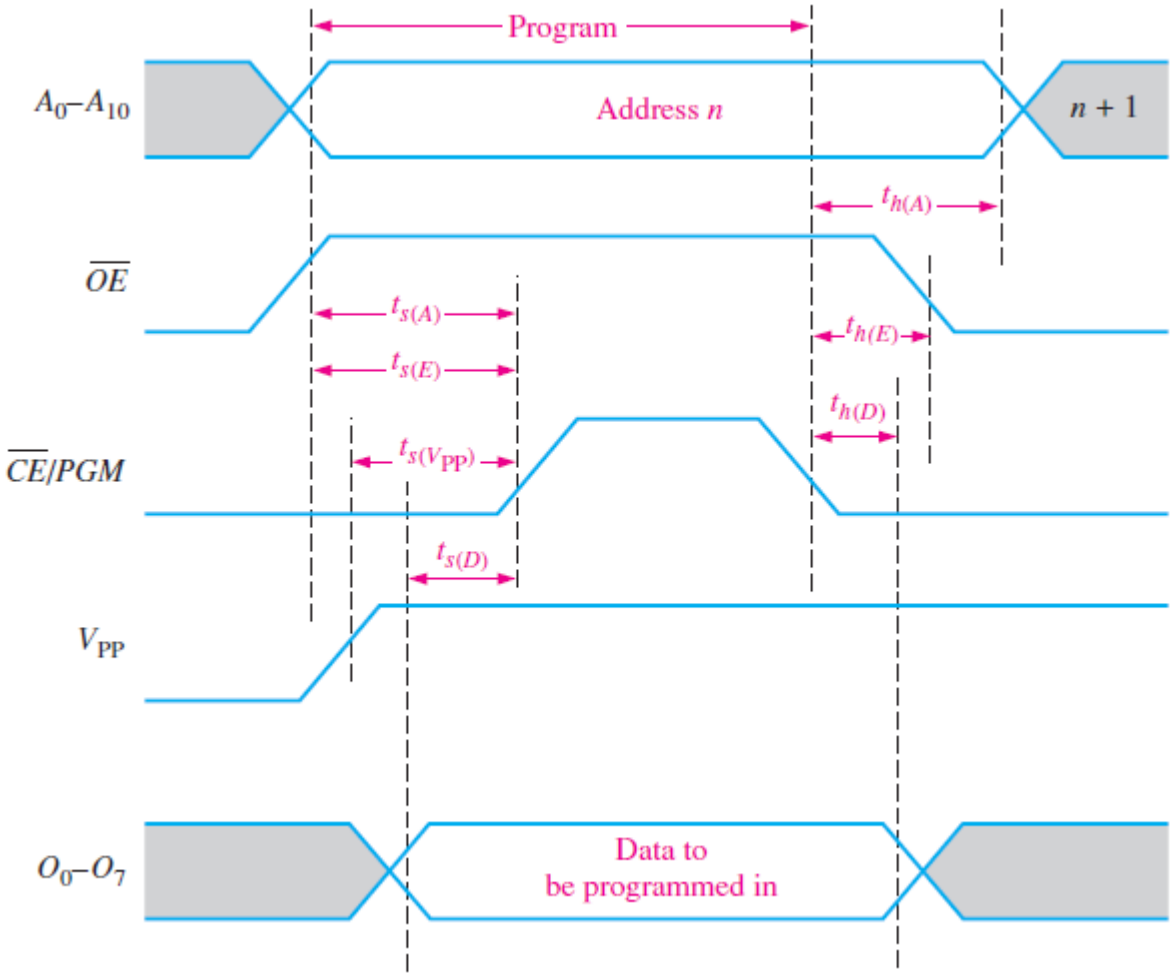
PROMs come from the manufacturer unprogrammed and are custom programmed in the field to meet the user's needs

Erasable PROM (**EPROM**)



To program or write to the device, a high dc voltage is applied to V_{PP} and $\overline{OE}$ is HIGH.

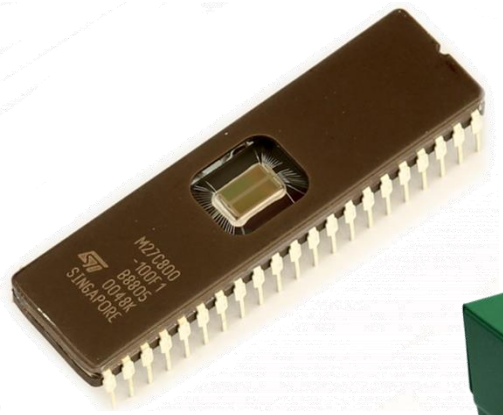
EPROM programming cycle

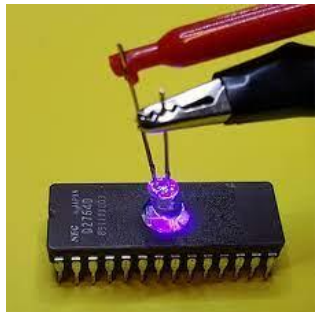


These signals are normally produced by an EPROM programmer

UV EPROMs

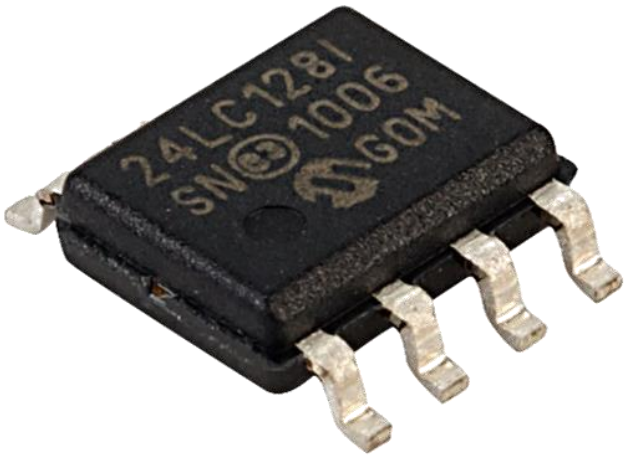
- You can recognize UV EPROM device by the UV transparent window on the package
- Erasure is done by exposure of the memory array chip to high-intensity ultraviolet radiation through the UV window on top of the package

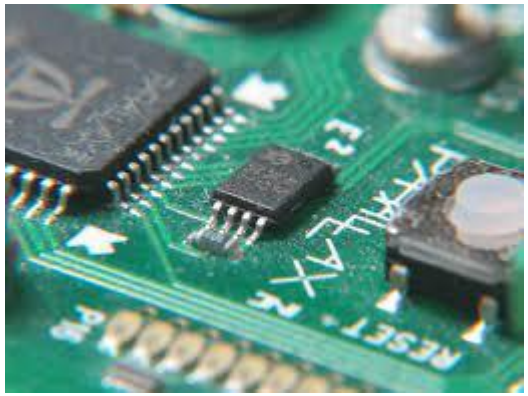




EEPROMs

- An electrically erasable PROM can be both erased and programmed with electrical pulses
- EEPROM can be rapidly programmed and erased in-circuit for reprogramming





Flash Memory

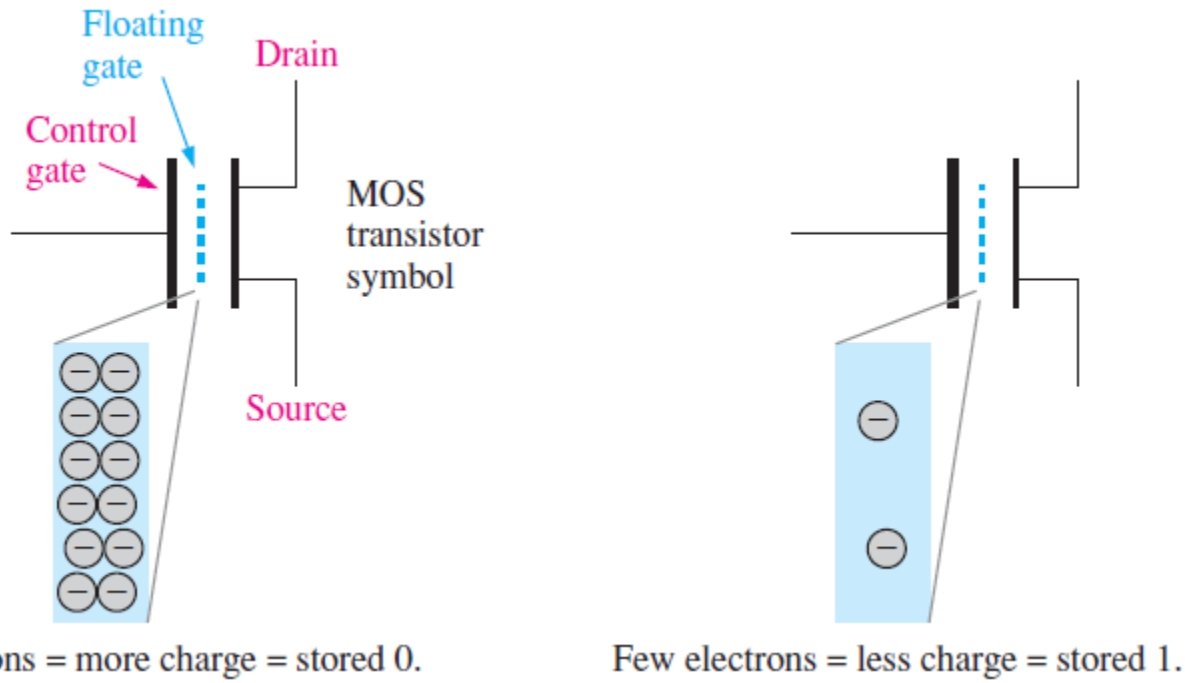
- Ideal memory
  - High storage capacity
  - Nonvolatility
  - In-system read and write capability
  - Comparatively fast operation
  - Cost effectiveness
- The traditional memory technologies such as ROM, PROM, EPROM, EEPROM, SRAM, and DRAM individually exhibit one or more of these characteristics

Flash memory has all of the desired characteristics!!

Flash Memory

- High-density read/write memories
  - High-density translates into large bit storage capacity
    - High-density means that a large number of cells can be packed into a given surface area on a chip
- Nonvolatile
  - Data can be stored indefinitely without power
- Three major operations in a flash memory
  - programming operation
  - Read operation
  - erase operation

Flash Memory

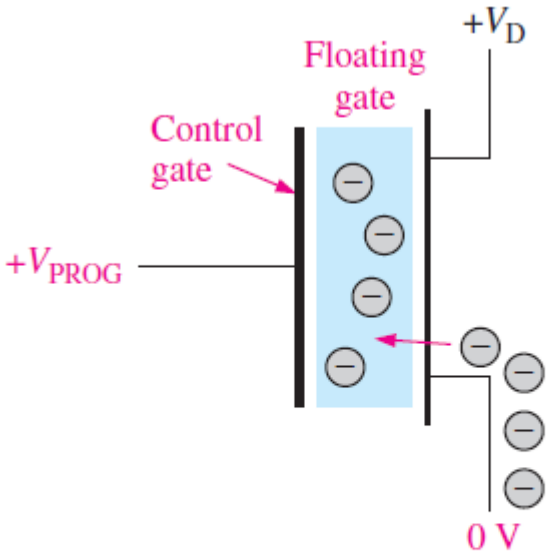


Floating gate stores electrons (charge) as a result of a sufficient voltage applied to control gate

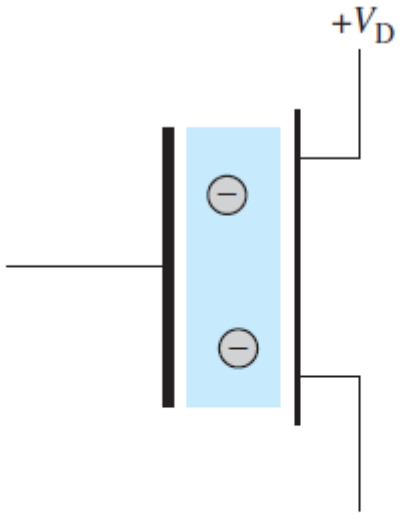
0 is stored when there is more charge and a 1 is stored when there is less or no charge

Floating gate charge associated with a stored 0 prevents control gate voltage from reaching turn-on threshold, whereas the small or zero charge associated with a stored 1 allows control gate voltage to exceed turn-on threshold

Programming



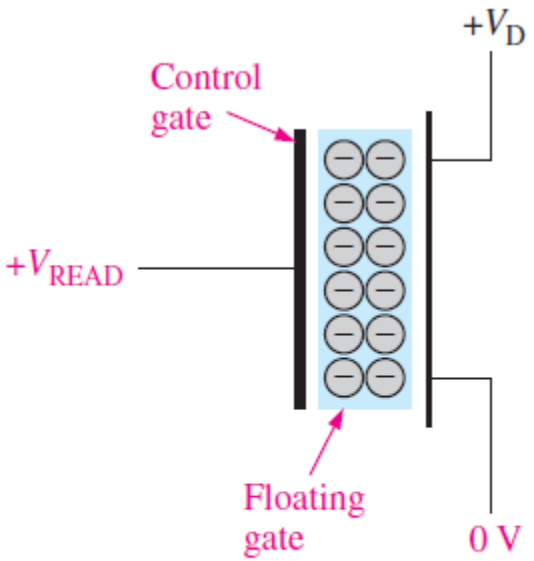
To store a 0, a sufficient positive voltage is applied to the control gate with respect to the source to add charge to the floating gate during programming.



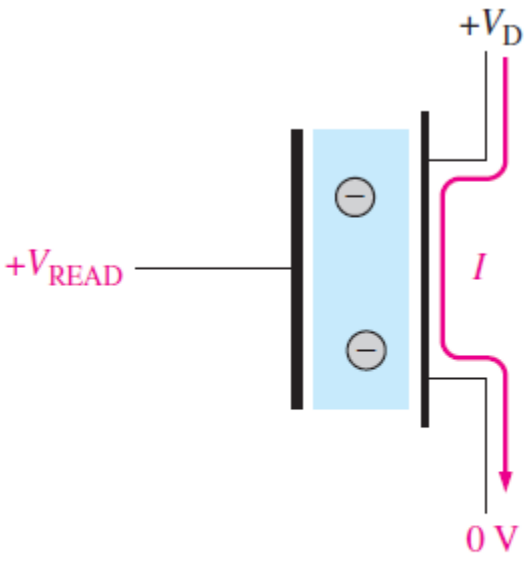
To store a 1, no charge is added and the cell is left in the erased condition.

- Initially, all cells are at 1 state
  - Because charge was removed from each cell in a previous erase operation
  - programming operation adds electrons (charge) to floating gate of cells that are to store a 0
    - Application of a sufficient positive voltage to control gate with respect to source during programming attracts electrons to floating gate
    - Once programmed, a cell can retain the charge for up to 100 years without any external power
  - No charge is added to those cells that are to store a 1

Read



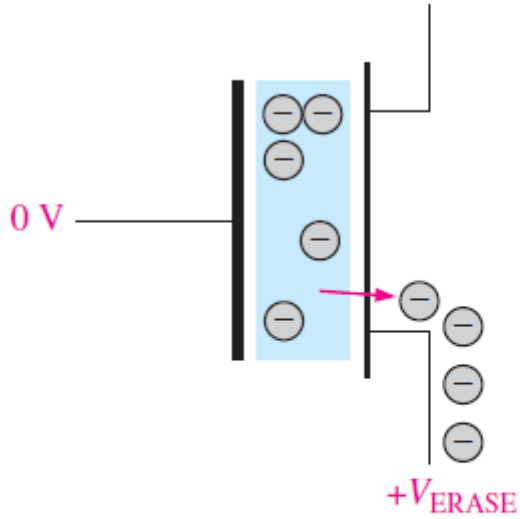
When a 0 is read, the transistor remains off because the charge on the floating gate prevents the read voltage from exceeding the turn-on threshold.



When a 1 is read, the transistor turns on because the absence of charge on the floating gate allows the read voltage to exceed the turn-on threshold.

- During a read operation
  - A positive voltage is applied to control gate
  - The amount of charge present on floating gate of a cell determines whether or not voltage applied to control gate will turn on transistor
    - If a 1 is stored, control gate voltage is sufficient to turn transistor on
    - If a 0 is stored, transistor will not turn on because control gate voltage is not sufficient to overcome negative charge stored in floating gate
    - Think of charge on floating gate as a voltage source that opposes voltage applied to control gate during a read operation.

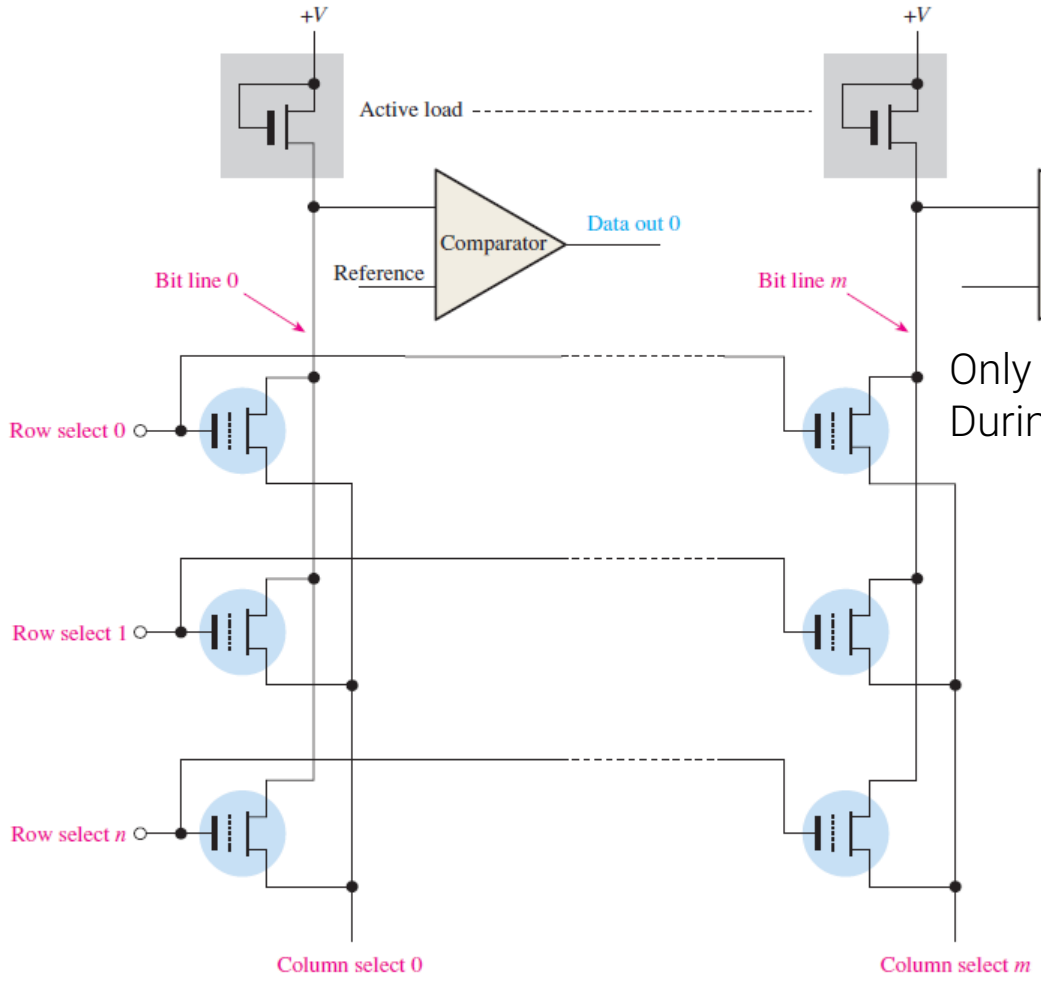
Erase



To erase a cell, a sufficient positive voltage is applied to the source with respect to the control gate to remove charge from the floating gate during the erase operation.

- During an erase operation:
  - Charge is removed from all the memory cells
    - A sufficient positive voltage is applied to transistor source with respect to control gate
    - This is opposite in polarity to that used in programming
      - This voltage attracts electrons from the floating gate and depletes it of charge
  - A flash memory is always erased prior to being reprogrammed.

Flash Memory Array

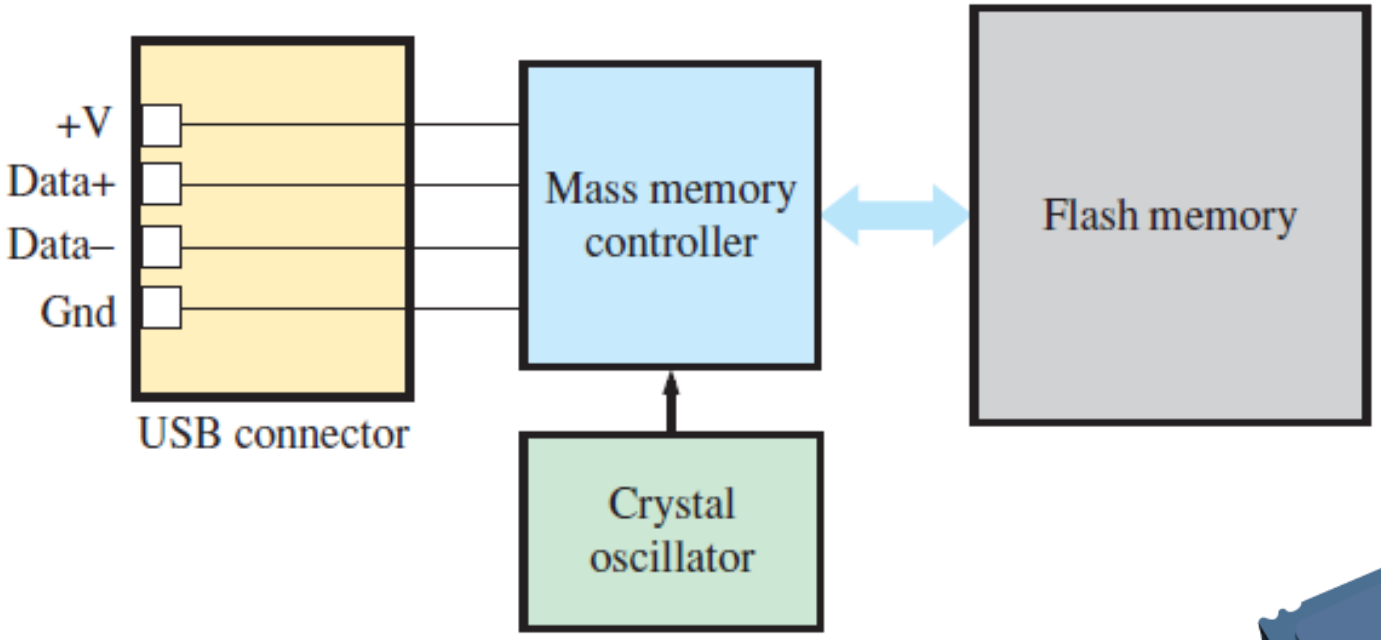


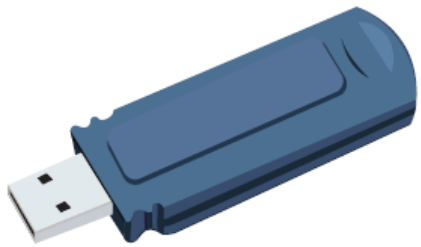
Only one row line is accessed at a time

During a read operation, When a cell in a given bit line turns on

- Stored 1:
  - There is current through the bit line
    - produces a voltage drop across active load
  - This voltage drop is compared to a reference voltage with a comparator circuit and an output level indicating a 1 is produced.
- Stored 0
  - There is no current or little current in bit line and an opposite level is produced on comparator output.

USB Flash Drive





Comparison of Types of Memories

Memory Type	Nonvolatile	High-Density	One-Transistor Cell	In-System Writability
Flash	Yes	Yes	Yes	Yes
SRAM	No	No	No	Yes
DRAM	No	Yes	Yes	Yes
ROM	Yes	Yes	Yes	No
EEPROM	Yes	No	No	Yes
UV EPROM	Yes	Yes	Yes	No

پایان

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