Experiment 3 - Binary-Search

Group 4

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***Abstract*— In this experiment we made a binary search module using an FPGA which got a binary number using FPGA's switches and found out which number was that and then showed that using a 7-segment display. The same method comparing with an analog comparator could be used in cyber–physical systems to make analog-to-digital convertors.**

***Keywords*— binary search, 7-segment display, BCD, FPGA, cyber–physical systems.**

I. Binary Search

Binary Search is a typical search algorithm which is able to find a member in a sorted array in a time of O(n). In this experiment we implemented a 0-to-255 binary search circuit on an FPGA.

There was some difficulties in implementation so that we used one more bit in all internal calculations and used 0 and 256 for initial min and max bounds. The circuit got a number and gave its nearest number between 0 and 255.

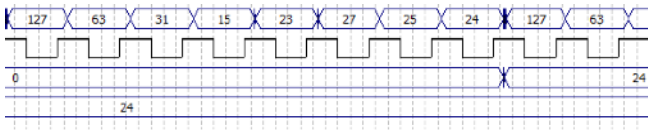

Fig. 1 Simulation of Binary Search Module

II. BCD Decoder

BCD is a number encoding system which is using widely for showing numbers using modular displays such as 7-segment displays.

There is some well-known methods for converting binary numbers to BCD. In this experiment we used a module based on shift-add-3 algorithm for this purpose. This module was implemented on FPGA. After that, the results have decoded using given decoder modules so that could be shown on 7-segment displays.

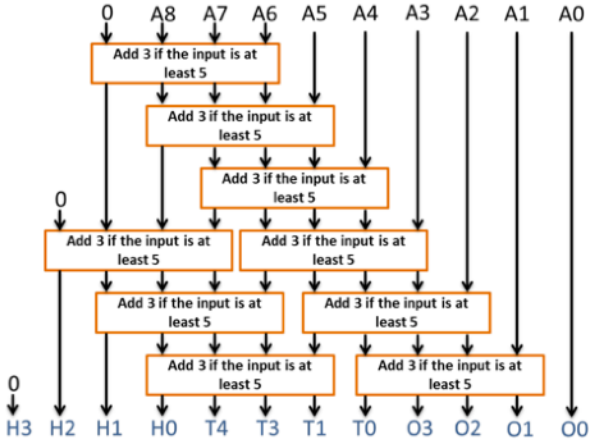

Fig. 2 Binary-to-BCD Decoder

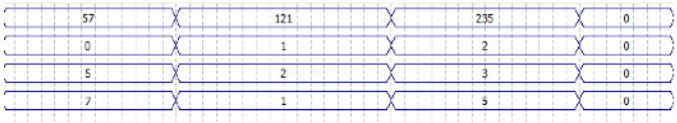

Fig. 3 Simulation of Binary-to-BCD Decoder

III. Combination

At the final part of experiment we used modules mentioned above to make a circuit which got a signal and showed its value by a number between 0 and 255 on a 3-part 7-segment display.

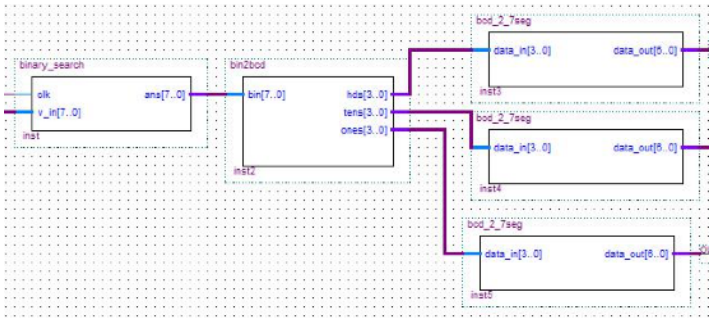

Fig. 4 Circuit RTL Design