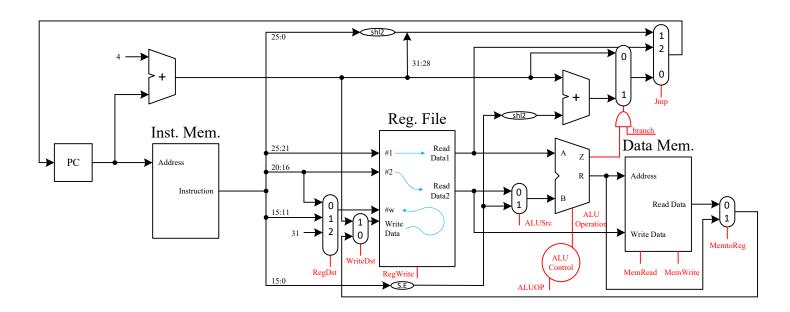
ALUOP	func	ALUOperation		
00	Not Imp.	010		
01	Not Imp.	011		
10	and	000		
10	or	001		
10	add	010		
10	sub	011		
10	slt	111		
11	Not Imp.	111		



31 26	25 21	20 16	15 11	10 6	5 0
RT	Rs	Rt	Rd	shift	func
31 26	25 21	20 16	15		0
addi	Rs	Rd		Data	
31 26	25 21	20 16	15		0
slti	Rs	Rd		Data	
31 26	25 21	20 16	15		0
lw	Rs	Rd		Addres	S
31 26	25 21	20 16	15		0
sw	Rs	Rd		Addres	S

31 26	25 21	20 16	15	0	
beq	Rs	Rd	Address		
31 26	25			0	
J		Address			
31 26	25 21	20		0	
Jr	Rs		Not important		
31 26	25			0	
Jal			Address		

OPC		RegDst	WriteDst	RegWrite	ALUSrc	ALUOP	Branch	Jmp	MemRead	MemWrite	MemtoReg
000000	RT	1	0	1	0	10	0	0	0	0	1
000001	addi	0	0	1	1	00	0	0	0	0	1
000010	slti	0	0	1	1	11	0	0	0	0	1
000011	lw	0	0	1	1	00	0	0	1	0	0
000100	sw	Х	X	0	1	00	0	0	0	1	х
000101	beq	X	X	0	0	01	1	0	0	0	X
000110	J	X	X	0	X	X	X	1	0	0	X
000111	Jr	X	X	0	X	X	X	2	0	0	Х
001000	Jal	2	1	1	X	X	X	1	0	0	x