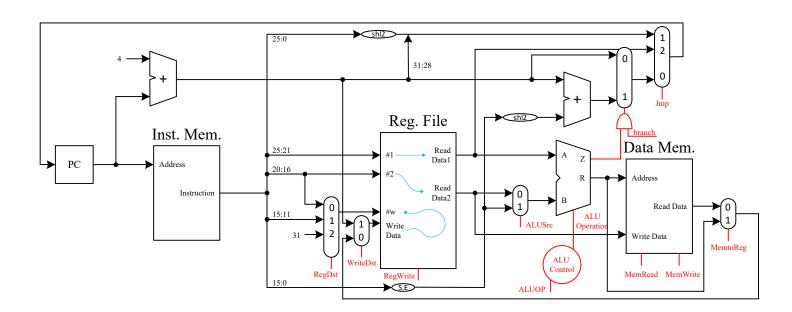
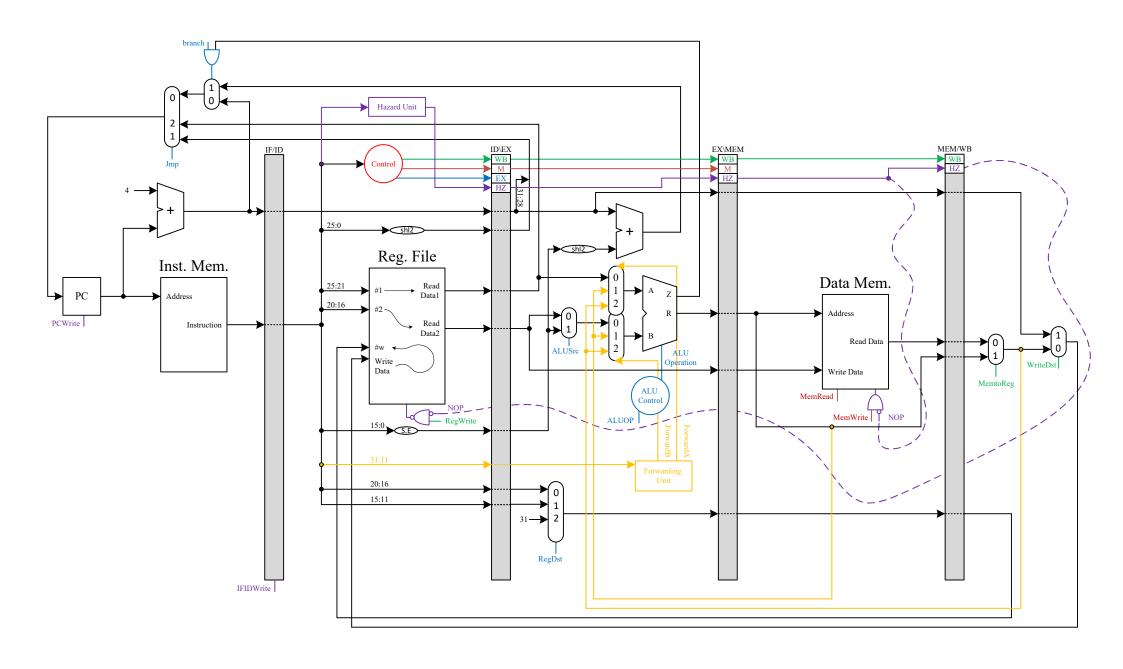
ALUOP	func	ALUOperation		
00	Not Imp.	010		
01	Not Imp.	011		
10	and	000		
10	or	001		
10	add	010		
10	sub	011		
10	slt	111		
11	Not Imp.	111		



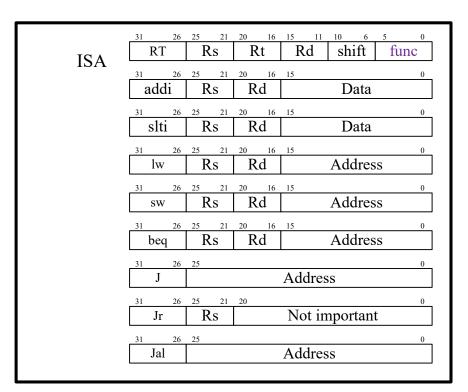
31 26 25 21 20 16 15 11 10 6 5 0	31 26 25 21 20 16 15
RT Rs Rt Rd shift func	beq Rs Rd Address
31 26 25 21 20 16 15 0	31 26 25
addi Rs Rd Data	J Address
31 26 25 21 20 16 15 0	_31
slti Rs Rd Data	Jr Rs Not important
31 26 25 21 20 16 15 0	31 26 25
lw Rs Rd Address	Jal Address
31 26 25 21 20 16 15 0	
sw Rs Rd Address	

OPC		RegDst	WriteDst	RegWrite	ALUSrc	ALUOP	Branch	Jmp	MemRead	MemWrite	MemtoReg
000000	RT	1	0	1	0	10	0	0	0	0	1
000001	addi	0	0	1	1	00	0	0	0	0	1
000010	slti	0	0	1	1	11	0	0	0	0	1
000011	lw	0	0	1	1	00	0	0	1	0	0
000100	sw	Х	Х	0	1	00	0	0	0	1	X
000101	beq	X	X	0	0	01	1	0	0	0	X
000110	J	X	X	0	X	X	X	1	0	0	X
000111	Jr	Х	X	0	X	X	X	2	0	0	X
001000	Jal	2	1	1	X	X	X	1	0	0	X



ALU

ALUOP	func	ALUOperation		
00	Not Imp.	010		
01	Not Imp.	011		
10	and	000		
10	or	001		
10	add	010		
10	sub	011		
10	slt	111		
11	Not Imp.	111		



## Control Unit

	RT	addi	slti	lw	sw	beq	J	Jr	Jal
EX	RegDst=01 ALUSrc =0 ALUOP =10	RegDst=00 ALUSrc =1 ALUOP =00	RegDst=00 ALUSrc =1 ALUOP =11	RegDst=00 ALUSrc =1 ALUOP =00	RegDst=xx ALUSrc =1 ALUOP =00	RegDst=xx ALUSrc =0 ALUOP =01	RegDst=xx ALUSrc =x ALUOP =xx	RegDst=xx ALUSrc =x ALUOP =xx	RegDst=10 ALUSrc =x ALUOP =xx
MEM	Jmp =00 MemRead =0	Jmp =00 MemRead =0		Jmp =00 MemRead =1	Jmp =00 MemRead =0	Jmp =00 MemRead =0	Jmp =01 MemRead =0	Jmp =10 MemRead =0	
WB	RegWrite=1	RegWrite=1	WriteDst=0 RegWrite=1 MemtoReg=1	RegWrite=1	RegWrite=0	RegWrite=0	RegWrite=0	RegWrite=0	RegWrite=1

