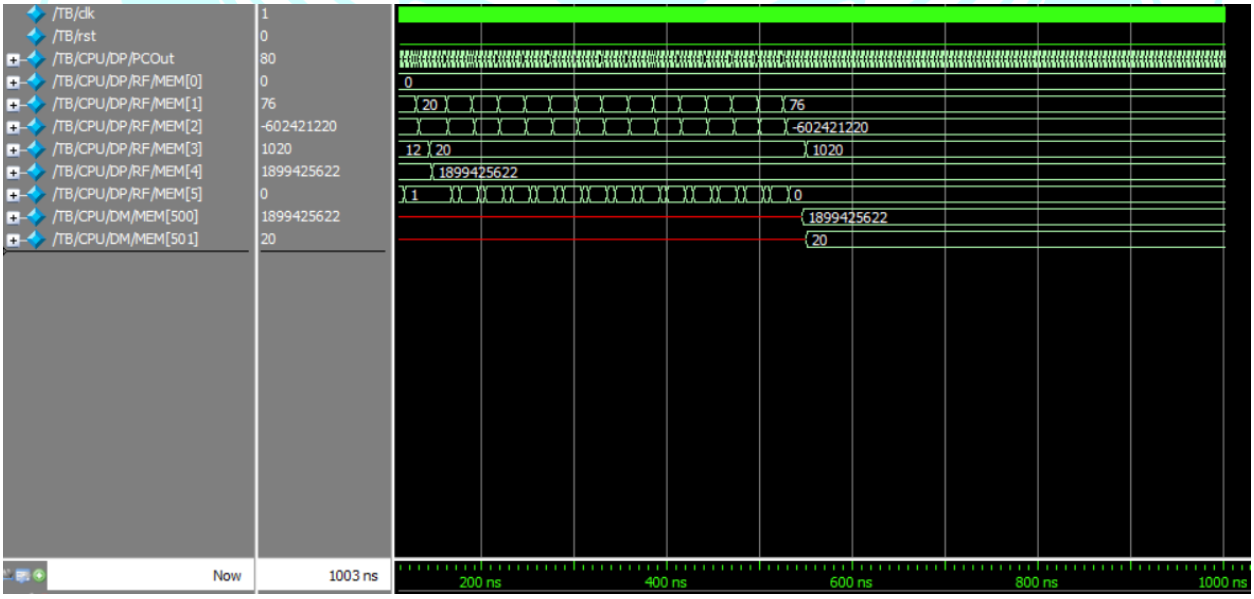
This submission includes the Datapath and Controller (“Datapath & Controller Units.pdf”), the Verilog codes (in “Verilog” folder), the pseudocode for testing (“Verilog\code.txt”), the binary code (“Verilog\inst_space.txt” has spaced code and “Verilog\inst.txt” has code without space), and a Python code (“Verilog\generate.py”) which generates 20 signed integers and stores them (“Verilog\data.txt” for binary values and “Verilog\data_interpretation.txt” for decimal values and expected answer).

For example, when “data.txt” is

```
11111011001010001001000110101111
10011110001101011001101100100101
11100110110011111110101001000001
01101010101001111110100110110001
10100010001011100111010011110101
01110001001101101110111101010110
00011110101010101001011110010100
01101011001011101110001111101001
11010100110100111111110000000010
11111100110101000001000001111011
00011011111100000111110010010111
00000101110101100110101110011000
01000001110100100000111000011110
11001001000100111010010110101100
10101010100100001101011110110110
10100100011001101001011010110000
10101100110001000010100011110010
10010010001101100111000111101000
11110010100110001100010100110000
11011100000101111100100000011100
```

the waveform is:



We have included some close-up views of the waveform: