```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   entity ResetCircuit is
7   port(
8         clock, Reset, data: in std_logic;
9         clr_PC, enable_PD: out std_logic);
10  end ResetCircuit;
11
12  architecture behavior of ResetCircuit is
13     begin
14        process(clock,Reset)
15           variable count: integer;
16              begin
17                 if clock'event and clock = '1' then
18                    if Reset = '1' then
19                       enable_PD <= '0';
20                       clr_PC <= '1';
21                       count := 0;
22                    elsif Reset = '0' then
23                       enable_PD <= '1';
24                       if count = 3 then
25                          count := 3;
26                          clr_PC <= '0';
27                       else
28                          count := count + 3;
29                       end if;
30                    end if;
31                 end if;
32        end process;
33  end behavior;
34
35
36
```