Department of Electrical, Computer
& Biomedical Engineering
Faculty of Engineering & Architectural Science

Programs: Computer Engineering

Course Number	**COE608**
Course Title	**Computer Organization and Architecture**
Semester/Year	**Winter 2020**
Instructor	**Nagi Mekhiel**

Lab Report No. 4b

Lab Title	**Data-Path Design**

Section No.	**04**
Group No.	
Submission Date	**03/10/2020**
Due Date	**03/10/2020**

Name	Student ID	Signature*
Duanwei Zhang	*500824903*	

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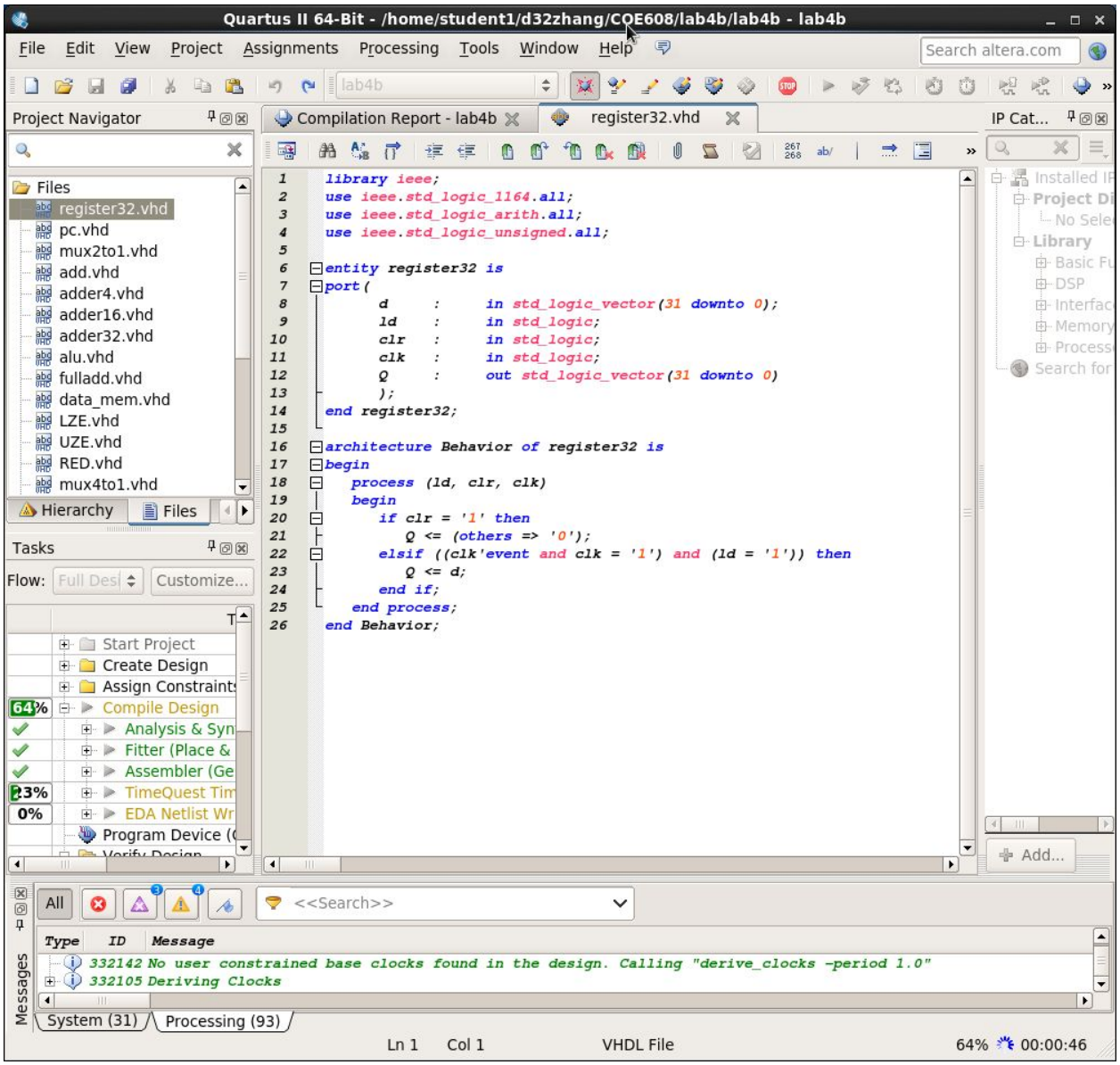
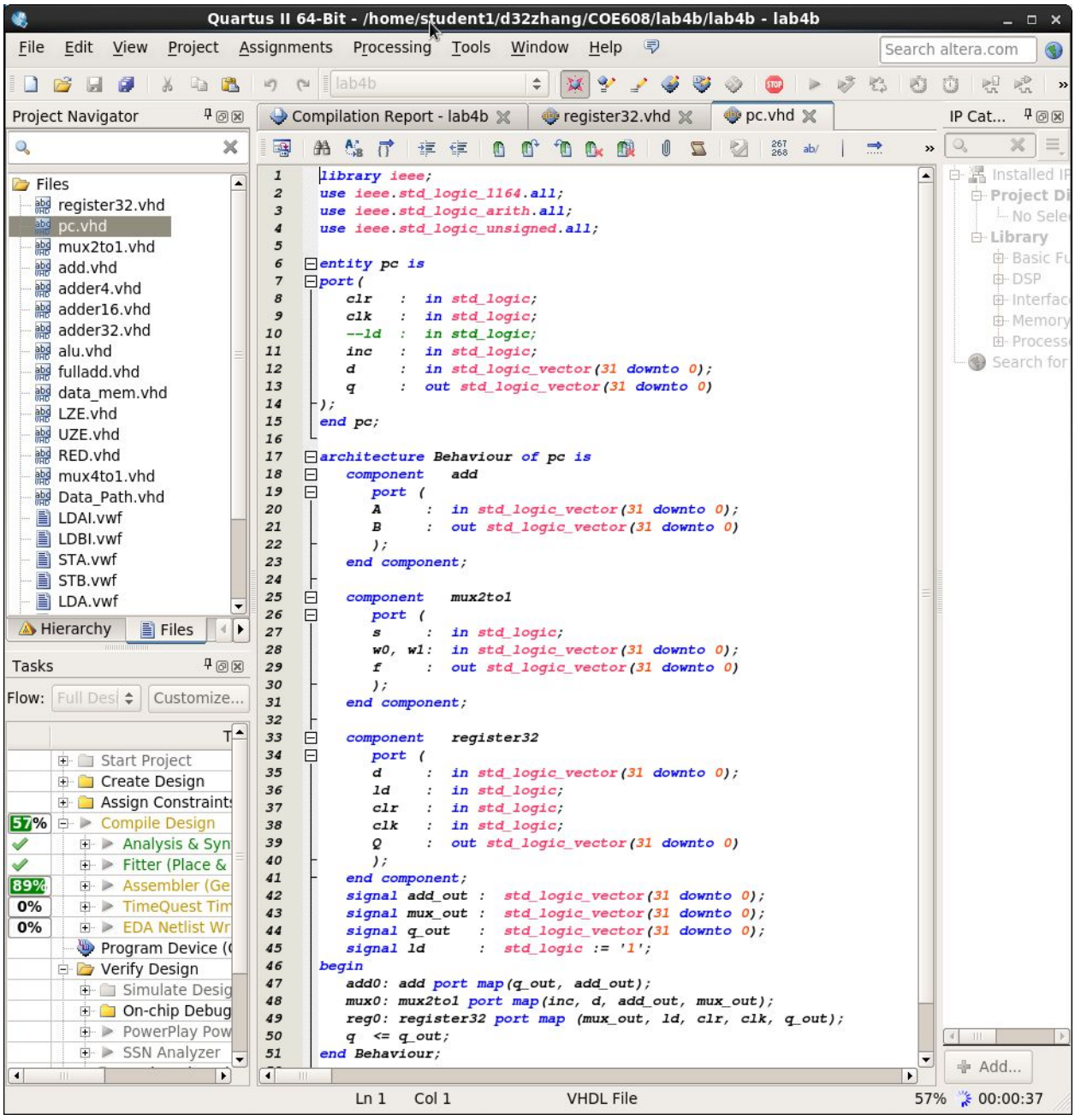
www.ryerson.ca/senate/current/pol60.pdf.

1. Register32.vhd



2. Pc.vhd


Quartus II 64-Bit - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b
File Edit View Project Assignments Processing Tools Window Help
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Project Navigator
Compilation Report - lab4b
register32.vhd
pc.vhd
IP Cat...
Files
register32.vhd
pc.vhd
mux2to1.vhd
add.vhd
adder4.vhd
adder16.vhd
adder32.vhd
alu.vhd
fulladd.vhd
data_mem.vhd
LZE.vhd
UZE.vhd
RED.vhd
mux4to1.vhd
Data_Path.vhd
LDAI.vwf
LDBI.vwf
STA.vwf
STB.vwf
LDA.vwf
Hierarchy
Files
Tasks
Flow:
Customize...
Start Project
Create Design
Assign Constraints
57%
Compile Design
Analysis & Syn
Fitter (Place &
89%
Assembler (Ge
0%
TimeQuest Tim
0%
EDA Netlist Wr
Program Device
Verify Design
Simulate Desig
On-chip Debug
PowerPlay Pow
SSN Analyzer
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.std_logic_arith.all;
4 use ieee.std_logic_unsigned.all;
5
6 entity pc is
7 port(
8 clr : in std_logic;
9 clk : in std_logic;
10 --ld : in std_logic;
11 inc : in std_logic;
12 d : in std_logic_vector(31 downto 0);
13 q : out std_logic_vector(31 downto 0)
14);
15 end pc;
16
17 architecture Behaviour of pc is
18 component add
19 port (
20 A : in std_logic_vector(31 downto 0);
21 B : out std_logic_vector(31 downto 0)
22);
23 end component;
24
25 component mux2to1
26 port (
27 s : in std_logic;
28 w0, w1: in std_logic_vector(31 downto 0);
29 f : out std_logic_vector(31 downto 0)
30);
31 end component;
32
33 component register32
34 port (
35 d : in std_logic_vector(31 downto 0);
36 ld : in std_logic;
37 clr : in std_logic;
38 clk : in std_logic;
39 Q : out std_logic_vector(31 downto 0)
40);
41 end component;
42 signal add_out : std_logic_vector(31 downto 0);
43 signal mux_out : std_logic_vector(31 downto 0);
44 signal q_out : std_logic_vector(31 downto 0);
45 signal ld : std_logic := '1';
46 begin
47 add0: add port map(q_out, add_out);
48 mux0: mux2to1 port map(inc, d, add_out, mux_out);
49 reg0: register32 port map (mux_out, ld, clr, clk, q_out);
50 q <= q_out;
51 end Behaviour;
Add...
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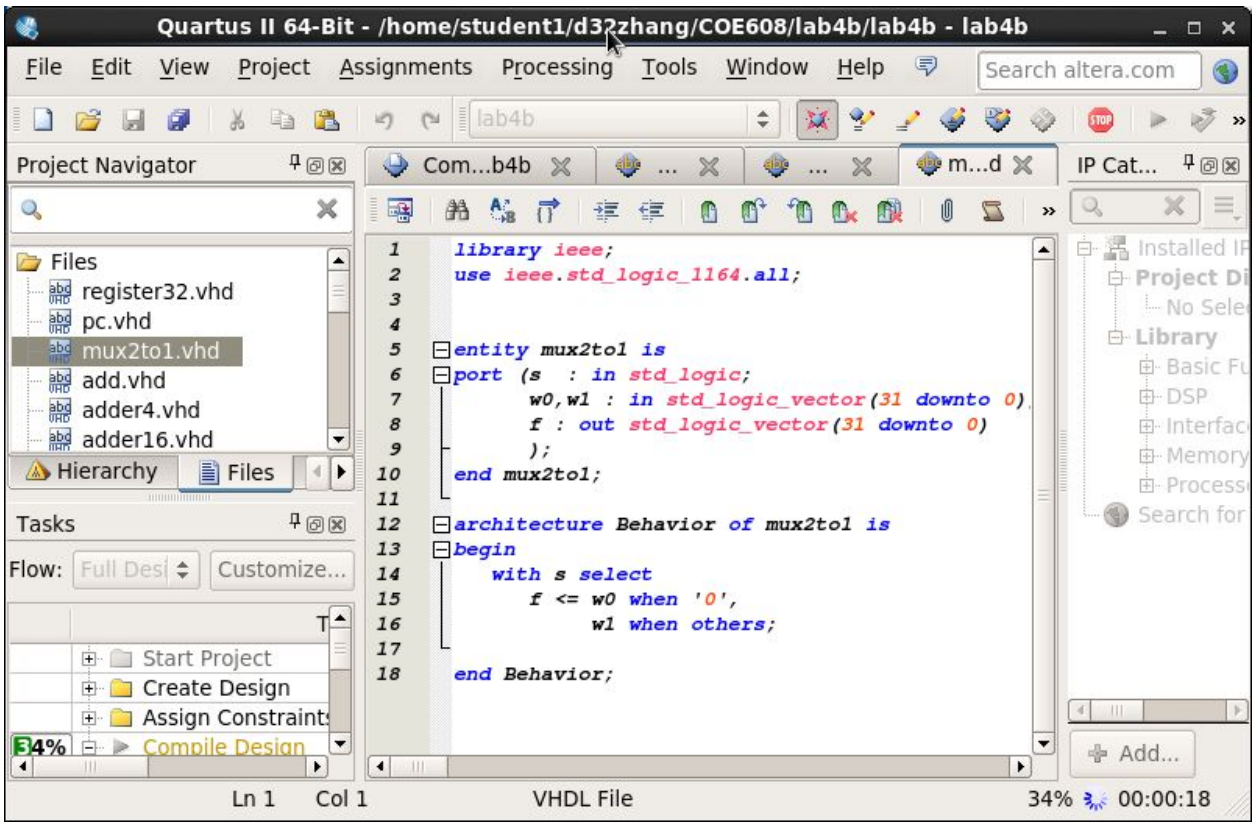
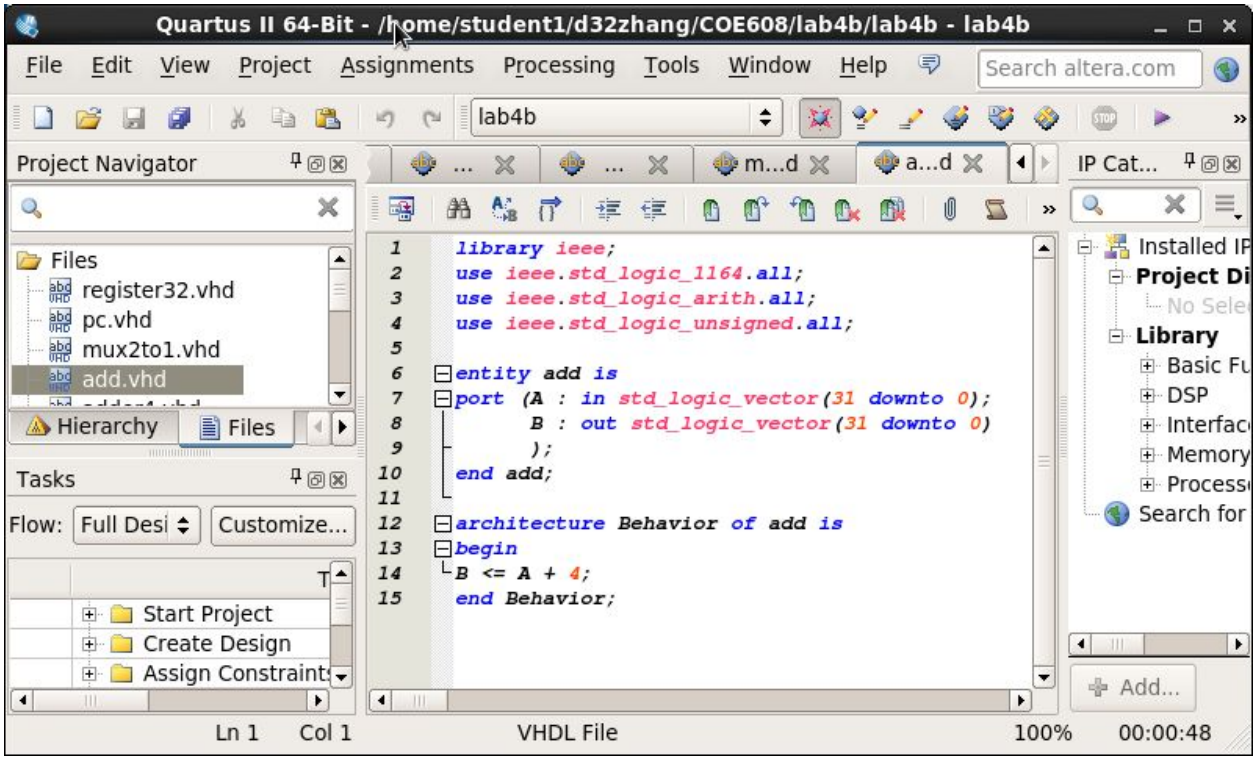
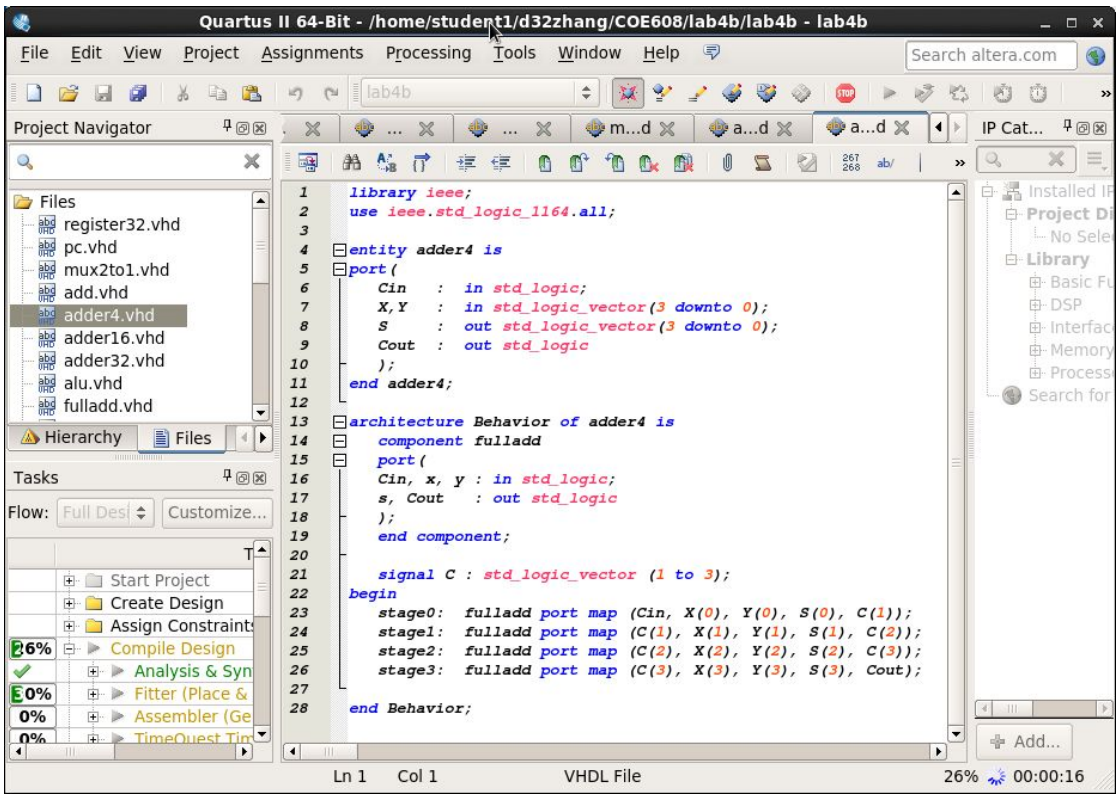
3. Mux2to1.vhd



4. Add.vhd

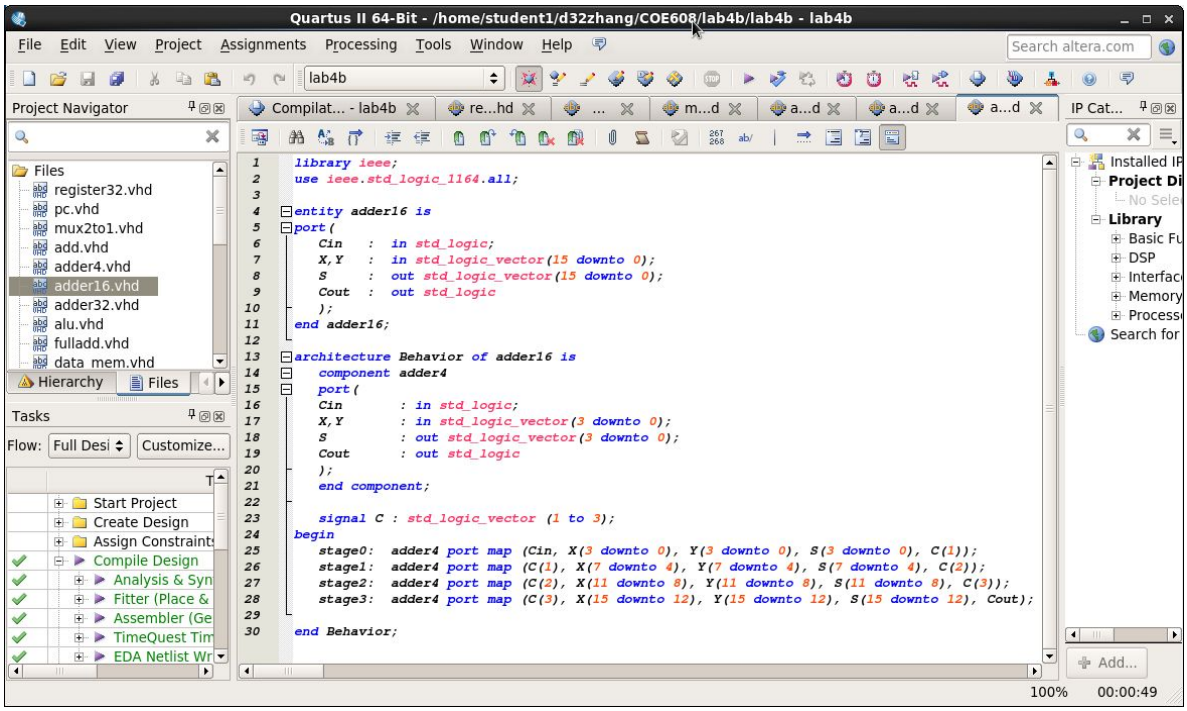


5. Adder4.vhd



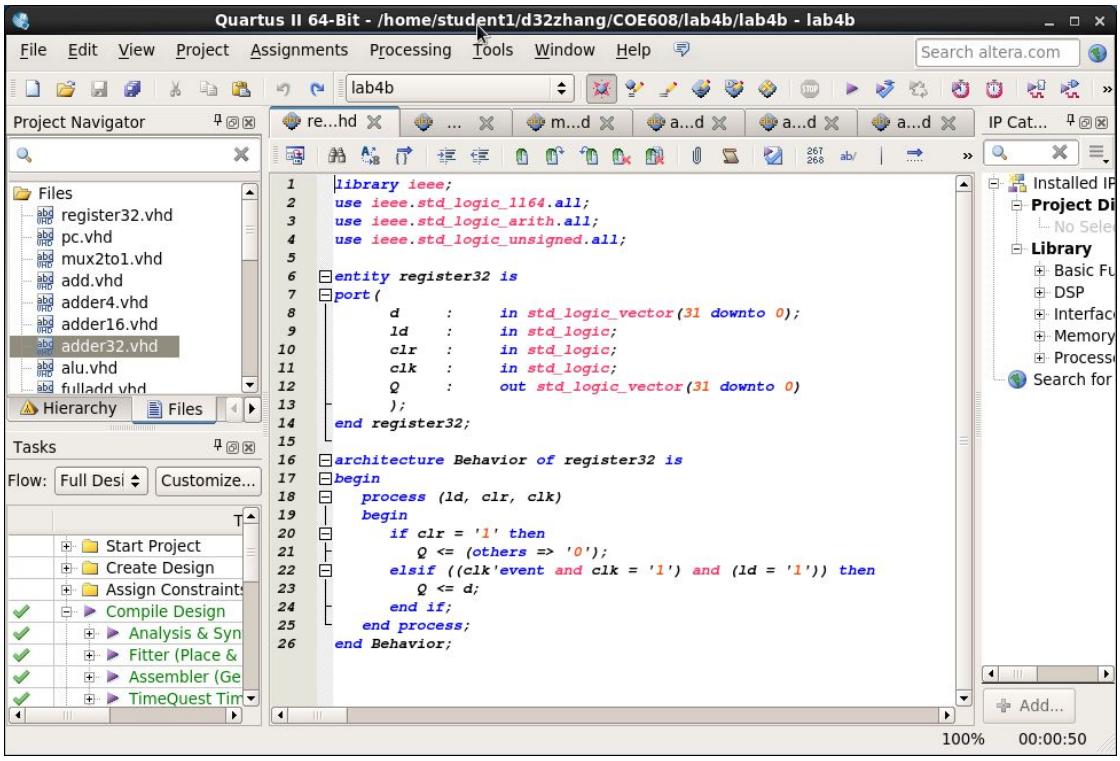

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity adder4 is
5  port(
6      Cin   :  in std_logic;
7      X,Y   :  in std_logic_vector(3 downto 0);
8      S     :  out std_logic_vector(3 downto 0);
9      Cout  :  out std_logic
10     );
11 end adder4;
12
13 architecture Behavior of adder4 is
14     component fulladd
15     port(
16     Cin, x, y : in std_logic;
17     s, Cout   : out std_logic
18     );
19     end component;
20
21     signal C : std_logic_vector (1 to 3);
22 begin
23     stage0:  fulladd port map (Cin, X(0), Y(0), S(0), C(1));
24     stage1:  fulladd port map (C(1), X(1), Y(1), S(1), C(2));
25     stage2:  fulladd port map (C(2), X(2), Y(2), S(2), C(3));
26     stage3:  fulladd port map (C(3), X(3), Y(3), S(3), Cout);
27
28 end Behavior;
```

6. Adder16.vhd



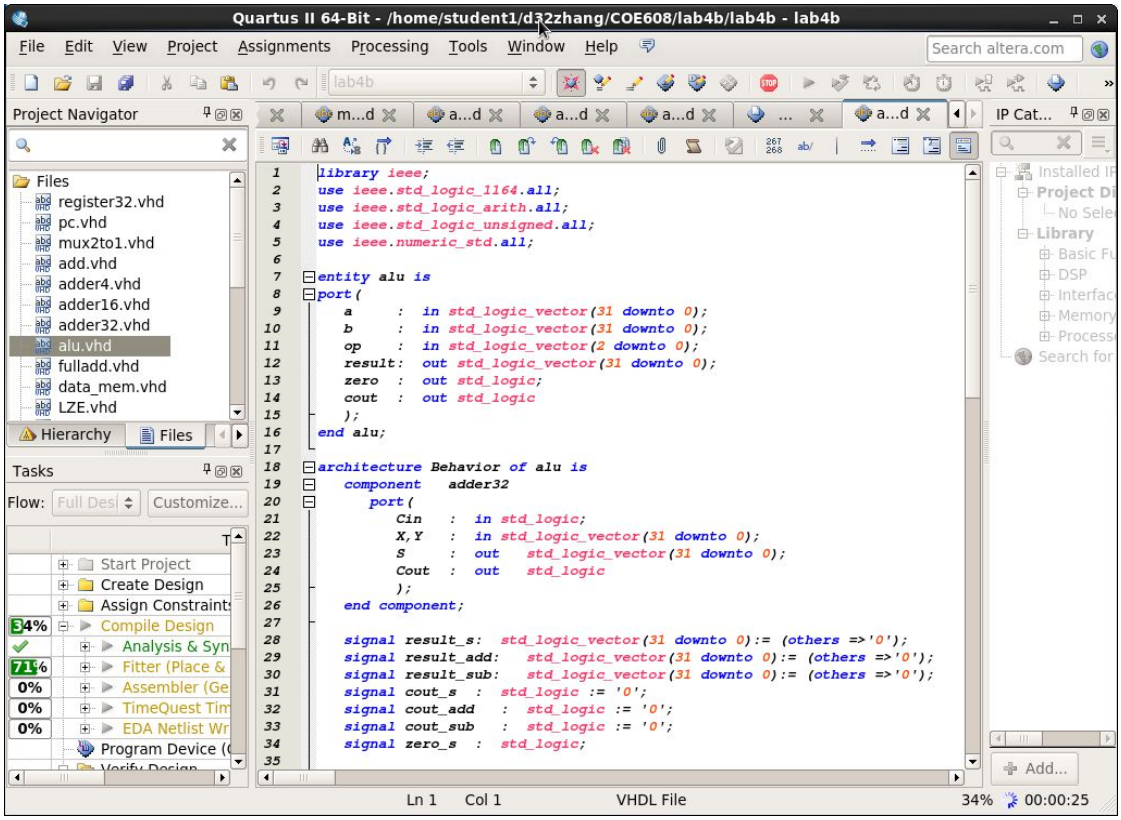

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity adder16 is
5  port(
6      Cin   :  in std_logic;
7      X,Y   :  in std_logic_vector(15 downto 0);
8      S     :  out std_logic_vector(15 downto 0);
9      Cout  :  out std_logic
10     );
11 end adder16;
12
13 architecture Behavior of adder16 is
14     component adder4
15     port(
16     Cin       : in std_logic;
17     X,Y       : in std_logic_vector(3 downto 0);
18     S         : out std_logic_vector(3 downto 0);
19     Cout      : out std_logic
20     );
21     end component;
22
23     signal C : std_logic_vector (1 to 3);
24 begin
25     stage0:  adder4 port map (Cin, X(3 downto 0), Y(3 downto 0), S(3 downto 0), C(1));
26     stage1:  adder4 port map (C(1), X(7 downto 4), Y(7 downto 4), S(7 downto 4), C(2));
27     stage2:  adder4 port map (C(2), X(11 downto 8), Y(11 downto 8), S(11 downto 8), C(3));
28     stage3:  adder4 port map (C(3), X(15 downto 12), Y(15 downto 12), S(15 downto 12), Cout);
29
30 end Behavior;
```

7. Adder32.vhd

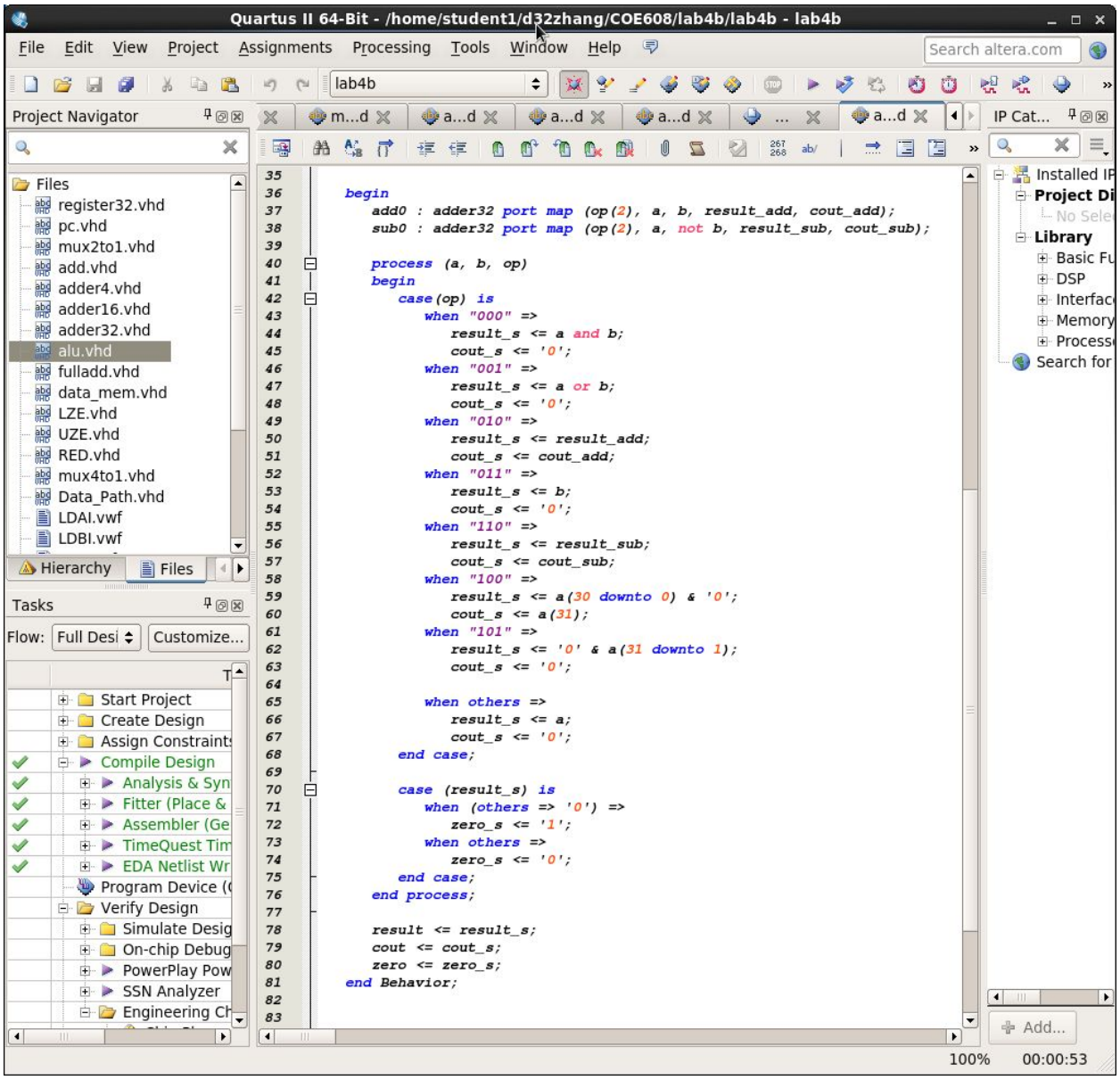



```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity register32 is
port(
      d     :     in std_logic_vector(31 downto 0);
      ld    :     in std_logic;
      clr   :     in std_logic;
      clk   :     in std_logic;
      Q     :     out std_logic_vector(31 downto 0)
      );
end register32;

architecture Behavior of register32 is
begin
   process (ld, clr, clk)
   begin
      if clr = '1' then
         Q <= (others => '0');
      elsif ((clk'event and clk = '1') and (ld = '1')) then
         Q <= d;
      end if;
   end process;
end Behavior;
```

8. Alu.vhd

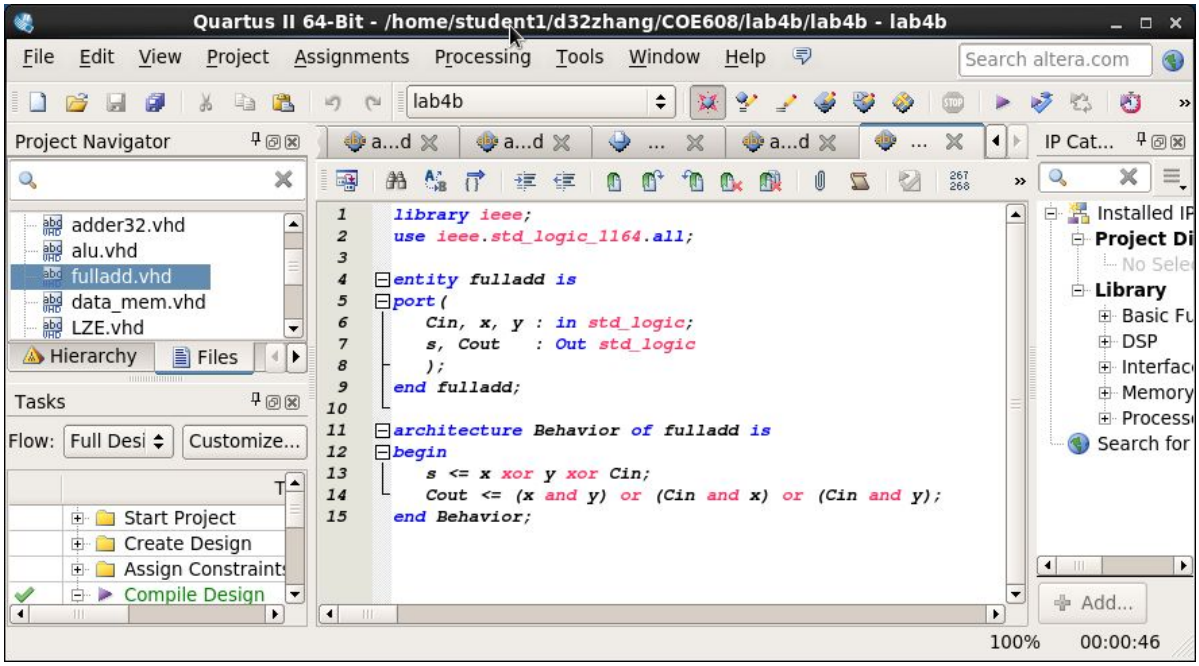



```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
use ieee.numeric_std.all;

entity alu is
port(
   a      :  in std_logic_vector(31 downto 0);
   b      :  in std_logic_vector(31 downto 0);
   op     :  in std_logic_vector(2 downto 0);
   result:  out std_logic_vector(31 downto 0);
   zero   :  out std_logic;
   cout   :  out std_logic
   );
end alu;

architecture Behavior of alu is
   component   adder32
      port(
         Cin   :  in std_logic;
         X,Y   :  in std_logic_vector(31 downto 0);
         S     :  out   std_logic_vector(31 downto 0);
         Cout  :  out   std_logic
         );
   end component;

   signal result_s:  std_logic_vector(31 downto 0):= (others =>'0');
   signal result_add:   std_logic_vector(31 downto 0):= (others =>'0');
   signal result_sub:   std_logic_vector(31 downto 0):= (others =>'0');
   signal cout_s  :  std_logic := '0';
   signal cout_add   :  std_logic := '0';
   signal cout_sub   :  std_logic := '0';
   signal zero_s  :  std_logic;
```



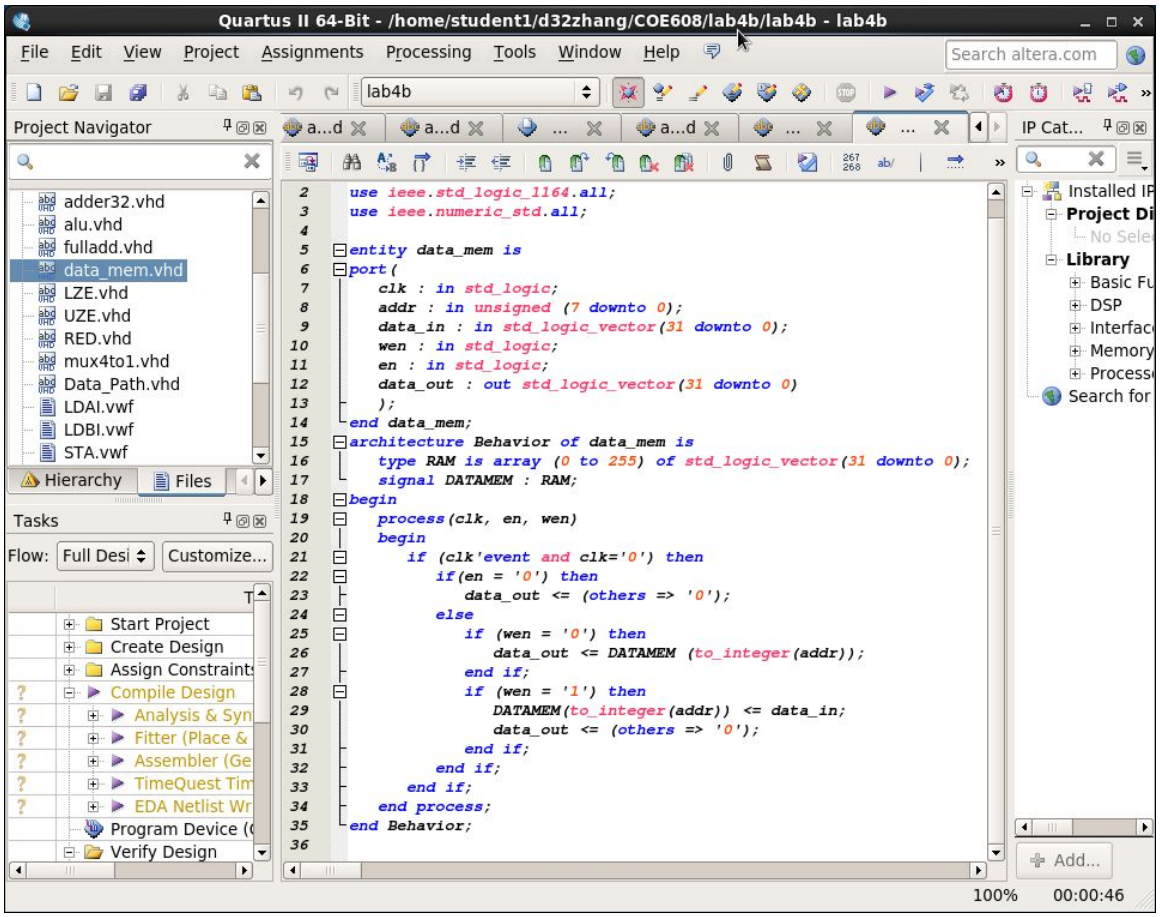

```
35
36      begin
37         add0 : adder32 port map (op(2), a, b, result_add, cout_add);
38         sub0 : adder32 port map (op(2), a, not b, result_sub, cout_sub);
39
40         process (a, b, op)
41         begin
42            case(op) is
43               when "000" =>
44                  result_s <= a and b;
45                  cout_s <= '0';
46               when "001" =>
47                  result_s <= a or b;
48                  cout_s <= '0';
49               when "010" =>
50                  result_s <= result_add;
51                  cout_s <= cout_add;
52               when "011" =>
53                  result_s <= b;
54                  cout_s <= '0';
55               when "110" =>
56                  result_s <= result_sub;
57                  cout_s <= cout_sub;
58               when "100" =>
59                  result_s <= a(30 downto 0) & '0';
60                  cout_s <= a(31);
61               when "101" =>
62                  result_s <= '0' & a(31 downto 1);
63                  cout_s <= '0';
64
65               when others =>
66                  result_s <= a;
67                  cout_s <= '0';
68            end case;
69
70            case (result_s) is
71               when (others => '0') =>
72                  zero_s <= '1';
73               when others =>
74                  zero_s <= '0';
75            end case;
76         end process;
77
78         result <= result_s;
79         cout <= cout_s;
80         zero <= zero_s;
81      end Behavior;
82
83
```

9. Fulladd.vhd



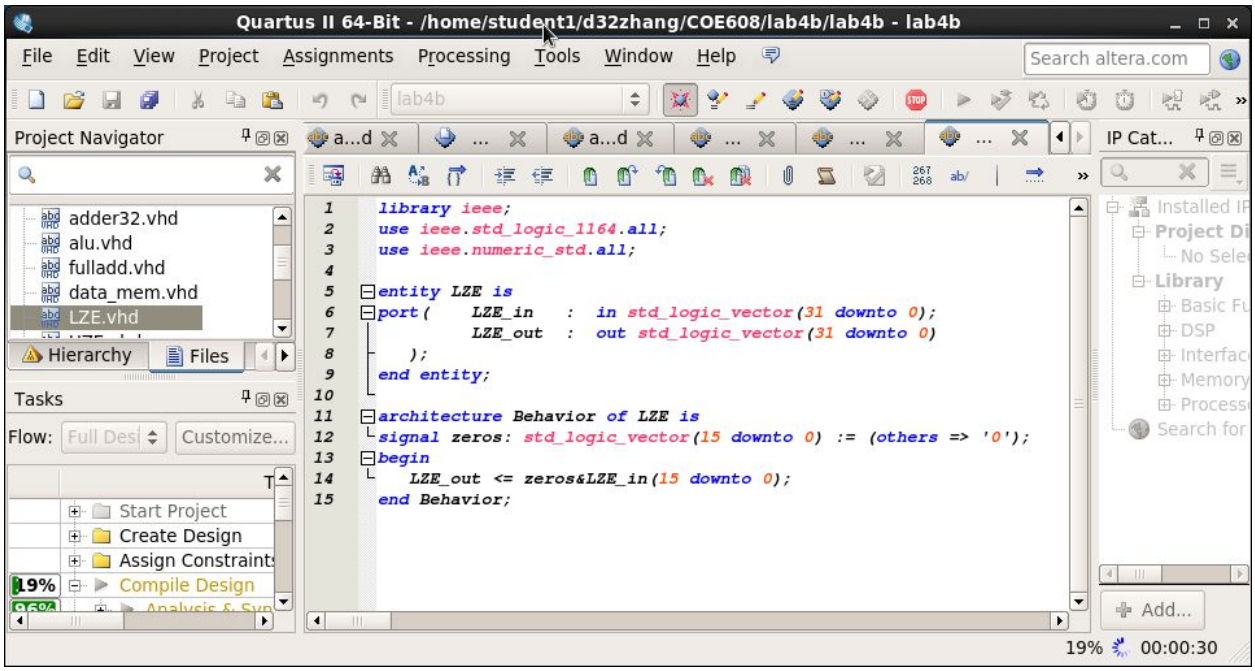

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity fulladd is
5  port(
6      Cin, x, y : in std_logic;
7      s, Cout   : Out std_logic
8      );
9  end fulladd;
10
11 architecture Behavior of fulladd is
12 begin
13     s <= x xor y xor Cin;
14     Cout <= (x and y) or (Cin and x) or (Cin and y);
15 end Behavior;
```

10. Data_mem.vhd

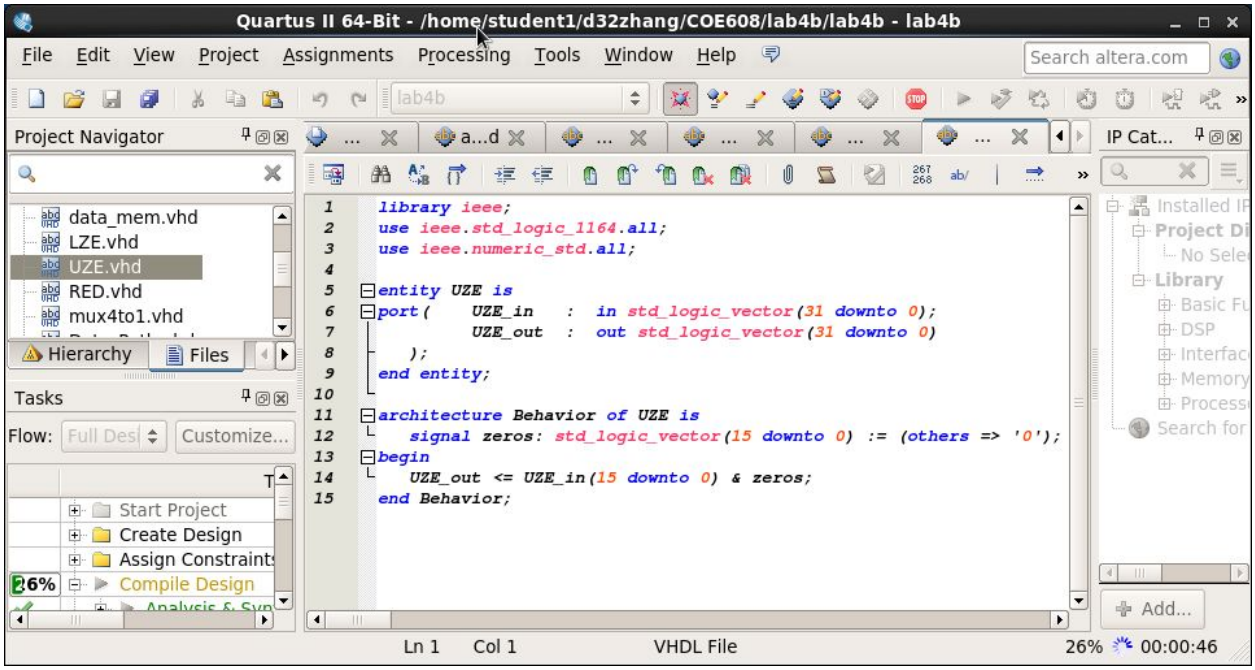



```
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity data_mem is
6  port(
7      clk : in std_logic;
8      addr : in unsigned (7 downto 0);
9      data_in : in std_logic_vector(31 downto 0);
10     wen : in std_logic;
11     en : in std_logic;
12     data_out : out std_logic_vector(31 downto 0)
13     );
14 end data_mem;
15 architecture Behavior of data_mem is
16     type RAM is array (0 to 255) of std_logic_vector(31 downto 0);
17     signal DATAMEM : RAM;
18 begin
19     process(clk, en, wen)
20     begin
21         if (clk'event and clk='0') then
22             if(en = '0') then
23                 data_out <= (others => '0');
24             else
25                 if (wen = '0') then
26                     data_out <= DATAMEM (to_integer(addr));
27                 end if;
28                 if (wen = '1') then
29                     DATAMEM(to_integer(addr)) <= data_in;
30                     data_out <= (others => '0');
31                 end if;
32             end if;
33         end if;
34     end process;
35 end Behavior;
36
```

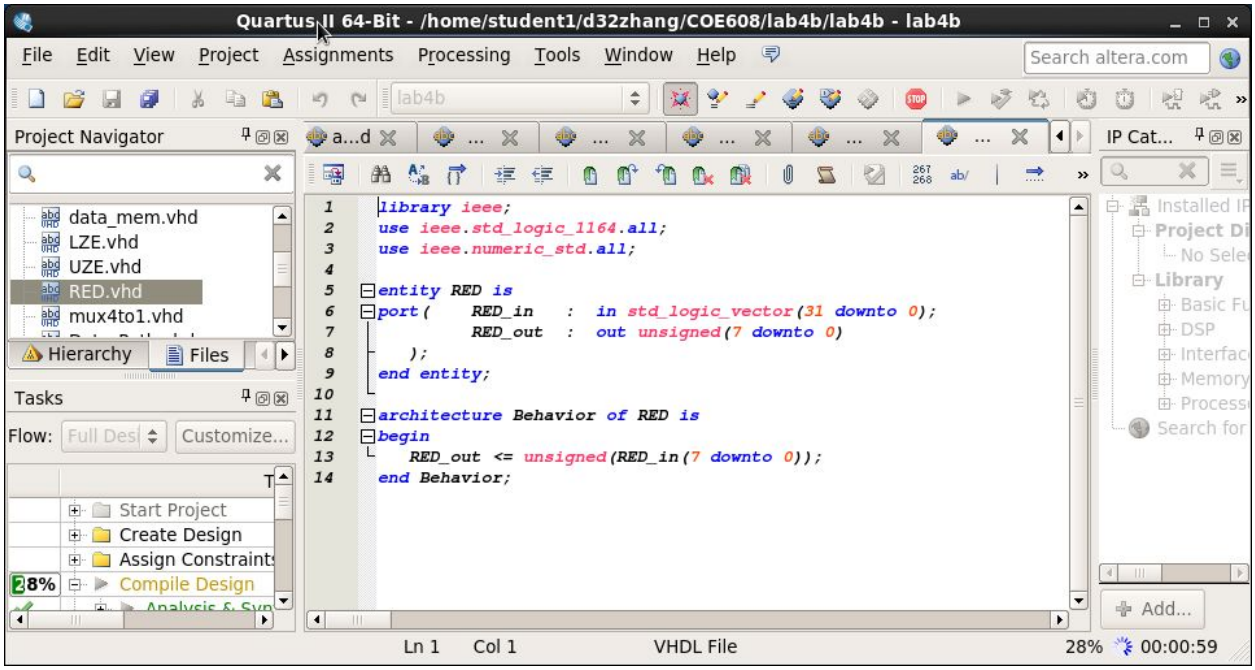
11. LZE.vhd



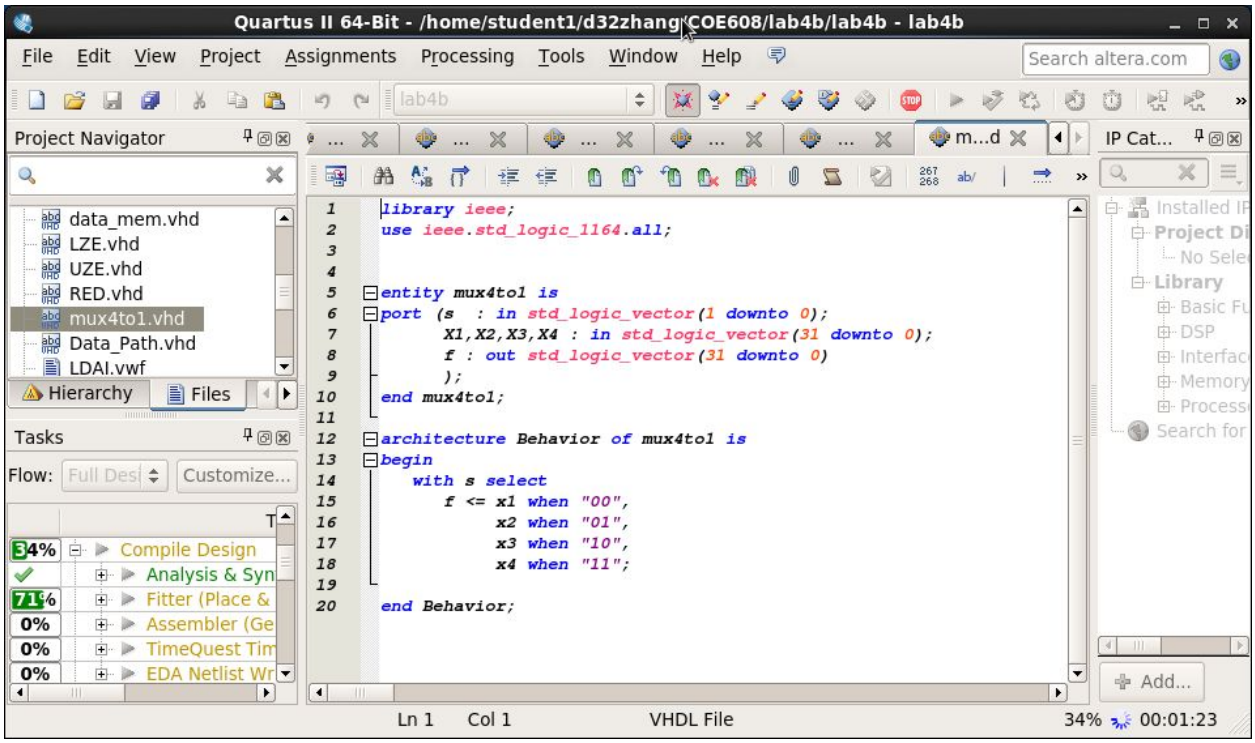
12. UZE.vhd



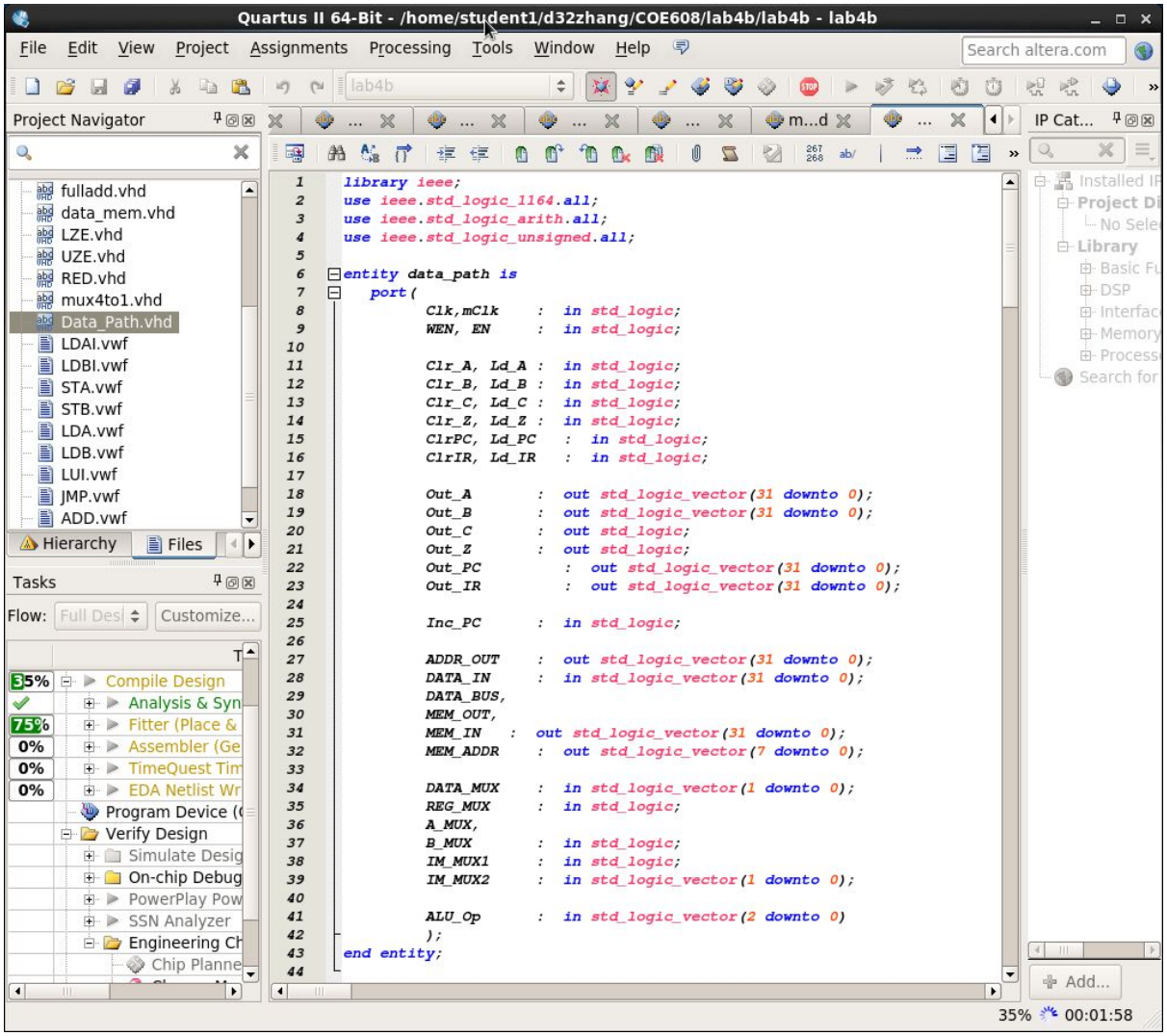
13. RED.vhd



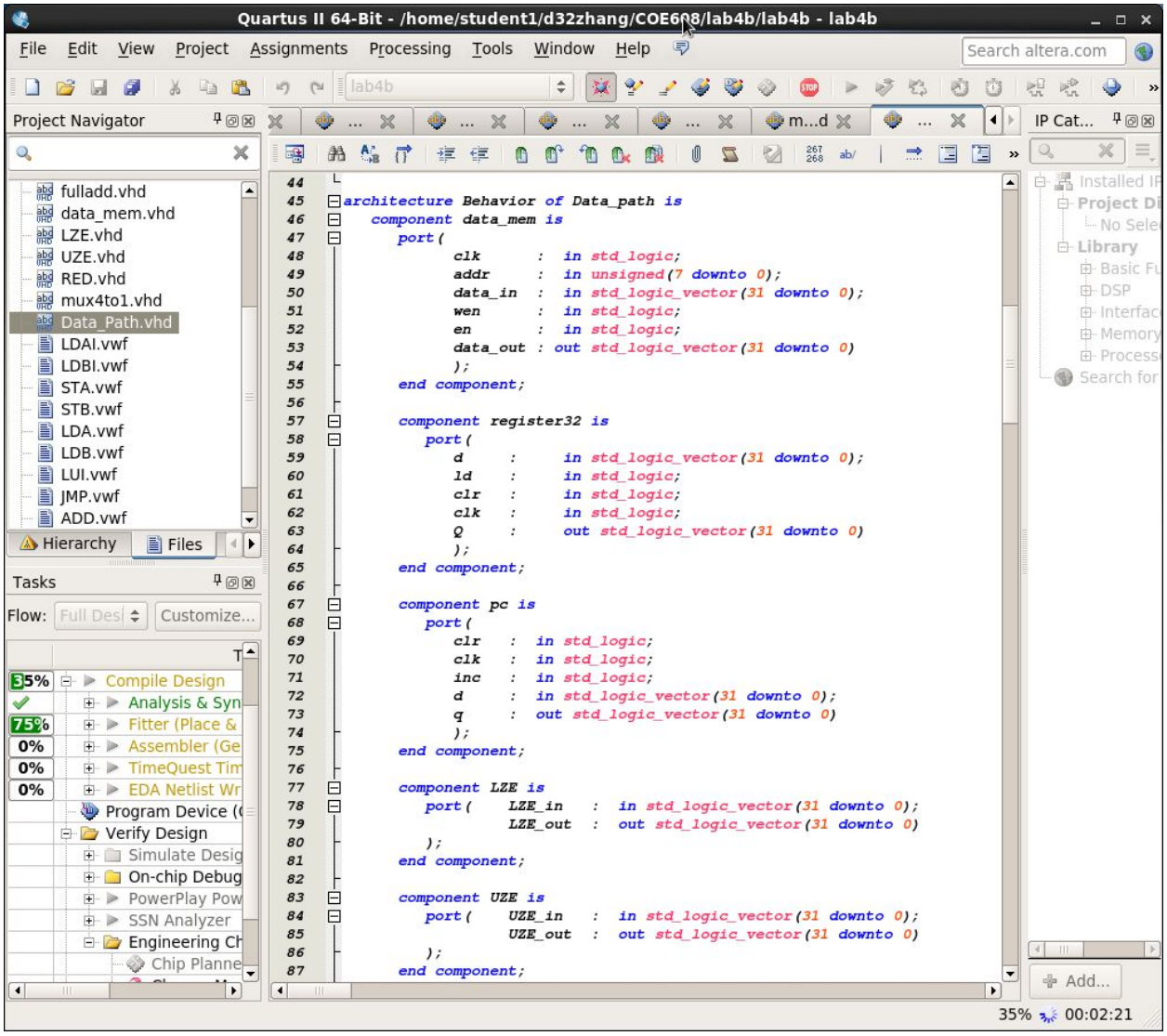
14. Mux4to1.vhd



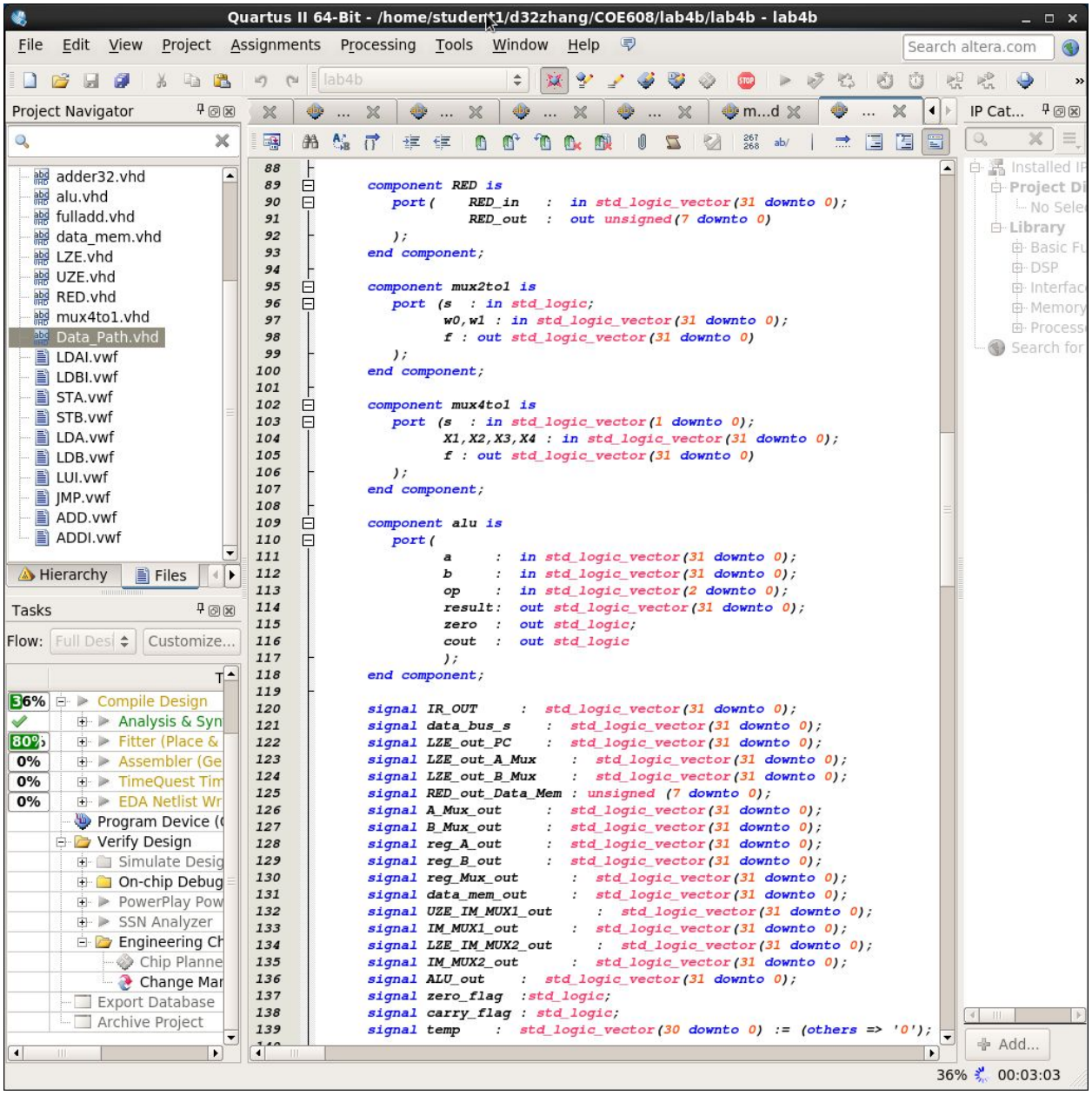
15. Data_Path.vhd



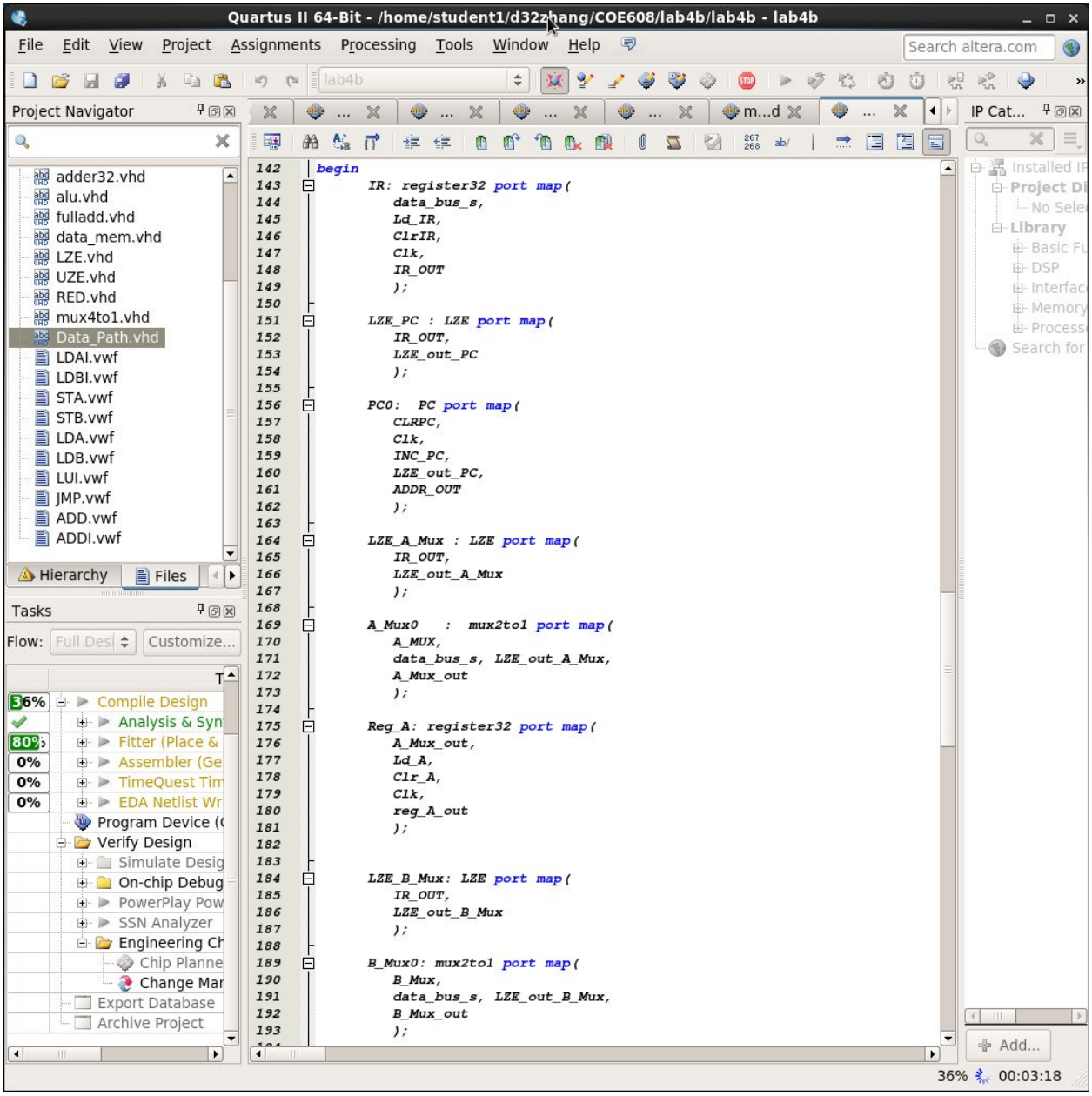

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   entity data_path is
7      port(
8            Clk,mClk    :  in std_logic;
9            WEN, EN     :  in std_logic;
10
11           Clr_A, Ld_A :  in std_logic;
12           Clr_B, Ld_B :  in std_logic;
13           Clr_C, Ld_C :  in std_logic;
14           Clr_Z, Ld_Z :  in std_logic;
15           ClrPC, Ld_PC   :  in std_logic;
16           ClrIR, Ld_IR   :  in std_logic;
17
18           Out_A       :  out std_logic_vector(31 downto 0);
19           Out_B       :  out std_logic_vector(31 downto 0);
20           Out_C       :  out std_logic;
21           Out_Z       :  out std_logic;
22           Out_PC         :  out std_logic_vector(31 downto 0);
23           Out_IR         :  out std_logic_vector(31 downto 0);
24
25           Inc_PC      :  in std_logic;
26
27           ADDR_OUT    :  out std_logic_vector(31 downto 0);
28           DATA_IN     :  in std_logic_vector(31 downto 0);
29           DATA_BUS,
30           MEM_OUT,
31           MEM_IN   :  out std_logic_vector(31 downto 0);
32           MEM_ADDR    :  out std_logic_vector(7 downto 0);
33
34           DATA_MUX    :  in std_logic_vector(1 downto 0);
35           REG_MUX     :  in std_logic;
36           A_MUX,
37           B_MUX       :  in std_logic;
38           IM_MUX1     :  in std_logic;
39           IM_MUX2     :  in std_logic_vector(1 downto 0);
40
41           ALU_Op      :  in std_logic_vector(2 downto 0)
42           );
43  end entity;
44
```



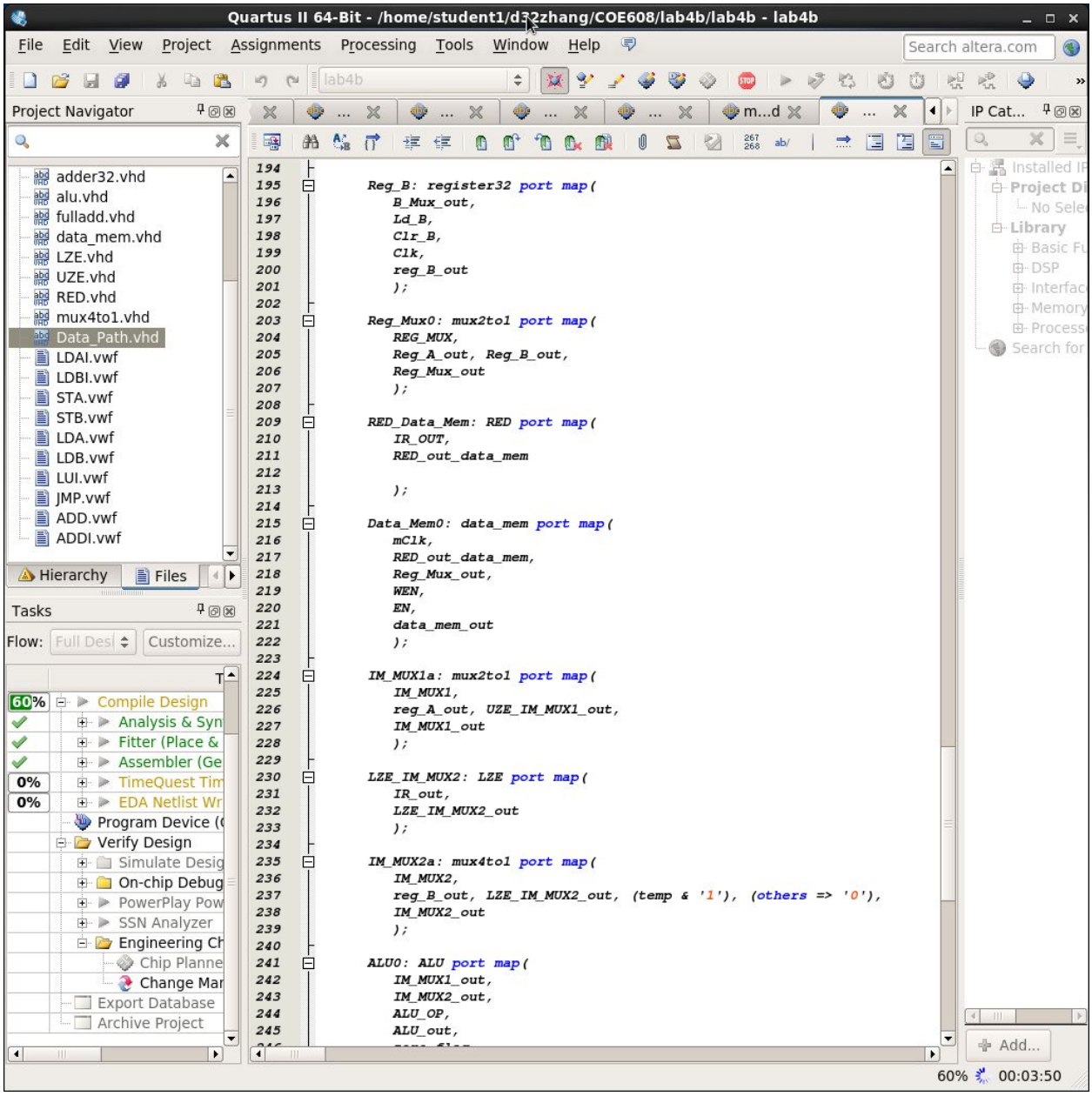

```
44
45  architecture Behavior of Data_path is
46     component data_mem is
47        port(
48              clk      :  in std_logic;
49              addr     :  in unsigned(7 downto 0);
50              data_in  :  in std_logic_vector(31 downto 0);
51              wen      :  in std_logic;
52              en       :  in std_logic;
53              data_out : out std_logic_vector(31 downto 0)
54              );
55        end component;
56
57        component register32 is
58           port(
59              d     :     in std_logic_vector(31 downto 0);
60              ld    :     in std_logic;
61              clr   :     in std_logic;
62              clk   :     in std_logic;
63              Q     :     out std_logic_vector(31 downto 0)
64              );
65        end component;
66
67        component pc is
68           port(
69              clr   :  in std_logic;
70              clk   :  in std_logic;
71              inc   :  in std_logic;
72              d     :  in std_logic_vector(31 downto 0);
73              q     :  out std_logic_vector(31 downto 0)
74              );
75        end component;
76
77        component LZE is
78           port(    LZE_in   :  in std_logic_vector(31 downto 0);
79                    LZE_out  :  out std_logic_vector(31 downto 0)
80           );
81        end component;
82
83        component UZE is
84           port(    UZE_in   :  in std_logic_vector(31 downto 0);
85                    UZE_out  :  out std_logic_vector(31 downto 0)
86           );
87        end component;
```



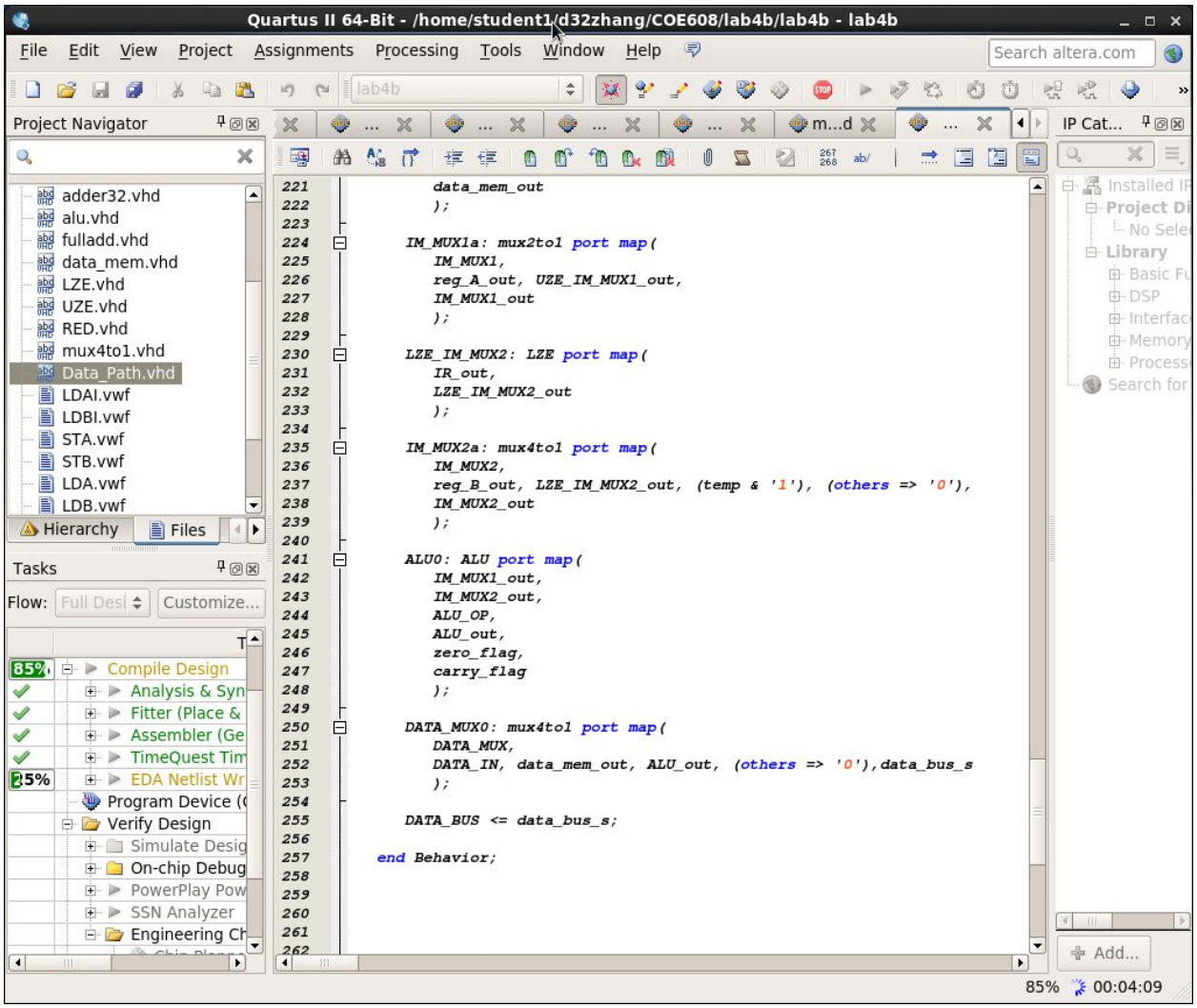

```
88
89      component RED is
90         port(    RED_in   :  in std_logic_vector(31 downto 0);
91                  RED_out  :  out unsigned(7 downto 0)
92         );
93      end component;
94
95      component mux2to1 is
96         port (s  : in std_logic;
97               w0,w1 : in std_logic_vector(31 downto 0);
98               f : out std_logic_vector(31 downto 0)
99         );
100     end component;
101
102     component mux4to1 is
103        port (s  : in std_logic_vector(1 downto 0);
104              X1,X2,X3,X4 : in std_logic_vector(31 downto 0);
105              f : out std_logic_vector(31 downto 0)
106        );
107     end component;
108
109     component alu is
110        port(
111              a      :  in std_logic_vector(31 downto 0);
112              b      :  in std_logic_vector(31 downto 0);
113              op     :  in std_logic_vector(2 downto 0);
114              result:   out std_logic_vector(31 downto 0);
115              zero   :  out std_logic;
116              cout   :  out std_logic
117              );
118     end component;
119
120     signal IR_OUT     :  std_logic_vector(31 downto 0);
121     signal data_bus_s     :  std_logic_vector(31 downto 0);
122     signal LZE_out_PC     :  std_logic_vector(31 downto 0);
123     signal LZE_out_A_Mux     :  std_logic_vector(31 downto 0);
124     signal LZE_out_B_Mux     :  std_logic_vector(31 downto 0);
125     signal RED_out_Data_Mem : unsigned (7 downto 0);
126     signal A_Mux_out      :  std_logic_vector(31 downto 0);
127     signal B_Mux_out      :  std_logic_vector(31 downto 0);
128     signal reg_A_out      :  std_logic_vector(31 downto 0);
129     signal reg_B_out      :  std_logic_vector(31 downto 0);
130     signal reg_Mux_out       :  std_logic_vector(31 downto 0);
131     signal data_mem_out      :  std_logic_vector(31 downto 0);
132     signal UZE_IM_MUX1_out      :  std_logic_vector(31 downto 0);
133     signal IM_MUX1_out       :  std_logic_vector(31 downto 0);
134     signal LZE_IM_MUX2_out      :  std_logic_vector(31 downto 0);
135     signal IM_MUX2_out       :  std_logic_vector(31 downto 0);
136     signal ALU_out     :  std_logic_vector(31 downto 0);
137     signal zero_flag  :std_logic;
138     signal carry_flag : std_logic;
139     signal temp     :  std_logic_vector(30 downto 0) := (others => '0');
```




```
142   begin
143         IR: register32 port map(
144            data_bus_s,
145            Ld_IR,
146            ClrIR,
147            Clk,
148            IR_OUT
149            );
150
151         LZE_PC : LZE port map(
152            IR_OUT,
153            LZE_out_PC
154            );
155
156         PC0:  PC port map(
157            CLRPC,
158            Clk,
159            INC_PC,
160            LZE_out_PC,
161            ADDR_OUT
162            );
163
164         LZE_A_Mux : LZE port map(
165            IR_OUT,
166            LZE_out_A_Mux
167            );
168
169         A_Mux0    :  mux2to1 port map(
170            A_MUX,
171            data_bus_s, LZE_out_A_Mux,
172            A_Mux_out
173            );
174
175         Reg_A: register32 port map(
176            A_Mux_out,
177            Ld_A,
178            Clr_A,
179            Clk,
180            reg_A_out
181            );
182
183
184         LZE_B_Mux: LZE port map(
185            IR_OUT,
186            LZE_out_B_Mux
187            );
188
189         B_Mux0: mux2to1 port map(
190            B_Mux,
191            data_bus_s, LZE_out_B_Mux,
192            B_Mux_out
193            );
```




```
194
195       Reg_B: register32 port map(
196          B_Mux_out,
197          Ld_B,
198          Clr_B,
199          Clk,
200          reg_B_out
201          );
202
203       Reg_Mux0: mux2to1 port map(
204          REG_MUX,
205          Reg_A_out, Reg_B_out,
206          Reg_Mux_out
207          );
208
209       RED_Data_Mem: RED port map(
210          IR_OUT,
211          RED_out_data_mem
212
213          );
214
215       Data_Mem0: data_mem port map(
216          mClk,
217          RED_out_data_mem,
218          Reg_Mux_out,
219          WEN,
220          EN,
221          data_mem_out
222          );
223
224       IM_MUX1a: mux2to1 port map(
225          IM_MUX1,
226          reg_A_out, UZE_IM_MUX1_out,
227          IM_MUX1_out
228          );
229
230       LZE_IM_MUX2: LZE port map(
231          IR_out,
232          LZE_IM_MUX2_out
233          );
234
235       IM_MUX2a: mux4to1 port map(
236          IM_MUX2,
237          reg_B_out, LZE_IM_MUX2_out, (temp & '1'), (others => '0'),
238          IM_MUX2_out
239          );
240
241       ALU0: ALU port map(
242          IM_MUX1_out,
243          IM_MUX2_out,
244          ALU_OP,
245          ALU_out,
```


Quartus II 64-Bit - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab4b
Project Navigator
adder32.vhd
alu.vhd
fulladd.vhd
data_mem.vhd
LZE.vhd
UZE.vhd
RED.vhd
mux4to1.vhd
Data_Path.vhd
LDAI.vwf
LDBI.vwf
STA.vwf
STB.vwf
LDA.vwf
LDB.vwf
Hierarchy
Files
Tasks
Flow:
Full Desi
Customize...
85%
Compile Design
Analysis & Syn
Fitter (Place &
Assembler (Ge
TimeQuest Tim
25%
EDA Netlist Wr
Program Device (
Verify Design
Simulate Desig
On-chip Debug
PowerPlay Pow
SSN Analyzer
Engineering Ch
IP Cat...
Installed IP
Project Di
No Sele
Library
Basic Fu
DSP
Interfac
Memory
Process
Search for
Add...
85%
00:04:09
221 data_mem_out
222);
223
224 IM_MUX1a: mux2to1 port map(
225 IM_MUX1,
226 reg_A_out, UZE_IM_MUX1_out,
227 IM_MUX1_out
228);
229
230 LZE_IM_MUX2: LZE port map(
231 IR_out,
232 LZE_IM_MUX2_out
233);
234
235 IM_MUX2a: mux4to1 port map(
236 IM_MUX2,
237 reg_B_out, LZE_IM_MUX2_out, (temp & '1'), (others => '0'),
238 IM_MUX2_out
239);
240
241 ALU0: ALU port map(
242 IM_MUX1_out,
243 IM_MUX2_out,
244 ALU_OP,
245 ALU_out,
246 zero_flag,
247 carry_flag
248);
249
250 DATA_MUX0: mux4to1 port map(
251 DATA_MUX,
252 DATA_IN, data_mem_out, ALU_out, (others => '0'),data_bus_s
253);
254
255 DATA_BUS <= data_bus_s;
256
257 end Behavior;
258
259
260
261
262

How does this data-path implement the INCA, ADDI, LDBI and LDA operations?

For INCA operation, we first load LD_A,LD_C,LD_Z, assign A MUX to 0, Data MUX to 10, IM_MUX1 TO 0, IM_MUX2 to 10, and then go to the operation code “010” in alu, alu calculates the assigned value to produce the result.

For ADDI operation, we first load LD_A,LD_C,LD_Z, assign A MUX to 0, Data MUX to 10, IM_MUX1 TO 0, IM_MUX2 to 01, and then go to the operation code “010” in alu, alu calculates the assigned value to produce the result.

For LDBI operation, we first load LD_B, assign B MUX to 1.

For ADDI operation, we first load LD_A, assign EN to 1, assign WEN to 0, assign A MUX to 0, and Data MUX to 01.

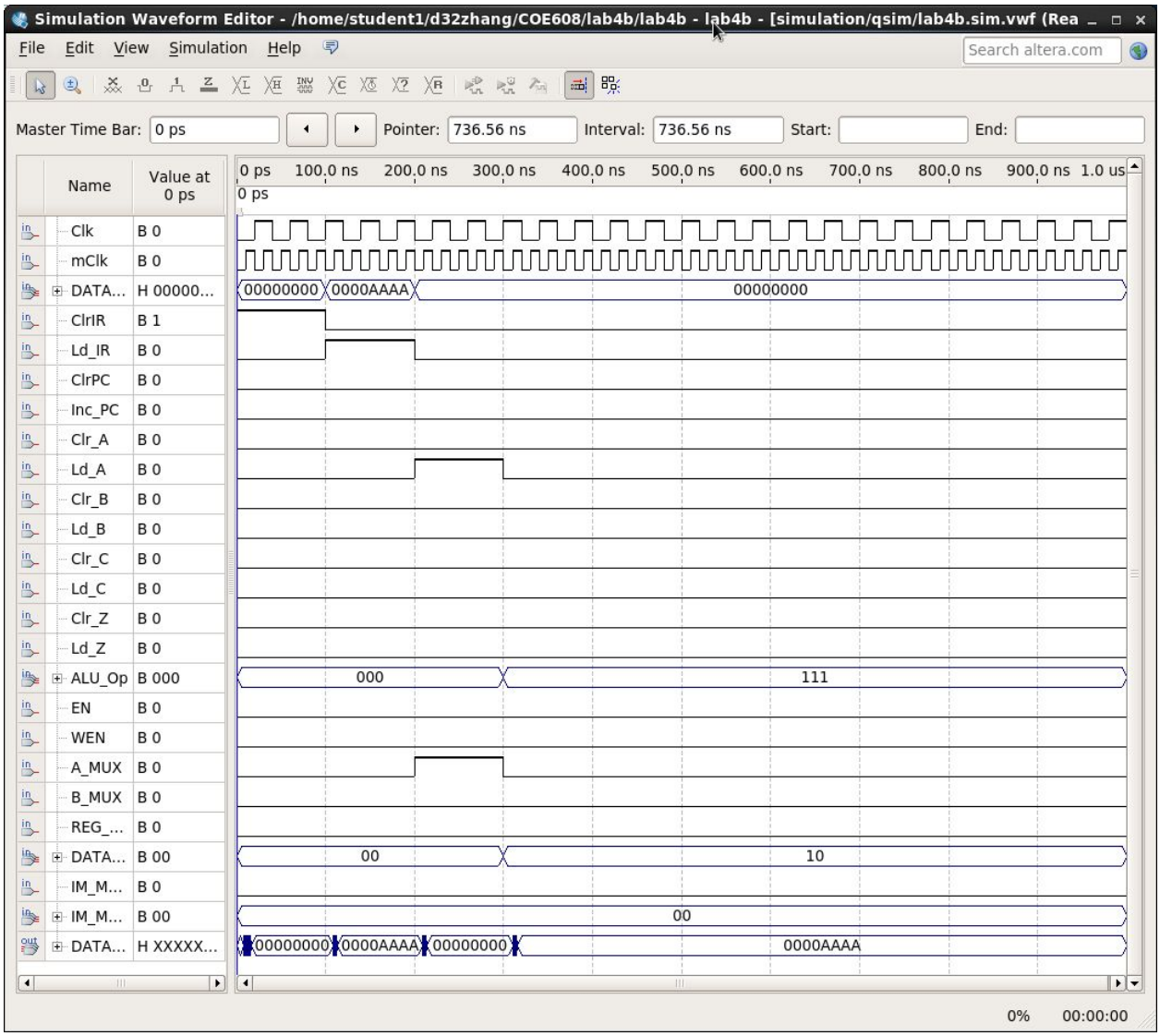
The data-path has a maximum reliable operating speed (Clk). What determines this speed? (i.e. how would you estimate the data-path circuit clock)?

Delays determine the maximum reliable operating speed, every time a different input was passed in, the corresponding result was generated with some delays, delays may be different than others.

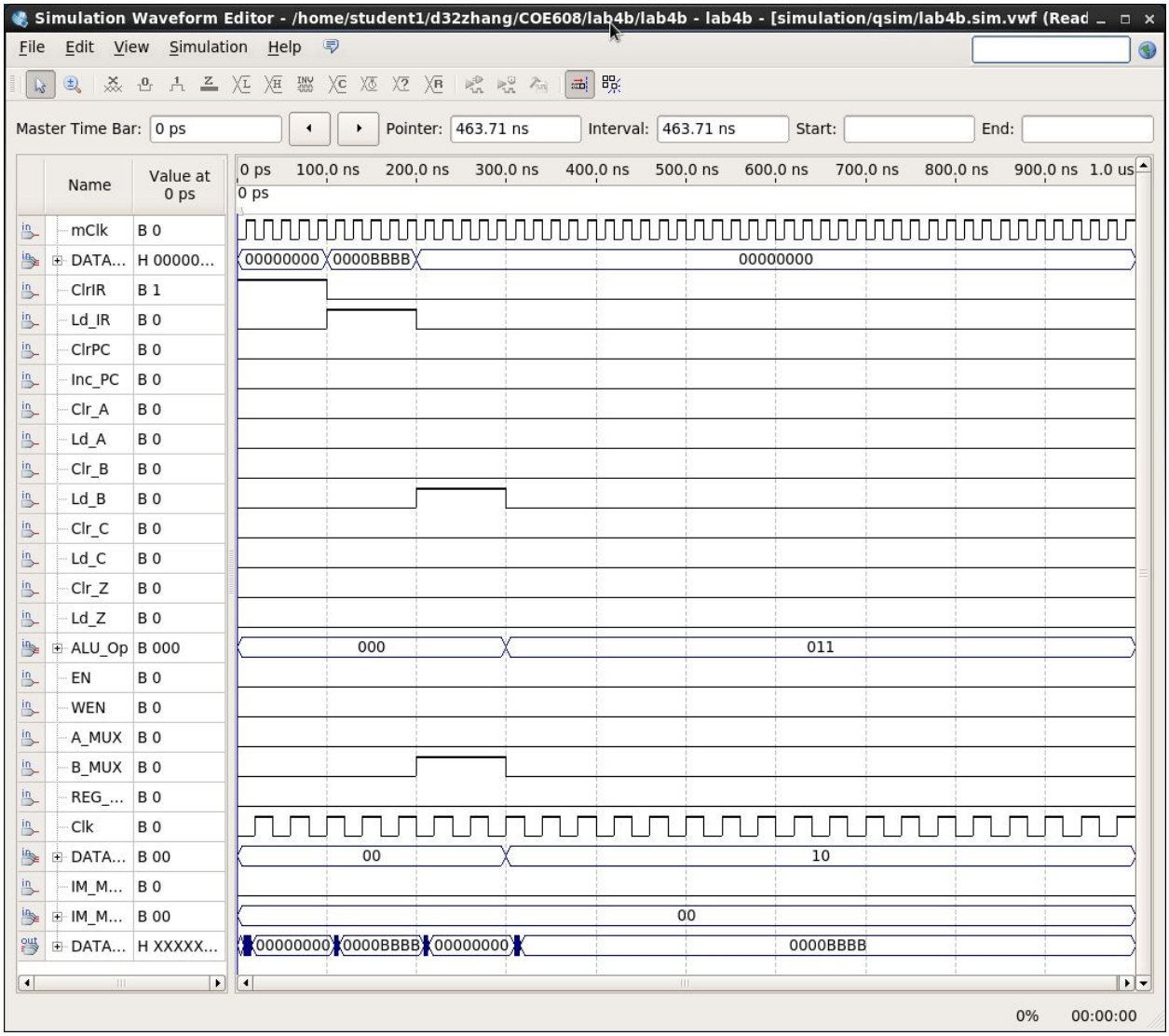
What is a reliable limit for you data-path clock?

The reliable limit for my data-path clock was 8.806.

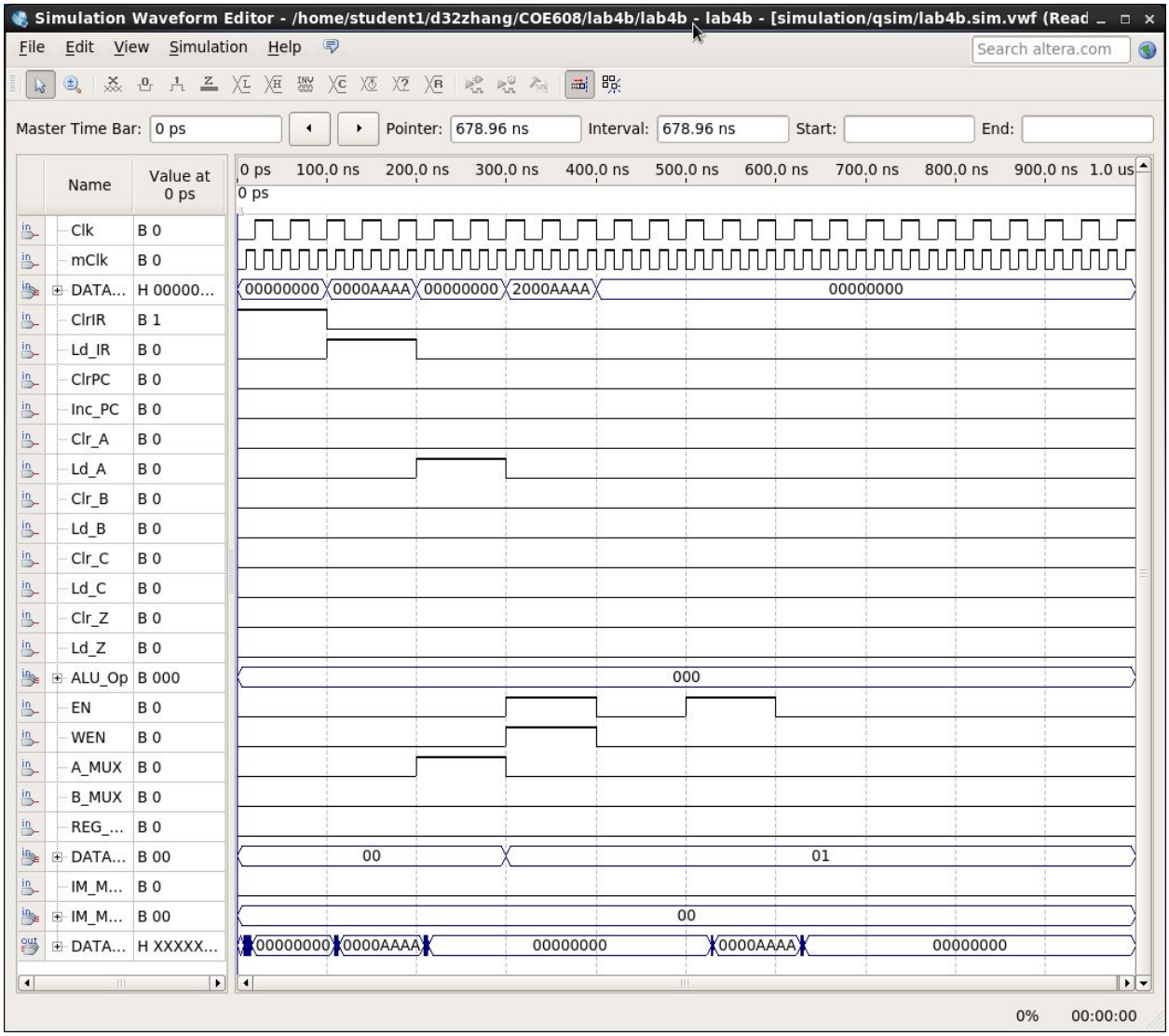
16. LDAI.vwf


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Rea
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 736.56 ns
Interval: 736.56 ns
Start:
End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
Clk B 0
mClk B 0
DATA... H 00000...
00000000 0000AAAA 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000 111
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00 10
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000 0000AAAA 00000000 0000AAAA
0% 00:00:00

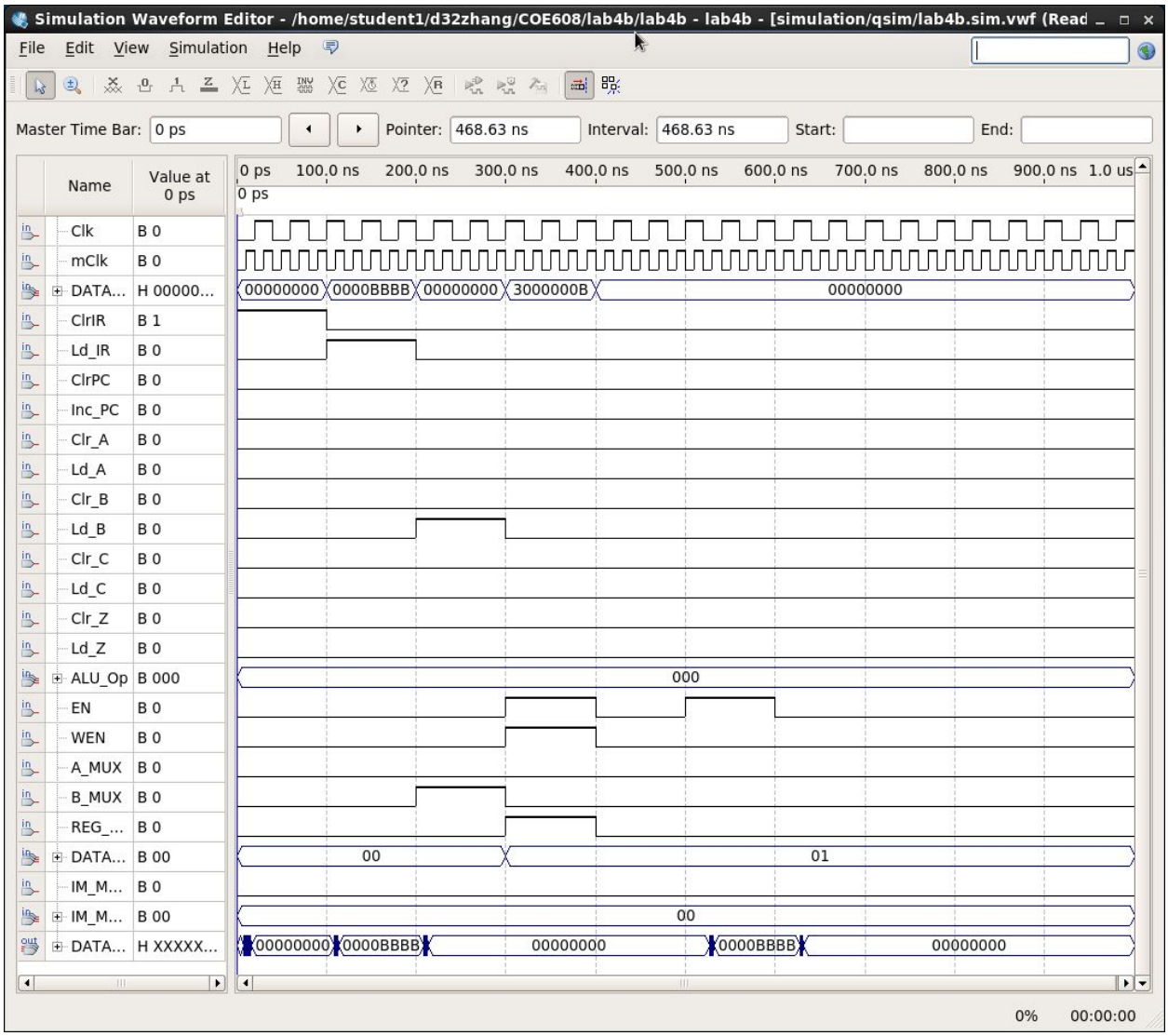
17. LDBI.vwf


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read
File Edit View Simulation Help
Master Time Bar: 0 ps Pointer: 463.71 ns Interval: 463.71 ns Start: End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
mClk B 0
DATA... H 00000...
00000000 0000BBBB 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000 011
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
Clk B 0
DATA... B 00
00 10
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000 0000BBBB 00000000 0000BBBB
0% 00:00:00

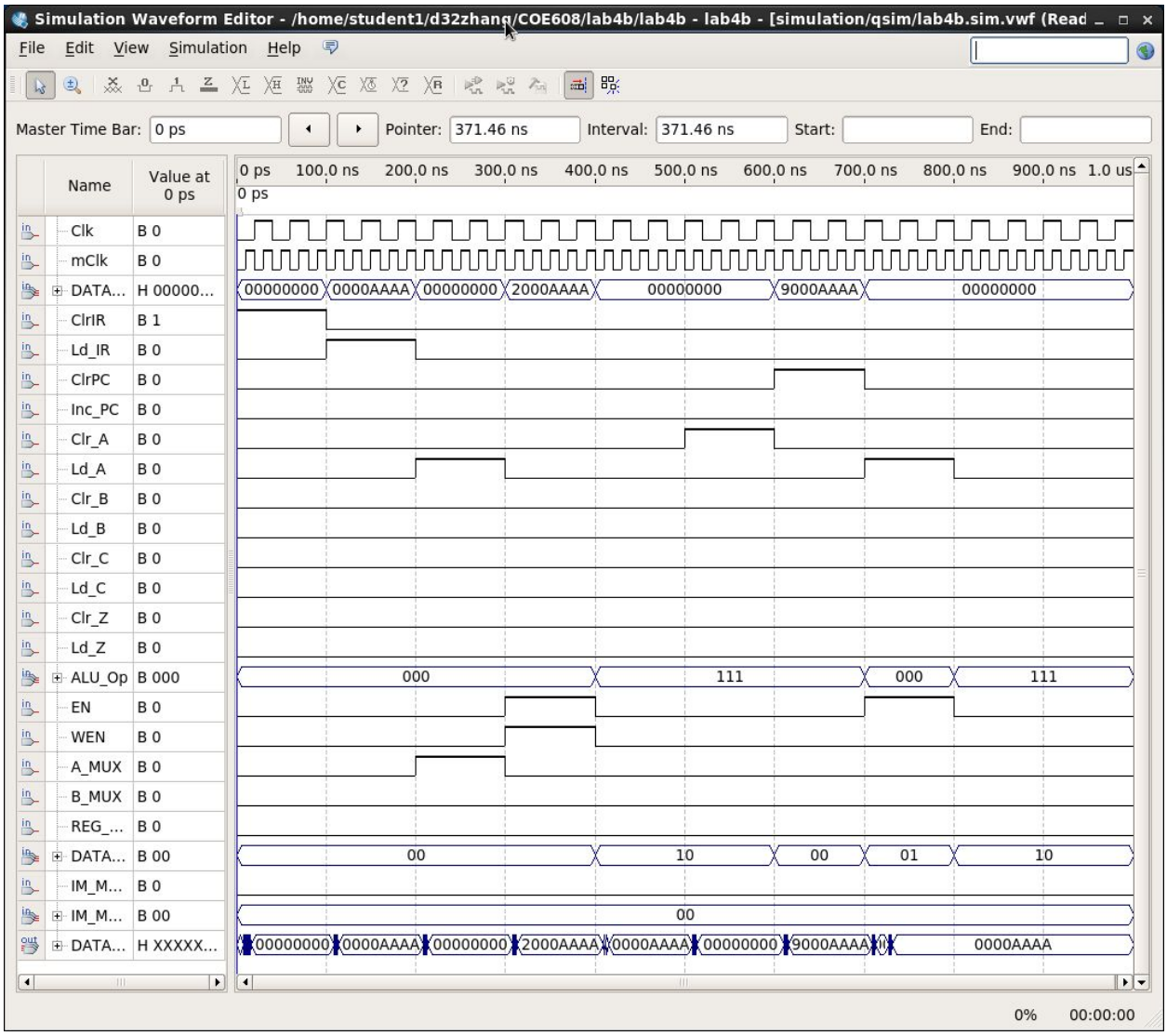
18. STA.vwf

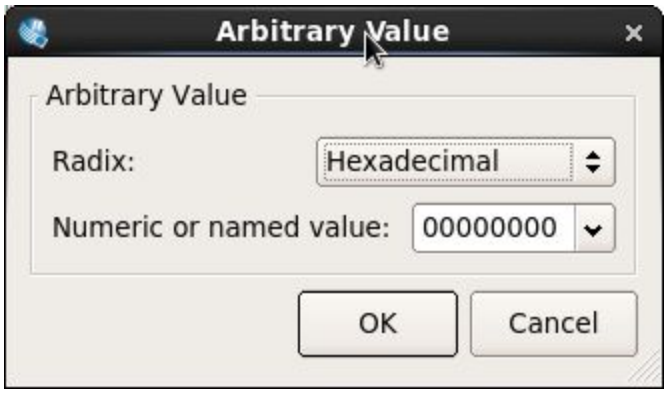

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 678.96 ns
Interval: 678.96 ns
Start:
End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
Clk B 0
mClk B 0
DATA... H 00000...
00000000 0000AAAA 00000000 2000AAAA 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00 01
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000 0000AAAA 00000000 0000AAAA 00000000
0% 00:00:00

19. STB.vwf

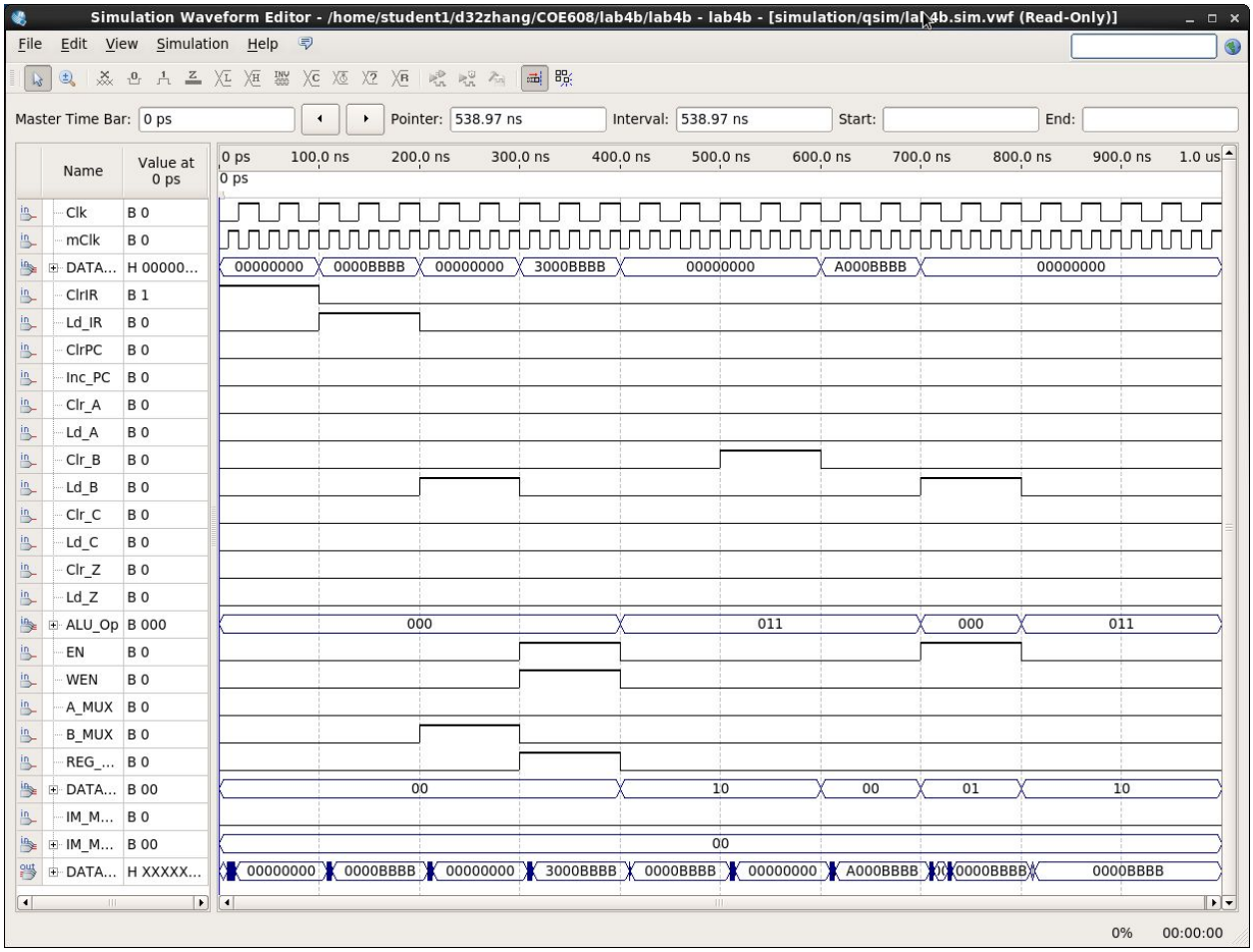

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 468.63 ns
Interval: 468.63 ns
Start:
End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
Clk B 0
mClk B 0
DATA... H 00000...
00000000 0000BBBB 00000000 3000000B 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00 01
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000 0000BBBB 00000000 0000BBBB 00000000
0% 00:00:00

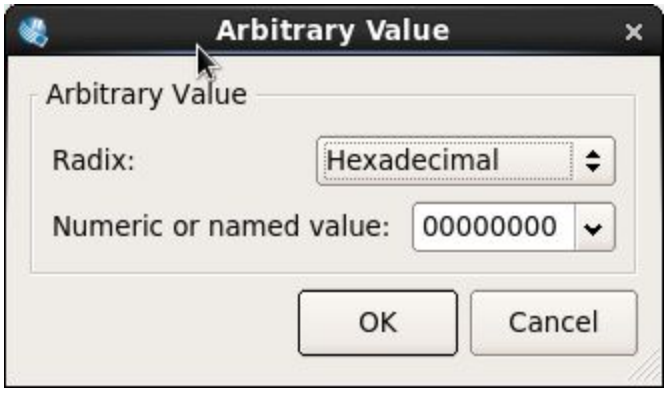
20. LDA.vwf


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read
File Edit View Simulation Help
Master Time Bar: 0 ps Pointer: 371.46 ns Interval: 371.46 ns Start: End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
Clk B 0
mClk B 0
DATA... H 00000...
00000000 0000AAAA 00000000 2000AAAA 00000000 9000AAAA 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000 111 000 111
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00 10 00 01 10
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000 0000AAAA 00000000 2000AAAA 0000AAAA 00000000 9000AAAA 0000AAAA
0% 00:00:00

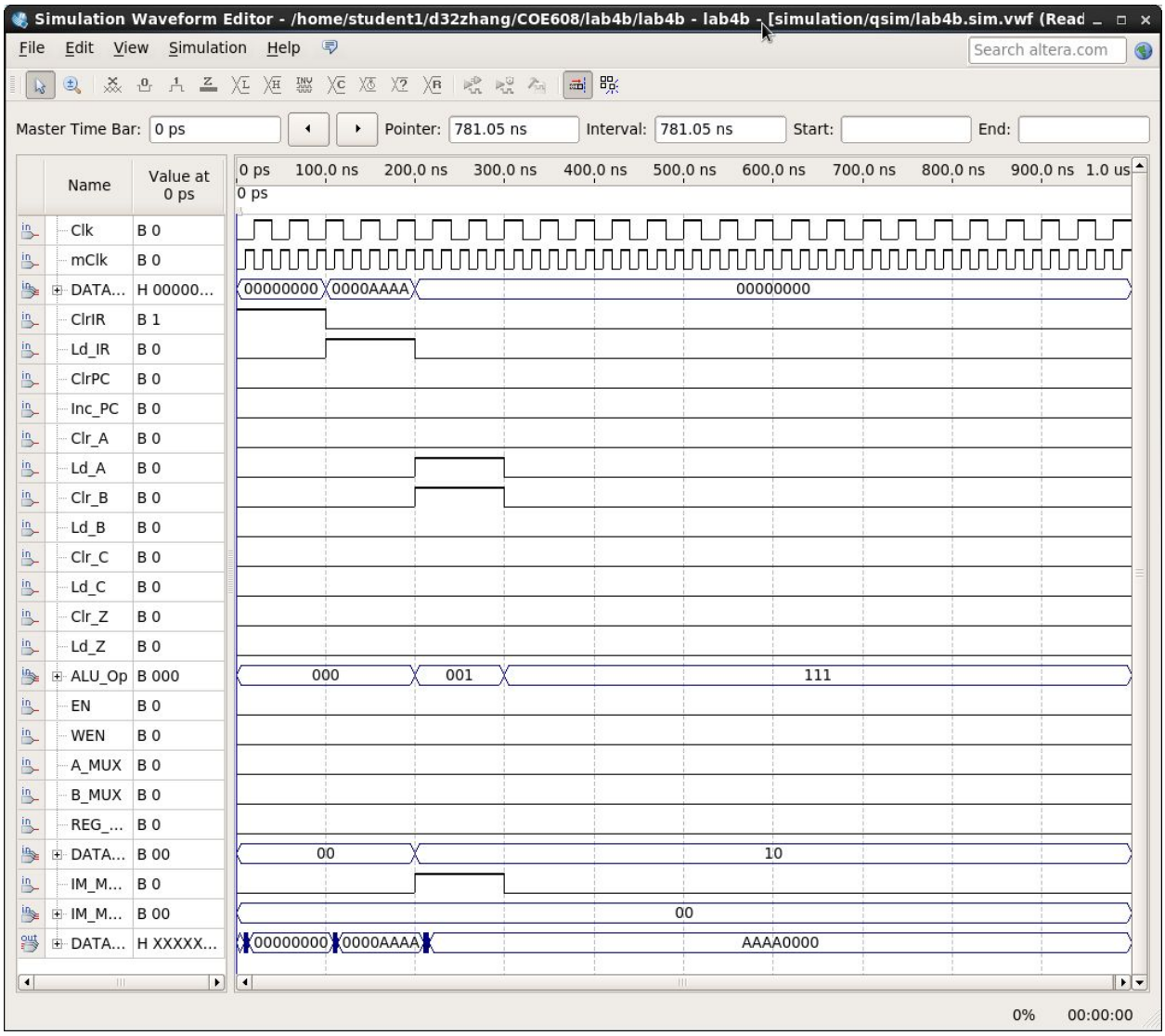

Arbitrary Value
Arbitrary Value
Radix: Hexadecimal
Numeric or named value: 00000000
OK
Cancel

21. LDB

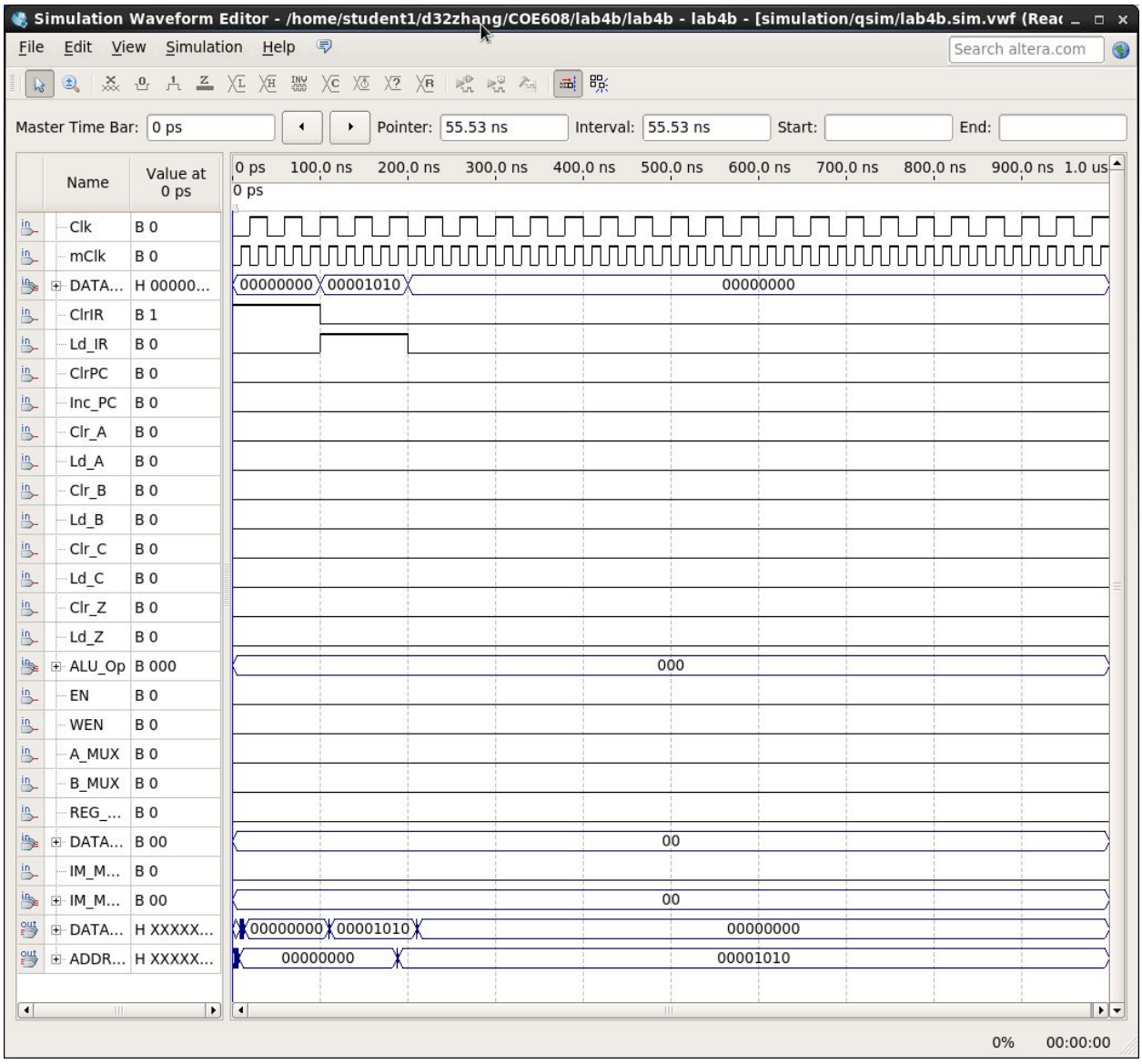

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps Pointer: 538.97 ns Interval: 538.97 ns Start: End:
Name
Value at 0 ps
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
00000000 0000BBBB 00000000 3000BBBB 00000000 A000BBBB 00000000
000 011 000 011
00 10 00 01 10
00
0% 00:00:00


Arbitrary Value
Arbitrary Value
Radix: Hexadecimal
Numeric or named value: 00000000
OK
Cancel

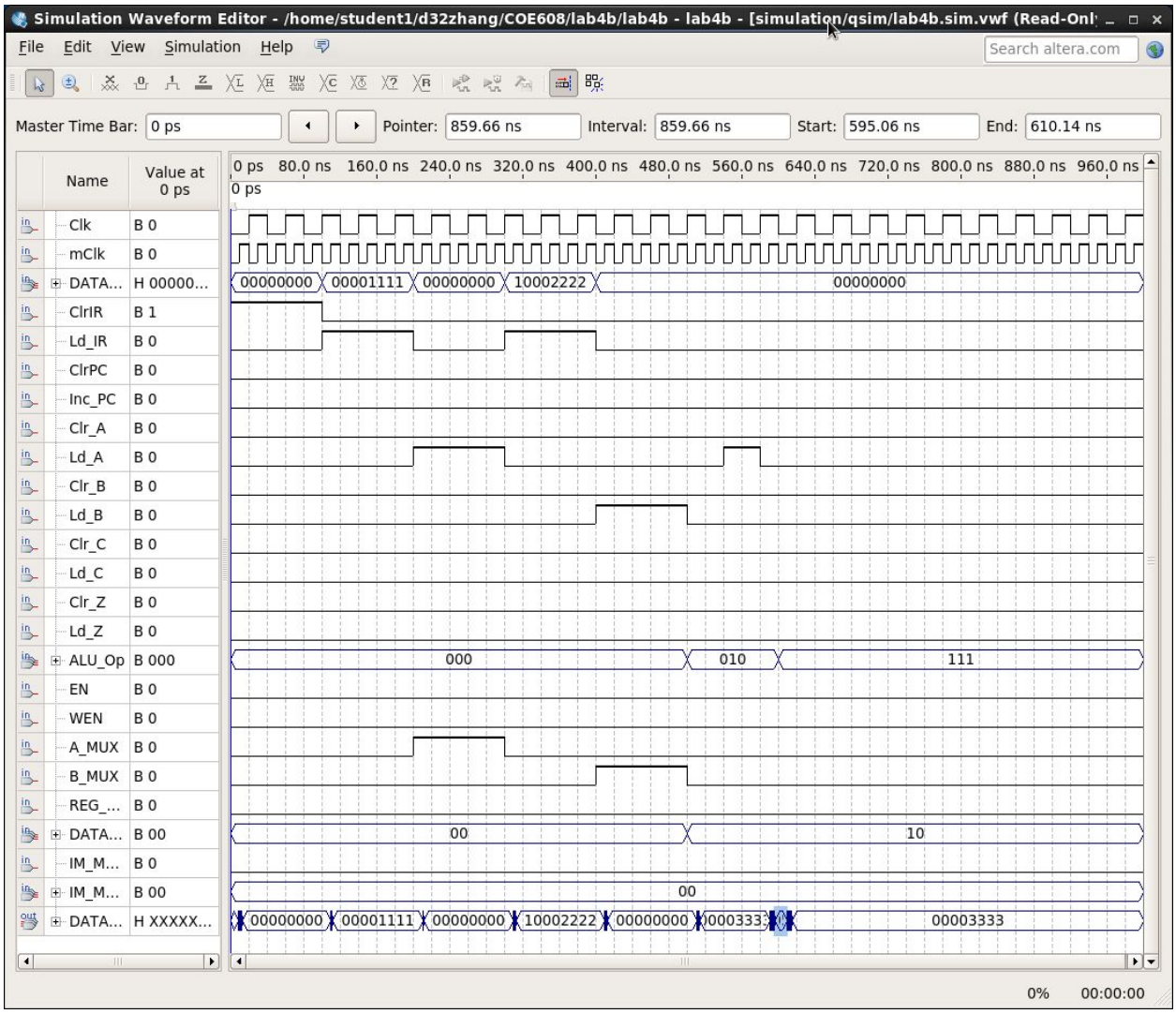
22. LUI

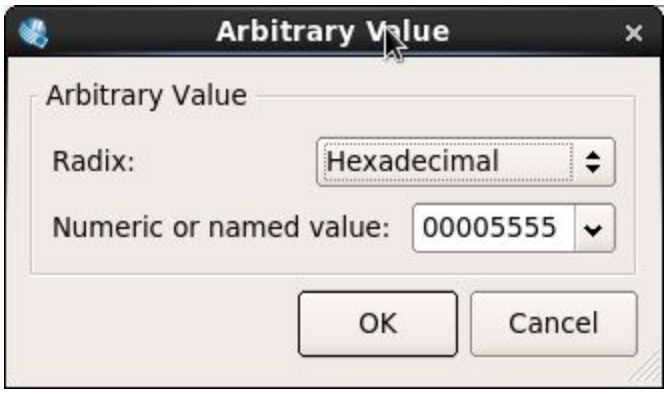

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 781.05 ns
Interval: 781.05 ns
Start:
End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000
0000AAAA
00000000
000
001
111
00
10
00
00000000
0000AAAA
AAAA0000
0%
00:00:00

23. JMP

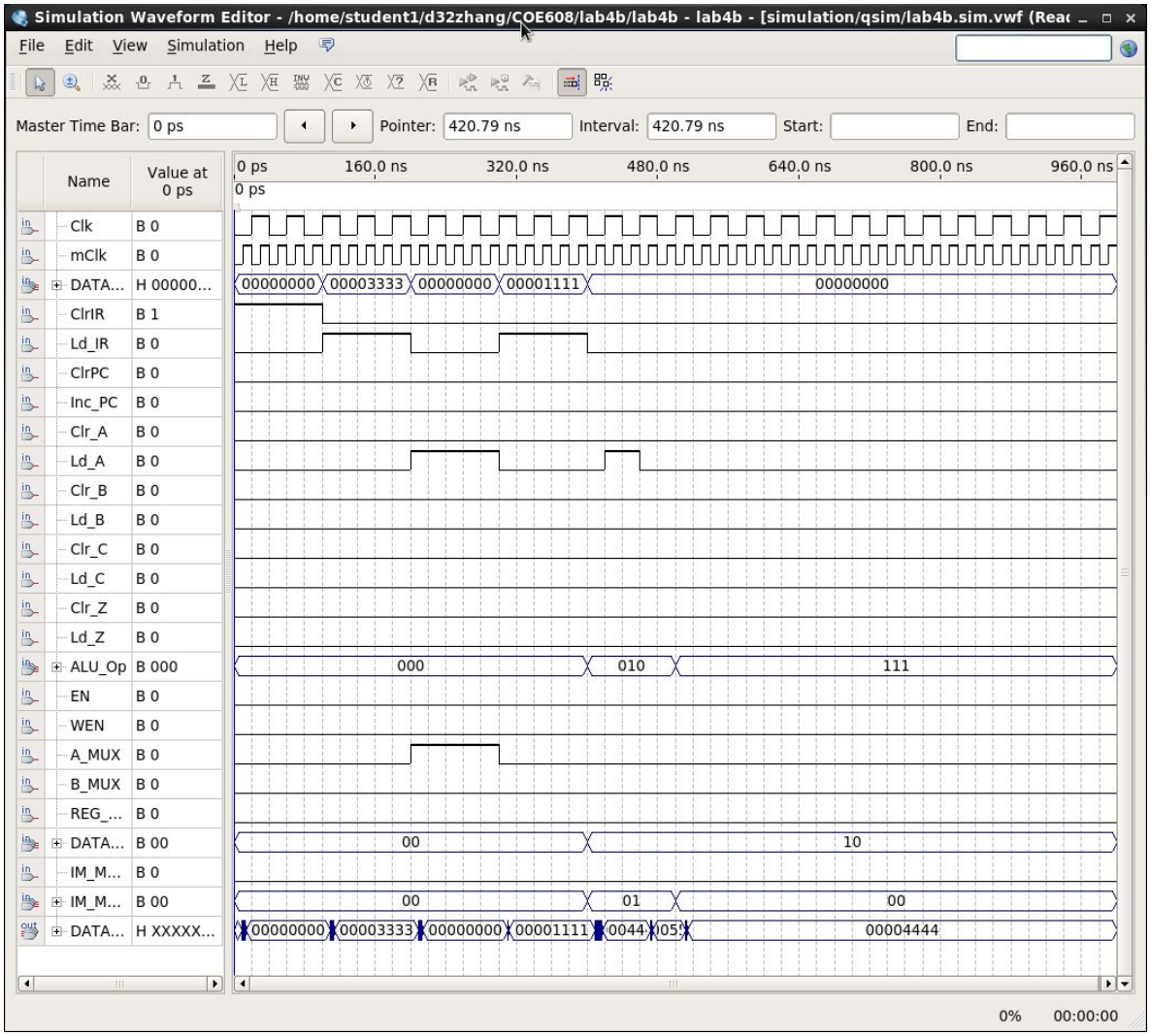

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 55.53 ns
Interval: 55.53 ns
Start:
End:
Name
Value at 0 ps
0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us
Clk B 0
mClk B 0
DATA... H 00000...
00000000 00001010 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000 00001010 00000000
ADDR... H XXXXX...
00000000 00001010
0% 00:00:00

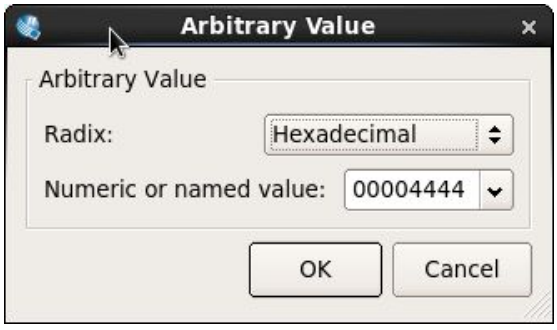
24. ADD

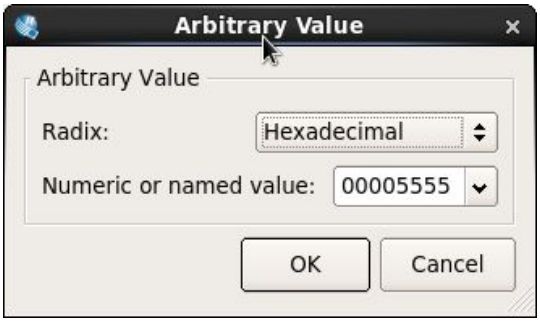

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Read-Onl
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 859.66 ns
Interval: 859.66 ns
Start: 595.06 ns
End: 610.14 ns
Name
Value at 0 ps
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000 00001111 00000000 10002222 00000000
000 010 111
00 10
00
00000000 00001111 00000000 10002222 00000000 00003333 00003333
0% 00:00:00


Arbitrary Value
Arbitrary Value
Radix: Hexadecimal
Numeric or named value: 00005555
OK
Cancel

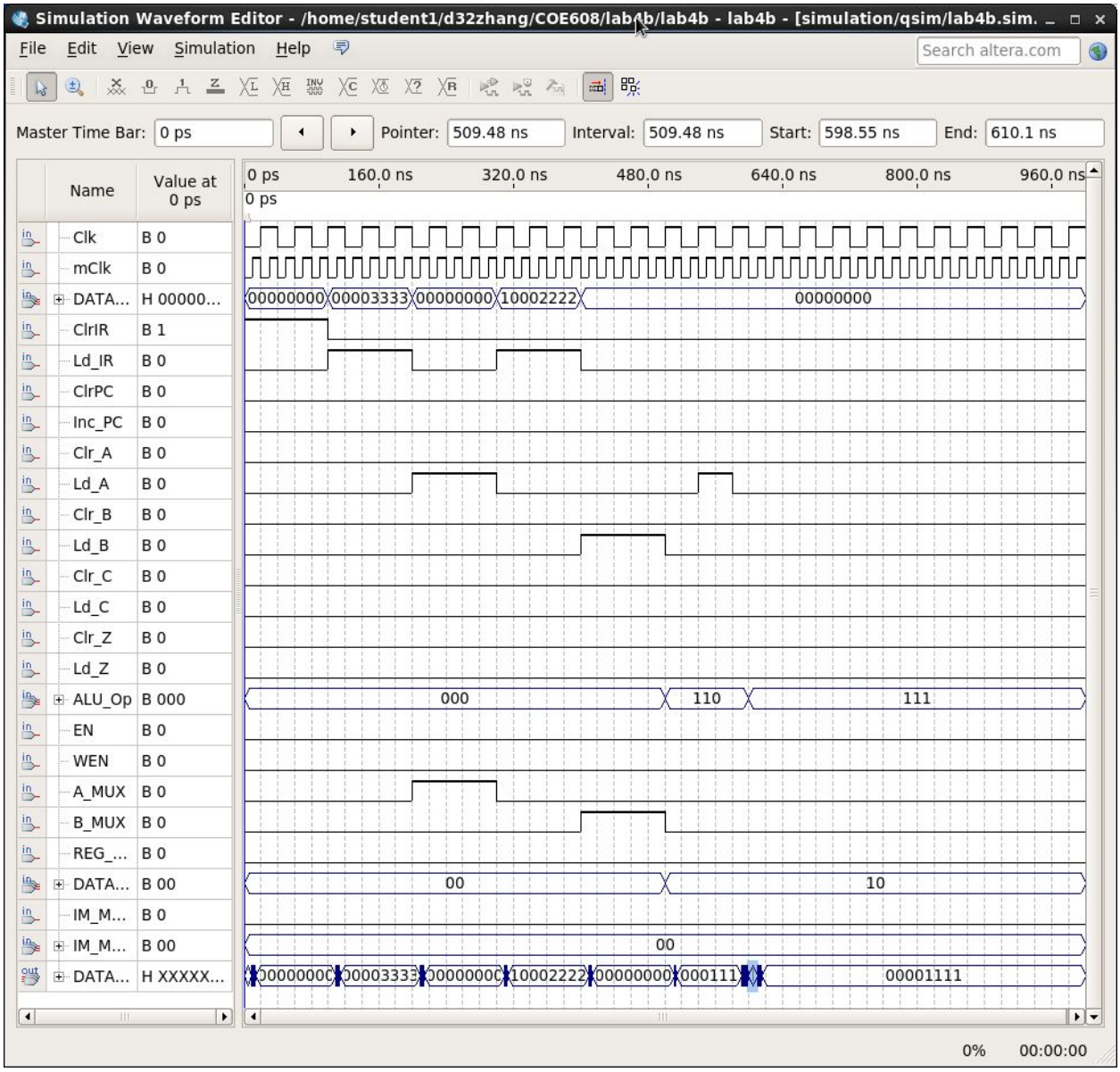
25. ADDI

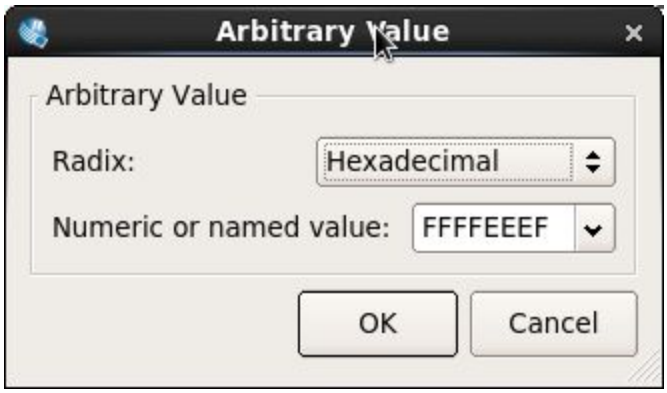

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.vwf (Reac
File Edit View Simulation Help
Master Time Bar: 0 ps Pointer: 420.79 ns Interval: 420.79 ns Start: End:
Name
Value at 0 ps
0 ps 160.0 ns 320.0 ns 480.0 ns 640.0 ns 800.0 ns 960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
00000000 00003333 00000000 00001111 00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000 010 111
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00 10
IM_M... B 0
IM_M... B 00
00 01 00
DATA... H XXXXX...
00000000 00003333 00000000 00001111 0044 005 00004444
0% 00:00:00


Arbitrary Value
Arbitrary Value
Radix: Hexadecimal
Numeric or named value: 00004444
OK Cancel

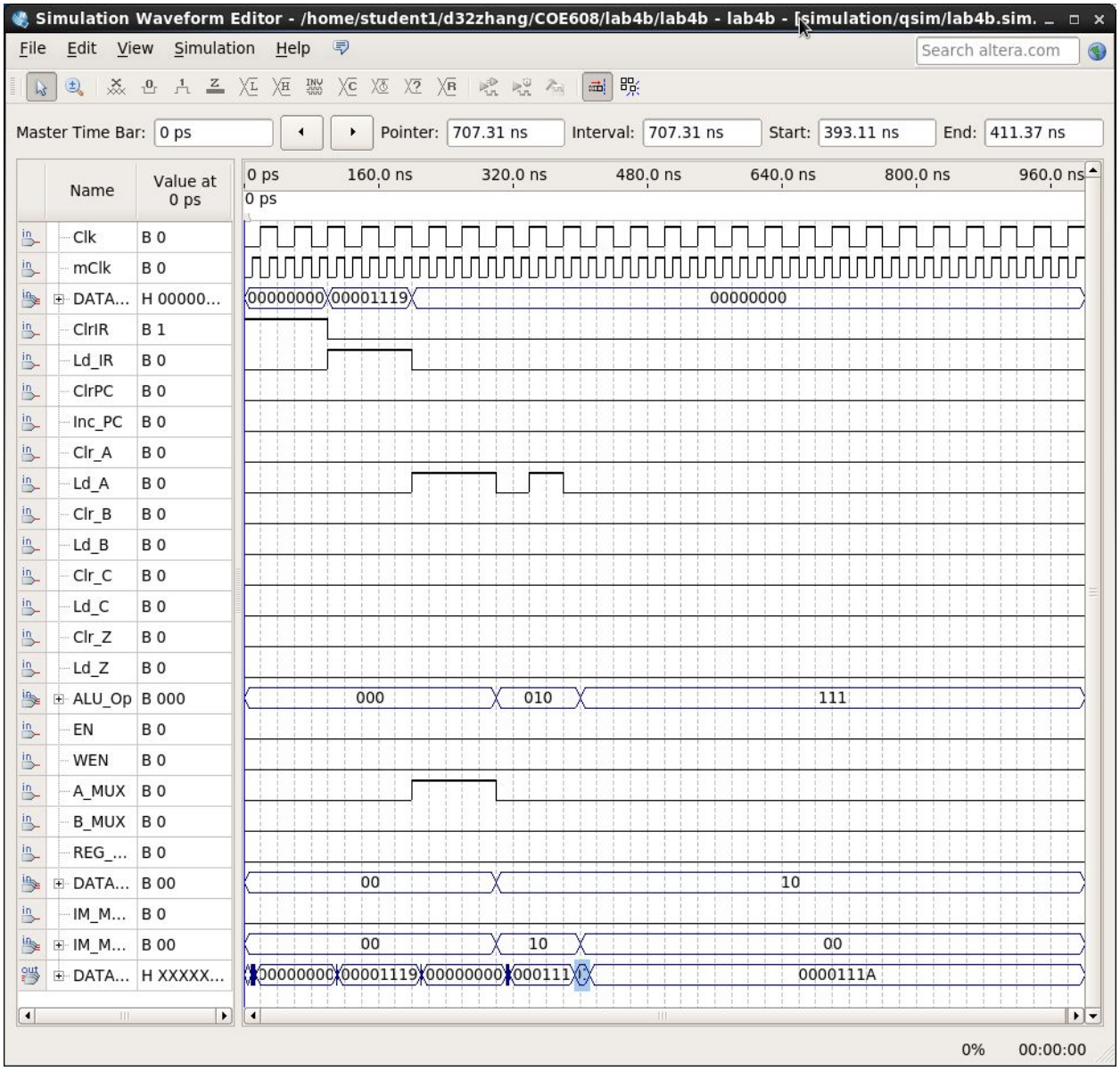

Arbitrary Value
Arbitrary Value
Radix: Hexadecimal
Numeric or named value: 00005555
OK Cancel

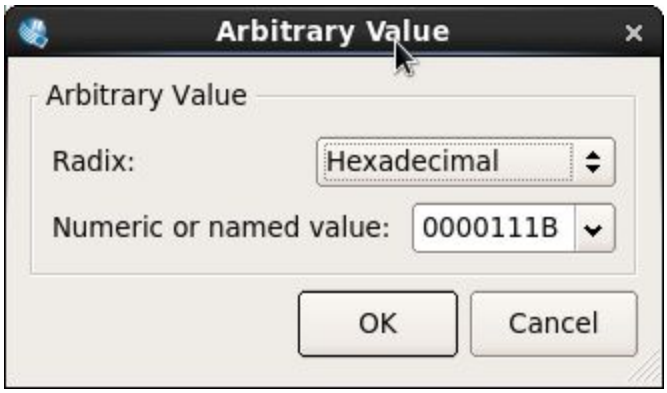
26. SUB


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 509.48 ns
Interval: 509.48 ns
Start: 598.55 ns
End: 610.1 ns
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
00000000
00003333
00000000
10002222
00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000
110
111
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00
10
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00001111
0%
00:00:00

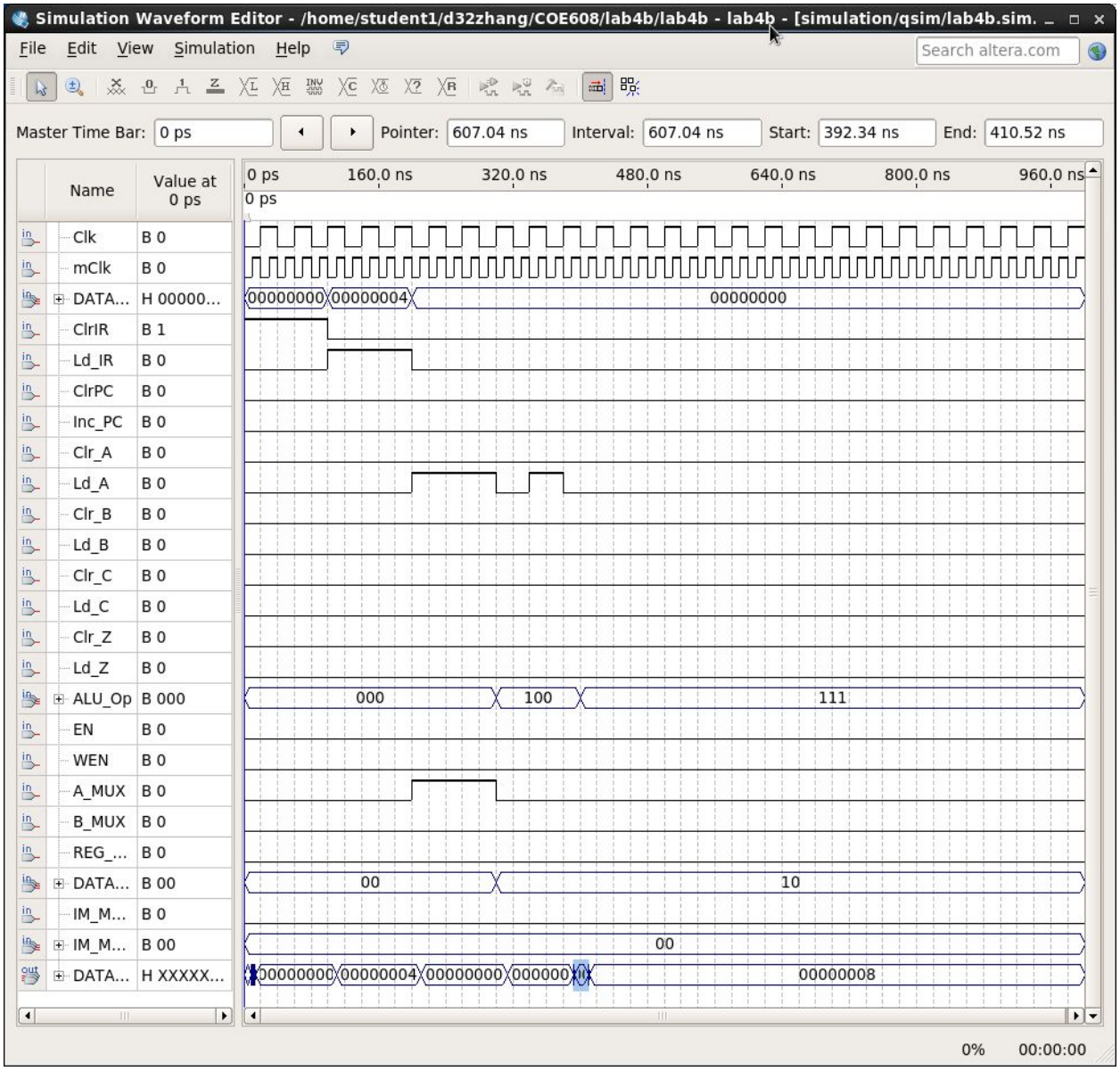

Arbitrary Value
Arbitrary Value
Radix:
Hexadecimal
Numeric or named value:
FFFFEEEF
OK
Cancel

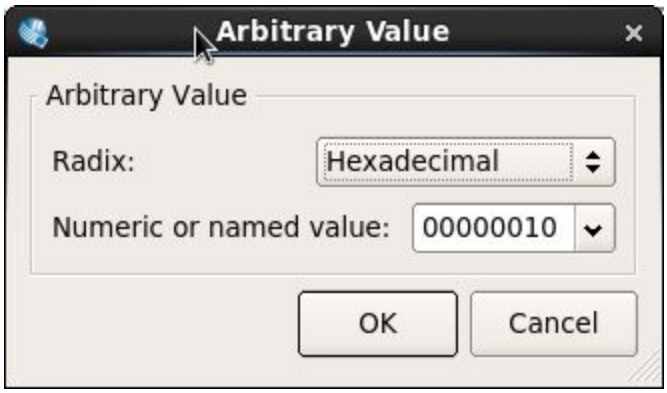
27. INCA


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 707.31 ns
Interval: 707.31 ns
Start: 393.11 ns
End: 411.37 ns
Name
Value at 0 ps
0 ps 160.0 ns 320.0 ns 480.0 ns 640.0 ns 800.0 ns 960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000 00001119 00000000
000 010 111
00 10
00 10 00
00000000 00001119 00000000 0000111B 0000111A
0% 00:00:00

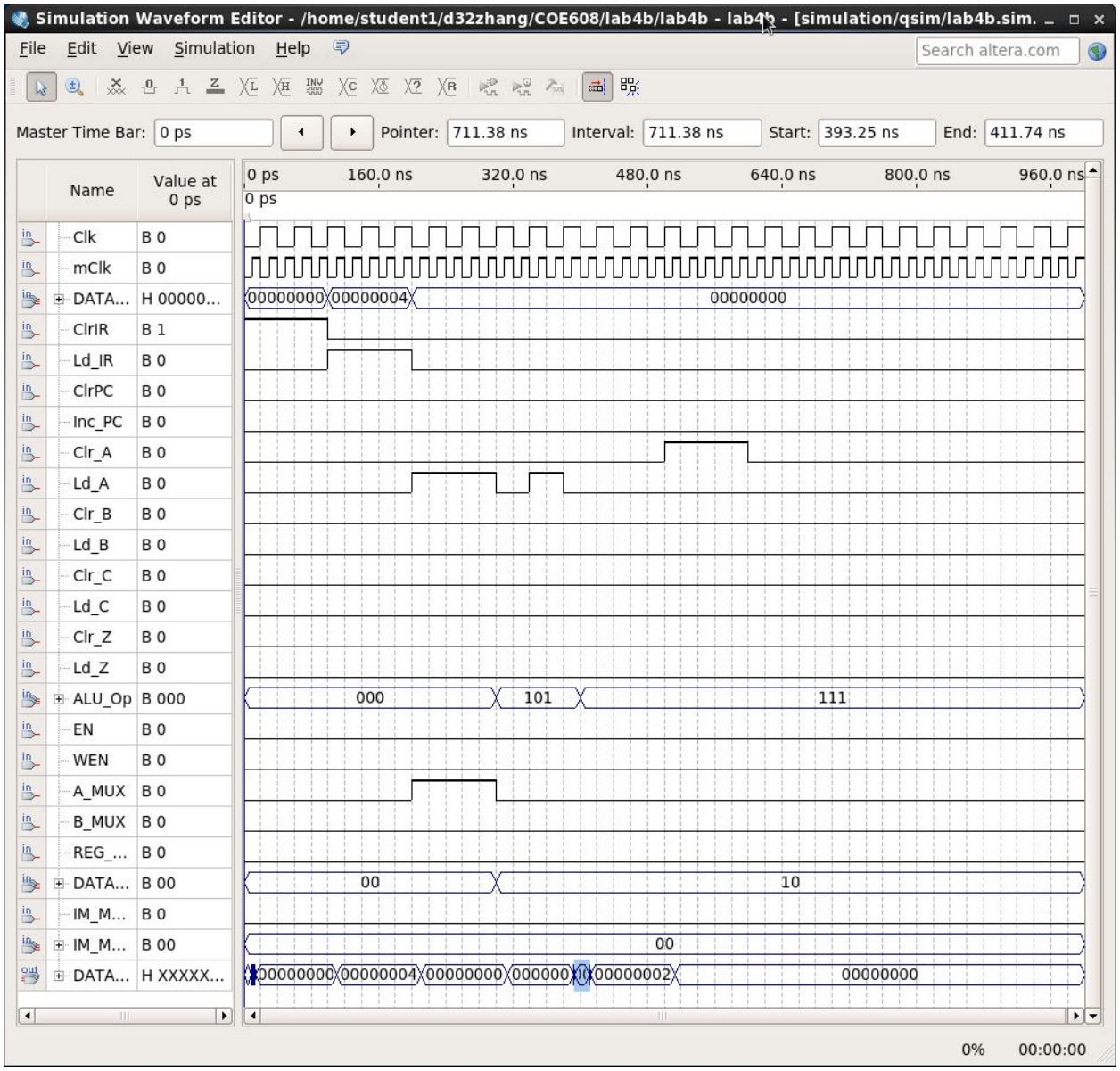

Arbitrary Value
Arbitrary Value
Radix: Hexadecimal
Numeric or named value: 0000111B
OK
Cancel

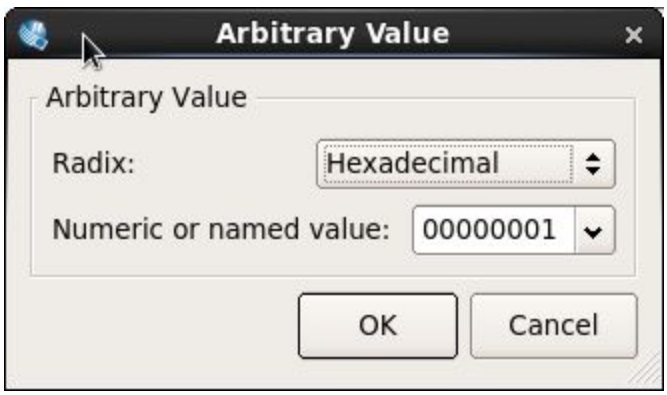
28. ROL


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 607.04 ns
Interval: 607.04 ns
Start: 392.34 ns
End: 410.52 ns
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000
00000004
00000008
000
100
111
00
10
0%
00:00:00

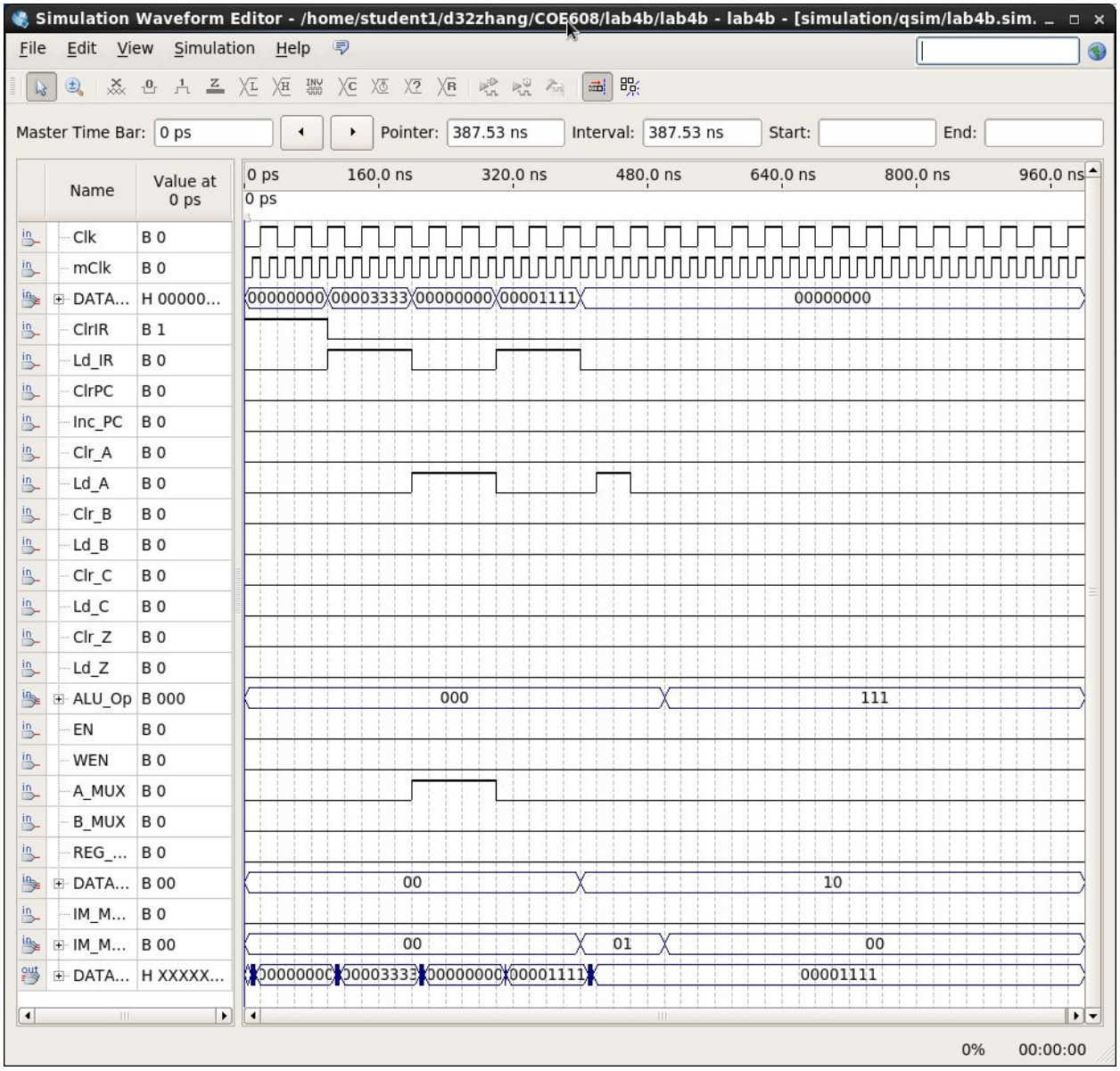

Arbitrary Value
Arbitrary Value
Radix:
Hexadecimal
Numeric or named value:
00000010
OK
Cancel

29. CLRA

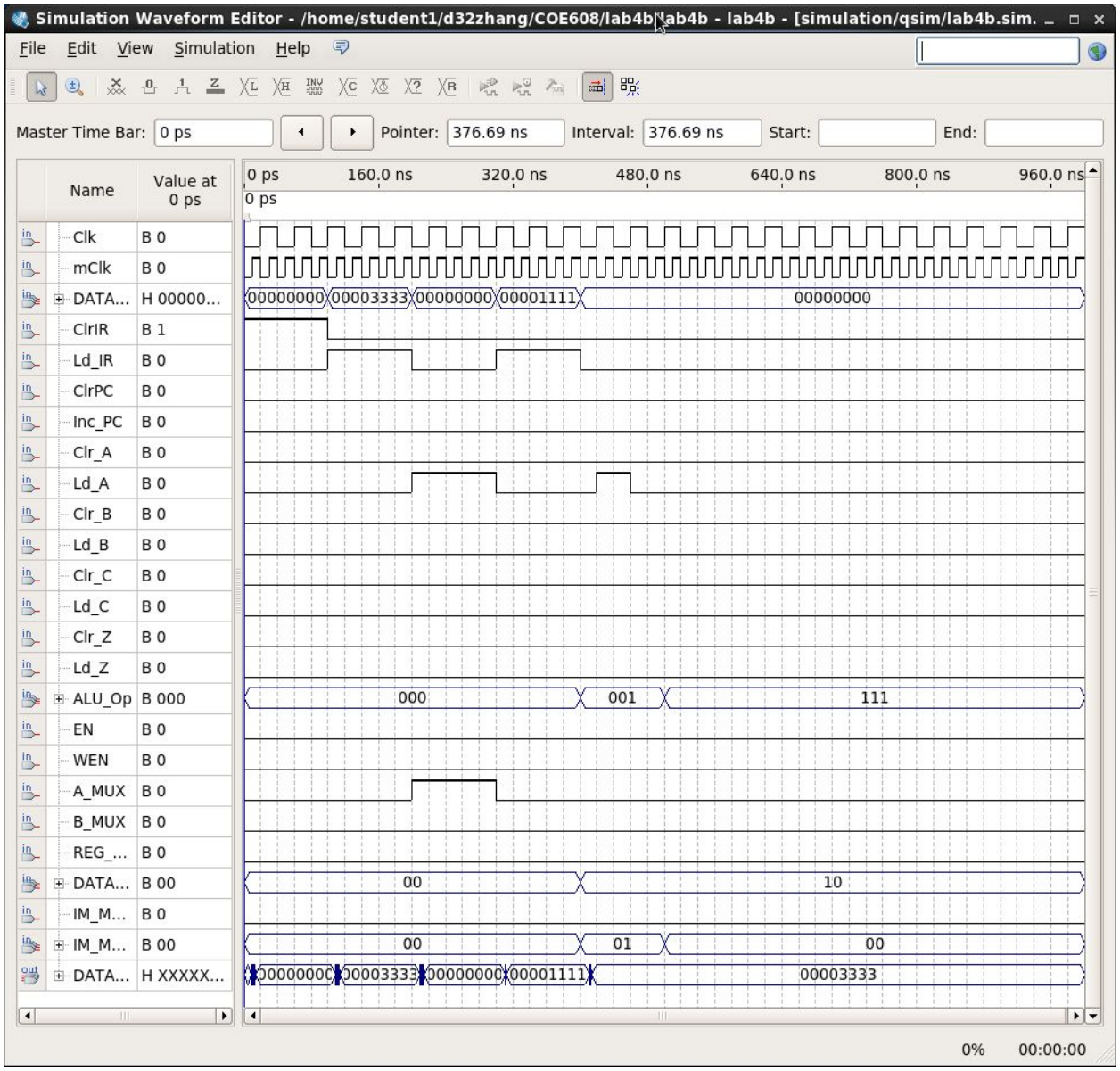

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 711.38 ns
Interval: 711.38 ns
Start: 393.25 ns
End: 411.74 ns
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000
00000004
00000000
000
101
111
00
10
00
00000000
00000004
00000000
000000
00000002
00000000
0%
00:00:00


Arbitrary Value
Arbitrary Value
Radix:
Hexadecimal
Numeric or named value:
00000001
OK
Cancel

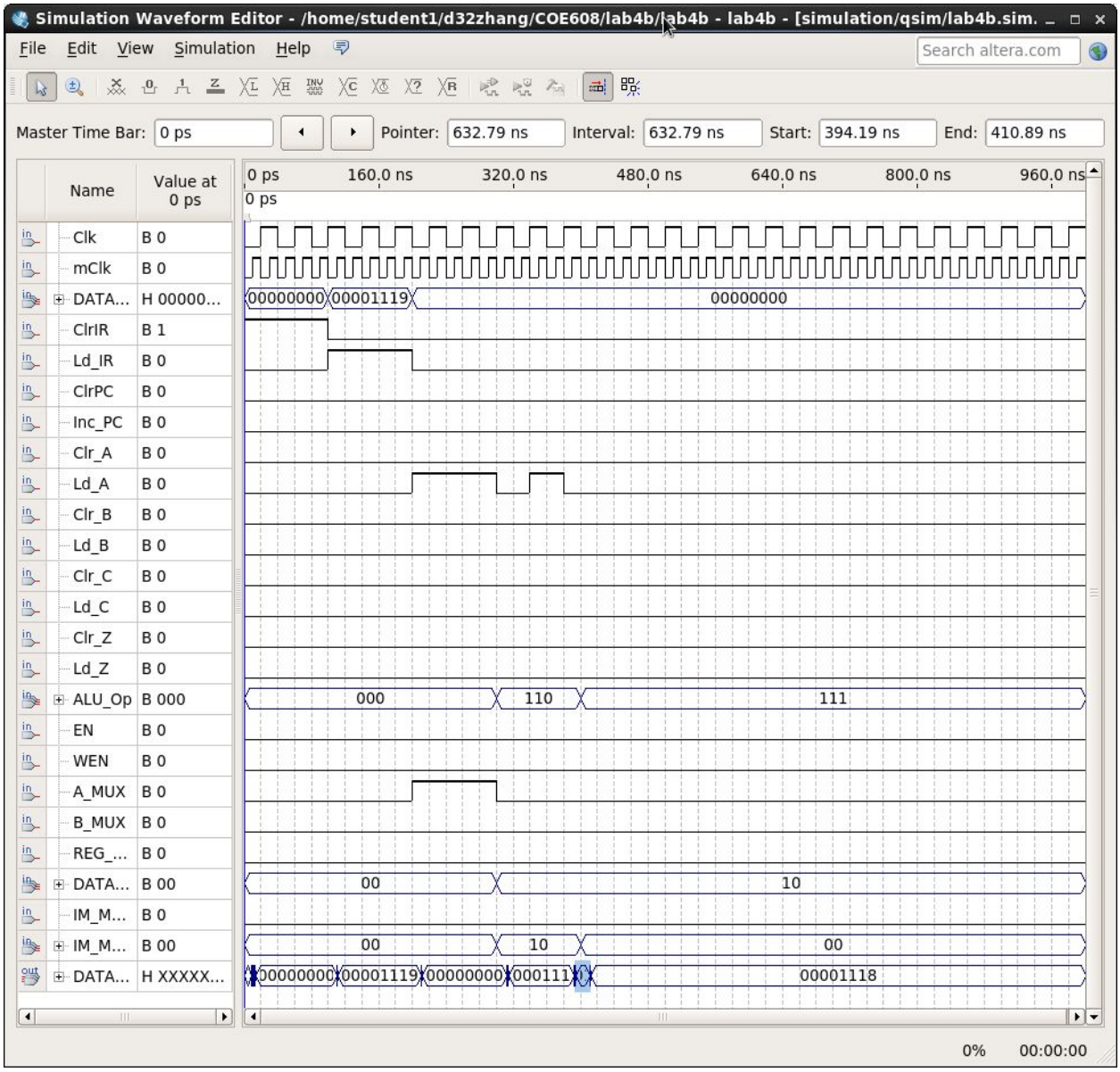
30. ANDI

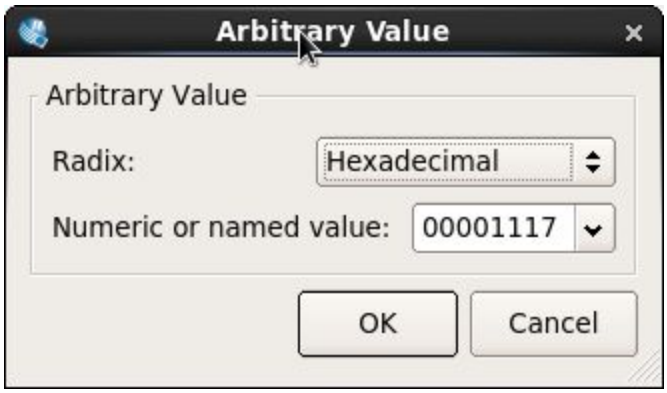

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 387.53 ns
Interval: 387.53 ns
Start:
End:
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000
00003333
00000000
00001111
00000000
000
111
00
10
00
01
00
00001111
0%
00:00:00

31. ORI

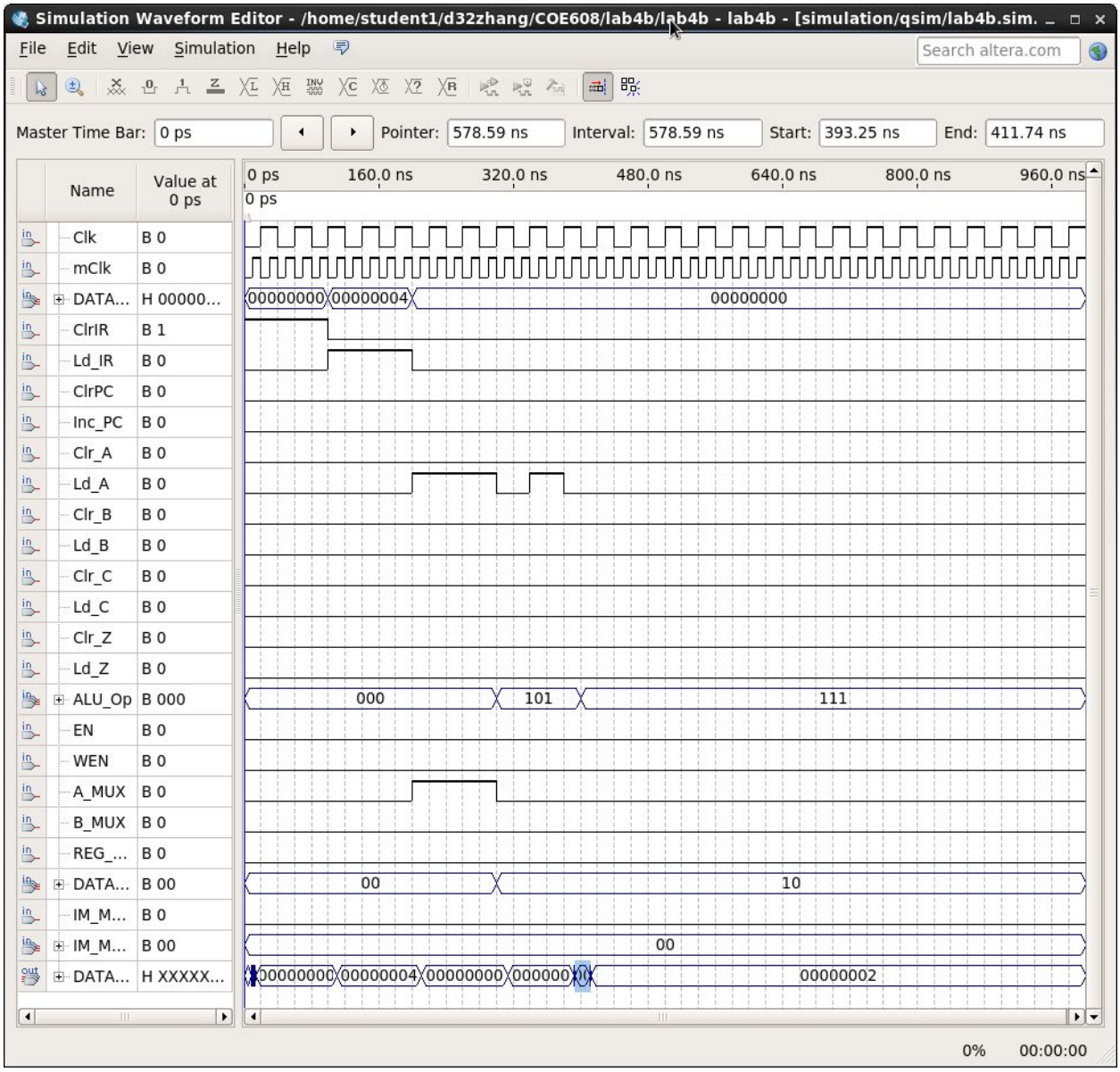

Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 376.69 ns
Interval: 376.69 ns
Start:
End:
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000
00003333
00000000
00001111
00000000
000
001
111
00
10
00
01
00
00003333
0%
00:00:00

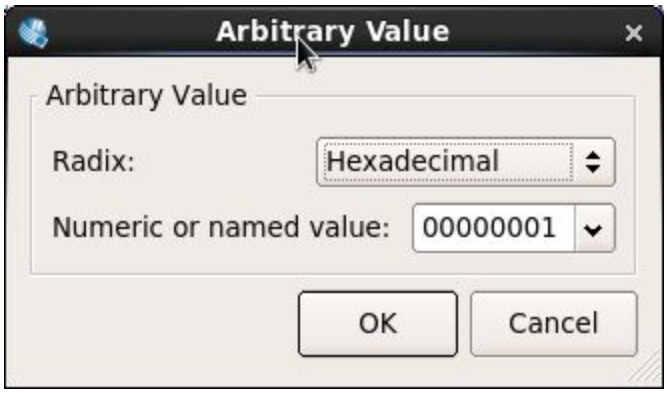
32. DECA


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 632.79 ns
Interval: 632.79 ns
Start: 394.19 ns
End: 410.89 ns
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
IM_M... B 0
IM_M... B 00
DATA... H XXXXX...
00000000
00001119
00000000
000
110
111
00
10
00
10
00
00000000
00001119
00000000
000111
00001118
0%
00:00:00


Arbitrary Value
Arbitrary Value
Radix:
Hexadecimal
Numeric or named value:
00001117
OK
Cancel

33. ROR


Simulation Waveform Editor - /home/student1/d32zhang/COE608/lab4b/lab4b - lab4b - [simulation/qsim/lab4b.sim.
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 578.59 ns
Interval: 578.59 ns
Start: 393.25 ns
End: 411.74 ns
Name
Value at 0 ps
0 ps
160.0 ns
320.0 ns
480.0 ns
640.0 ns
800.0 ns
960.0 ns
Clk B 0
mClk B 0
DATA... H 00000...
00000000
00000004
00000000
ClrIR B 1
Ld_IR B 0
ClrPC B 0
Inc_PC B 0
Clr_A B 0
Ld_A B 0
Clr_B B 0
Ld_B B 0
Clr_C B 0
Ld_C B 0
Clr_Z B 0
Ld_Z B 0
ALU_Op B 000
000
101
111
EN B 0
WEN B 0
A_MUX B 0
B_MUX B 0
REG_... B 0
DATA... B 00
00
10
IM_M... B 0
IM_M... B 00
00
DATA... H XXXXX...
00000000
00000004
00000000
00000000
00000002
0%
00:00:00


Arbitrary Value
Arbitrary Value
Radix:
Hexadecimal
Numeric or named value:
00000001
OK
Cancel

Student Name: Duanwei Zhang **Student#:** 500824903 **Section:** 04

INST	CLR_IR LD_IR	LD_PC INC_PC	CLR_A LD_A	CLR_B LD_B	CLR_C LD_C	CLR_Z LD_Z	ALU OP	EN WEN	A/B MUX	REG MUX	Data MUX	IM_MUX1 IM_MUX2
LDA	0/0	0/0	0/1	0/0	0/0	0/0	XXX	1/0	0/X	X	01	X
LDB	0/0	0/0	0/0	0/1	0/0	0/0	XXX	1/0	X/0	X	01	X
STA	0/0	0/0	0/0	0/0	0/0	0/0	XXX	1/1	X	0	X	X
STB	0/0	0/0	0/0	0/0	0/0	0/0	XXX	1/1	X	1	X	X
JMP	0/0	1/0	0/0	0/0	0/0	0/0	XXX	X	X	X	X	X
LDAI	0/0	0/0	0/1	0/0	0/0	0/0	XXX	X	1/X	X	X	X
LDBI	0/0	0/0	0/0	0/1	0/0	0/0	XXX	X	X/1	X	X	X
LUI	0/0	0/0	0/1	1/0	0/0	0/0	001	X	0/X	X	10	1/X
ANDI	0/0	0/0	0/1	0/0	0/1	0/1	000	X	0/X	X	10	0/01
DECA	0/0	0/0	0/1	0/0	0/1	0/1	110	X	0/X	X	10	0/10
ADD	0/0	0/0	0/1	0/0	0/1	0/1	010	X	0/X	X	10	0/00
SUB	0/0	0/0	0/1	0/0	0/1	0/1	110	X	0/X	X	10	0/00
INCA	0/0	0/0	0/1	0/0	0/1	0/1	010	X	0/X	X	10	0/10
AND	0/0	0/0	0/1	0/0	0/1	0/1	000	X	0/X	X	10	0/09
ADDI	0/0	0/0	0/1	0/0	0/1	0/1	010	X	0/X	X	10	0/01
ORI	0/0	0/0	0/1	0/0	0/1	0/1	001	X	0/X	X	10	0/01
ROL	0/0	0/0	0/1	0/0	0/1	0/1	100	X	0/X	X	10	0/X
ROR	0/0	0/0	0/1	0/0	0/1	0/1	101	X	0/X	X	10	0/X
CLRA	0/0	0/0	1/0	0/0	0/0	0/0	XXX	X	X	X	X	X
CLRB	0/0	0/0	0/0	1/0	0/0	0/0	XXX	X	X	X	X	X
CLRC	0/0	0/0	0/0	0/0	1/0	0/0	XXX	X	X	X	X	X
CLRZ	0/0	0/0	0/0	0/0	0/0	1/0	XXX	X	X	X	X	X
PC <= PC+4	0/0	1/1	0/0	0/0	0/0	0/0	XXX	X	X	X	X	X
IR <= M[INST]	0/1	0/0	0/0	0/0	0/0	0/0	XXX	X	X	X	00	X
PC <= IR[15..0]	0/0	1/0	0/0	0/0	0/0	0/0	XXX	X	X	X	X	X

Table 1: Data-Path Control Signals