```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity op_inv is
   port(
      enable: in std_logic;
      op: in std_logic_vector(2 downto 0);
      op_out : out std_logic_vector (2 downto 0));
end op_inv;

architecture behavior of op_inv is
   begin
      process(enable, op)
         begin
            if enable = '0' then
               op_out <= op;
            elsif enable = '1' then
               op_out <= not op;
            else
               op_out <= "---";
            end if;
      end process;
end behavior;
```