```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   entity adder is
7      port (
8         x, y: in std_logic;
9         mode: in std_logic;
10        cin : in std_logic;
11        cout : out std_logic;
12        s : out std_logic);
13  end adder;
14
15  architecture behavior of adder is
16     signal temp : std_logic;
17        begin
18           process(mode)
19              begin
20                 if (mode = '1') then
21                    temp <= (y xor mode);
22                 else
23                    temp <= y;
24                 end if;
25              s <= (x xor temp xor cin) or (x and temp and cin);
26              cout <= (x and temp) or (x and cin) or (cin and temp);
27           end process;
28  end behavior;
29
30
31
```