```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6
7   entity adder8 is
8      port(
9         cin, mode: in std_logic;
10        x, y : in std_logic_vector(31 downto 0);
11        s: out std_logic_vector(31 downto 0);
12        cout: out std_logic);
13  end adder8;
14
15  architecture description of adder8 is
16     signal c7, c6, c5, c4, c3, c2, c1, c0: std_logic;
17        component adder
18           port(
19              x, y, mode, cin: in std_logic;
20              cout, s : out std_logic);
21        end component adder;
22           begin
23              st0: adder port map (x(0), y(0), mode, mode, c1, s(0));
24              st1: adder port map (x(1), y(1), mode, c1, c2, s(1));
25              st2: adder port map (x(2), y(2), mode, c2, c3, s(2));
26              st3: adder port map (x(3), y(3), mode, c3, c4, s(3));
27              st4: adder port map (x(4), y(4), mode, c4, c5, s(4));
28              st5: adder port map (x(5), y(5), mode, c5, c6, s(5));
29              st6: adder port map (x(6), y(6), mode, c6, c7, s(6));
30              st7: adder port map (x(7), y(7), mode, c7, cout, s(7));
31  end description;
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