```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_unsigned.all;
4
5   entity uze is
6      port(
7         uze_in : in std_logic_vector(31 downto 0);
8         uze_out: out std_logic_vector(31 downto 0));
9   end uze;
10
11  architecture behavior of uze is
12     signal zeros : std_logic_vector(15 downto 0) := (others => '0');
13        begin
14           uze_out <= uze_in(31 downto 16) & zeros;
15  end behavior;
16
17
```