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COE 608: Computer Architecture and Design

COE 608: Lab 4, Part 2 Report

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Objective

The purpose of this lab is to put together everything we have done so far, with the addition of the upper zero extender, lower zero extender, and reducer with the program counter, arithmetic logical unit, multiplexers, and operational inverters into a functioning data-path for the MIPS instructional set architecture.

Design and Implementation

I first started with the reducers, LZE and UZE implementations. I did the data-path last. The following truth-tables provide examples of some of the purposes of the LZE, UZE, and reducer. The LZE extends zeroes by padding the bits from 15 down to 0. The UZE does the inverse of the LZE operation by padding zeroes from 31 down to 16. The reducer helps to reduce a 32-bit data into 8-bit data. The data-path is programmed in VHDL using the structural behavior, by utilizing port mapping and signals to denote the wires and buses between the many devices used throughout the course.

The truth tables for each of the new devices are illustrated in the following pages.

See the following figures below: Figure 1: UZE Truth Table, Figure 2: LZE Truth Table, Figure 3: Reducer Truth Table and Figure 4: Data-path signals truth table.

Upper Zero Extender	
In (hex)	Out (hex)
0 0 0 0 0 0 1	0 0 0 0 0 0 0
0 0 0 0 0 0 A	0 0 0 0 0 0 0
0 0 0 F 9 E D F	0 0 0 F 0 0 0 0
A B C 8 5 F G 1	A B C 8 0 0 0 0

Figure 1: UZE Truth Table

Next, is the Lower Zero Extender Truth Table:

Lower Zero Extender	
In (hex)	Out (hex)
0 0 0 0 0 0 1	0 0 0 0 0 0 1
0 0 0 0 0 0 A	0 0 0 0 0 0 0 A
0 0 0 F 9 E D F	0 0 0 0 9 E D F
A B C 8 5 F G 1	0 0 0 0 5 F G 1

Figure 2: LZE Truth Table

Next, is the Reducer Truth Table:

Reducer	
In (hex)	Out (hex)
0 0 0 0 0 0 1	0 1
0 0 0 0 0 0 A	0 A
0 0 0 F 9 E D F	9 E D F
A B C 8 5 F G 1	5 F G 1

Figure 3: Reducer Truth Table

Finally, the Data-path Truth Table:

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INST		CLR_IR LD_IR	LD_PC INC_PC	CLR_A LD_A	CLR_B LD_B	CLR_C LD_C	CLR_Z LD_Z	ALU_OP	EN_WEN	A/B_MUX	REG_MUX	Data_MUX	IM_MUX1 IM_MUX2
LDA	00	00	01	00	00	00	00	XXX	10	0/X	X	1	X
LDB	00	00	00	01	00	00	00	XXX	10	X/0	X	1	X
STA	00	00	00	00	00	00	00	XXX	11	X	0	X	X
JMP	00	00	00	00	00	00	00	XXX	11	X	1	X	X
STAB	00	10	00	00	00	00	00	XXX	X	X	X	X	X
LDAI	00	00	01	00	00	00	00	XXX	X	1/X	X	X	X
LDBI	00	00	00	01	00	00	00	XXX	X	X/1	X	X	X
LUI	00	00	01	10	00	00	00	1	X	0/X	X	10	1/X
ANDI	00	00	01	00	01	01	01	0	X	0/X	X	10	0/01
DECA	00	00	01	00	01	01	01	110	X	0/X	X	10	0/10
AND	00	00	01	00	01	01	01	10	X	0/X	X	10	0/00
ADDI	00	00	01	00	01	01	01	110	X	0/X	X	10	0/00
SUB	00	00	01	00	01	01	01	10	X	0/X	X	10	0/10
INCA	00	00	01	00	01	01	01	0	X	0/X	X	10	0/00
ORI	00	00	01	00	01	01	01	10	X	0/X	X	10	0/01
ROL	00	00	01	00	01	01	01	1	X	0/X	X	10	0/01
ROR	00	00	01	00	01	01	01	100	X	0/X	X	10	0/X
CLRA	00	00	01	00	01	01	01	101	X	0/X	X	10	0/X
CLRC	00	00	10	00	00	00	00	XXX	X	X	X	X	X
CLRZ	00	00	00	10	00	00	00	XXX	X	X	X	X	X
PC <= PC + 4	00	10	00	00	00	00	00	XXX	X	X	X	X	X
IR <= M[INT]	01	00	00	00	00	00	00	XXX	X	X	X	0	X
PC IR[15:0]	00	10	00	00	00	00	00	XXX	X	X	X	X	X

Figure 4: Data-path signals truth table

Observations and Results

Below are the functional and timing waveforms derived for each of the new components listed for this lab.

The following figures are the observations of this project:

Figure 5: LZE Functional Waveform, Figure 6: LZE Timing Waveform, Figure 7: UZE Functional Waveform, Figure 8: UZE Timing Waveform, Figure 9: Reducer Functional Waveform, Figure 10: Reducer Timing Waveform, Figure 11: Data-path Random Input Waveform, Figure 12: Data-path Output Functional Waveform, and Figure 13: Data-path Output Timing Waveform are the figures of interest.

LZE: Functional and Timing

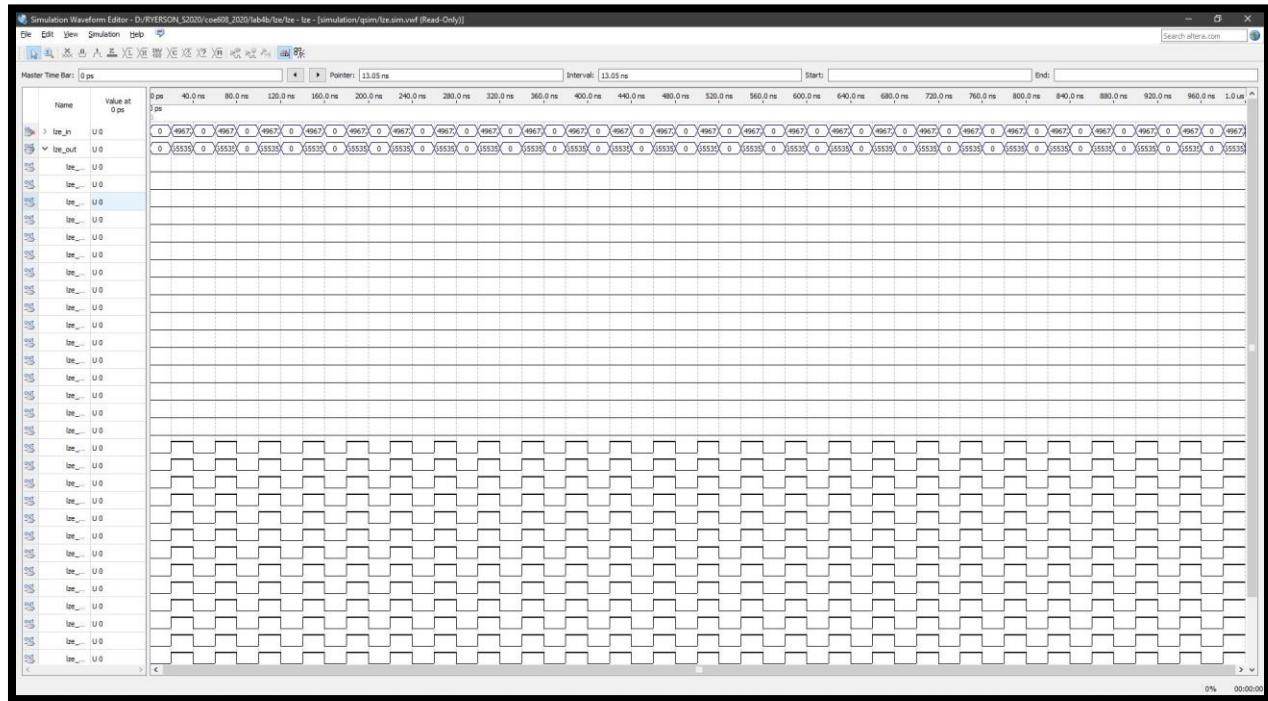


Figure 5: LZE Functional Waveform

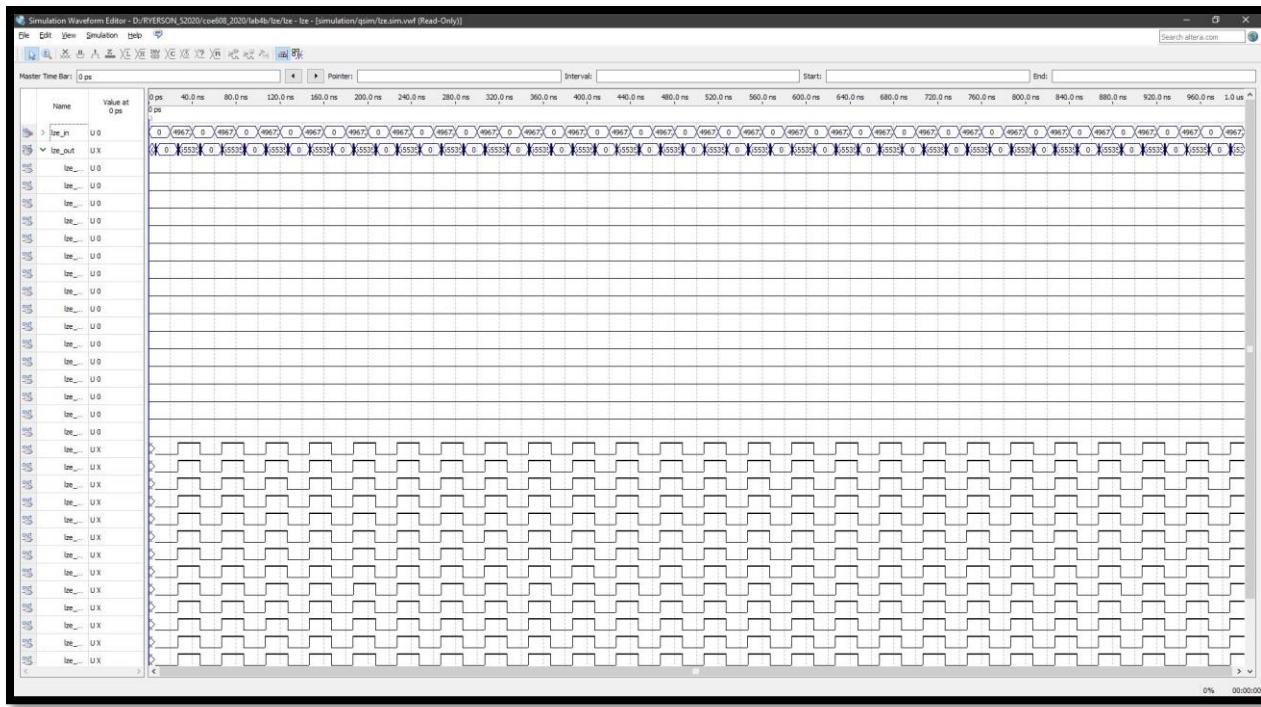


Figure 6: LZE Timing Waveform

UZE: Functional and Timing

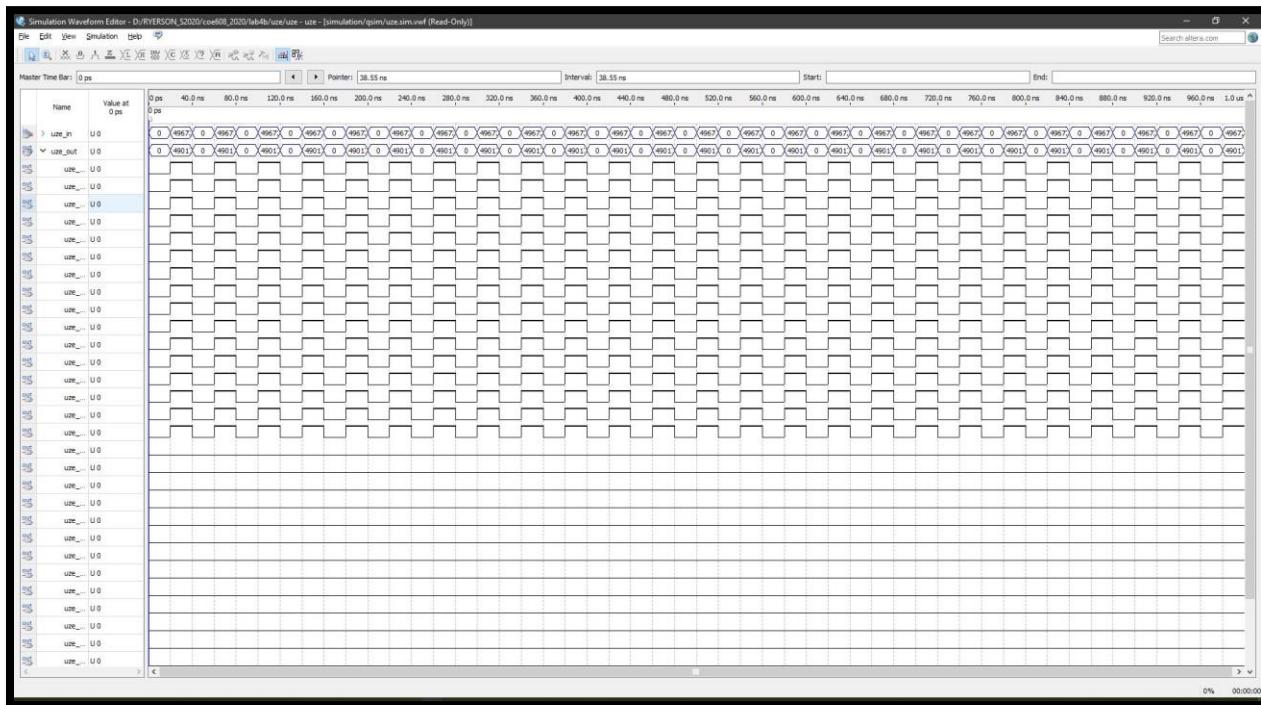


Figure 7: UZE Functional Waveform

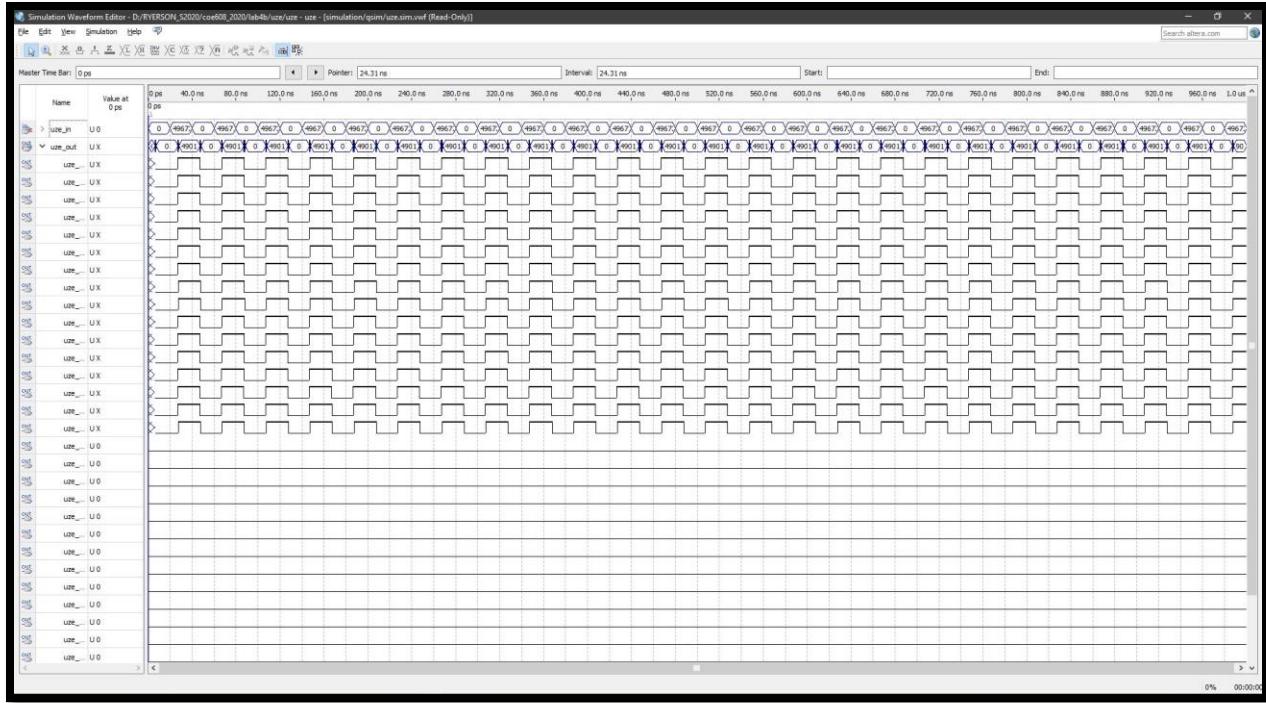


Figure 8: UZE Timing Waveform

Reducer: Functional and Timing

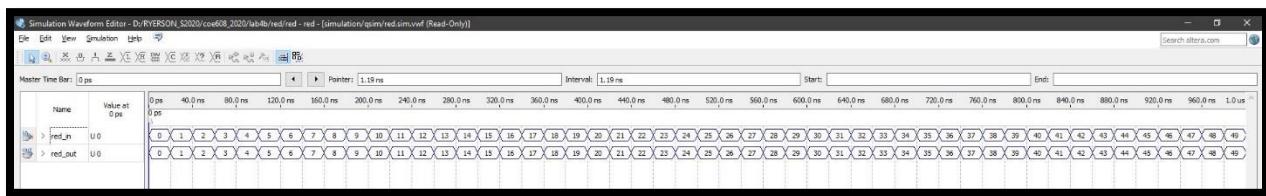


Figure 9: Reducer Functional Waveform



Figure 10: Reducer Timing Waveform

Data-path: Functional and Timing

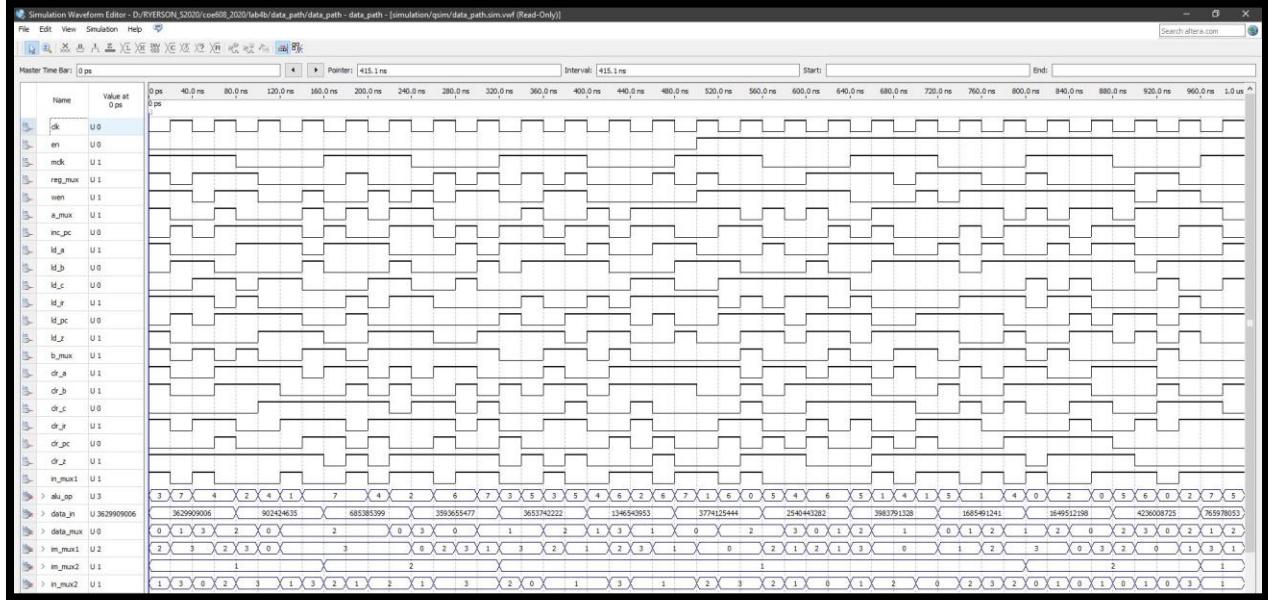


Figure 11: Data-path Random Input Waveform

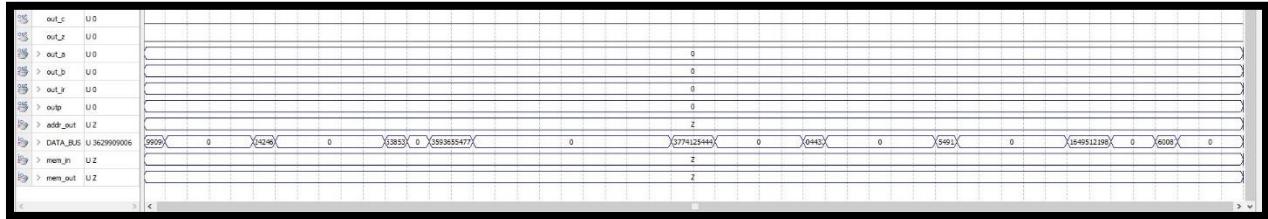


Figure 12: Data-path Output Functional Waveform

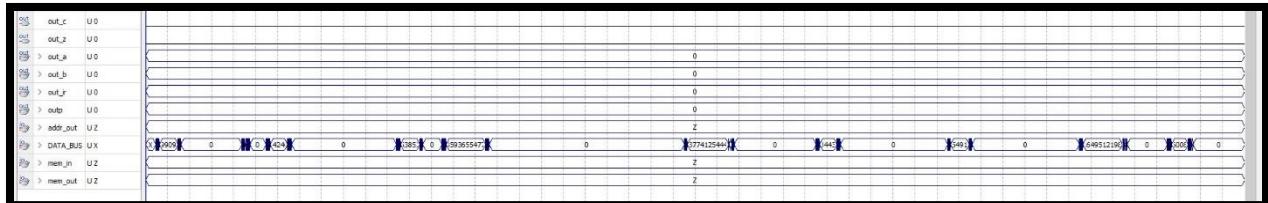


Figure 13: Data-path Output Timing Waveform

For the purposes of understand the operations of MIPS data-path, we have also included the results of specific operations. The random operations waveforms above are not very helpful in demonstrating whether a specific operation works or not.

The following waveform screenshots are courtesy of Duanwei Zhang:

The following figures illustrate the most important operations for the MIPS data-path:

Figure 14: LDAI Operation Waveform, Figure 15: LDBI Operation Waveform, Figure 16: STA Operation Waveform, Figure 17: STB Operation Waveform, Figure 18: LDA Operation Waveform, Figure 19: LDB Operation Waveform, Figure 20: LUI Operation Waveform, Figure 21: JMP Operation Waveform, Figure 22: ADD Operation Waveform, Figure 23: ADDI Operation Waveform, Figure 24: SUB Operation Waveform, Figure 25: INCA Operation Waveform, Figure 26: ROL Operation Waveform, Figure 27: CLRA Operation Waveform, Figure 28: ANDI Operation Waveform, Figure 29: ORI Operation Waveform, Figure 30: DECA Operation Waveform, and Figure 31: ROR Operation Waveform.

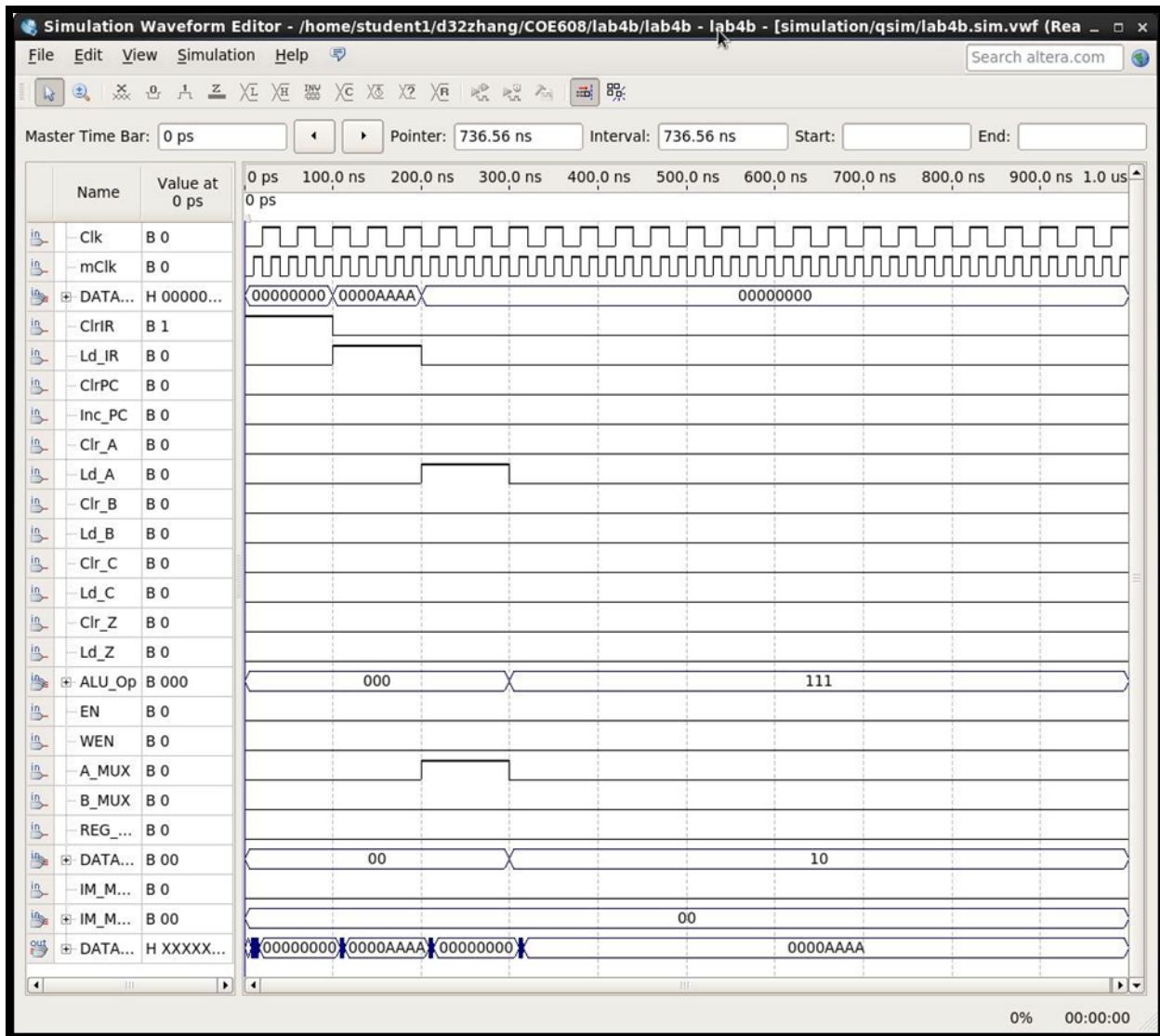


Figure 14: LDAI Operation Waveform

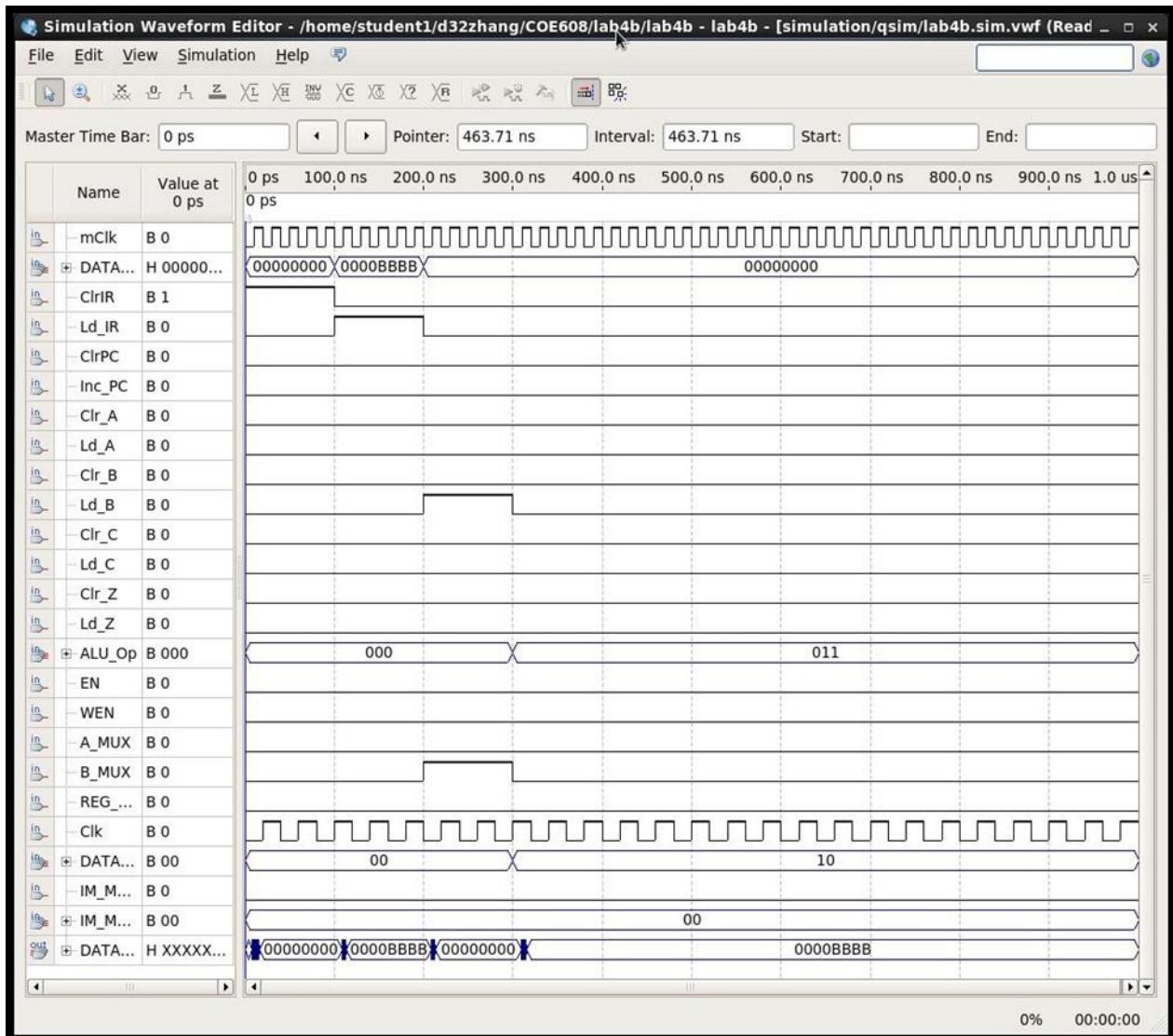


Figure 15: LDBI Operation Waveform

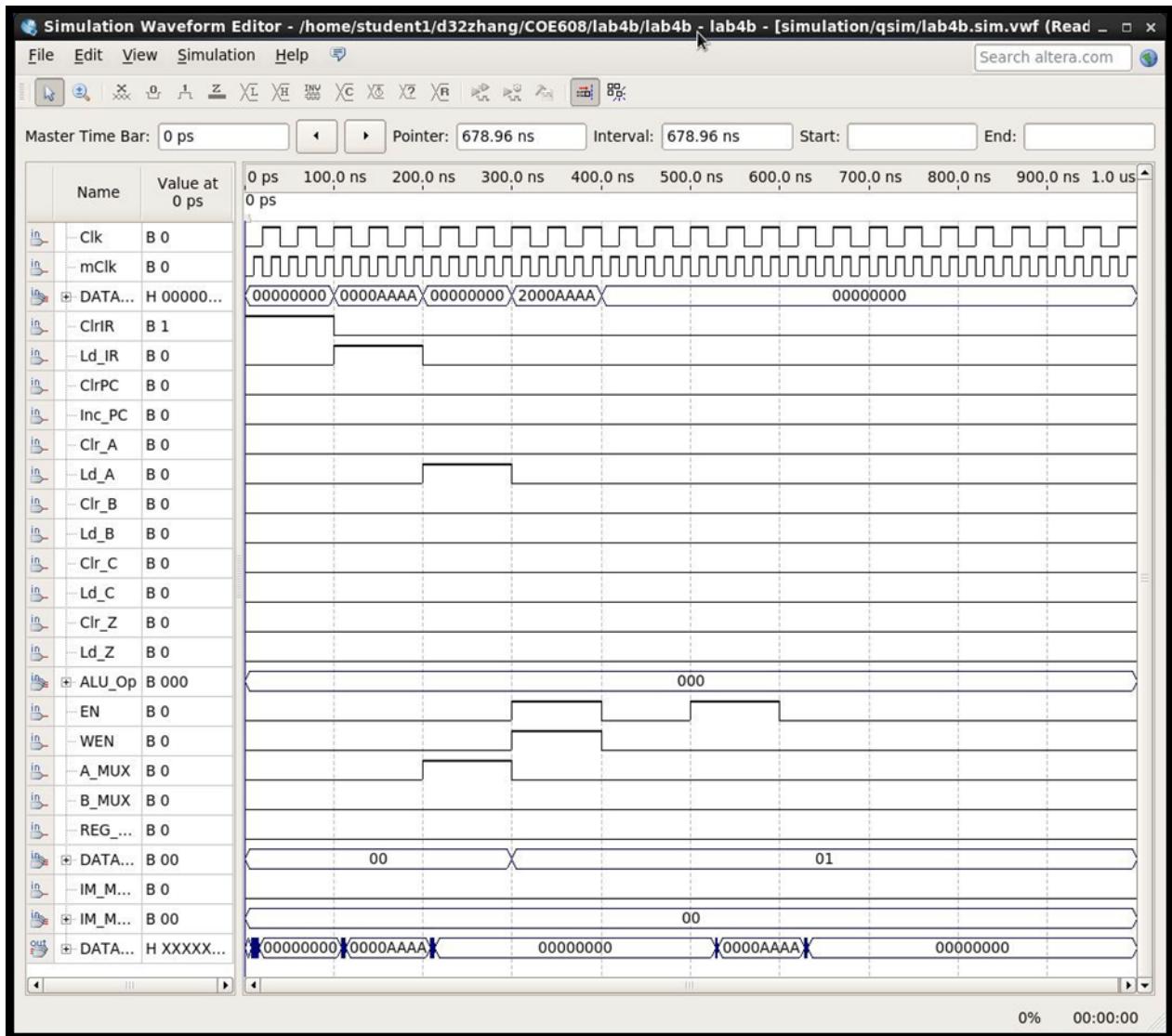


Figure 16: STA Operation Waveform

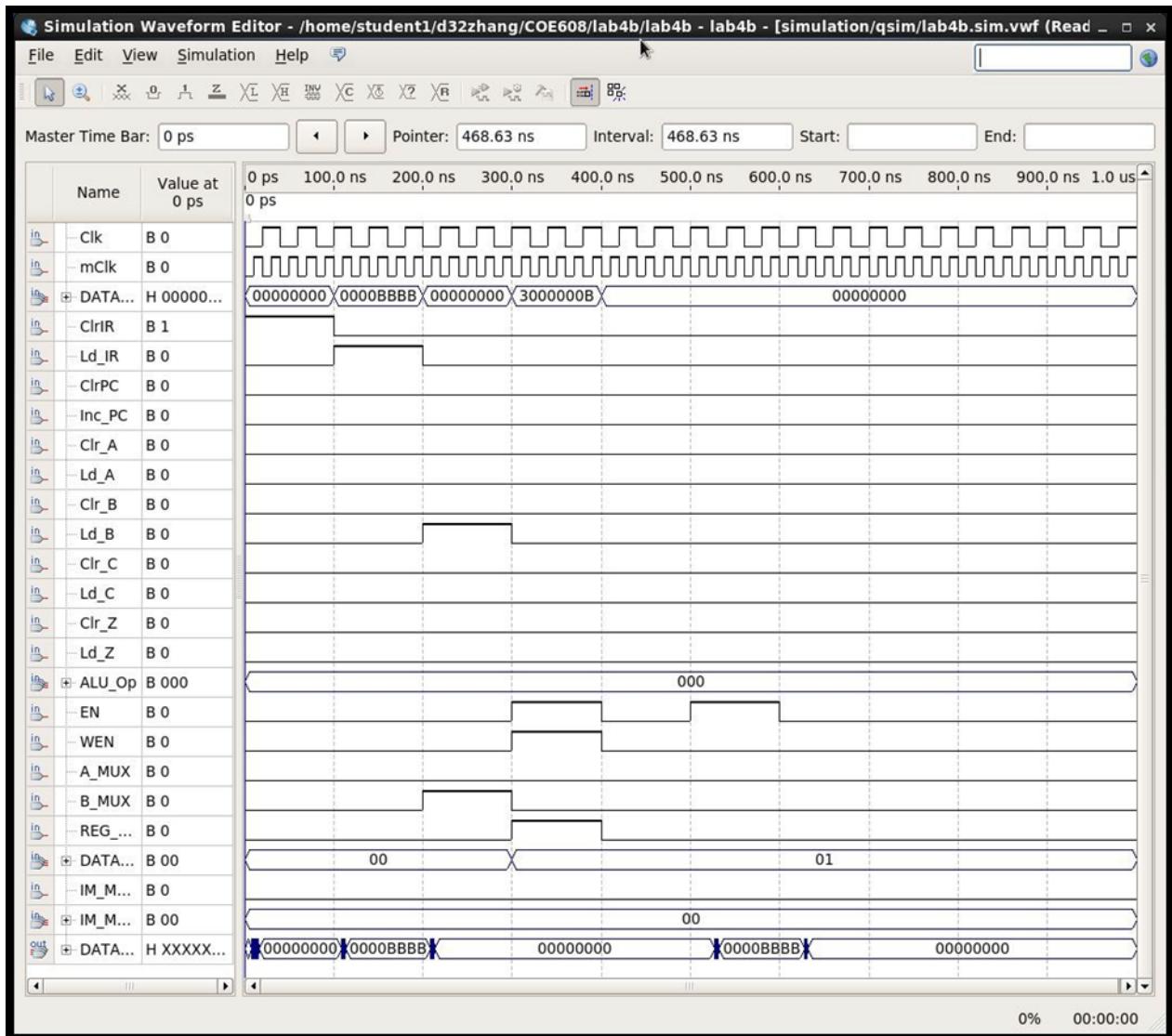


Figure 17: STB Operation Waveform

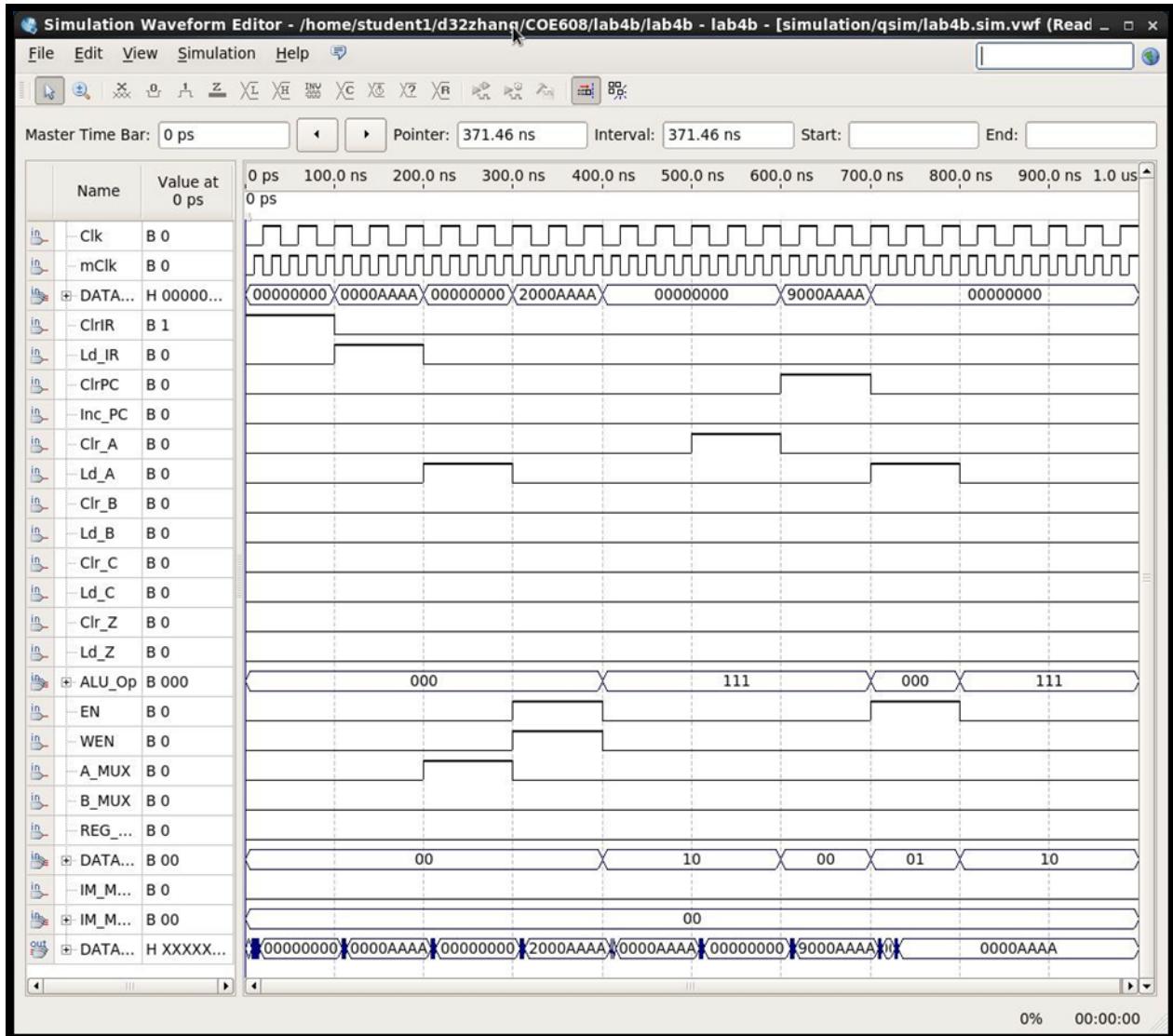


Figure 18: LDA Operation Waveform

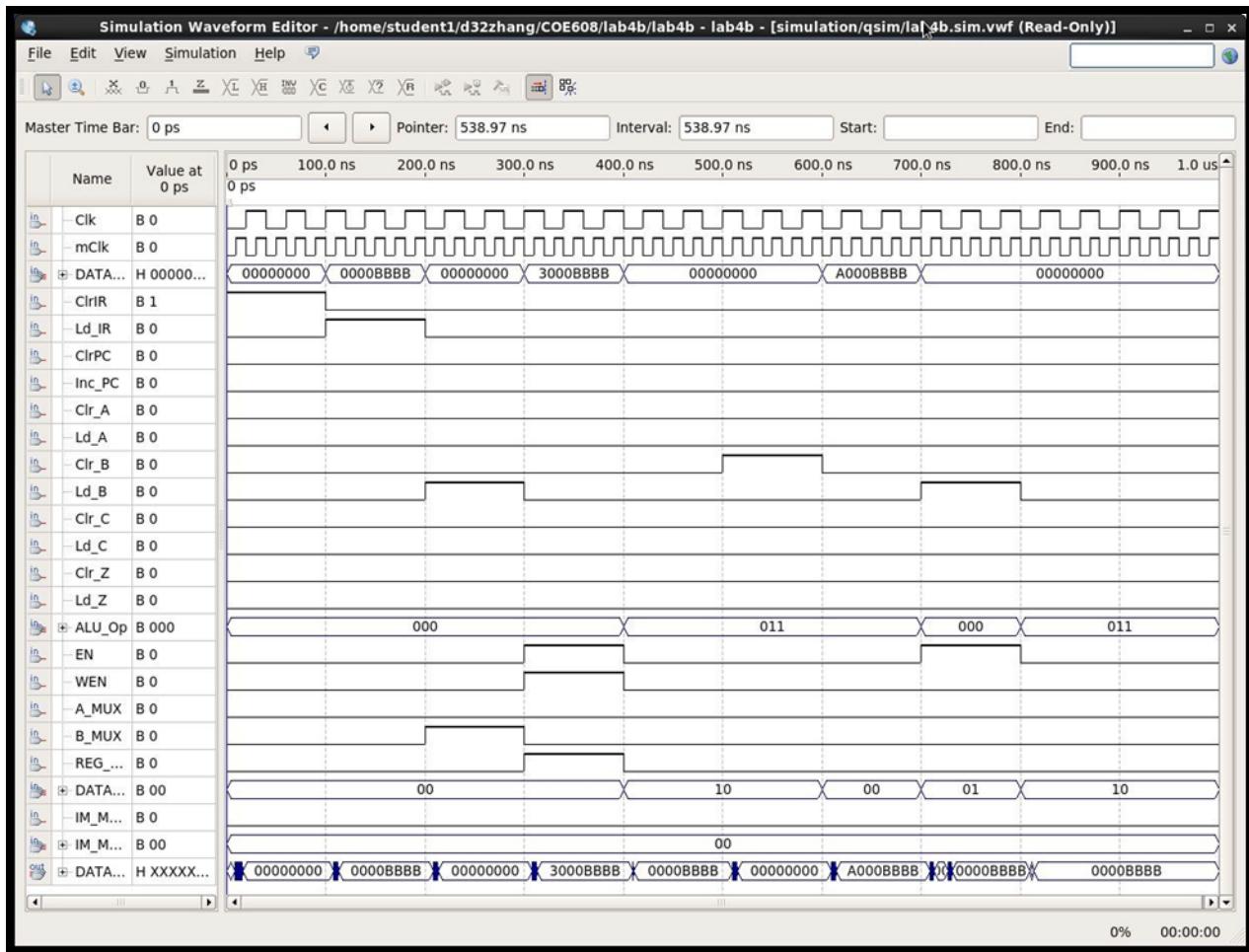


Figure 19: LDB Operation Waveform

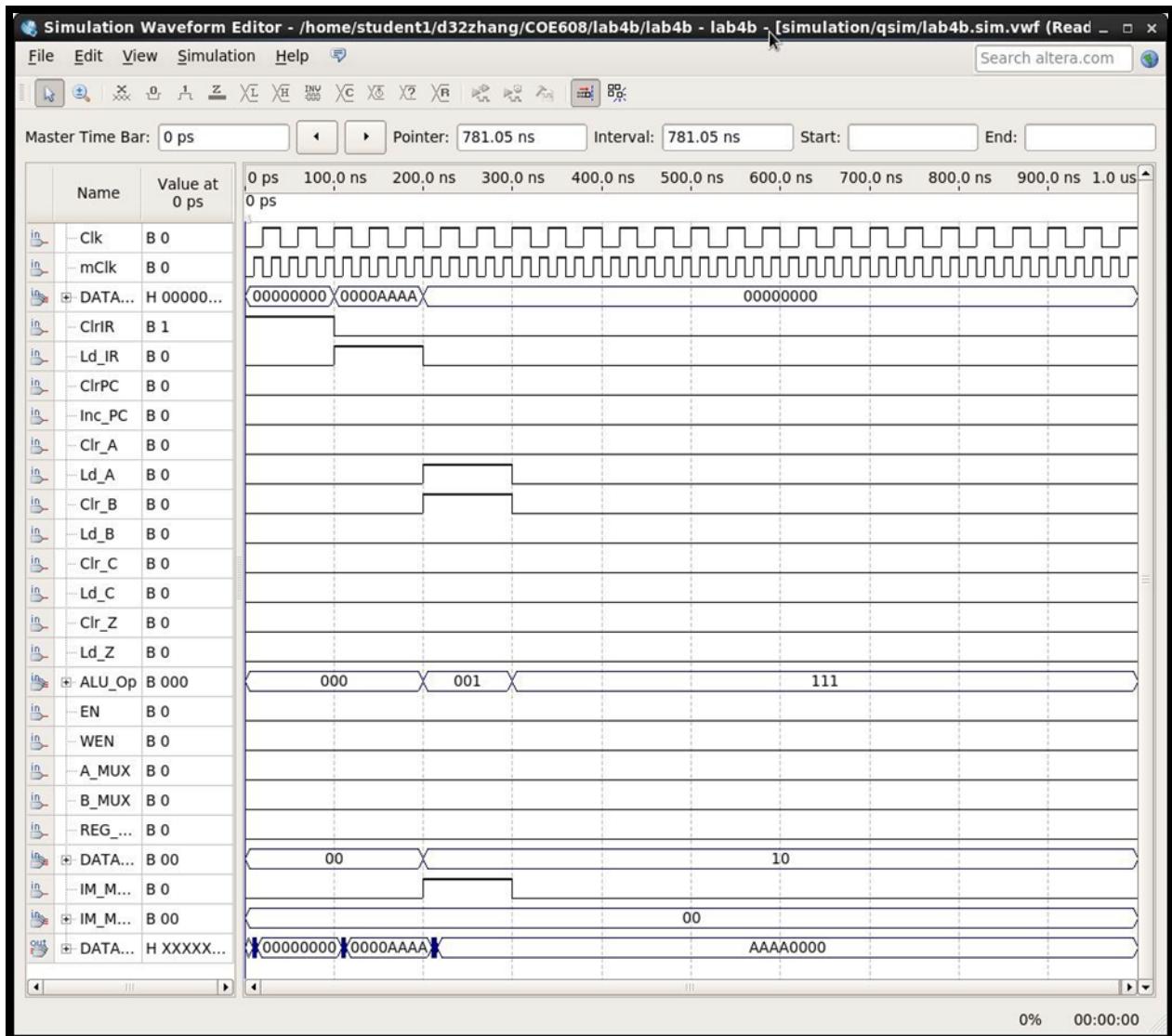


Figure 20: LUI Operation Waveform

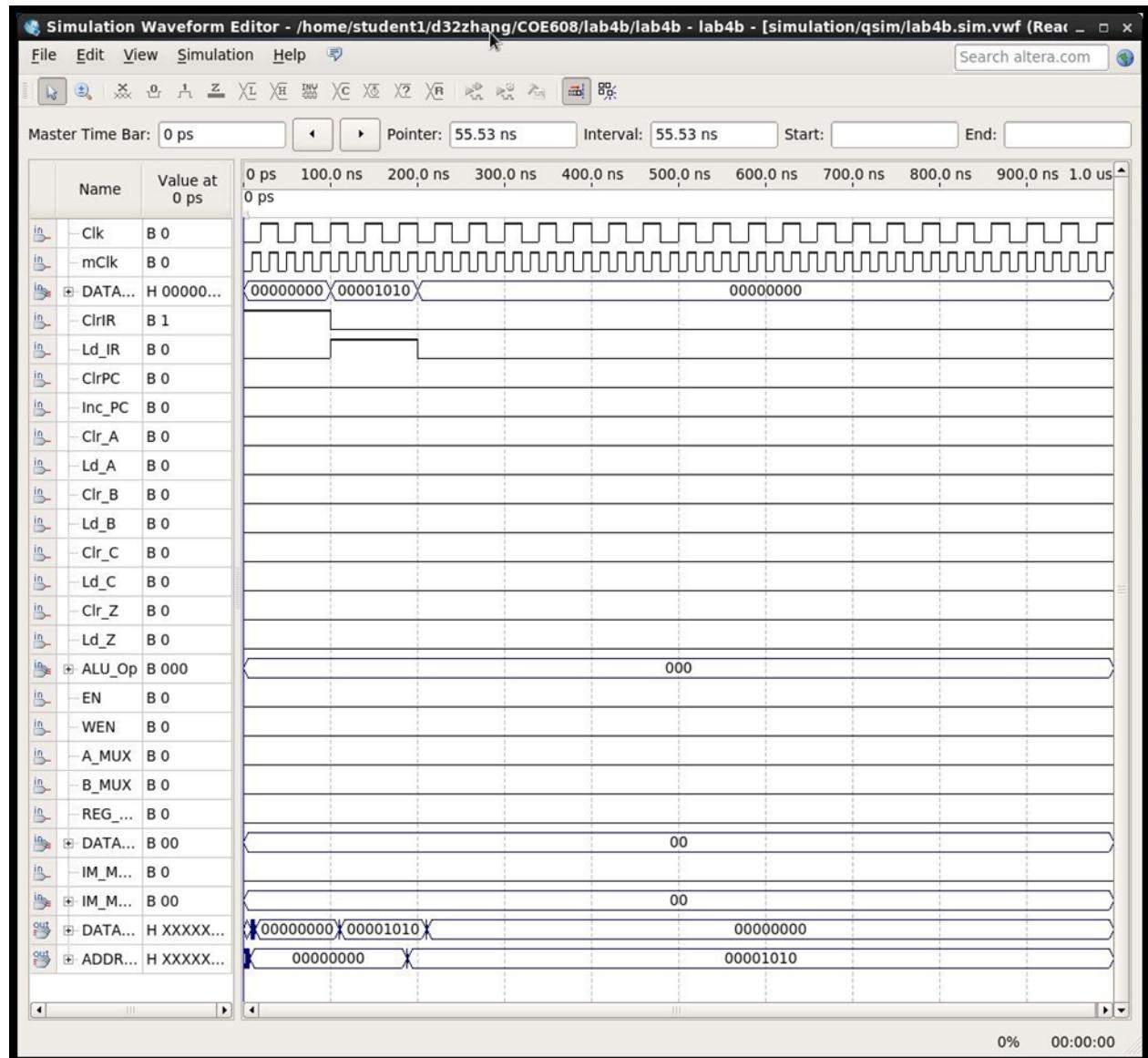


Figure 21: JMP Operation Waveform

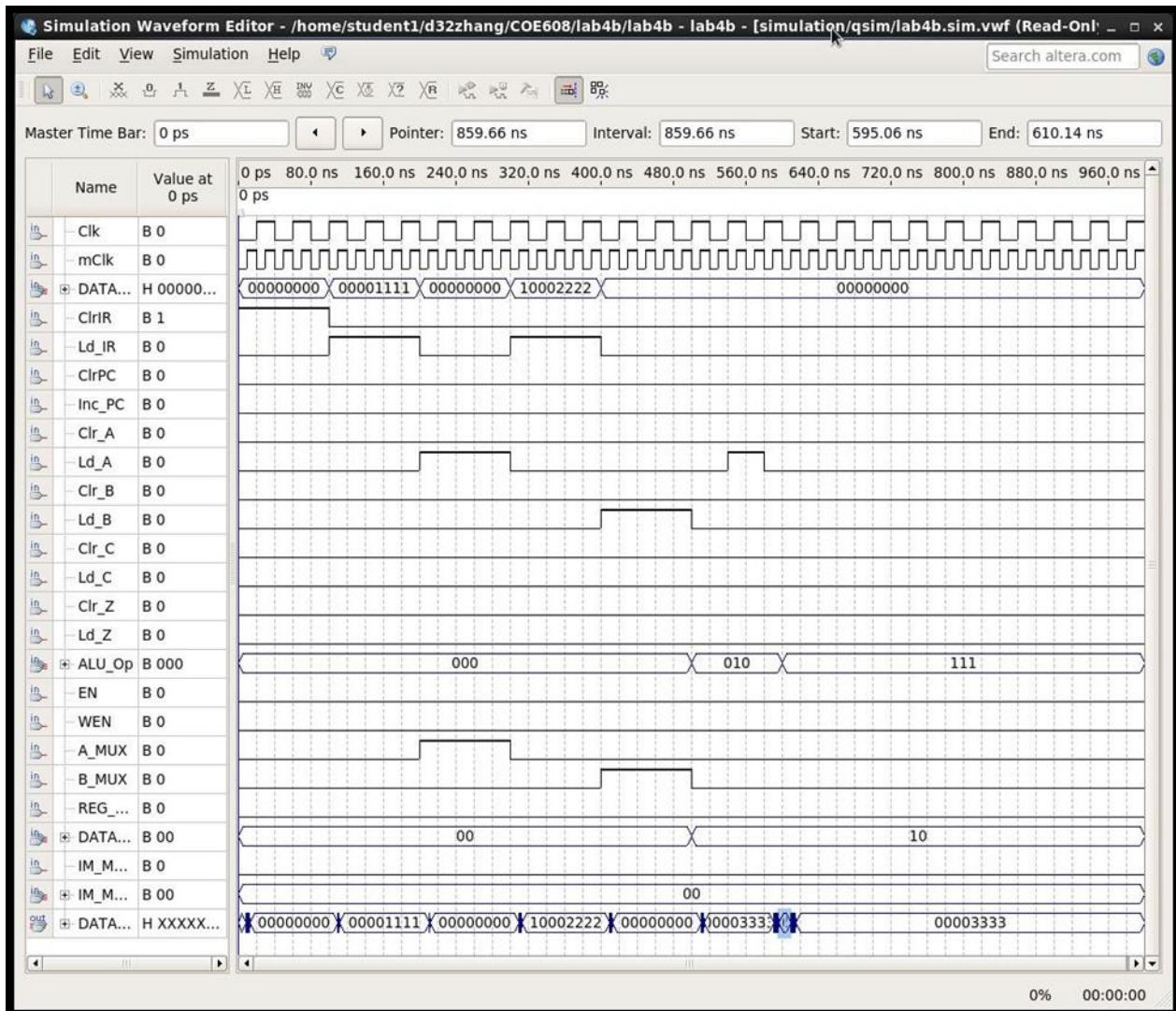


Figure 22: ADD Operation Waveform

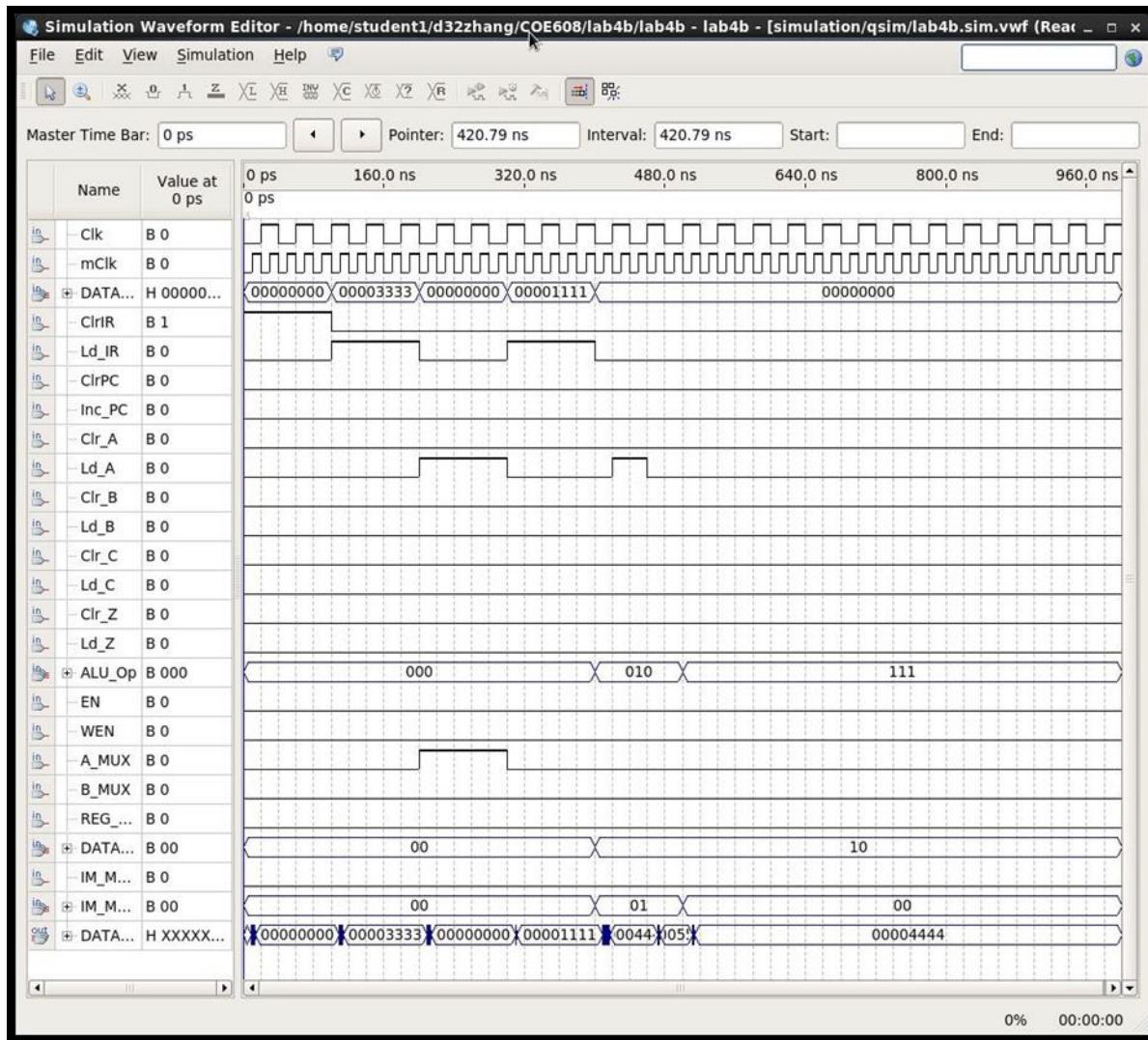


Figure 23: ADDI Operation Waveform

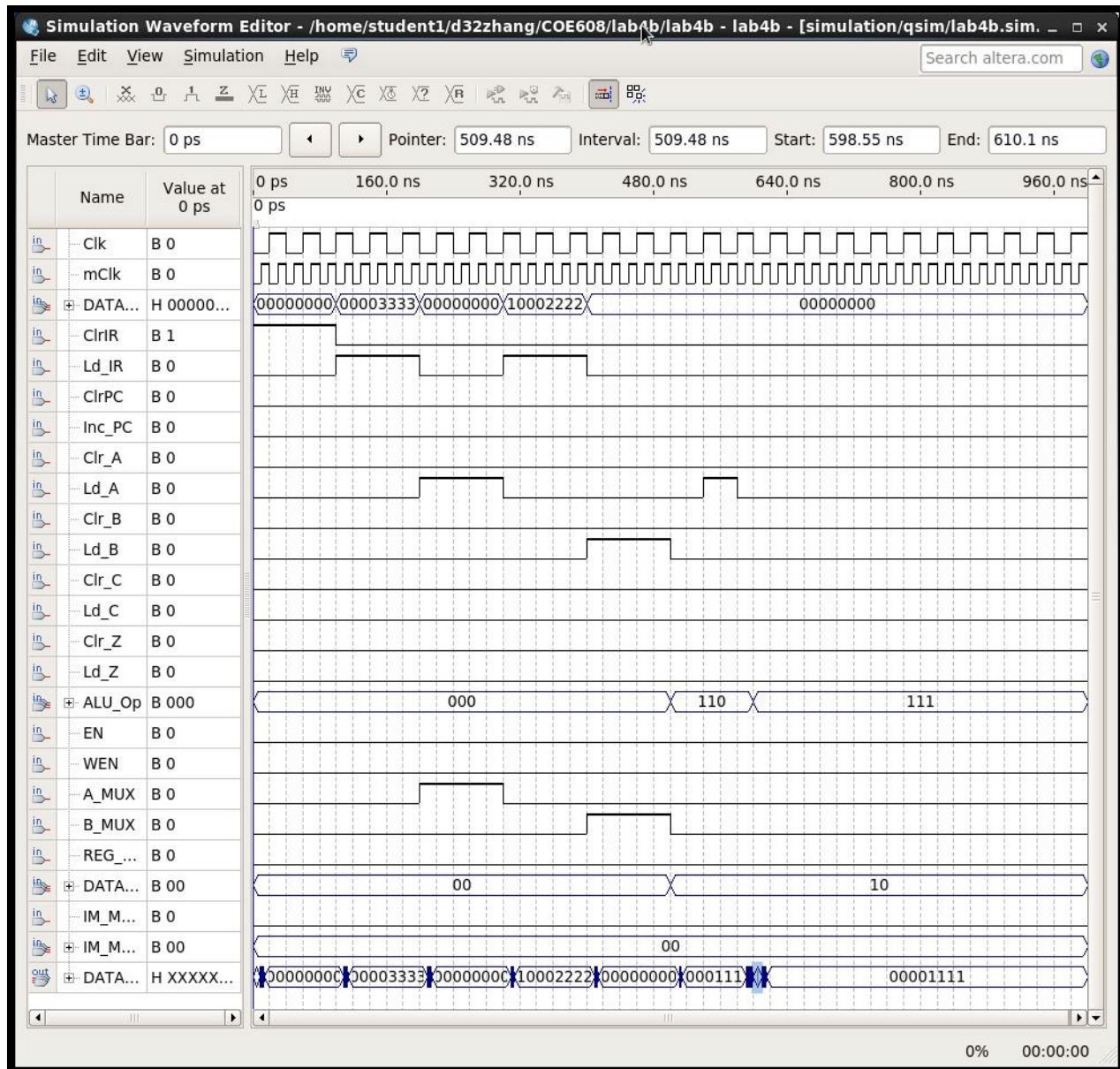


Figure 24: SUB Operation Waveform

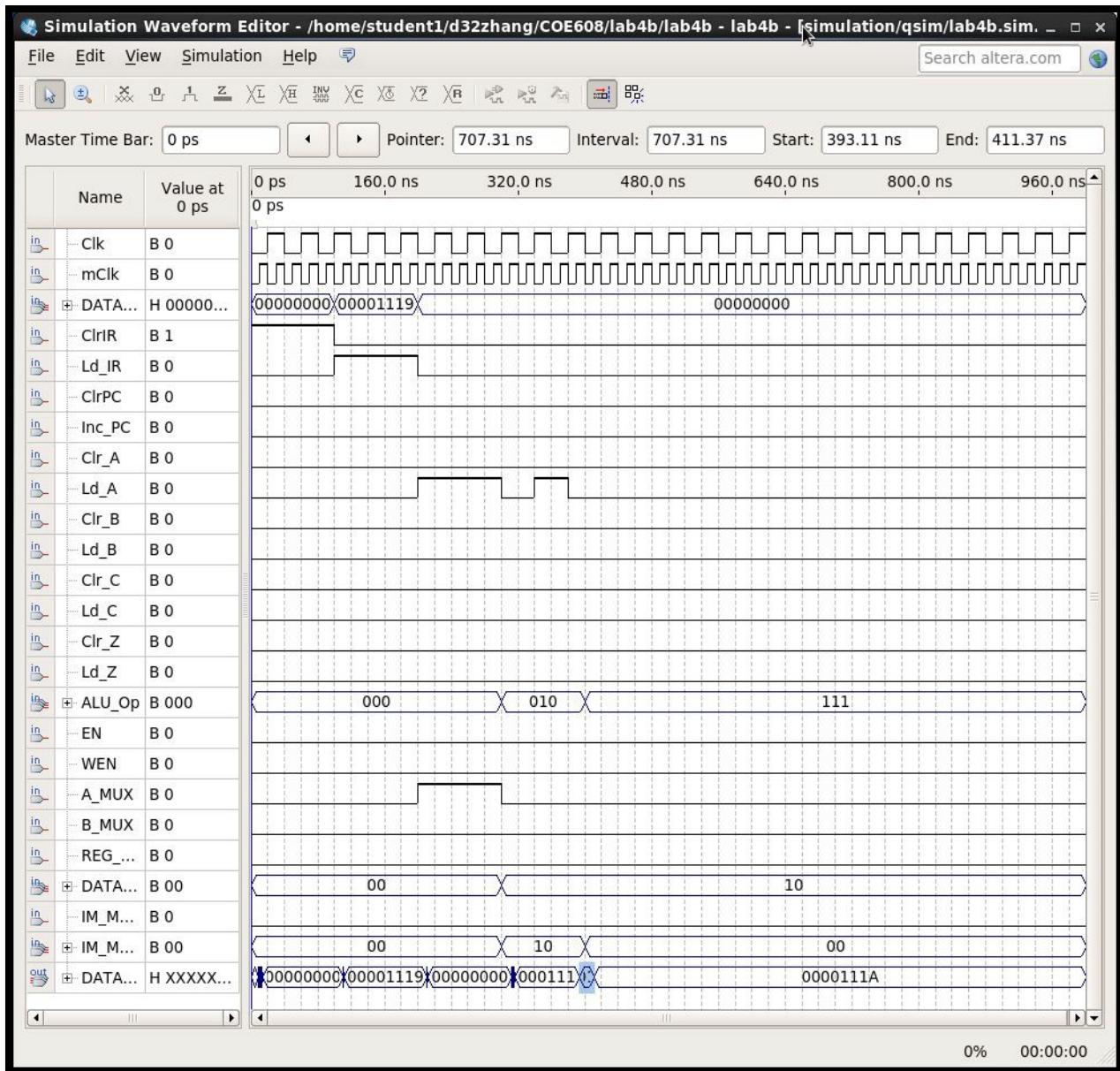


Figure 25: INCA Operation Waveform

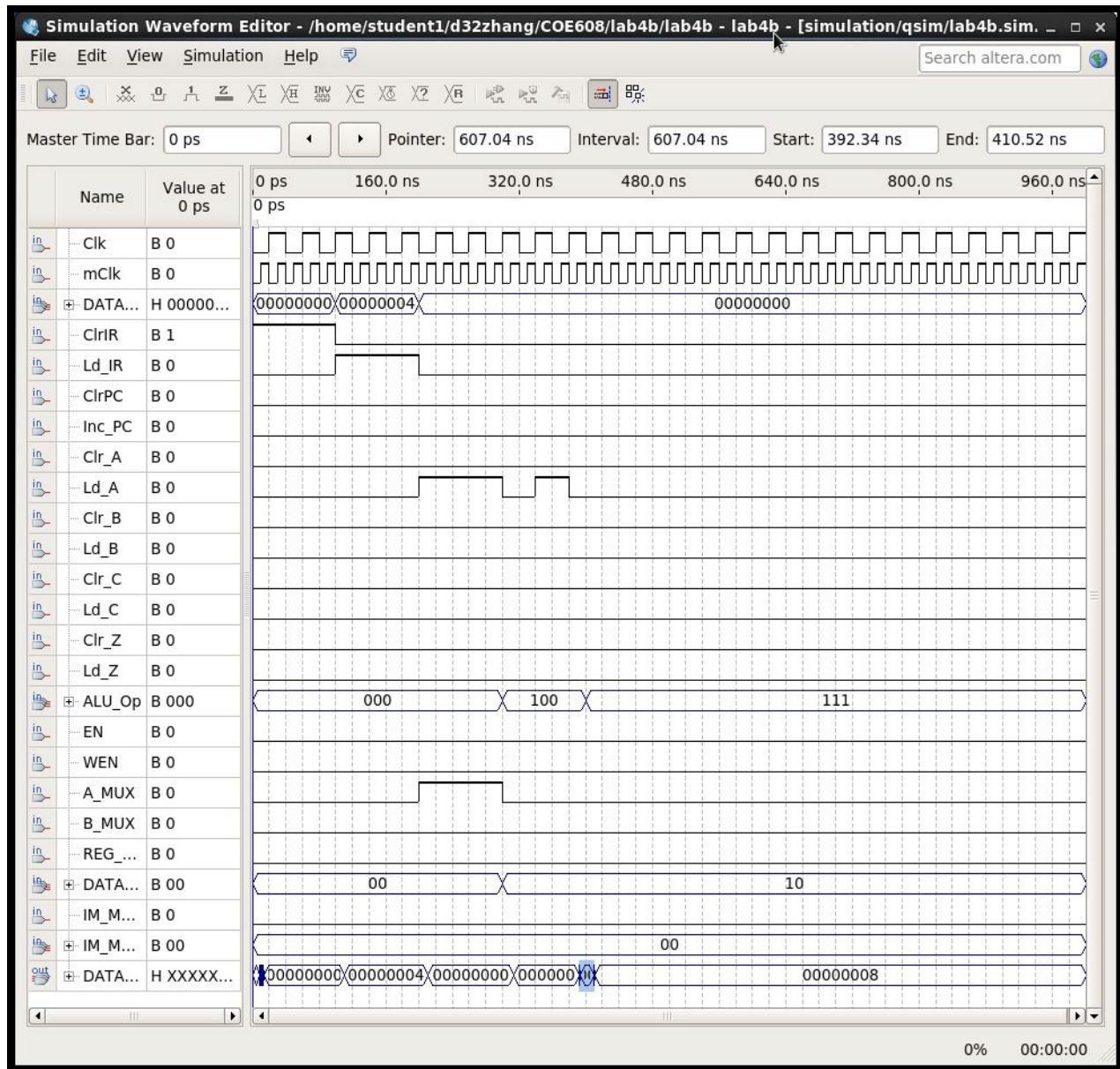


Figure 26: ROL Operation Waveform

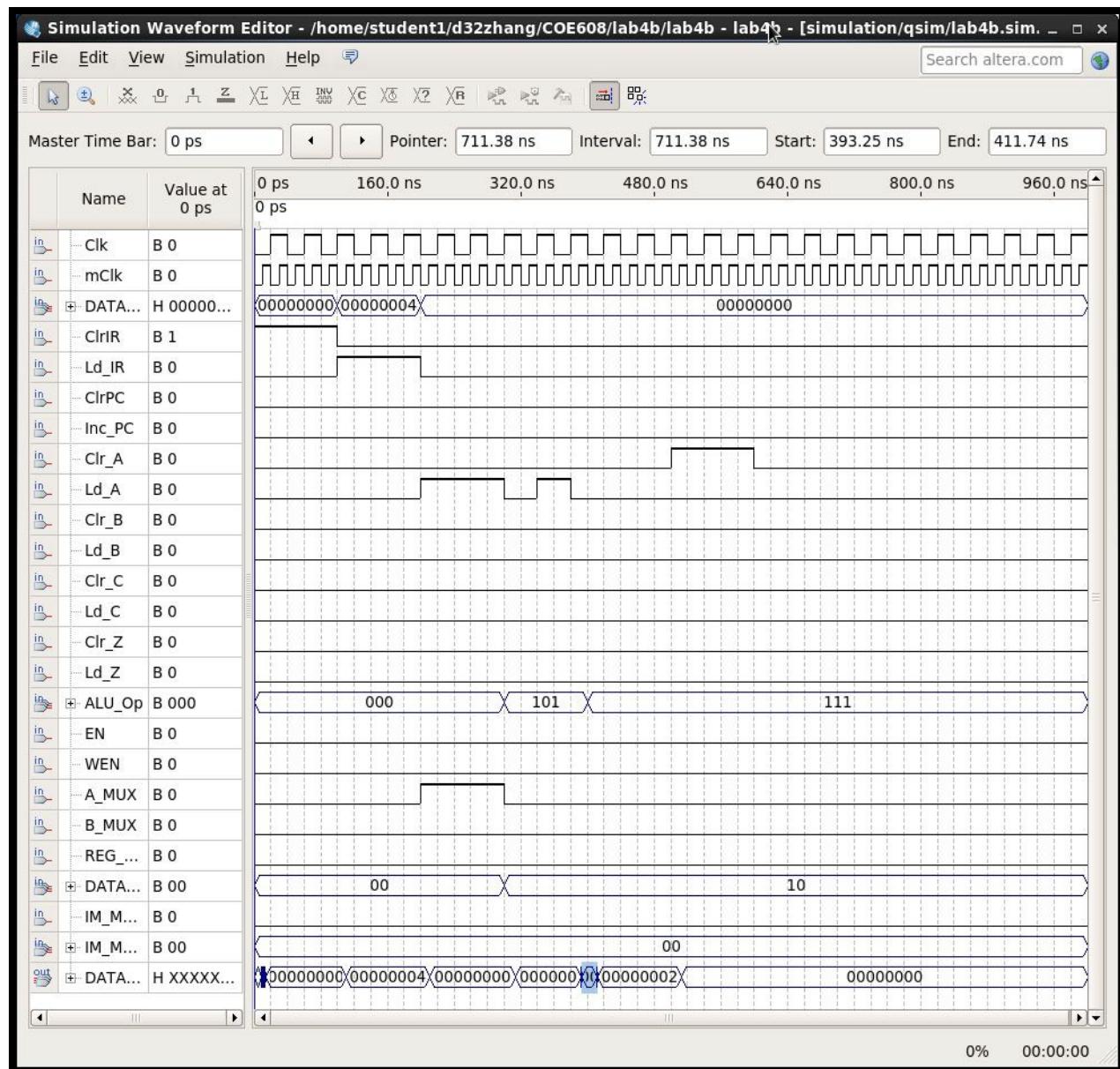


Figure 27: CLRA Operation Waveform

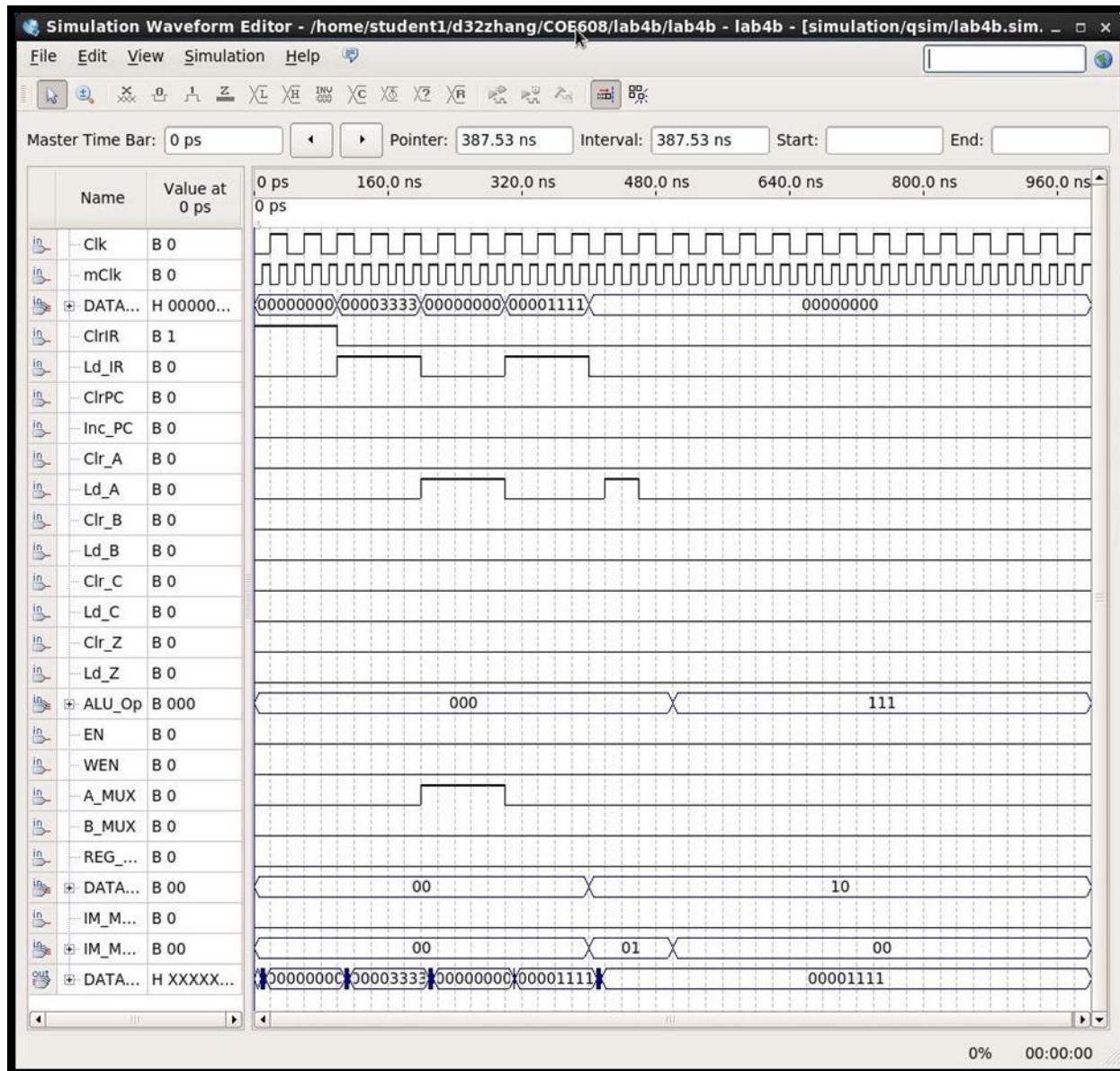


Figure 28: ANDI Operation Waveform

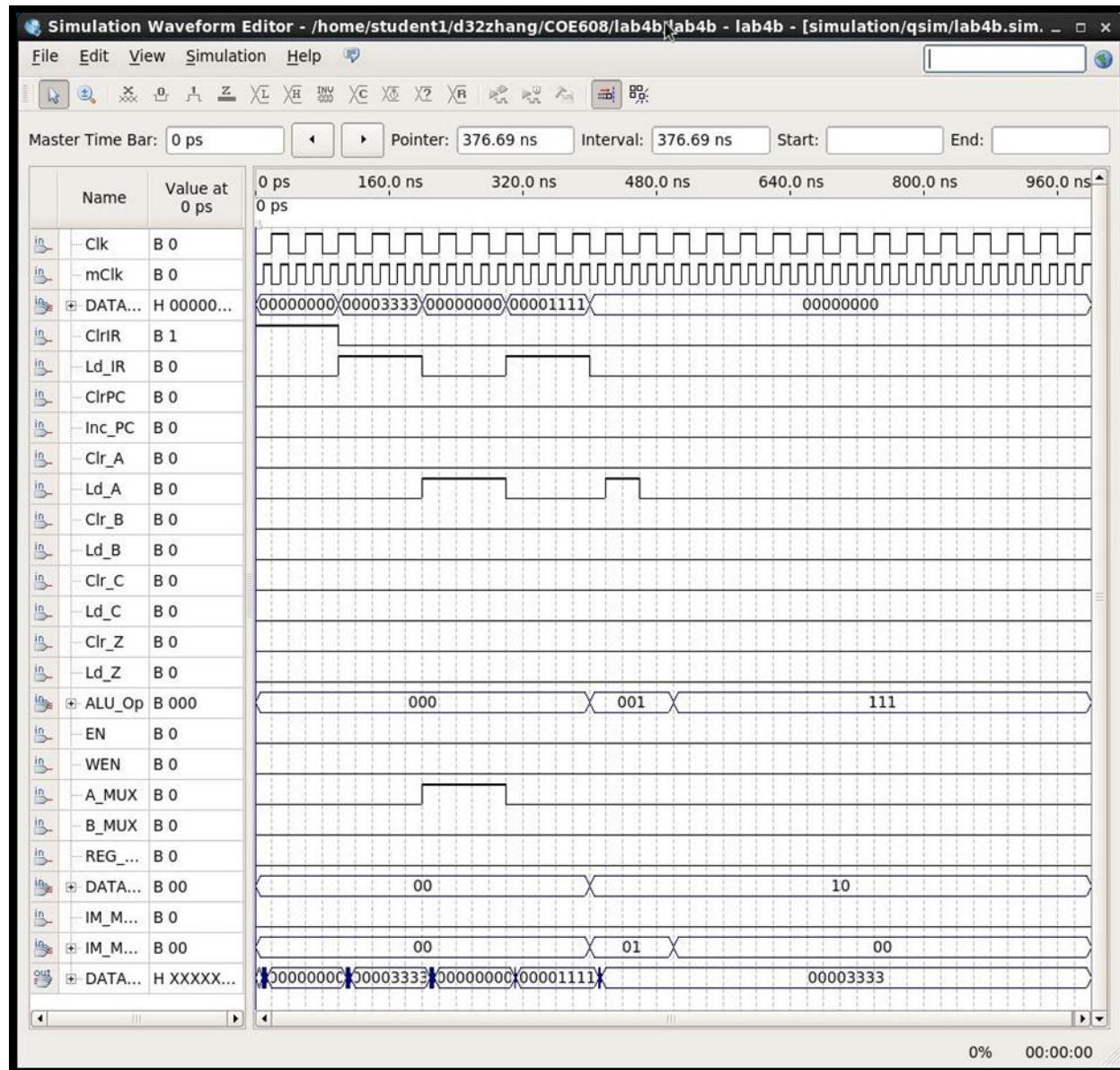


Figure 29: ORI Operation Waveform

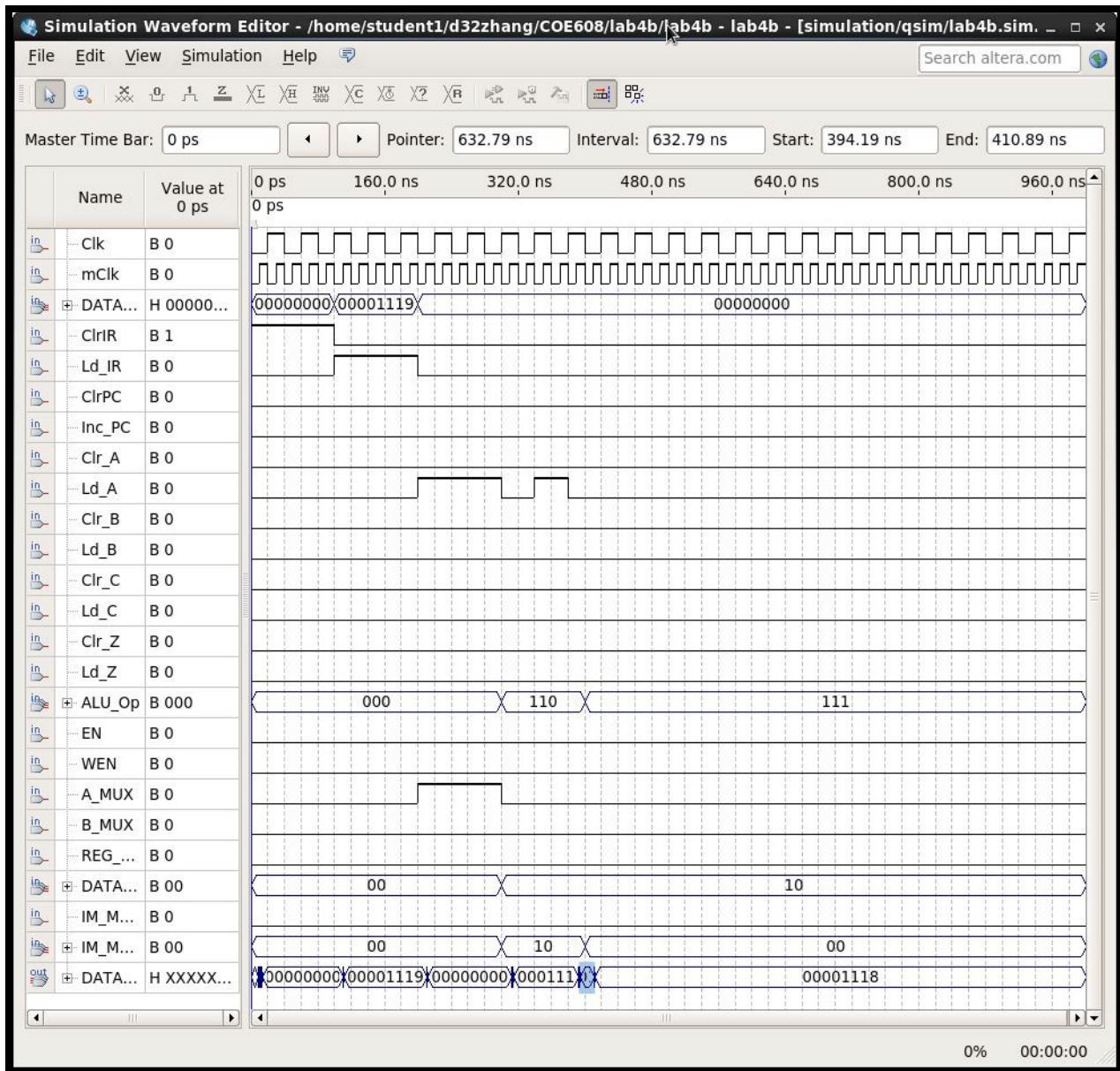


Figure 30: DECA Operation Waveform

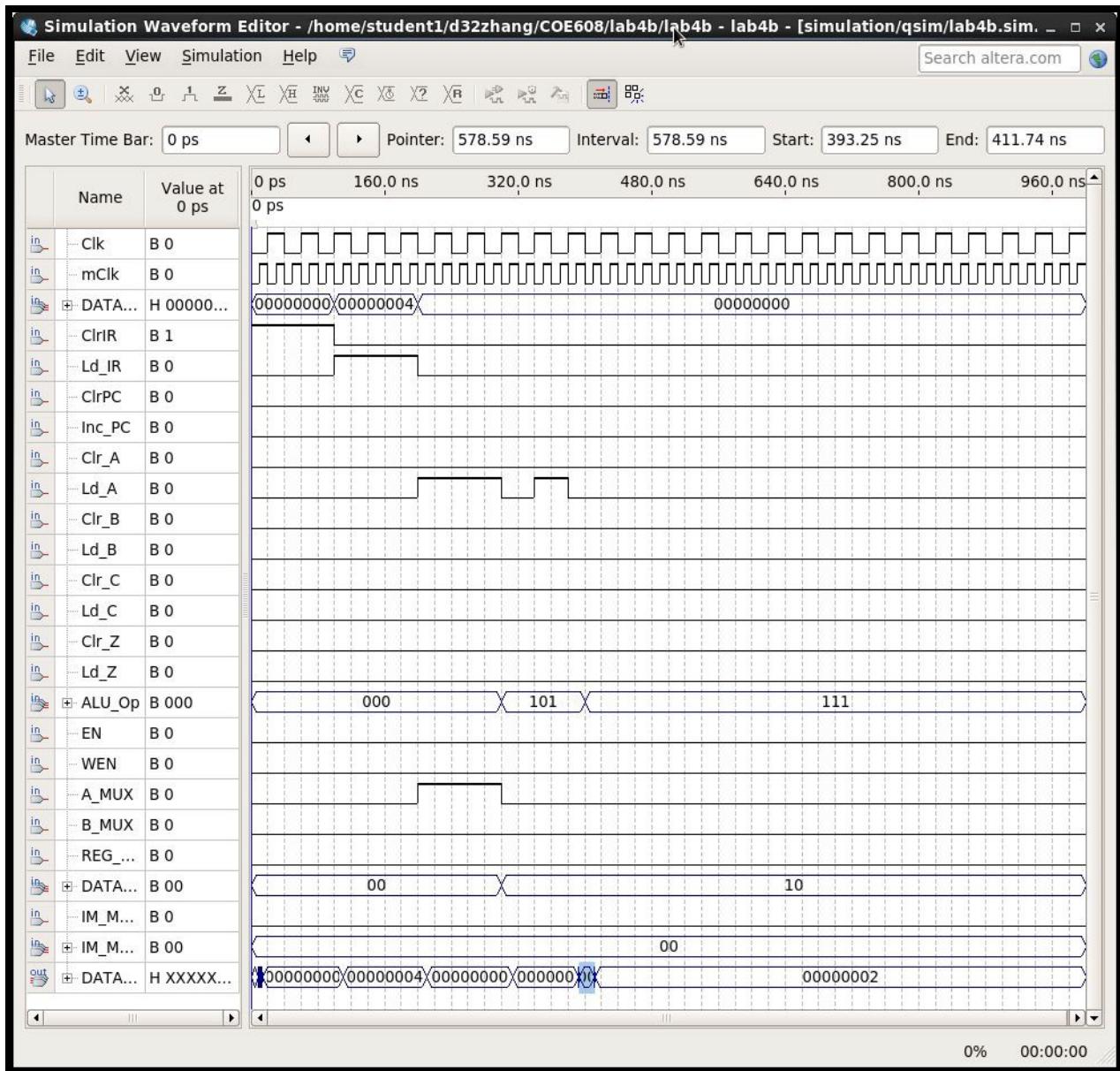


Figure 31: ROR Operation Waveform

Discussions and Conclusions

The data-path implements INCA, ADDI, LDBI and LDA operations by using a finite state machine to select these advanced operations.

The main determinant of the data-path speed is the longest operation performed. In this case, the worst-case timing depends on the operation that is most time-consuming. From Figure 13, it appears the worst-case delay is 10 ns.

The most reliable limit for the data-path clock is 10 ns.

Appendix: VHDL Codes and Screenshots of Waveforms

I have provided the VHDLD and screenshots of the waveforms for easier reading. I also included Duan Wei Zhang's draft report to include the actual data that was captured in each operation waveform listed from Figure 14 to Figure 31.