```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5   entity register1 is
6      port (
7      d,ld,clr,clk: in std_logic;
8      Q: out std_logic);
9   end register1;
10
11  architecture description of register1 is
12     begin
13        process (ld, clr,clk)
14           begin
15              if ld = '0' or clr = '1' then
16                 Q <= '0';
17              elsif rising_edge(clk) then
18                 Q <= '1';
19              end if;
20        end process;
21  end description;
22
23
```