```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_unsigned.all;
4
5   entity mux4to1 is
6      port
7         (s : in std_logic_vector(1 downto 0);
8         x0, x1, x2, x3 : in std_logic_vector(31 downto 0);
9         f : out std_logic_vector(31 downto 0));
10  end mux4to1;
11
12  architecture behavior of mux4to1 is
13     begin
14        with s select
15           f <= x0 when "00",
16                x1 when "01",
17                x2 when "10",
18                x3 when "11";
19  end behavior;
20
21
22
```