Ryerson University

Department of Electrical, Computer & Biomedical Engineering
Faculty of Engineering & Architectural Science

Programs: Computer Engineering

Course Number	**COE608**
Course Title	**Computer Organization and Architecture**
Semester/Year	**Winter 2020**
Instructor	**Patrick Siddavaatam**

Lab Report No.	**2**

Lab Title	**CPU Register Set Design**

Section No.	**011**
Group No.	
Submission Date	**4 July 2020**
Due Date	**9 July 2020**

Name	Student ID	Signature*
Duanwei Zhang	*500824903*	DZ
Xinyu Hadrian Hu	500194233	XHH

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www.ryerson.ca/senate/current/pol60.pdf.

Name: Xinyu Hadrian Hu, and Duan Wei Zhang

Student Number: 500194233, and 500824903

Date: June 26, 2020

COE 608: Computer Architecture and Design

COE 608: Lab 2 Report

Objective

The purpose of this lab to generate the VHDL codes for the one-bit register, the thirty-two-bit registers, and the program counter, and test the registers and program counter with the ModelSIM waveforms in Quartus software.

Design and Implementation

The implementation of the 1-bit register and the 32-bit register follow similar procedures. The program counter has a different truth table.

1-bit register				
ld	**d**	**clr**	**clk**	**Q**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Figure 1: 1-bit register Truth Table

The truth table for the 32-bit register is below, taken from a sample of readings from the actual waveforms generated:

32-bit register				
ld	d (unsigned)	clr	clk	Q (unsigned)
1	0	0	0	0
1	1	0	1	0
1	2	0	0	0
1	3	0	1	2
1	4	0	0	2
1	5	0	1	4
1	6	0	0	4
1	7	0	1	6
1	8	0	0	6
1	9	0	1	8
1	10	0	0	8
1	11	0	1	10
1	12	0	0	10
1	13	0	1	12
1	14	0	0	12
1	15	0	1	14
1	16	0	0	14
1	17	0	1	16
1	18	0	0	16
1	19	0	1	18
1	20	1	0	0
1	21	1	1	0
1	22	1	0	0
1	23	1	1	0
1	24	1	0	0
1	25	1	1	0
1	26	1	0	0
1	27	1	1	0
1	28	1	0	0
1	29	1	1	0
1	30	1	0	0
1	31	1	1	0
1	32	1	0	0
1	33	1	1	0
1	34	1	0	0
1	35	1	1	0
1	36	1	0	0
1	37	1	1	0
1	38	1	0	0
1	39	1	1	0

Figure 2: 32-bit register Truth Table

Note that d and Q are unsigned decimal integers, to make the truth table easier to generate. In reality, the values would have to be converted to 32-bit binary, which is a lot of zeros and ones, which makes it very difficult to tabulate.

Finally, the truth table for the program counter is shown below:

program counter					
clk	clr	inc	ld	d (unsigned)	q (unsigned)
0	0	0	0	0	0
1	0	0	0	1	0
0	1	0	0	2	0
1	1	0	0	3	0
0	0	0	0	4	0
1	0	0	0	5	0
0	1	0	0	6	0
1	1	0	0	7	0
0	0	1	0	8	0
1	0	1	0	9	0
0	1	1	0	10	0
1	1	1	0	11	10
0	0	1	0	12	0
1	0	1	0	13	0
0	1	1	0	14	0
1	1	1	0	15	0
0	0	0	1	16	0
1	0	0	1	17	0
0	1	0	1	18	0
1	1	0	1	19	0
0	0	0	1	20	0
1	0	0	1	21	0
0	1	0	1	22	0
1	1	0	1	23	0
0	0	1	1	24	0
1	0	1	1	25	0
0	1	1	1	26	0
1	1	1	1	27	26
0	0	1	1	28	0
1	0	1	1	29	0
0	1	1	1	30	0
1	1	1	1	31	0

Figure 3: Program Counter Truth Table

The value of the program counter will only increase by 4 when clk, clr and inc are all true.

Register1: Functional and Timing Waveforms

Below are the waveforms, both functional and timing:

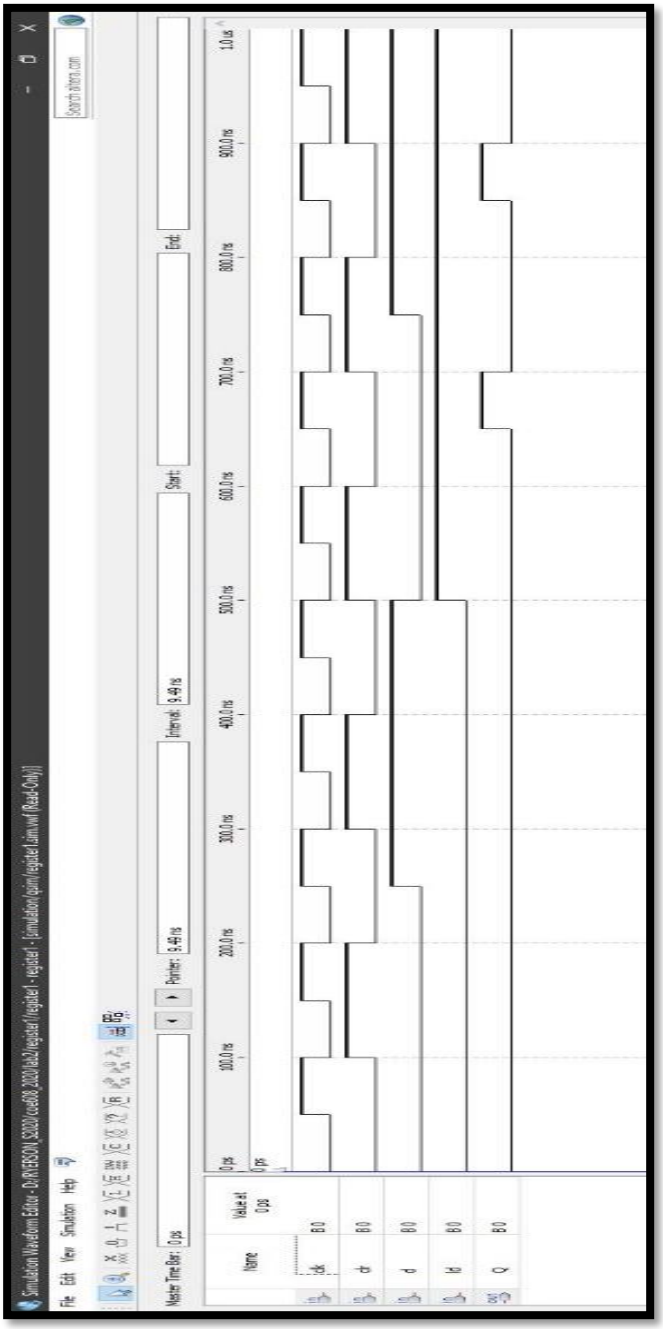


Figure 4: Functional Waveform for register1

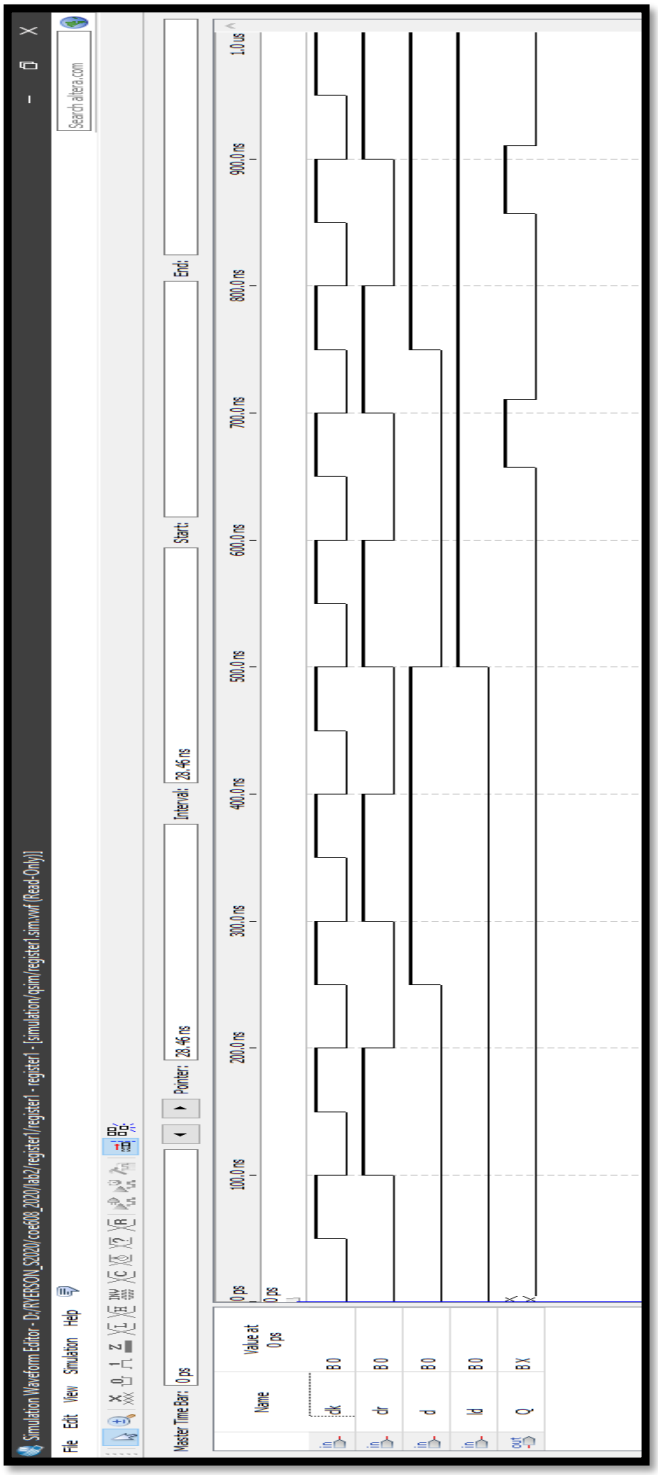


Figure 5: Timing Waveform for register1

As can be observed above for the register1 waveforms, there is no significant delays in the timing simulation compared to the functional simulation.

Register32: Functional and Timing Waveforms

The waveforms for the 32-bit register, both functional and timing are illustrated below:

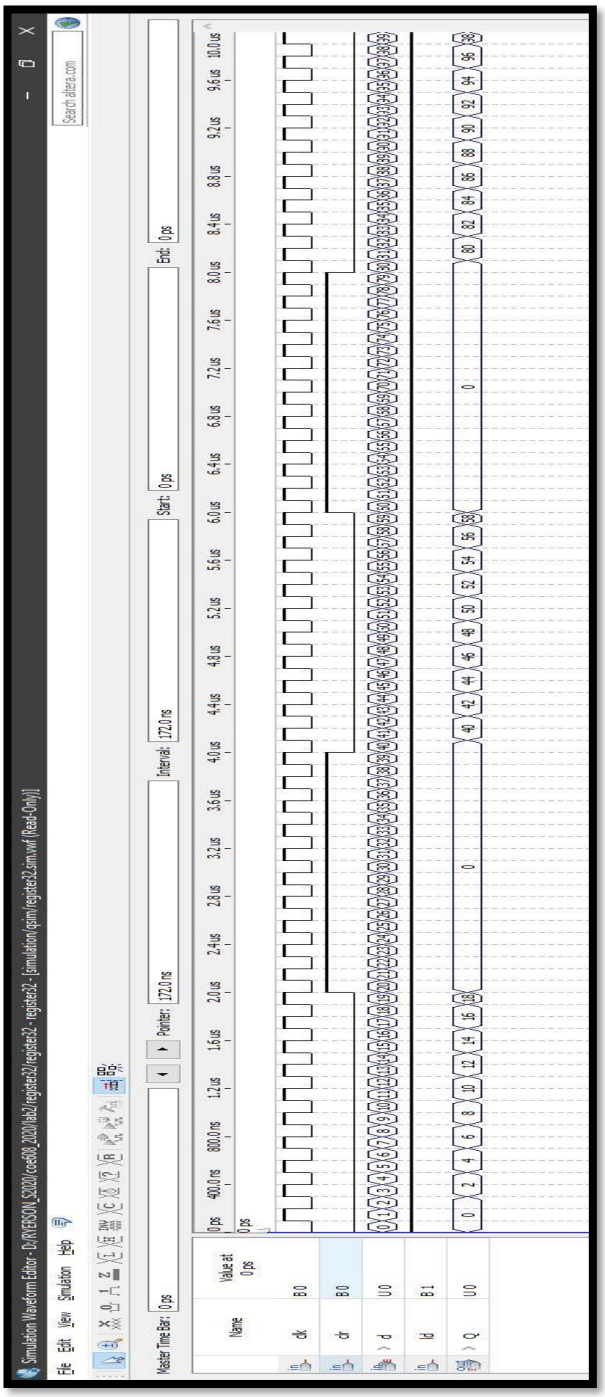


Figure 6: Functional Waveform for register32

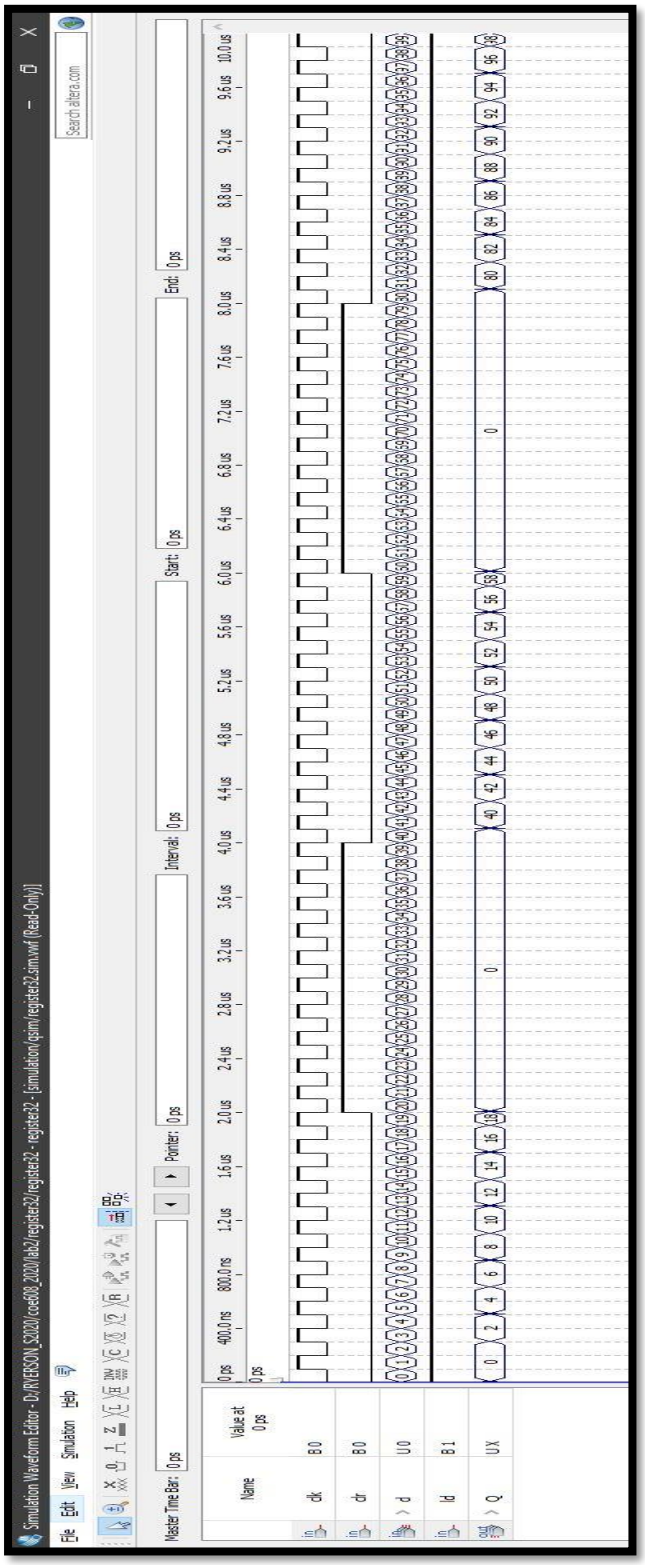


Figure 7: Timing Waveform for Register32

As can be observed above, there is more delays in the 32-bit register compared with the 1-bit register.

Next, the VHDL code, and respective functional and timing waveforms for the program counter:

PC: Functional and Timing Waveforms

The functional waveform for the PC is shown below:

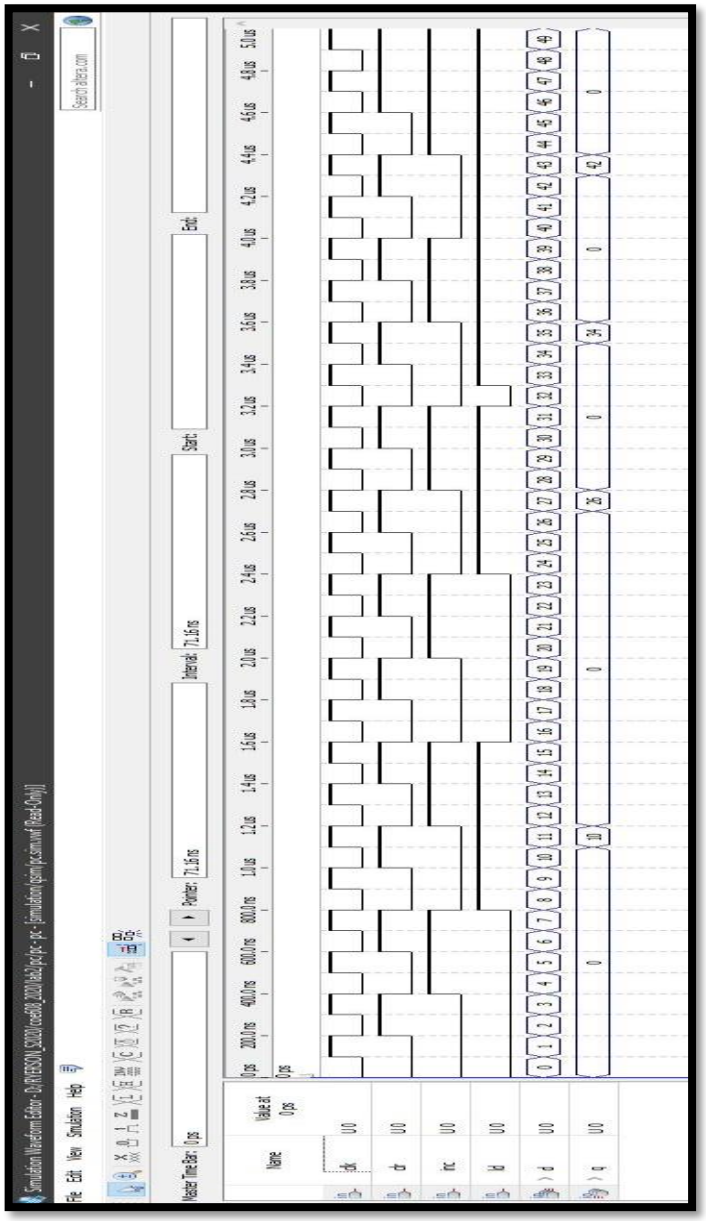


Figure 8: PC Functional Waveform

Next, the timing simulation for the PC:

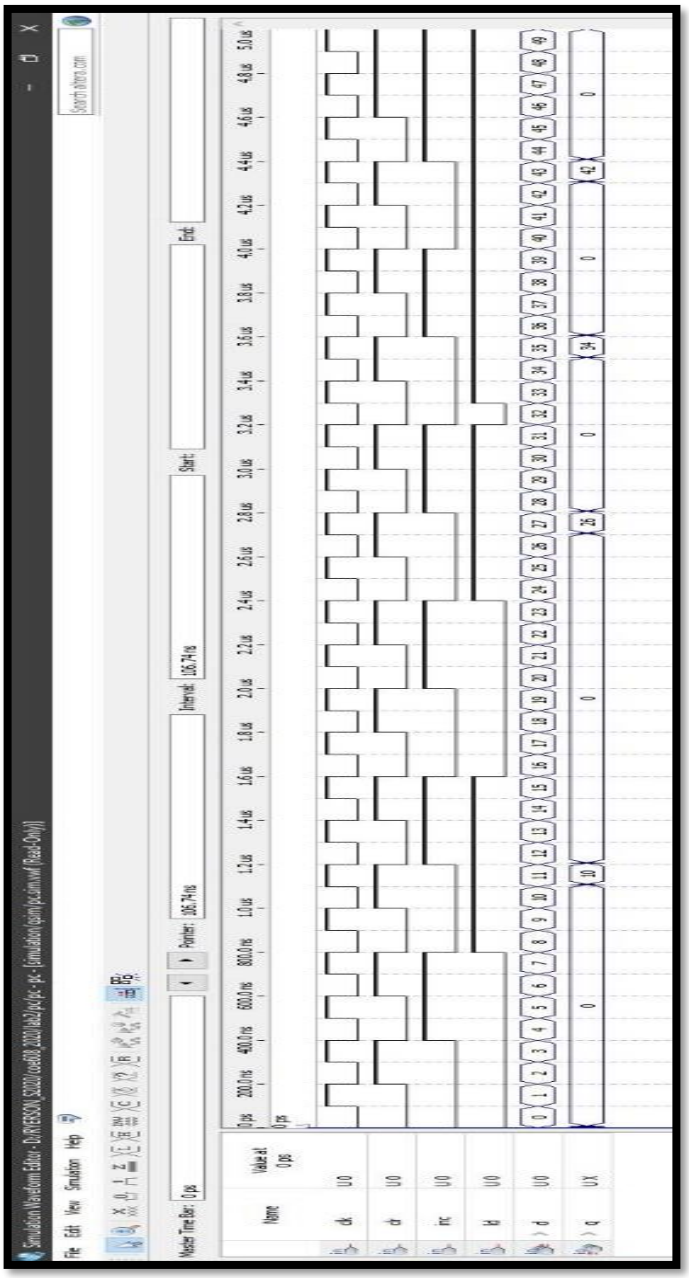


Figure 9: PC Timing Waveform Diagram

As can be observed, there is some delay, within a few nanoseconds in the timing simulation diagram for the Program Counter.

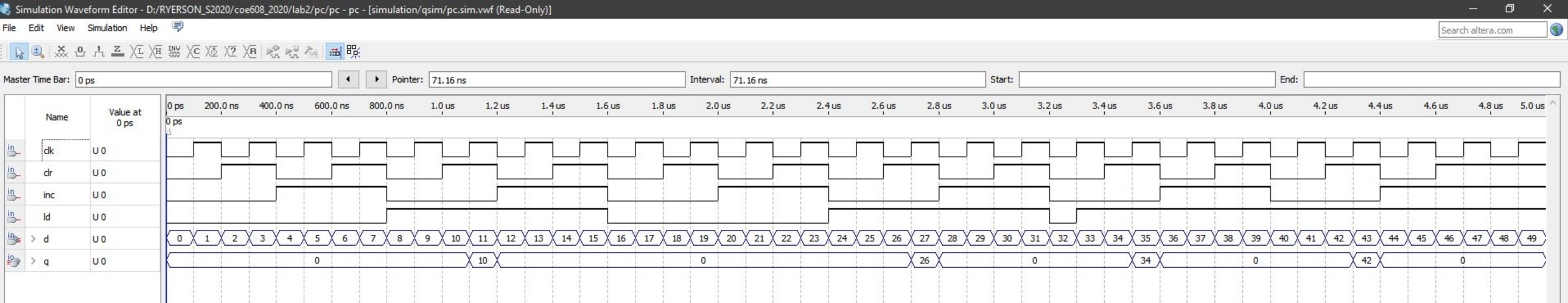
The primary causes of delays is due to architectural implementation of the VHDL code. Perhaps more efficient VHDL coding will produce less delay in the timing simulations. Nevertheless, the

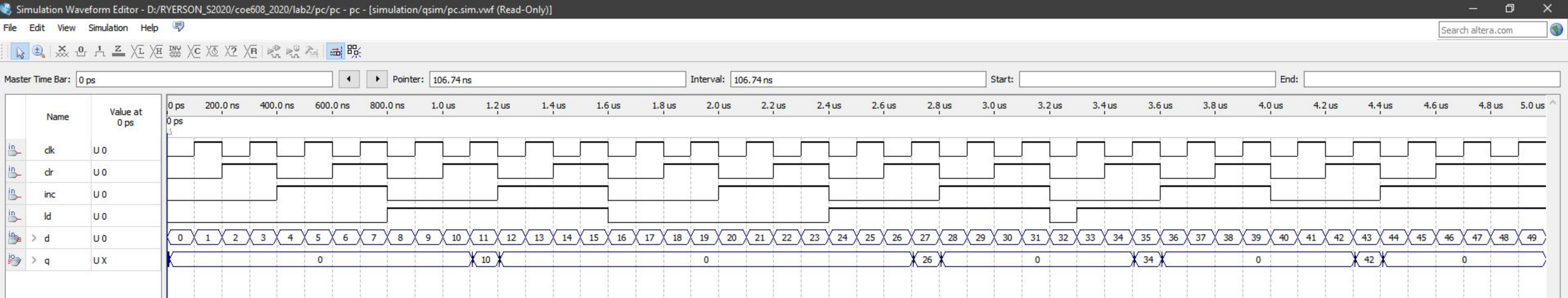
delays observed thus far in the PC, the registers are minute and should not hinder over-all system performance.

Appendices: VHDL Codes for the Registers and Program Counter

The files are attached as PDF to make this document easier to read.

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   entity pc is
7      port(
8      clr, clk, ld, inc: in std_logic;
9      d: in std_logic_vector(31 downto 0);
10     q: inout std_logic_vector(31 downto 0));
11  end pc;
12
13  architecture description of pc is
14     begin
15        process(clk,clr,ld,inc)
16           begin
17              if clr = '0' then
18                 q <= (others => '0');
19                 elsif rising_edge(clk) then
20                    if ld = '1' then
21                       if inc = '0' then
22                       q <= d;
23                          if ld = '1' and inc = '1' then
24                             q <= q+4;
25                          end if;
26                       end if;
27                    end if;
28             end if;
29       end process;
30  end description;
```


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab2/pc/pc - pc - [simulation/qsim/pc.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 71.16 ns
Interval: 71.16 ns
Start:
End:
Name
Value at 0 ps
clk U 0
clr U 0
inc U 0
ld U 0
d U 0
q U 0
0 ps 200.0 ns 400.0 ns 600.0 ns 800.0 ns 1.0 us 1.2 us 1.4 us 1.6 us 1.8 us 2.0 us 2.2 us 2.4 us 2.6 us 2.8 us 3.0 us 3.2 us 3.4 us 3.6 us 3.8 us 4.0 us 4.2 us 4.4 us 4.6 us 4.8 us 5.0 us
0 ps
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
0 10 0 26 0 34 0 42 0


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab2/pc/pc - pc - [simulation/qsim/pc.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 106.74 ns
Interval: 106.74 ns
Start:
End:
Name
Value at 0 ps
clk U 0
clr U 0
inc U 0
ld U 0
d U 0
q U X
0 ps 200.0 ns 400.0 ns 600.0 ns 800.0 ns 1.0 us 1.2 us 1.4 us 1.6 us 1.8 us 2.0 us 2.2 us 2.4 us 2.6 us 2.8 us 3.0 us 3.2 us 3.4 us 3.6 us 3.8 us 4.0 us 4.2 us 4.4 us 4.6 us 4.8 us 5.0 us
0 ps
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
0 10 0 26 0 34 0 42 0

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5   entity register1 is
6      port (
7      d,ld,clr,clk: in std_logic;
8      Q: out std_logic);
9   end register1;
10
11  architecture description of register1 is
12     begin
13        process (ld, clr,clk)
14           begin
15              if ld = '0' or clr = '1' then
16                 Q <= '0';
17              elsif rising_edge(clk) then
18                 Q <= '1';
19              end if;
20        end process;
21  end description;
22
23
```

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab2/register1/register1 - register1 - [simulation/qsim/register1.sim.vwf (Read-Only)]

File Edit View Simulation Help

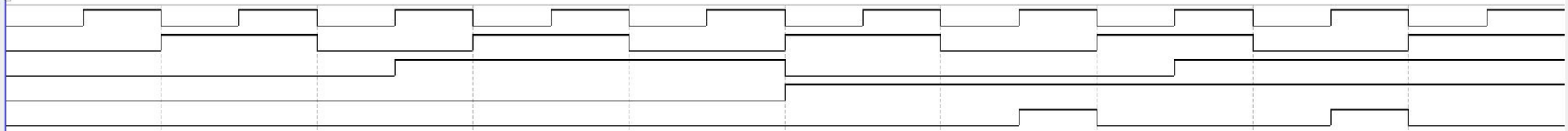
Search altera.com

Master Time Bar: 0 ps | Pointer: 9.49 ns | Interval: 9.49 ns | Start: | End:

	Name	Value at 0 ps
in	clk	B 0
in	clr	B 0
in	d	B 0
in	ld	B 0
out	Q	B 0

0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us

0 ps



0% 00:00:00

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab2/register1/register1 - register1 - [simulation/qsim/register1.sim.vwf (Read-Only)]

File Edit View Simulation Help

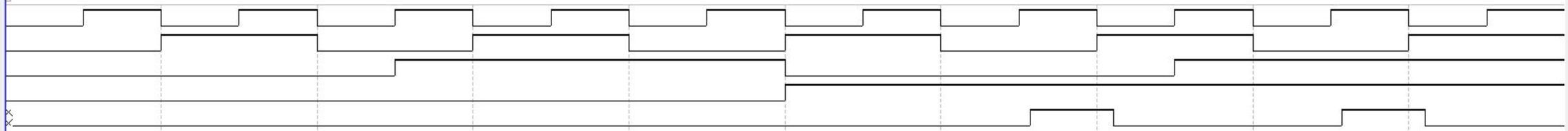
Search altera.com

Master Time Bar: 0 ps Pointer: 28.46 ns Interval: 28.46 ns Start: End:

Name	Value at 0 ps
clk	B 0
clr	B 0
d	B 0
ld	B 0
Q	B X

0 ps 100.0 ns 200.0 ns 300.0 ns 400.0 ns 500.0 ns 600.0 ns 700.0 ns 800.0 ns 900.0 ns 1.0 us

0 ps



0% 00:00:00

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5   entity register32 is
6      port (
7      d: in std_logic_vector(31 downto 0);
8      ld,clr,clk: in std_logic;
9      Q: out std_logic_vector(31 downto 0));
10  end register32;
11
12  architecture description of register32 is
13     begin
14        process (ld, clr,clk)
15           begin
16              if ld = '0' or clr = '1' then
17                 Q <= (others => '0');
18              elsif rising_edge(clk) then
19                 Q <= d;
20              end if;
21        end process;
22  end description;
23
```

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab2/register32/register32 - register32 - [simulation/qsim/register32.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 0 ps Interval: 0 ps Start: 0 ps End: 0 ps

Name	Value at 0 ps
clk	B 0
clr	B 0
d	U 0
ld	B 1
Q	U X

0 ps 400.0 ns 800.0 ns 1.2 us 1.6 us 2.0 us 2.4 us 2.8 us 3.2 us 3.6 us 4.0 us 4.4 us 4.8 us 5.2 us 5.6 us 6.0 us 6.4 us 6.8 us 7.2 us 7.6 us 8.0 us 8.4 us 8.8 us 9.2 us 9.6 us 10.0 us

0 ps

d: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 50 51 52 53 54 55 56 57 58 59 70 71 72 73 74 75 76 77 78 79 30 31 32 33 34 35 36 37 38 39 30 31 32 33 34 35 36 37 38 39 99

Q: 0 2 4 6 8 10 12 14 16 18 0 40 42 44 46 48 50 52 54 56 58 0 80 82 84 86 88 90 92 94 96 98

0% 00:00:00

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab2/register32/register32 - register32 - [simulation/qsim/register32.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 172.0 ns | Interval: 172.0 ns | Start: 0 ps | End: 0 ps

	Name	Value at 0 ps
in	clk	B 0
in	clr	B 0
in	d	U 0
in	ld	B 1
out	Q	U 0

0 ps 400.0 ns 800.0 ns 1.2 us 1.6 us 2.0 us 2.4 us 2.8 us 3.2 us 3.6 us 4.0 us 4.4 us 4.8 us 5.2 us 5.6 us 6.0 us 6.4 us 6.8 us 7.2 us 7.6 us 8.0 us 8.4 us 8.8 us 9.2 us 9.6 us 10.0 us

0 ps

d: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 50 51 52 53 54 55 56 57 58 59 70 71 72 73 74 75 76 77 78 79 30 31 32 33 34 35 36 37 38 39 30 31 32 33 34 35 36 37 38 39

Q: 0 2 4 6 8 10 12 14 16 18 0 40 42 44 46 48 50 52 54 56 58 0 80 82 84 86 88 90 92 94 96 98

0% 00:00:00