```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity memoryModule is
6     port (
7        clk: in std_logic;
8        addr: in unsigned (7 downto 0);
9        data_in : in std_logic_vector(31 downto 0);
10       wen, en: in std_logic;
11       data_out: out std_logic_vector(31 downto 0));
12 end memoryModule;
13
14 architecture description of memoryModule is
15    type memory2D is array (7 downto 0) of std_logic_vector(31 downto 0);
16    signal memoryModuleArray : memory2D;
17       begin
18          process(clk,en,wen)
19             begin
20                if falling_edge(clk) then
21                   if (en = '1' and wen = '0') then
22                      data_out <= memoryModuleArray(to_integer(unsigned(addr)));
23                   elsif (en = '1' and wen = '1') then
24                      memoryModuleArray(to_integer(unsigned(addr))) <= data_in;
25                      data_out <= (others => '0');
26                   end if;
27                end if;
28                if en = '0' then
29                   data_out <= (others => '0');
30                end if;
31          end process;
32 end description;
33
34
```