```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   entity octal_bcd_conv is
7      port(
8         input_8 : in std_logic_vector(7 downto 0);
9         out_top4: out std_logic_vector(3 downto 0);
10        out_bot4 : out std_logic_vector(3 downto 0));
11  end octal_bcd_conv;
12
13  architecture behavior of octal_bcd_conv is
14     begin
15        process(input_8)
16           begin
17              out_top4 <= input_8(7 downto 4);
18              out_bot4 <= input_8(3 downto 0);
19        end process;
20  end behavior;
21
22
```