```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   entity Control_NEW is
4      port(
5            clk, mclk            :  in    std_logic;
6            enable               :  in    std_logic;
7            statusC, statusZ     :  in    std_logic;
8            INST                 :  in    std_logic_vector(31 downto 0);
9            A_Mux, B_Mux         :  out   std_logic;
10           IM_MUX1, REG_Mux     :  out   std_logic;
11           IM_MUX2, DATA_Mux    :  out   std_logic_vector(1 downto 0);
12           ALU_op               :  out   std_logic_vector(2 downto 0);
13           inc_PC, ld_PC        :  out   std_logic;
14           clr_IR               :  out   std_logic;
15           ld_IR                :  out   std_logic;
16           clr_A, clr_B, clr_C, clr_Z :  out   std_logic;
17           ld_A, ld_B, ld_C, ld_Z     :  out   std_logic;
18           T                    :  out   std_logic_vector(2 downto 0);
19           wen, en              :  out   std_logic
20        );
21  end Control_NEW;
22
23  architecture Behaviour of Control_NEW is
24     type state_type is (s0, t0, t1, t2);
25     signal y : state_type;
26     signal Inst_sig: std_logic_vector(3 downto 0);
27     signal Inst_sig2: std_logic_vector(3 downto 0);
28
29  begin
30     Inst_sig <= INST(31 DOWNTO 28);
31     Inst_sig2 <= INST(27 DOWNTO 24);
32     --STATE MACHINE--
33     process (clk, mclk, INST, statusC, statusZ, enable)
34     begin
35        if (enable = '0') then
36           y <= s0;
37        elsif (clk' event and clk = '1') then
38           case (y) is
39              when s0 => y <= t0;
40              when t0 => y <= t1;
41              when t1 => y <= t2;
42              when t2 => y <= t0;
43           end case;
44        end if;
45     end process;
46
47     process (y)
48     begin
49        case (y) is
50           when s0 =>      --IR <= M[INST]
51                 clr_IR      <= '0';
52                 ld_IR       <= '1';
53                 ld_PC       <= '0';
54                 inc_PC      <= '0';
55                 clr_A       <= '0';
56                 ld_A        <= '0';
57                 clr_B       <= '0';
58                 ld_B        <= '0';
59                 clr_C       <= '0';
60                 ld_C        <= '0';
61                 clr_Z       <= '0';
62                 ld_Z        <= '0';
```

```
63                ALU_op      <= "XXX";
64                en          <= 'X';
65                wen         <= 'X';
66                A_Mux       <= 'X';
67                B_Mux       <= 'X';
68                REG_Mux     <= 'X';
69                DATA_Mux    <= "00";
70                IM_MUX1     <= 'X';
71                IM_MUX2     <= "XX";
72          when t0 =>        --IR <= M[INST]
73                clr_IR      <= '0';
74                ld_IR       <= '1';
75                ld_PC       <= '0';
76                inc_PC      <= '0';
77                clr_A       <= '0';
78                ld_A        <= '0';
79                clr_B       <= '0';
80                ld_B        <= '0';
81                clr_C       <= '0';
82                ld_C        <= '0';
83                clr_Z       <= '0';
84                ld_Z        <= '0';
85                ALU_op      <= "XXX";
86                en          <= 'X';
87                wen         <= 'X';
88                A_Mux       <= 'X';
89                B_Mux       <= 'X';
90                REG_Mux     <= 'X';
91                DATA_Mux    <= "00";
92                IM_MUX1     <= 'X';
93                IM_MUX2     <= "XX";
94          when t1 =>        --PC <= PC + 4
95                clr_IR      <= '0';
96                ld_IR       <= '0';
97                ld_PC       <= '1';
98                inc_PC      <= '1';
99                clr_A       <= '0';
100               ld_A        <= '0';
101               clr_B       <= '0';
102               ld_B        <= '0';
103               clr_C       <= '0';
104               ld_C        <= '0';
105               clr_Z       <= '0';
106               ld_Z        <= '0';
107               ALU_op      <= "XXX";
108               en          <= 'X';
109               wen         <= 'X';
110               A_Mux       <= 'X';
111               B_Mux       <= 'X';
112               REG_Mux     <= 'X';
113               DATA_Mux    <= "XX";
114               IM_MUX1     <= 'X';
115               IM_MUX2     <= "XX";
116
117               case (Inst_sig) is      -- MIGHT NEED TO CHANGE PC INC
118
119                  when "0010" =>       --STA
120                        clr_IR      <= '0';
121                        ld_IR       <= '0';
122                        ld_PC       <= '1';
123                        inc_PC      <= '1';
124                        clr_A       <= '0';
```

```
125                     ld_A        <= '0';
126                     clr_B       <= '0';
127                     ld_B        <= '0';
128                     clr_C       <= '0';
129                     ld_C        <= '0';
130                     clr_Z       <= '0';
131                     ld_Z        <= '0';
132                     ALU_op      <= "XXX";
133                     en          <= '1';
134                     wen         <= '1';
135                     A_Mux       <= 'X';
136                     B_Mux       <= 'X';
137                     REG_Mux     <= '0';
138                     DATA_Mux    <= "XX";
139                     IM_MUX1     <= 'X';
140                     IM_MUX2     <= "XX";
141                 when "0011" =>      --STB
142                     clr_IR      <= '0';
143                     ld_IR       <= '0';
144                     ld_PC       <= '1';
145                     inc_PC      <= '1';
146                     clr_A       <= '0';
147                     ld_A        <= '0';
148                     clr_B       <= '0';
149                     ld_B        <= '0';
150                     clr_C       <= '0';
151                     ld_C        <= '0';
152                     clr_Z       <= '0';
153                     ld_Z        <= '0';
154                     ALU_op      <= "XXX";
155                     en          <= '1';
156                     wen         <= '1';
157                     A_Mux       <= 'X';
158                     B_Mux       <= 'X';
159                     REG_Mux     <= '1';
160                     DATA_Mux    <= "XX";
161                     IM_MUX1     <= 'X';
162                     IM_MUX2     <= "XX";
163                 when "1001" =>      --LDA
164                     clr_IR      <= '0';
165                     ld_IR       <= '0';
166                     ld_PC       <= '1';
167                     inc_PC      <= '1';
168                     clr_A       <= '0';
169                     ld_A        <= '1';
170                     clr_B       <= '0';
171                     ld_B        <= '0';
172                     clr_C       <= '0';
173                     ld_C        <= '0';
174                     clr_Z       <= '0';
175                     ld_Z        <= '0';
176                     ALU_op      <= "XXX";
177                     en          <= '1';
178                     wen         <= '0';
179                     A_Mux       <= '0';
180                     B_Mux       <= 'X';
181                     REG_Mux     <= 'X';
182                     DATA_Mux    <= "01";
183                     IM_MUX1     <= 'X';
184                     IM_MUX2     <= "XX";
185                 when "1010" =>      --LDB
186                     clr_IR      <= '0';
```

```
187                         ld_IR       <= '0';
188                         ld_PC       <= '1';
189                         inc_PC      <= '1';
190                         clr_A       <= '0';
191                         ld_A        <= '0';
192                         clr_B       <= '0';
193                         ld_B        <= '1';
194                         clr_C       <= '0';
195                         ld_C        <= '0';
196                         clr_Z       <= '0';
197                         ld_Z        <= '0';
198                         ALU_op      <= "XXX";
199                         en          <= '1';
200                         wen         <= '0';
201                         A_Mux       <= 'X';
202                         B_Mux       <= '0';
203                         REG_Mux     <= 'X';
204                         DATA_Mux    <= "01";
205                         IM_MUX1     <= 'X';
206                         IM_MUX2     <= "XX";
207                      when others =>
208                         clr_IR <= '0';
209                   end case;
210                when t2 =>
211                   case (Inst_sig) is
212                      when "0000" =>       --LDAI
213                         clr_IR      <= '0';
214                         ld_IR       <= '0';
215                         ld_PC       <= '0';
216                         inc_PC      <= '0';
217                         clr_A       <= '0';
218                         ld_A        <= '1';
219                         clr_B       <= '0';
220                         ld_B        <= '0';
221                         clr_C       <= '0';
222                         ld_C        <= '0';
223                         clr_Z       <= '0';
224                         ld_Z        <= '0';
225                         ALU_op      <= "XXX";
226                         en          <= 'X';
227                         wen         <= 'X';
228                         A_Mux       <= '1';
229                         B_Mux       <= 'X';
230                         REG_Mux     <= 'X';
231                         DATA_Mux    <= "XX";
232                         IM_MUX1     <= 'X';
233                         IM_MUX2     <= "XX";
234                      when "0001" =>       --LDBI
235                         clr_IR      <= '0';
236                         ld_IR       <= '0';
237                         ld_PC       <= '0';
238                         inc_PC      <= '0';
239                         clr_A       <= '0';
240                         ld_A        <= '0';
241                         clr_B       <= '0';
242                         ld_B        <= '1';
243                         clr_C       <= '0';
244                         ld_C        <= '0';
245                         clr_Z       <= '0';
246                         ld_Z        <= '0';
247                         ALU_op      <= "XXX";
248                         en          <= 'X';
```

```
249                     wen         <= 'X';
250                     A_Mux       <= 'X';
251                     B_Mux       <= '1';
252                     REG_Mux     <= 'X';
253                     DATA_Mux    <= "XX";
254                     IM_MUX1     <= 'X';
255                     IM_MUX2     <= "XX";
256                 when "0010" =>      --STA
257                     clr_IR      <= '0';
258                     ld_IR       <= '0';
259                     ld_PC       <= '0';
260                     inc_PC      <= '0';
261                     clr_A       <= '0';
262                     ld_A        <= '0';
263                     clr_B       <= '0';
264                     ld_B        <= '0';
265                     clr_C       <= '0';
266                     ld_C        <= '0';
267                     clr_Z       <= '0';
268                     ld_Z        <= '0';
269                     ALU_op      <= "XXX";
270                     en          <= '1';
271                     wen         <= '1';
272                     A_Mux       <= 'X';
273                     B_Mux       <= 'X';
274                     REG_Mux     <= '0';
275                     DATA_Mux    <= "XX";
276                     IM_MUX1     <= 'X';
277                     IM_MUX2     <= "XX";
278                 when "0011" =>      --STB
279                     clr_IR      <= '0';
280                     ld_IR       <= '0';
281                     ld_PC       <= '0';
282                     inc_PC      <= '0';
283                     clr_A       <= '0';
284                     ld_A        <= '0';
285                     clr_B       <= '0';
286                     ld_B        <= '0';
287                     clr_C       <= '0';
288                     ld_C        <= '0';
289                     clr_Z       <= '0';
290                     ld_Z        <= '0';
291                     ALU_op      <= "XXX";
292                     en          <= '1';
293                     wen         <= '1';
294                     A_Mux       <= 'X';
295                     B_Mux       <= 'X';
296                     REG_Mux     <= '1';
297                     DATA_Mux    <= "XX";
298                     IM_MUX1     <= 'X';
299                     IM_MUX2     <= "XX";
300                 when "1001" =>      --LDA
301                     clr_IR      <= '0';
302                     ld_IR       <= '0';
303                     ld_PC       <= '0';
304                     inc_PC      <= '0';
305                     clr_A       <= '0';
306                     ld_A        <= '1';
307                     clr_B       <= '0';
308                     ld_B        <= '0';
309                     clr_C       <= '0';
310                     ld_C        <= '0';
```

```
311                         clr_Z       <= '0';
312                         ld_Z        <= '0';
313                         ALU_op      <= "XXX";
314                         en          <= '1';
315                         wen         <= '0';
316                         A_Mux       <= '0';
317                         B_Mux       <= 'X';
318                         REG_Mux     <= 'X';
319                         DATA_Mux    <= "01";
320                         IM_MUX1     <= 'X';
321                         IM_MUX2     <= "XX";
322                   when "1010" =>        --LDB
323                         clr_IR      <= '0';
324                         ld_IR       <= '0';
325                         ld_PC       <= '0';
326                         inc_PC      <= '0';
327                         clr_A       <= '0';
328                         ld_A        <= '0';
329                         clr_B       <= '0';
330                         ld_B        <= '1';
331                         clr_C       <= '0';
332                         ld_C        <= '0';
333                         clr_Z       <= '0';
334                         ld_Z        <= '0';
335                         ALU_op      <= "XXX";
336                         en          <= '1';
337                         wen         <= '0';
338                         A_Mux       <= 'X';
339                         B_Mux       <= '0';
340                         REG_Mux     <= 'X';
341                         DATA_Mux    <= "01";
342                         IM_MUX1     <= 'X';
343                         IM_MUX2     <= "XX";
344                   when "0100" =>        --LUI
345                         clr_IR      <= '0';
346                         ld_IR       <= '0';
347                         ld_PC       <= '0';
348                         inc_PC      <= '0';
349                         clr_A       <= '0';
350                         ld_A        <= '1';
351                         clr_B       <= '1';
352                         ld_B        <= '0';
353                         clr_C       <= '0';
354                         ld_C        <= '0';
355                         clr_Z       <= '0';
356                         ld_Z        <= '0';
357                         ALU_op      <= "001";
358                         en          <= 'X';
359                         wen         <= 'X';
360                         A_Mux       <= '0';
361                         B_Mux       <= 'X';
362                         REG_Mux     <= 'X';
363                         DATA_Mux    <= "10";
364                         IM_MUX1     <= '1';
365                         IM_MUX2     <= "XX";
366                   when "0101" =>        --JMP
367                         clr_IR      <= '0';
368                         ld_IR       <= '0';
369                         ld_PC       <= '1';
370                         inc_PC      <= '0';
371                         clr_A       <= '0';
372                         ld_A        <= '0';
```

```
373                         clr_B       <= '0';
374                         ld_B        <= '0';
375                         clr_C       <= '0';
376                         ld_C        <= '0';
377                         clr_Z       <= '0';
378                         ld_Z        <= '0';
379                         ALU_op      <= "XXX";
380                         en          <= 'X';
381                         wen         <= 'X';
382                         A_Mux       <= 'X';
383                         B_Mux       <= 'X';
384                         REG_Mux     <= 'X';
385                         DATA_Mux    <= "XX";
386                         IM_MUX1     <= 'X';
387                         IM_MUX2     <= "XX";
388                   when "0111" =>
389                      case (Inst_sig2) is
390                         when "0000" => --ADD
391                               clr_IR      <= '0';
392                               ld_IR       <= '0';
393                               ld_PC       <= '0';
394                               inc_PC      <= '0';
395                               clr_A       <= '0';
396                               ld_A        <= '1';
397                               clr_B       <= '0';
398                               ld_B        <= '0';
399                               clr_C       <= '0';
400                               ld_C        <= '1';
401                               clr_Z       <= '0';
402                               ld_Z        <= '1';
403                               ALU_op      <= "010";
404                               en          <= 'X';
405                               wen         <= 'X';
406                               A_Mux       <= '0';
407                               B_Mux       <= 'X';
408                               REG_Mux     <= 'X';
409                               DATA_Mux    <= "10";
410                               IM_MUX1     <= '0';
411                               IM_MUX2     <= "00";
412                         when "0001" => --ADDI
413                               clr_IR      <= '0';
414                               ld_IR       <= '0';
415                               ld_PC       <= '0';
416                               inc_PC      <= '0';
417                               clr_A       <= '0';
418                               ld_A        <= '1';
419                               clr_B       <= '0';
420                               ld_B        <= '0';
421                               clr_C       <= '0';
422                               ld_C        <= '1';
423                               clr_Z       <= '0';
424                               ld_Z        <= '1';
425                               ALU_op      <= "010";
426                               en          <= 'X';
427                               wen         <= 'X';
428                               A_Mux       <= '0';
429                               B_Mux       <= 'X';
430                               REG_Mux     <= 'X';
431                               DATA_Mux    <= "10";
432                               IM_MUX1     <= '0';
433                               IM_MUX2     <= "01";
434                         when "0010" => --SUB
```

```
435                         clr_IR      <= '0';
436                         ld_IR       <= '0';
437                         ld_PC       <= '0';
438                         inc_PC      <= '0';
439                         clr_A       <= '0';
440                         ld_A        <= '1';
441                         clr_B       <= '0';
442                         ld_B        <= '0';
443                         clr_C       <= '0';
444                         ld_C        <= '1';
445                         clr_Z       <= '0';
446                         ld_Z        <= '1';
447                         ALU_op      <= "110";
448                         en          <= 'X';
449                         wen         <= 'X';
450                         A_Mux       <= '0';
451                         B_Mux       <= 'X';
452                         REG_Mux     <= 'X';
453                         DATA_Mux    <= "10";
454                         IM_MUX1     <= '0';
455                         IM_MUX2     <= "00";
456                     when "0011" => --INCA
457                         clr_IR      <= '0';
458                         ld_IR       <= '0';
459                         ld_PC       <= '0';
460                         inc_PC      <= '0';
461                         clr_A       <= '0';
462                         ld_A        <= '1';
463                         clr_B       <= '0';
464                         ld_B        <= '0';
465                         clr_C       <= '0';
466                         ld_C        <= '1';
467                         clr_Z       <= '0';
468                         ld_Z        <= '1';
469                         ALU_op      <= "010";
470                         en          <= 'X';
471                         wen         <= 'X';
472                         A_Mux       <= '0';
473                         B_Mux       <= 'X';
474                         REG_Mux     <= 'X';
475                         DATA_Mux    <= "10";
476                         IM_MUX1     <= '0';
477                         IM_MUX2     <= "10";
478                     when "0100" => --ROL
479                         clr_IR      <= '0';
480                         ld_IR       <= '0';
481                         ld_PC       <= '0';
482                         inc_PC      <= '0';
483                         clr_A       <= '0';
484                         ld_A        <= '1';
485                         clr_B       <= '0';
486                         ld_B        <= '0';
487                         clr_C       <= '0';
488                         ld_C        <= '1';
489                         clr_Z       <= '0';
490                         ld_Z        <= '1';
491                         ALU_op      <= "100";
492                         en          <= 'X';
493                         wen         <= 'X';
494                         A_Mux       <= '0';
495                         B_Mux       <= 'X';
496                         REG_Mux     <= 'X';
```

```
497                         DATA_Mux    <= "10";
498                         IM_MUX1     <= '0';
499                         IM_MUX2     <= "XX";
500                     when "0101" => --CLRA
501                         clr_IR      <= '0';
502                         ld_IR       <= '0';
503                         ld_PC       <= '0';
504                         inc_PC      <= '0';
505                         clr_A       <= '1';
506                         ld_A        <= '0';
507                         clr_B       <= '0';
508                         ld_B        <= '0';
509                         clr_C       <= '0';
510                         ld_C        <= '0';
511                         clr_Z       <= '0';
512                         ld_Z        <= '0';
513                         ALU_op      <= "XXX";
514                         en          <= 'X';
515                         wen         <= 'X';
516                         A_Mux       <= 'X';
517                         B_Mux       <= 'X';
518                         REG_Mux     <= 'X';
519                         DATA_Mux    <= "XX";
520                         IM_MUX1     <= 'X';
521                         IM_MUX2     <= "XX";
522                     when "0110" => --CLRB
523                         clr_IR      <= '0';
524                         ld_IR       <= '0';
525                         ld_PC       <= '0';
526                         inc_PC      <= '0';
527                         clr_A       <= '0';
528                         ld_A        <= '0';
529                         clr_B       <= '1';
530                         ld_B        <= '0';
531                         clr_C       <= '0';
532                         ld_C        <= '0';
533                         clr_Z       <= '0';
534                         ld_Z        <= '0';
535                         ALU_op      <= "XXX";
536                         en          <= 'X';
537                         wen         <= 'X';
538                         A_Mux       <= 'X';
539                         B_Mux       <= 'X';
540                         REG_Mux     <= 'X';
541                         DATA_Mux    <= "XX";
542                         IM_MUX1     <= 'X';
543                         IM_MUX2     <= "XX";
544                     when "0111" => --CLRC
545                         clr_IR      <= '0';
546                         ld_IR       <= '0';
547                         ld_PC       <= '0';
548                         inc_PC      <= '0';
549                         clr_A       <= '0';
550                         ld_A        <= '0';
551                         clr_B       <= '0';
552                         ld_B        <= '0';
553                         clr_C       <= '1';
554                         ld_C        <= '0';
555                         clr_Z       <= '0';
556                         ld_Z        <= '0';
557                         ALU_op      <= "XXX";
558                         en          <= 'X';
```

```
559                     wen         <= 'X';
560                     A_Mux       <= 'X';
561                     B_Mux       <= 'X';
562                     REG_Mux     <= 'X';
563                     DATA_Mux    <= "XX";
564                     IM_MUX1     <= 'X';
565                     IM_MUX2     <= "XX";
566                 when "1000" => --CLRZ
567                     clr_IR      <= '0';
568                     ld_IR       <= '0';
569                     ld_PC       <= '0';
570                     inc_PC      <= '0';
571                     clr_A       <= '0';
572                     ld_A        <= '0';
573                     clr_B       <= '0';
574                     ld_B        <= '0';
575                     clr_C       <= '0';
576                     ld_C        <= '0';
577                     clr_Z       <= '1';
578                     ld_Z        <= '0';
579                     ALU_op      <= "XXX";
580                     en          <= 'X';
581                     wen         <= 'X';
582                     A_Mux       <= 'X';
583                     B_Mux       <= 'X';
584                     REG_Mux     <= 'X';
585                     DATA_Mux    <= "XX";
586                     IM_MUX1     <= 'X';
587                     IM_MUX2     <= "XX";
588                 when "1001" => --ANDI
589                     clr_IR      <= '0';
590                     ld_IR       <= '0';
591                     ld_PC       <= '0';
592                     inc_PC      <= '0';
593                     clr_A       <= '0';
594                     ld_A        <= '1';
595                     clr_B       <= '0';
596                     ld_B        <= '0';
597                     clr_C       <= '0';
598                     ld_C        <= '1';
599                     clr_Z       <= '0';
600                     ld_Z        <= '1';
601                     ALU_op      <= "000";
602                     en          <= 'X';
603                     wen         <= 'X';
604                     A_Mux       <= '0';
605                     B_Mux       <= 'X';
606                     REG_Mux     <= 'X';
607                     DATA_Mux    <= "10";
608                     IM_MUX1     <= '0';
609                     IM_MUX2     <= "01";
610                     --
611                 when "1011" =>    --AND
612                     clr_IR      <= '0';
613                     ld_IR       <= '0';
614                     ld_PC       <= '0';
615                     inc_PC      <= '0';
616                     clr_A       <= '0';
617                     ld_A        <= '1';
618                     clr_B       <= '0';
619                     ld_B        <= '0';
620                     clr_C       <= '0';
```

```
621                     ld_C        <= '1';
622                     clr_Z       <= '0';
623                     ld_Z        <= '1';
624                     ALU_op      <= "000";
625                     en          <= 'X';
626                     wen         <= 'X';
627                     A_Mux       <= '0';
628                     B_Mux       <= 'X';
629                     REG_Mux     <= 'X';
630                     DATA_Mux    <= "10";
631                     IM_MUX1     <= '0';
632                     IM_MUX2     <= "00";
633                     --
634                 when "1101" => --ORI
635                     clr_IR      <= '0';
636                     ld_IR       <= '0';
637                     ld_PC       <= '0';
638                     inc_PC      <= '0';
639                     clr_A       <= '0';
640                     ld_A        <= '1';
641                     clr_B       <= '0';
642                     ld_B        <= '0';
643                     clr_C       <= '0';
644                     ld_C        <= '1';
645                     clr_Z       <= '0';
646                     ld_Z        <= '1';
647                     ALU_op      <= "001";
648                     en          <= 'X';
649                     wen         <= 'X';
650                     A_Mux       <= '0';
651                     B_Mux       <= 'X';
652                     REG_Mux     <= 'X';
653                     DATA_Mux    <= "10";
654                     IM_MUX1     <= '0';
655                     IM_MUX2     <= "01";
656                 when "1110" => --DECA
657                     clr_IR      <= '0';
658                     ld_IR       <= '0';
659                     ld_PC       <= '0';
660                     inc_PC      <= '0';
661                     clr_A       <= '0';
662                     ld_A        <= '1';
663                     clr_B       <= '0';
664                     ld_B        <= '0';
665                     clr_C       <= '0';
666                     ld_C        <= '1';
667                     clr_Z       <= '0';
668                     ld_Z        <= '1';
669                     ALU_op      <= "110";
670                     en          <= 'X';
671                     wen         <= 'X';
672                     A_Mux       <= '0';
673                     B_Mux       <= 'X';
674                     REG_Mux     <= 'X';
675                     DATA_Mux    <= "10";
676                     IM_MUX1     <= '0';
677                     IM_MUX2     <= "10";
678                 when "1111" => --ROR
679                     clr_IR      <= '0';
680                     ld_IR       <= '0';
681                     ld_PC       <= '0';
682                     inc_PC      <= '0';
```

```
683                                 clr_A       <= '0';
684                                 ld_A        <= '1';
685                                 clr_B       <= '0';
686                                 ld_B        <= '0';
687                                 clr_C       <= '0';
688                                 ld_C        <= '1';
689                                 clr_Z       <= '0';
690                                 ld_Z        <= '1';
691                                 ALU_op      <= "101";
692                                 en          <= 'X';
693                                 wen         <= 'X';
694                                 A_Mux       <= '0';
695                                 B_Mux       <= 'X';
696                                 REG_Mux     <= 'X';
697                                 DATA_Mux    <= "10";
698                                 IM_MUX1     <= '0';
699                                 IM_MUX2     <= "XX";
700                              when others =>
701                                 clr_IR <= '0';
702                           end case;
703                        when others =>
704                           clr_IR <= '0';
705                  end case;
706            end case;
707         end process;
708      with y select
709         T <= "000" when s0,
710              "001" when t0,
711              "010" when t1,
712              "100" when t2,
713              "000" when others;
714   end Behaviour;
```