Date: June 27, 2020 alu8.vhd 1 library ieee; use ieee.std_logic_1164.all; use ieee.std_logic_arith.all; 3 use ieee.std_logic_unsigned.all; 5 use ieee.numeric_std.all; 7 entity alu8 is 8 port(9 a, b: in std_logic_vector(7 downto 0); 10 op: in std_logic_vector(2 downto 0); result: inout std_logic_vector(7 downto 0); 11 12 cout, zero: out std_logic); 13 end alu8; 14 15 architecture description of alu8 is 16 component adder8 is 17 port (18 cin, mode: in std_logic; 19 x, y: in std_logic_vector(7 downto 0); 20 s : out std_logic_vector(7 downto 0); 21 cout: out std_logic); 22 end component adder8; 23 signal addd: std_logic_vector(7 downto 0); 24 signal coutplus: std_logic; 25 signal shift: std_logic_vector(7 downto 0); 26 begin 27 muxadd: adder8 port map (op(2), op(2), a, b, addd, coutplus); 28 process (op) 29 begin 30 if op = "000" then 31 result <= a and b; elsif op = "001" then 32 33 result <= a or b; 34 elsif op = "010" then 35 result <= addd; 36 cout <= coutplus;</pre> elsif op = "110" then 37 38 result <= addd; 39 cout <= coutplus;</pre> 40 elsif op = "100" then 41 shift(0) <= a(7);42 $shift(7 downto 1) \le a(6 downto 0);$ 43 result <= shift; 44 elsif op = "101" then 45 shift(7) <= a(0);46 $shift(6 downto 0) \le a(7 downto 1);$ 47 result <= shift; 48 49 result <= (others => '0'); 50 end if; 51 if result = "00000000" then 52 53 zero <= '1'; 54 else 55 zero <= '0'; 56 end if; 57 58 end process; 59 60 end description; 61

62

1 of 1 Revision: alu8

Project: alu8