```vhdl
 1    library ieee;
 2    use ieee.std_logic_1164.all;
 3    use ieee.std_logic_arith.all;
 4    use ieee.std_logic_unsigned.all;
 5        entity mux2too1 is
 6        port(
 7            st : in std_logic;
 8            w0,w1 : in std_logic;
 9            cin : out std_logic
10            );
11            end mux2too1;
12
13    architecture description of mux2too1 is begin
14        --if (st = '0') then -- st if start
15            --cin <= '0';
16            --elsif(st = '1')then
17            --cin <= '1';
18        --end if; --st if end
19    end description;
20
```