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Date: June 26, 2020

COE 608: Computer Architecture and Design

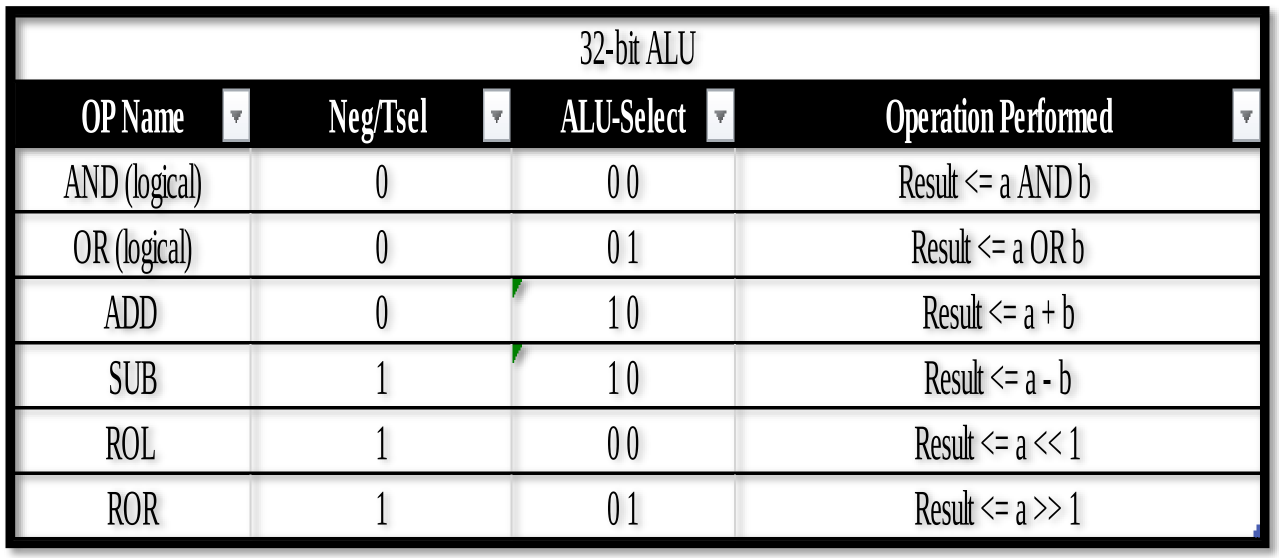
COE 608: Lab 3, Part 1 Report

Purpose

The purpose of this lab is to generate the components of a 32-bit ALU, with six different operations. The addition and subtraction units must be done in structural form of VHDL.

Design and Implementation

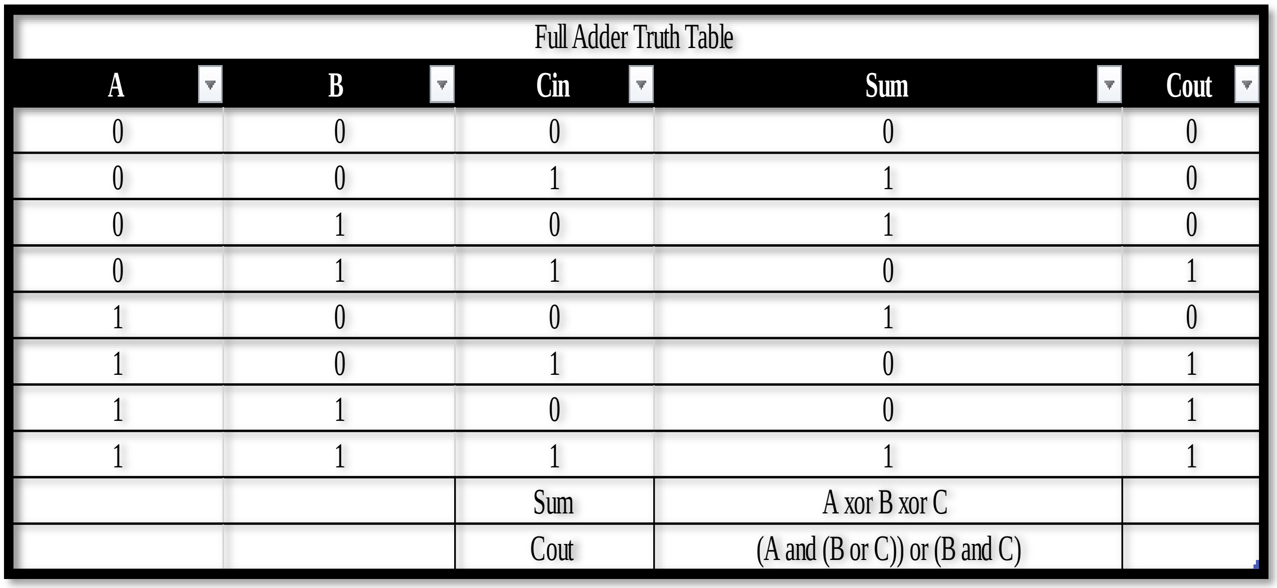
The goal of the 32-bit ALU is to perform the following operations:



32-bit ALU			
OP Name	Neg/Tsel	ALU-Select	Operation Performed
AND (logical)	0	0 0	Result <= a AND b
OR (logical)	0	0 1	Result <= a OR b
ADD	0	1 0	Result <= a + b
SUB	1	1 0	Result <= a - b
ROL	1	0 0	Result <= a << 1
ROR	1	0 1	Result <= a >> 1

Figure 1: ALU Operations

The first step is to create the adder, since it is not possible to use behavioral model in this lab to create the adder circuit.

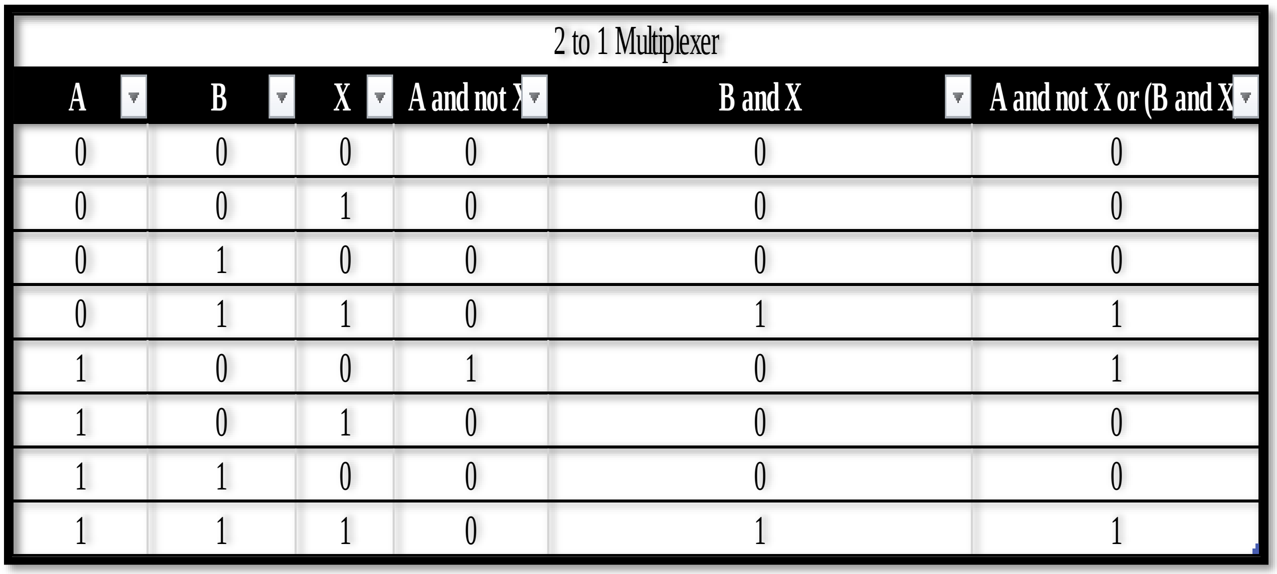


Full Adder Truth Table

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
		Sum	A xor B xor C	
		Cout	(A and (B or C)) or (B and C)	

Figure 2: Full Adder Circuit with logical functions

Next, the operation of the two-to-one multiplexer is illustrated below:

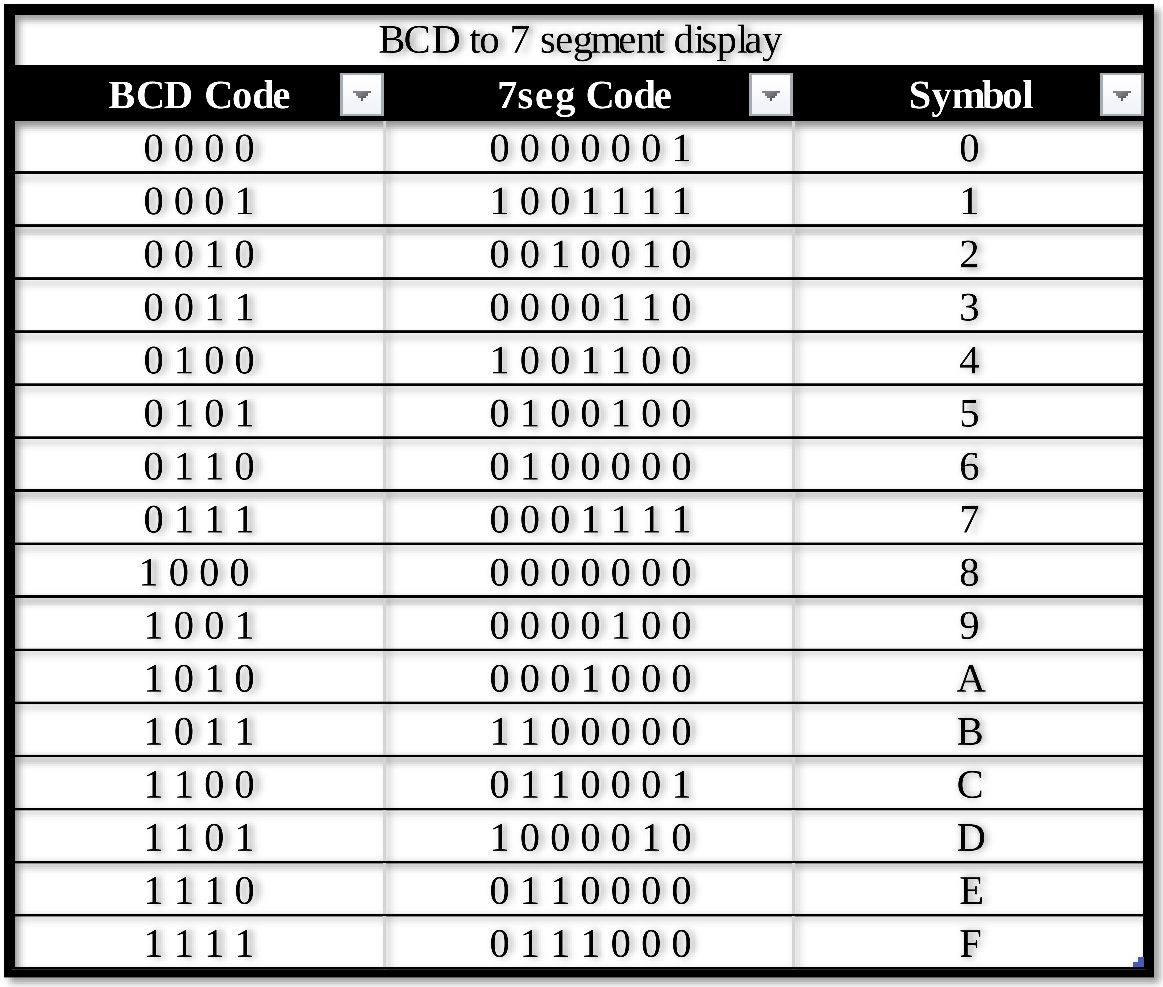


2 to 1 Multiplexer

A	B	X	A and not X	B and X	A and not X or (B and X
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

Figure 3: Two-to-one multiplexer

Next, the binary-coded-decimal to seven-segment converter is shown below. It is assumed that the seven-segment display is cathode-active.



BCD to 7 segment display

BCD Code	7seg Code	Symbol
0 0 0 0	0 0 0 0 0 0 1	0
0 0 0 1	1 0 0 1 1 1 1	1
0 0 1 0	0 0 1 0 0 1 0	2
0 0 1 1	0 0 0 0 1 1 0	3
0 1 0 0	1 0 0 1 1 0 0	4
0 1 0 1	0 1 0 0 1 0 0	5
0 1 1 0	0 1 0 0 0 0 0	6
0 1 1 1	0 0 0 1 1 1 1	7
1 0 0 0	0 0 0 0 0 0 0	8
1 0 0 1	0 0 0 0 1 0 0	9
1 0 1 0	0 0 0 1 0 0 0	A
1 0 1 1	1 1 0 0 0 0 0	B
1 1 0 0	0 1 1 0 0 0 1	C
1 1 0 1	1 0 0 0 0 1 0	D
1 1 1 0	0 1 1 0 0 0 0	E
1 1 1 1	0 1 1 1 0 0 0	F

Figure 4: BCD to 7 segment display Truth Table

<u>One-bit Adder: Functional and Timing Waveforms</u>

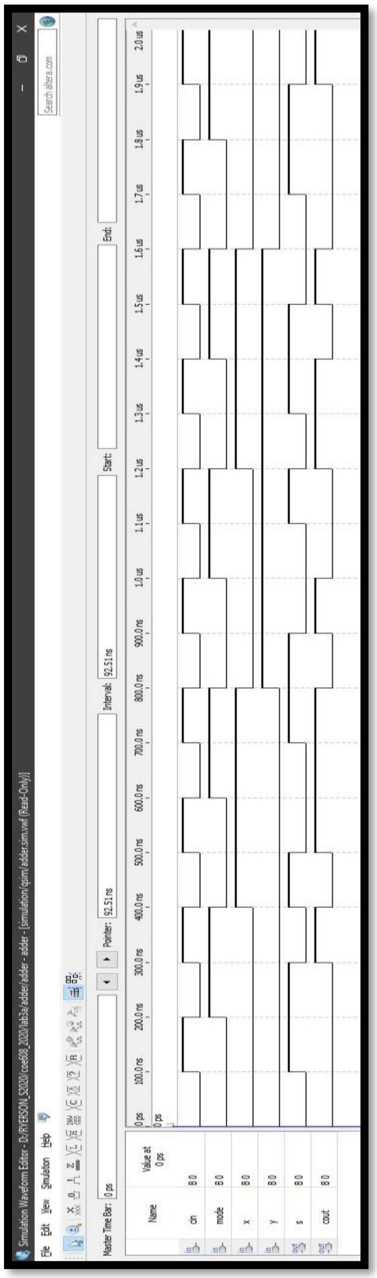


Figure 5: 1-bit Adder Functional Waveform

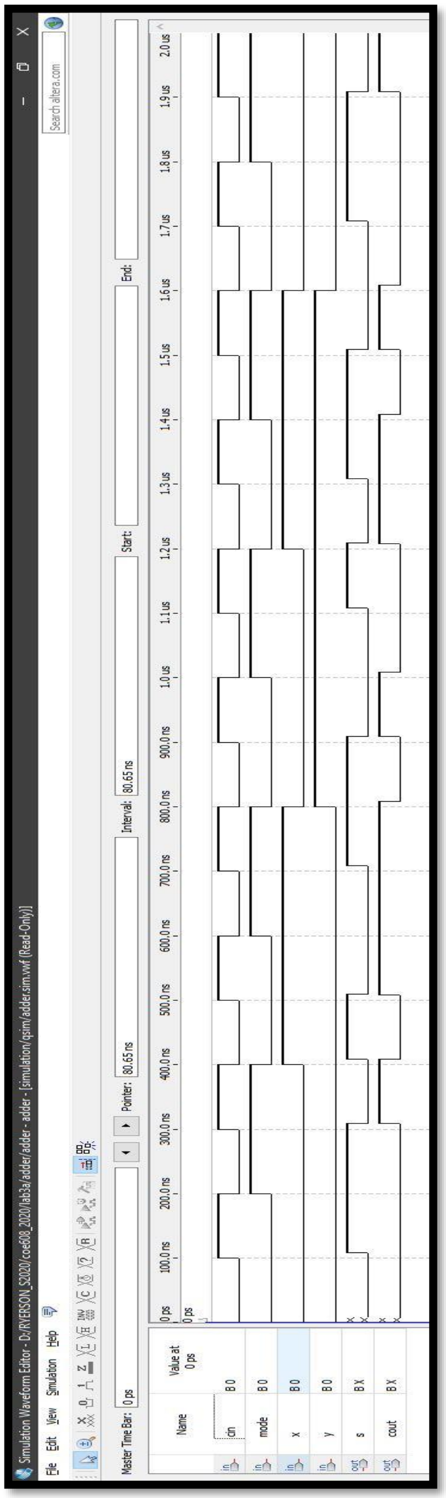


Figure 6: 1-bit Adder Timing Waveform

32-bit Adder: Functional and Timing Waveforms

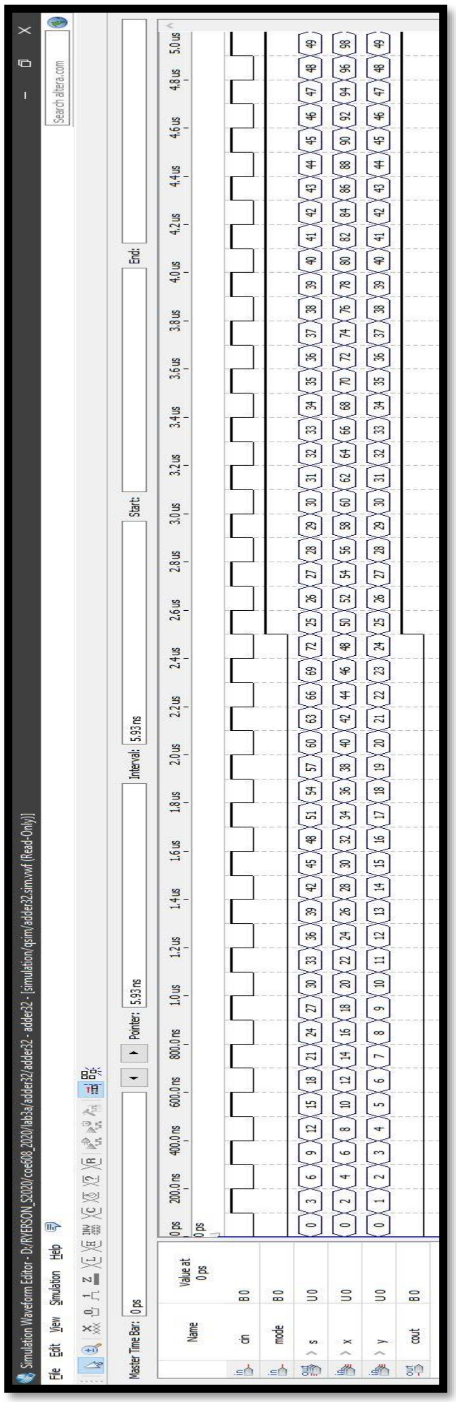

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/adder32/adder32 - adder32 - [simulation/qsim/adder32.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 5.93 ns
Interval: 5.93 ns
Start:
End:
Name
Value at 0 ps
cin B 0
mode B 0
s U 0
x U 0
y U 0
cout B 0

Figure 7: 32-bit Adder Functional Waveform

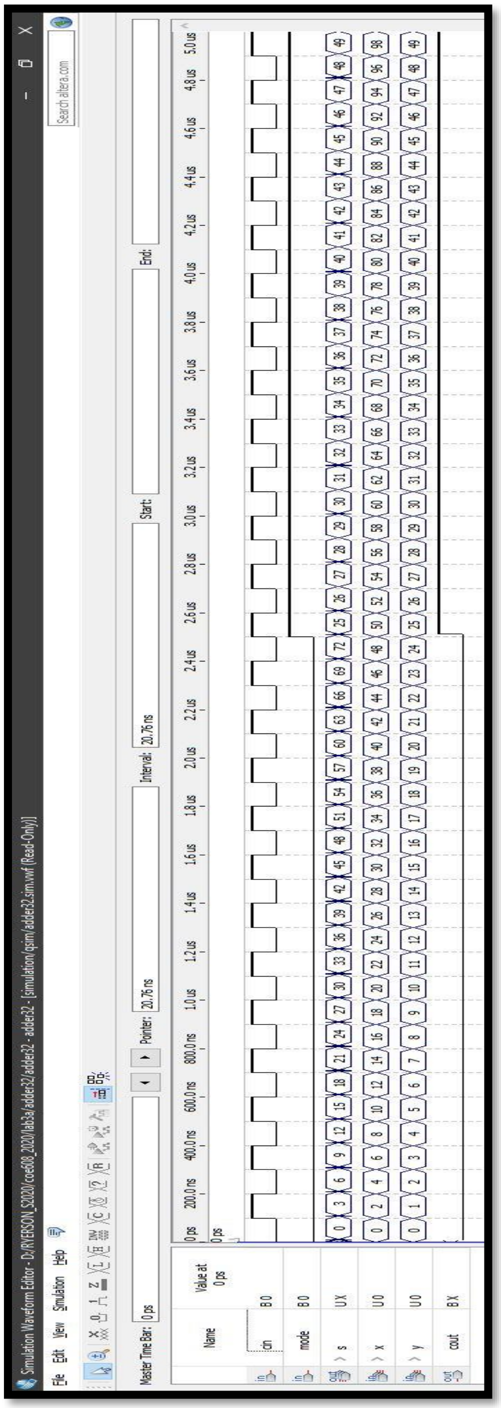

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/adder32/adder32 - adder32 - [simulation/qsim/adder32.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 20.76 ns
Interval: 20.76 ns
Start:
End:
Name
Value at 0 ps
cin B 0
mode B 0
s U X
x U 0
y U 0
cout B X

Figure 8: 32-bit Adder Timing Waveform

2 to 1 Multiplexer: Functional and Timing Waveforms

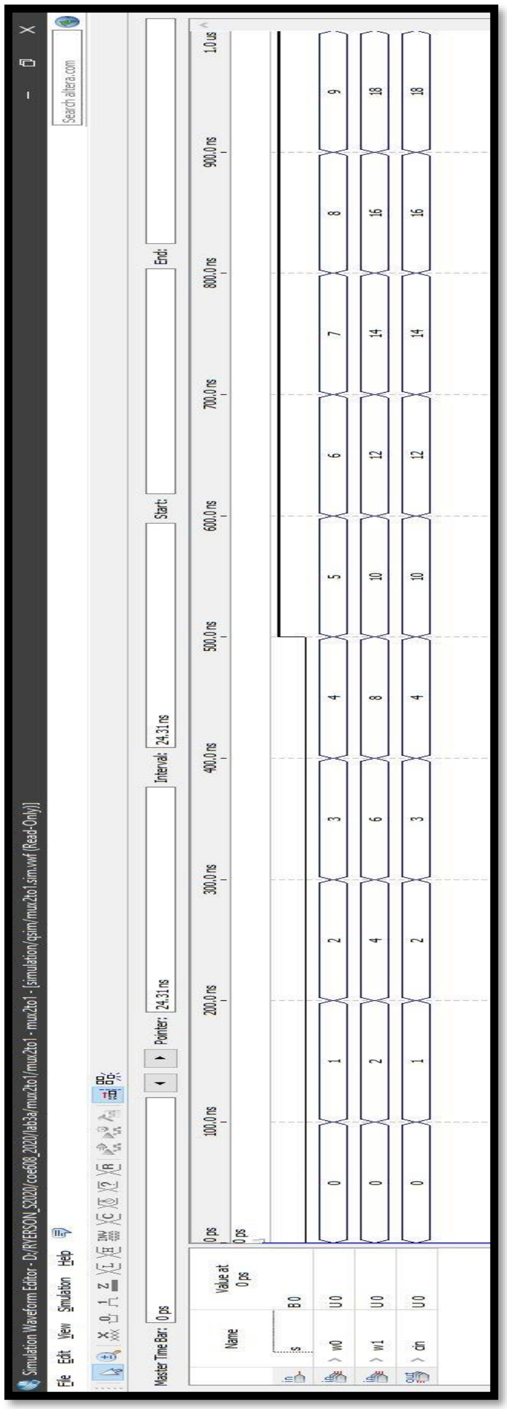


Figure 9: 2-to1 Multiplexer Functional Waveform

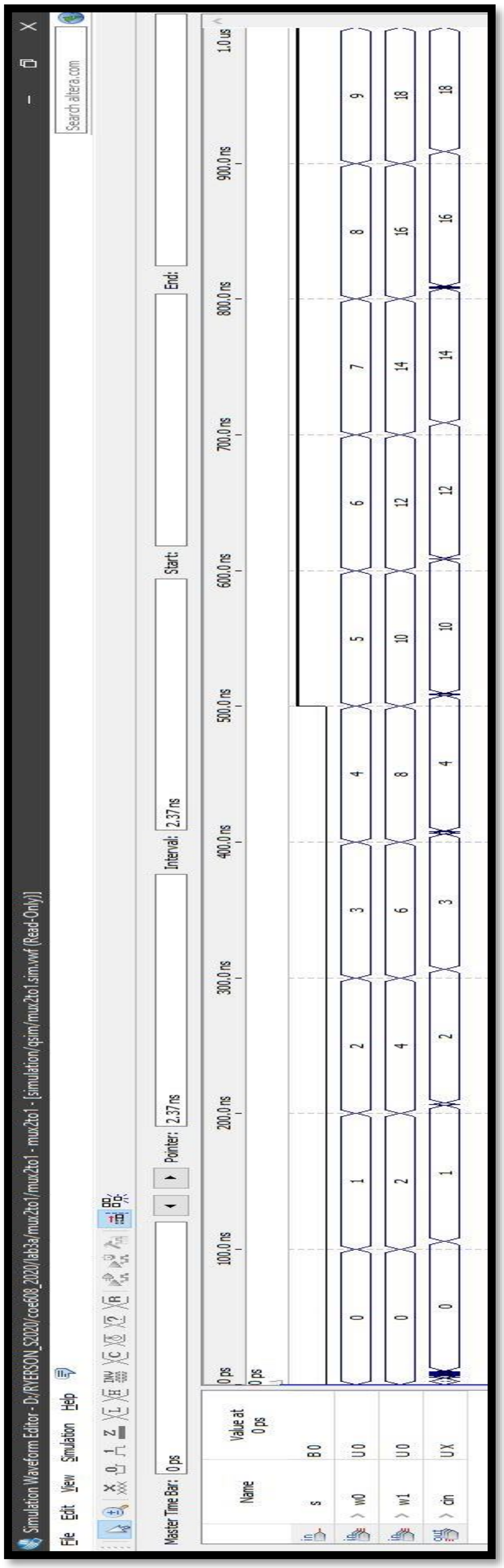


Figure 10: 2-to-1 Multiplexer Timing Waveform

32-bit ALU: Functional and Timing Waveforms

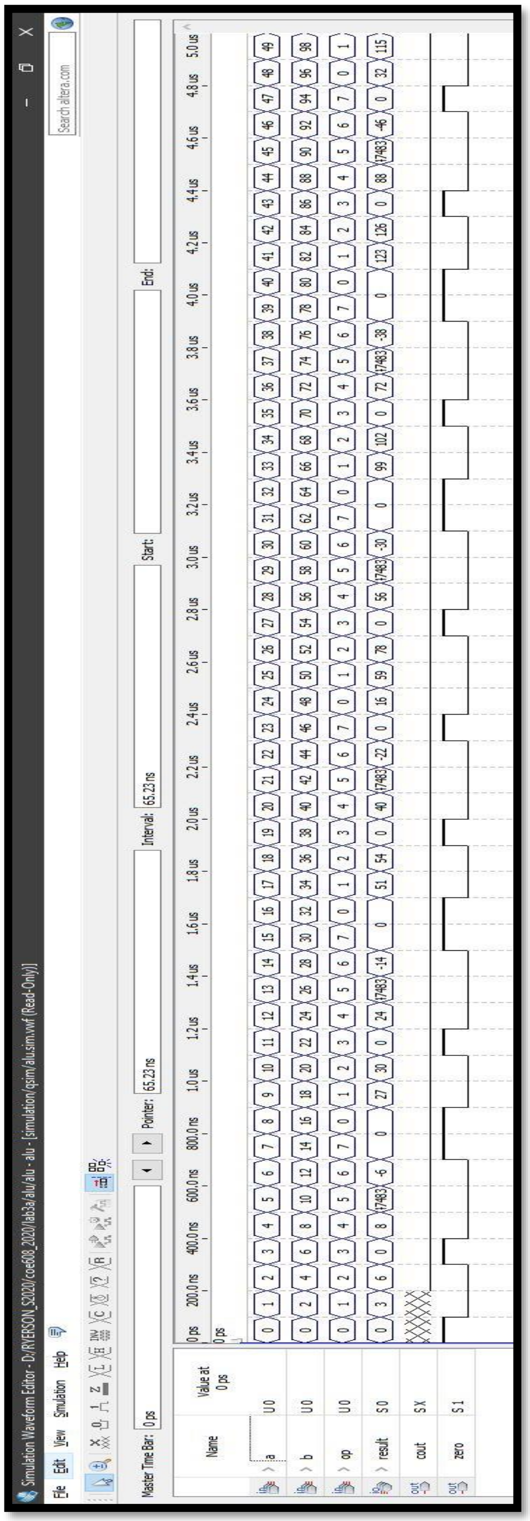


Figure 11: 32-bit ALU Functional Waveform

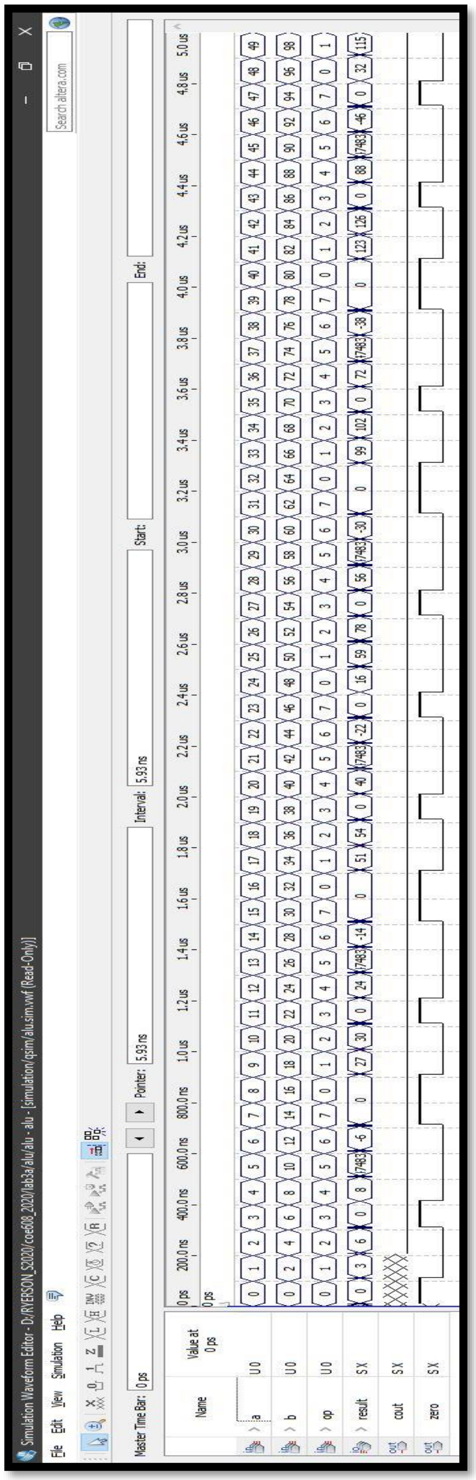

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/alu/alu - alu - [simulation/qsim/alu.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 5.93 ns
Interval: 5.93 ns
Start:
End:
Name
Value at 0 ps
a
b
op
result
cout
zero
U 0
U 0
U 0
S X
S X
S X

Figure 12: 32-bit ALU Timing Waveform

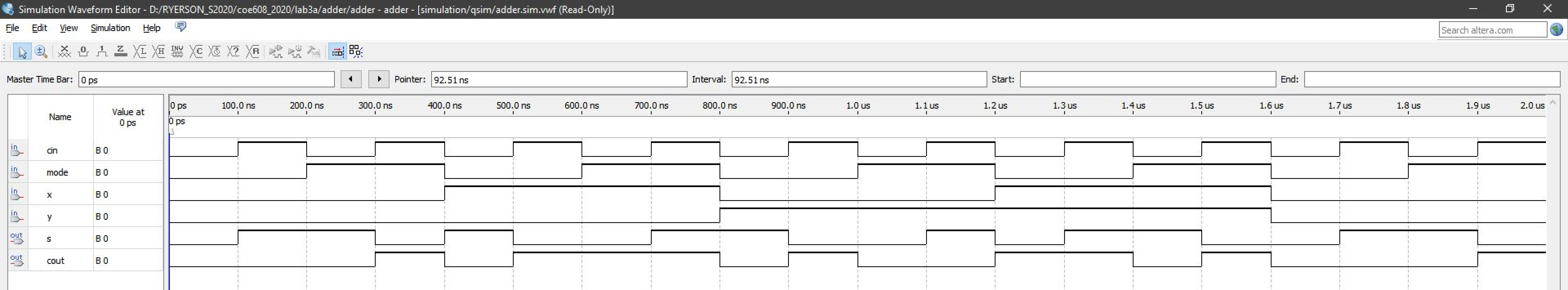
<u>Discussions and Conclusions</u>

All of the above devices work as expected. The worst-case delay of the 32-bit ALU is 1 ns, for most outputs. The longest delay occurs at the positive or negative signs of the output. The worst delay for the negative output symbol is 40 ns.

<u>Appendices: VHDL Codes for the ALU and other Supporting Devices</u>

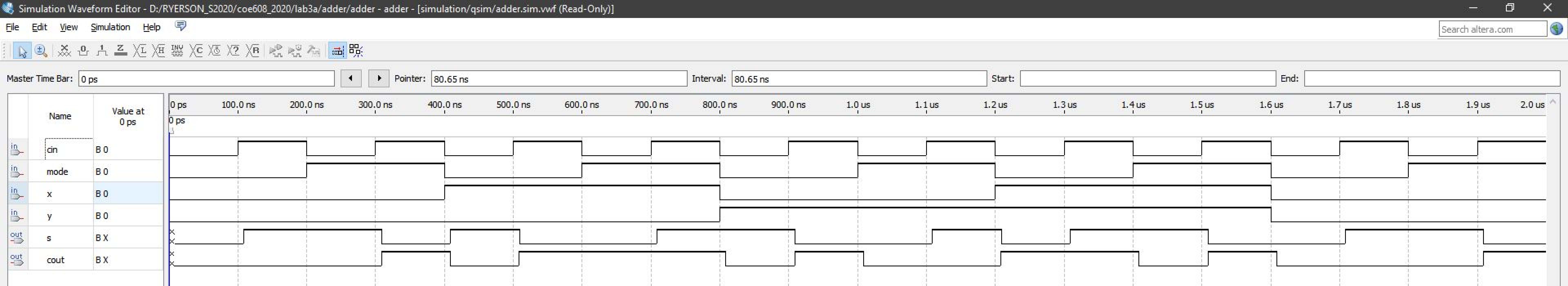
The files are attached as PDF to make this document easier to read.

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity adder is
   port (
      x, y: in std_logic;
      mode: in std_logic;
      cin : in std_logic;
      cout : out std_logic;
      s : out std_logic);
end adder;

architecture behavior of adder is
   signal temp : std_logic;
      begin
         process(mode)
            begin
               if (mode = '1') then
                  temp <= (y xor mode);
               else
                  temp <= y;
               end if;
            s <= (x xor temp xor cin) or (x and temp and cin);
            cout <= (x and temp) or (x and cin) or (cin and temp);
         end process;
end behavior;


```


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/adder/adder - adder - [simulation/qsim/adder.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 92.51 ns Interval: 92.51 ns Start: End:

Name	Value at 0 ps
cin	B 0
mode	B 0
x	B 0
y	B 0
s	B 0
cout	B 0



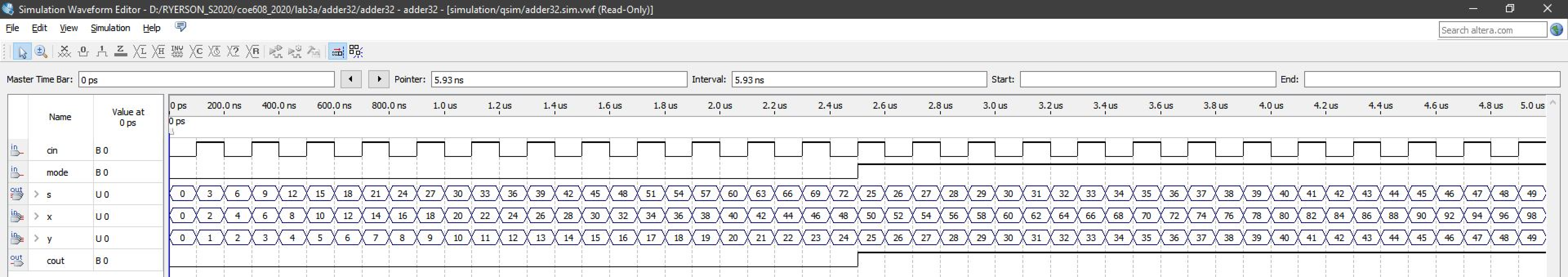
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/adder/adder - adder - [simulation/qsim/adder.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 80.65 ns Interval: 80.65 ns Start: End:

Name	Value at 0 ps
cin	B 0
mode	B 0
x	B 0
y	B 0
s	B X
cout	B X

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

ENTITY adder32 IS
   PORT(cin       :IN STD_LOGIC;
        mode      :IN STD_LOGIC; -- 1 = sub , 0 = add
        x         : in std_logic_vector(31 downto 0);
        y         : in std_logic_vector(31 downto 0);
        s         : out std_logic_vector(31 downto 0);
        cout      :OUT STD_LOGIC
   );
end adder32;

ARCHITECTURE description of adder32 IS
   SIGNAL c31,c30,c29,c28,c27,c26,c25,c24,c23,c22,c21,c20,c19,c18,c17,c16,c15,c14,c13,c12,
c11,c10,c9,c8,c7,c6,c5,c4,c3,c2,c1,c0 : STD_LOGIC;
   COMPONENT adder
      port(
      x : in std_logic;
      y : in std_logic;
      mode : in std_logic;
      cin : in std_logic;
      cout : out std_logic;
      s : out std_logic
      );
      END COMPONENT;
BEGIN
      --st0: adder port map (x(0), y(0), mode, cin, c1, s(0));
      st0: adder port map (x(0), y(0), mode, mode, c1, s(0));
      st1: adder port map (x(1), y(1), mode, c1, c2, s(1));
      st2: adder port map (x(2), y(2), mode, c2, c3, s(2));
      st3: adder port map (x(3), y(3), mode, c3, c4, s(3));
      st4: adder port map (x(4), y(4), mode, c4, c5, s(4));
      st5: adder port map (x(5), y(5), mode, c5, c6, s(5));
      st6: adder port map (x(6), y(6), mode, c6, c7, s(6));
      st7: adder port map (x(7), y(7), mode, c7, c8, s(7));
      st8: adder port map (x(8), y(8), mode, c8, c9, s(8));
      st9: adder port map (x(9), y(9), mode, c9, c10, s(9));
      st10: adder port map (x(10), y(10), mode, c10, c11, s(10));
      st11: adder port map (x(11), y(11), mode, c11, c12, s(11));
      st12: adder port map (x(12), y(12), mode, c12, c13, s(12));
      st13: adder port map (x(13), y(13), mode, c13, c14, s(13));
      st14: adder port map (x(14), y(14), mode, c14, c15, s(14));
      st15: adder port map (x(15), y(15), mode, c15, c16, s(15));
      st16: adder port map (x(16), y(16), mode, c16, c17, s(16));
      st17: adder port map (x(17), y(17), mode, c17, c18, s(17));
      st18: adder port map (x(18), y(18), mode, c18, c19, s(18));
      st19: adder port map (x(19), y(19), mode, c19, c20, s(19));
      st20: adder port map (x(20), y(20), mode, c20, c21, s(20));
      st21: adder port map (x(21), y(21), mode, c21, c22, s(21));
      st22: adder port map (x(22), y(22), mode, c22, c23, s(22));
      st23: adder port map (x(23), y(23), mode, c23, c24, s(23));
      st24: adder port map (x(24), y(24), mode, c24, c25, s(24));
      st25: adder port map (x(25), y(25), mode, c25, c26, s(25));
      st26: adder port map (x(26), y(26), mode, c26, c27, s(26));
      st27: adder port map (x(27), y(27), mode, c27, c28, s(27));
      st28: adder port map (x(28), y(28), mode, c28, c29, s(28));
      st29: adder port map (x(29), y(29), mode, c29, c30, s(29));
      st30: adder port map (x(30), y(30), mode, c30, c31, s(30));
      st31: adder port map (x(31), y(31), mode, c31, cout, s(31));
```

```
end description;

```

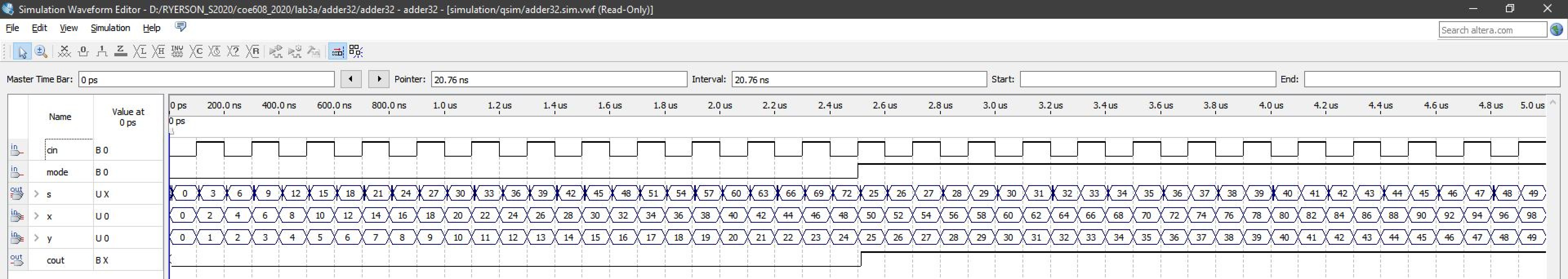


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/adder32/adder32 - adder32 - [simulation/qsim/adder32.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 5.93 ns Interval: 5.93 ns Start: End:

```
0 ps  200.0 ns  400.0 ns  600.0 ns  800.0 ns  1.0 us  1.2 us  1.4 us  1.6 us  1.8 us  2.0 us  2.2 us  2.4 us  2.6 us  2.8 us  3.0 us  3.2 us  3.4 us  3.6 us  3.8 us  4.0 us  4.2 us  4.4 us  4.6 us  4.8 us  5.0 us
```

Name	Value at 0 ps	
cin	B 0	
mode	B 0	
s	U 0	0 3 6 9 12 15 18 21 24 27 30 33 36 39 42 45 48 51 54 57 60 63 66 69 72 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
x	U 0	0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98
y	U 0	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
cout	B 0	

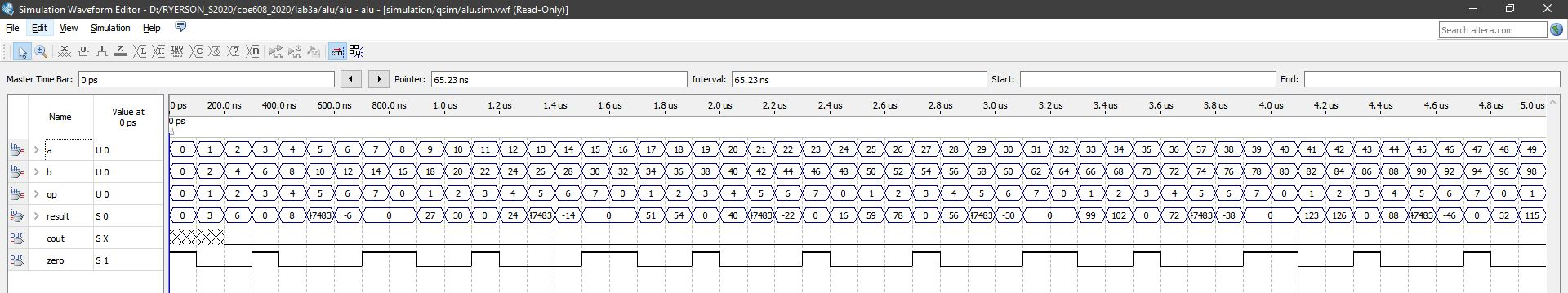


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/adder32/adder32 - adder32 - [simulation/qsim/adder32.sim.vwf (Read-Only)]

Master Time Bar: 0 ps
Pointer: 20.76 ns
Interval: 20.76 ns
Start:
End:

```
Name    Value at 0 ps
cin     B 0
mode    B 0
s       U X     0 3 6 9 12 15 18 21 24 27 30 33 36 39 42 45 48 51 54 57 60 63 66 69 72 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
x       U 0     0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98
y       U 0     0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
cout    B X
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
use ieee.numeric_std.all;

entity alu is
   port(
      a, b: in std_logic_vector(31 downto 0);
      op: in std_logic_vector(2 downto 0);
      result: inout std_logic_vector(31 downto 0);
      cout, zero: out std_logic);
end alu;

architecture description of alu is
   component adder32 is
      port(
         cin, mode: in std_logic;
         x, y: in std_logic_vector(31 downto 0);
         s : out std_logic_vector(31 downto 0);
         cout: out std_logic);
   end component adder32;
      signal addd: std_logic_vector(31 downto 0);
      signal coutplus: std_logic;
      signal shift: std_logic_vector(31 downto 0);
         begin
            muxadd: adder32 port map (op(2), op(2), a, b, addd, coutplus);
               process (op)
                  begin
                     if op = "000" then
                        result <= a and b;
                     elsif op = "001" then
                        result <= a or b;
                     elsif op = "010" then
                        result <= addd;
                        cout <= coutplus;
                     elsif op = "110" then
                        result <= addd;
                        cout <= coutplus;
                     elsif op = "100" then
                        shift(0) <= a(31);
                        shift(31 downto 1) <= a(30 downto 0);
                        result <= shift;
                     elsif op = "101" then
                        shift(31) <= a(0);
                        shift(30 downto 0) <= a(31 downto 1);
                        result <= shift;
                     else
                        result <= (others => '0');
                     end if;

                     if result = "00000000000000000000000000000000"  then
                        zero <= '1';
                     else
                        zero <= '0';
                     end if;

               end process;

end description;


```

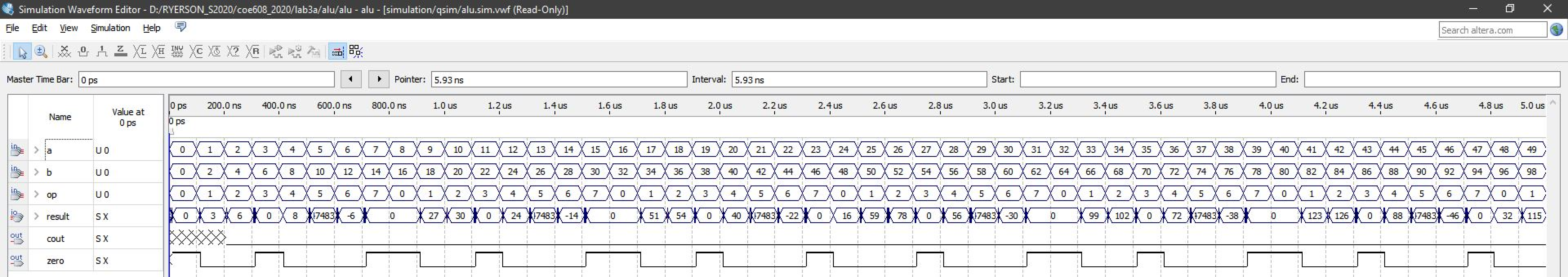

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/alu/alu - alu - [simulation/qsim/alu.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps   Pointer: 65.23 ns   Interval: 65.23 ns   Start: End:

```
Name     Value at 0 ps   0 ps  200.0 ns  400.0 ns  600.0 ns  800.0 ns  1.0 us  1.2 us  1.4 us  1.6 us  1.8 us  2.0 us  2.2 us  2.4 us  2.6 us  2.8 us  3.0 us  3.2 us  3.4 us  3.6 us  3.8 us  4.0 us  4.2 us  4.4 us  4.6 us  4.8 us  5.0 us
a        U 0    0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
b        U 0    0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98
op       U 0    0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1
result   S 0    0 3 6 0 8 !7483 -6 0 27 30 0 24 !7483 -14 0 51 54 0 40 !7483 -22 0 16 59 78 0 56 !7483 -30 0 99 102 0 72 !7483 -38 0 123 126 0 88 !7483 -46 0 32 115
cout     S X
zero     S 1
```

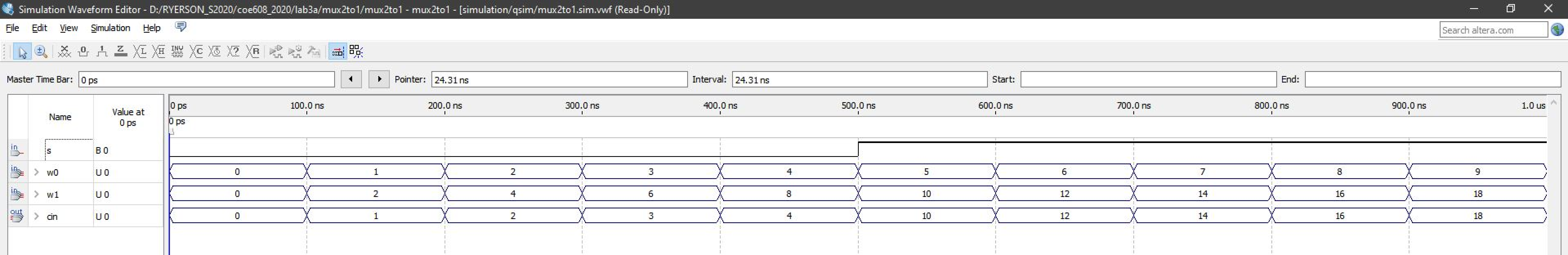


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/alu/alu - alu - [simulation/qsim/alu.sim.vwf (Read-Only)]

Master Time Bar: 0 ps   Pointer: 5.93 ns   Interval: 5.93 ns   Start: End:

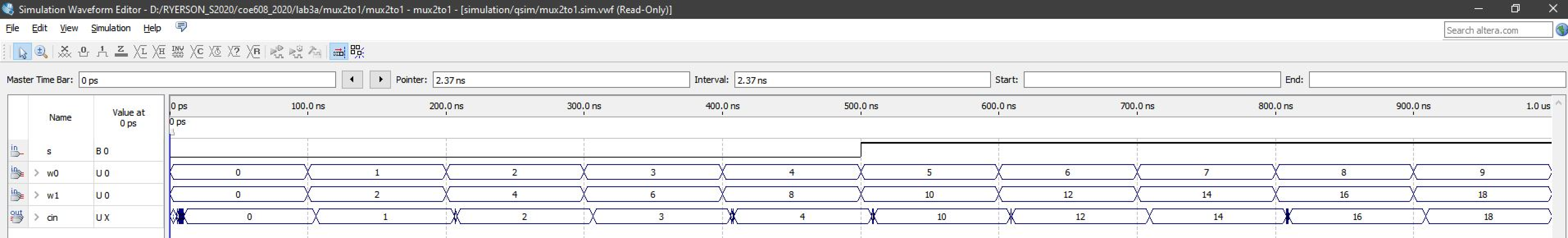
```
Name     Value at 0 ps
a        U 0
b        U 0
op       U 0
result   S X
cout     S X
zero     S X

Time:   0 ps  200.0 ns  400.0 ns  600.0 ns  800.0 ns  1.0 us  1.2 us  1.4 us  1.6 us  1.8 us  2.0 us  2.2 us  2.4 us  2.6 us  2.8 us  3.0 us  3.2 us  3.4 us  3.6 us  3.8 us  4.0 us  4.2 us  4.4 us  4.6 us  4.8 us  5.0 us

a       0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
b       0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98
op      0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1
result  0 3 6 0 8 |7483 -6 0 27 30 0 24 |7483 -14 0 51 54 0 40 |7483 -22 0 16 59 78 0 56 |7483 -30 0 99 102 0 72 |7483 -38 0 123 126 0 88 |7483 -46 0 32 115
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
   entity mux2too1 is
   port(
      st : in std_logic;
      w0,w1 : in std_logic;
      cin : out std_logic
      );
      end mux2too1;

architecture description of mux2too1 is begin
   --if (st = '0') then -- st if start
      --cin <= '0';
      --elsif(st = '1')then
      --cin <= '1';
   --end if; --st if end
end description;

```


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/mux2to1/mux2to1 - mux2to1 - [simulation/qsim/mux2to1.sim.vwf (Read-Only)]

Master Time Bar: 0 ps
Pointer: 24.31 ns
Interval: 24.31 ns
Start:
End:

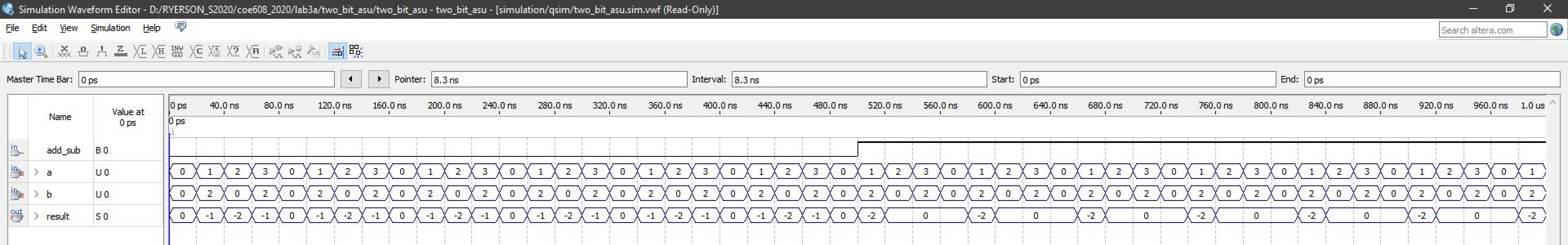
Name	Value at 0 ps	0 ps	100.0 ns	200.0 ns	300.0 ns	400.0 ns	500.0 ns	600.0 ns	700.0 ns	800.0 ns	900.0 ns
s	B 0	0	0	0	0	0	1	1	1	1	1
w0	U 0	0	1	2	3	4	5	6	7	8	9
w1	U 0	0	2	4	6	8	10	12	14	16	18
cin	U 0	0	1	2	3	4	10	12	14	16	18


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/mux2to1/mux2to1 - mux2to1 - [simulation/qsim/mux2to1.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 2.37 ns Interval: 2.37 ns Start: End:

Name	Value at 0 ps	0 ps	100.0 ns	200.0 ns	300.0 ns	400.0 ns	500.0 ns	600.0 ns	700.0 ns	800.0 ns	900.0 ns
s	B 0	0	0	0	0	0	1	1	1	1	1
w0	U 0	0	1	2	3	4	5	6	7	8	9
w1	U 0	0	2	4	6	8	10	12	14	16	18
cin	U X	0	1	2	3	4	10	12	14	16	18

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity two_bit_asu is
   port (
   a, b: in std_logic_vector(1 downto 0);
   add_sub: in std_logic;
   result: out std_logic_vector(1 downto 0));
end two_bit_asu;

architecture behavior of two_bit_asu is
   begin
      process(a,b,add_sub)
         begin
            if add_sub = '0' then --adding
               result <= a or b;
            elsif add_sub = '1' then --subtracting
               result <= (a or (not b))+ 1;
            end if;
      end process;
end behavior;
```


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/two_bit_asu/two_bit_asu - two_bit_asu - [simulation/qsim/two_bit_asu.sim.vwf (Read-Only)]

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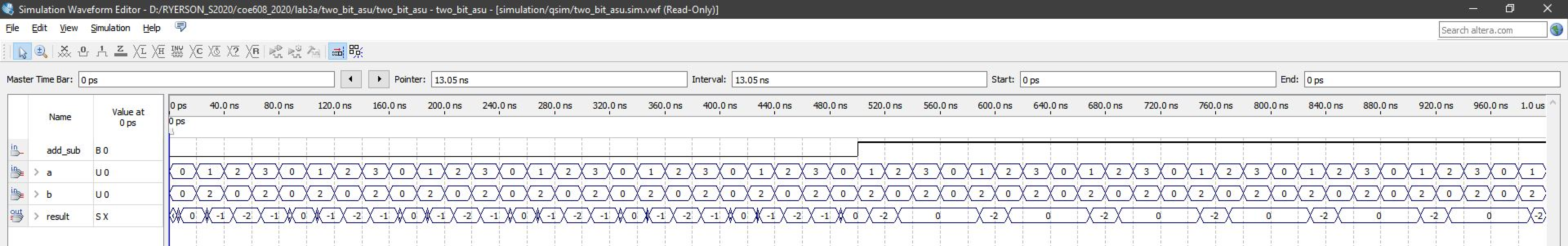
Master Time Bar: 0 ps
Pointer: 8.3 ns
Interval: 8.3 ns
Start: 0 ps
End: 0 ps

```
Name      Value at 0 ps   0 ps  40.0 ns  80.0 ns  120.0 ns  160.0 ns  200.0 ns  240.0 ns  280.0 ns  320.0 ns  360.0 ns  400.0 ns  440.0 ns  480.0 ns  520.0 ns  560.0 ns  600.0 ns  640.0 ns  680.0 ns  720.0 ns  760.0 ns  800.0 ns  840.0 ns  880.0 ns  920.0 ns  960.0 ns  1.0 us
add_sub   B 0
a         U 0     0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1
b         U 0     0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2
result    S 0     0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -2 0 -2 0 -2 0 -2 0 -2 0 -2 0 -2 0 -2
```



Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab3a/two_bit_asu/two_bit_asu - two_bit_asu - [simulation/qsim/two_bit_asu.sim.vwf (Read-Only)]

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 13.05 ns Interval: 13.05 ns Start: 0 ps End: 0 ps

Name	Value at 0 ps
add_sub	B 0
a	U 0
b	U 0
result	S X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us
0 ps
a: 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1
b: 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2
result: 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -1 -2 -1 0 -2 0 -2 0 -2 0 -2 0 -2 0 -2 0 -2