Ryerson University

Department of Electrical, Computer & Biomedical Engineering
Faculty of Engineering & Architectural Science

Programs: Computer Engineering

Course Number	**COE608**
Course Title	**Computer Organization and Architecture**
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Instructor	**Patrick Siddavaatam**

Lab Report No. 5

Lab Title	**CPU Control Unit Design**

Section No.	**011**
Group No.	
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Due Date	**10 August 2020**

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Date: July 30, 2020

COE 608: Computer Architecture and Design

COE 608: Lab 5 Report

Objective

The purpose of this lab was to create the Control Unit for the CPU.

Design and Implementation

The implementation of the CPU Control Unit is based on the idea of finite state machines. Finite state machines are the basis for the control unit since the change of state means that the instructions can change. Finite state machines have an initial starting state, followed by several other states. Each state has an input and an output. As the input changes, the output either remains in the original state, our present state, or it may change to the next state. Finite state machines can be either implemented using Mealy or Moore methods. The Mealy method depends on the present state and present input. The Moore finite state machine only depends on the present state. The efficiency of each finite state machine varies from situation to situation, and the needs of the designer and end-user requirements.

An operational decoder is also used to help determine the operation needed for each opcode of the MIPS ISA.

The finite state machine model from the VHDL code of the program is provided below:

See Figure 1: Finite State Machine of the CPU Control Unit.

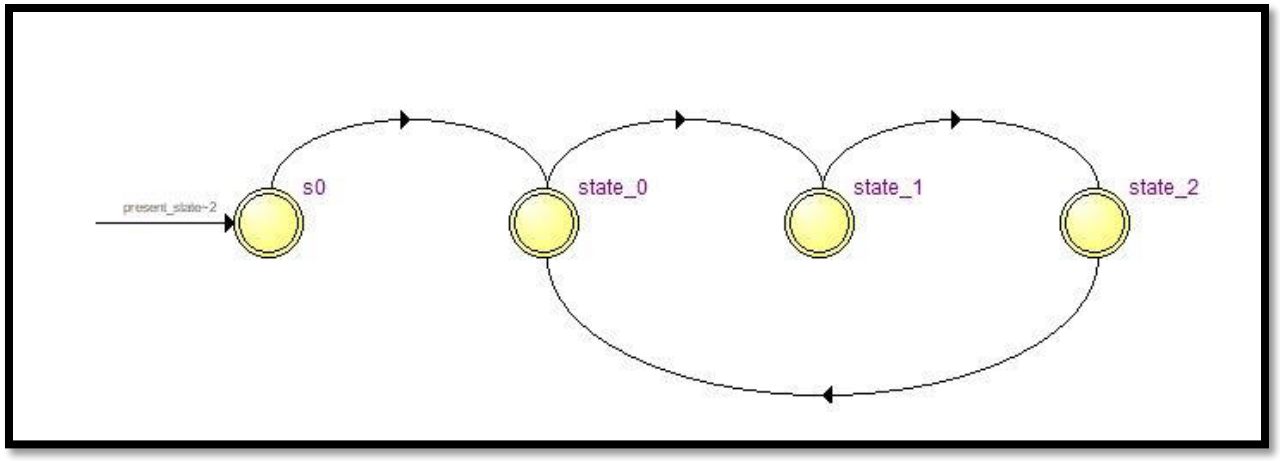


Figure 1: Finite State Machine of the CPU Control Unit

CPU Control Unit: Functional and Timing

The next two figures are the waveforms, both functional and timing of the final CPU control unit:

See Figure 2: CPU Control Unit Functional Waveform and Figure 3: CPU Control Unit Timing Waveform below.

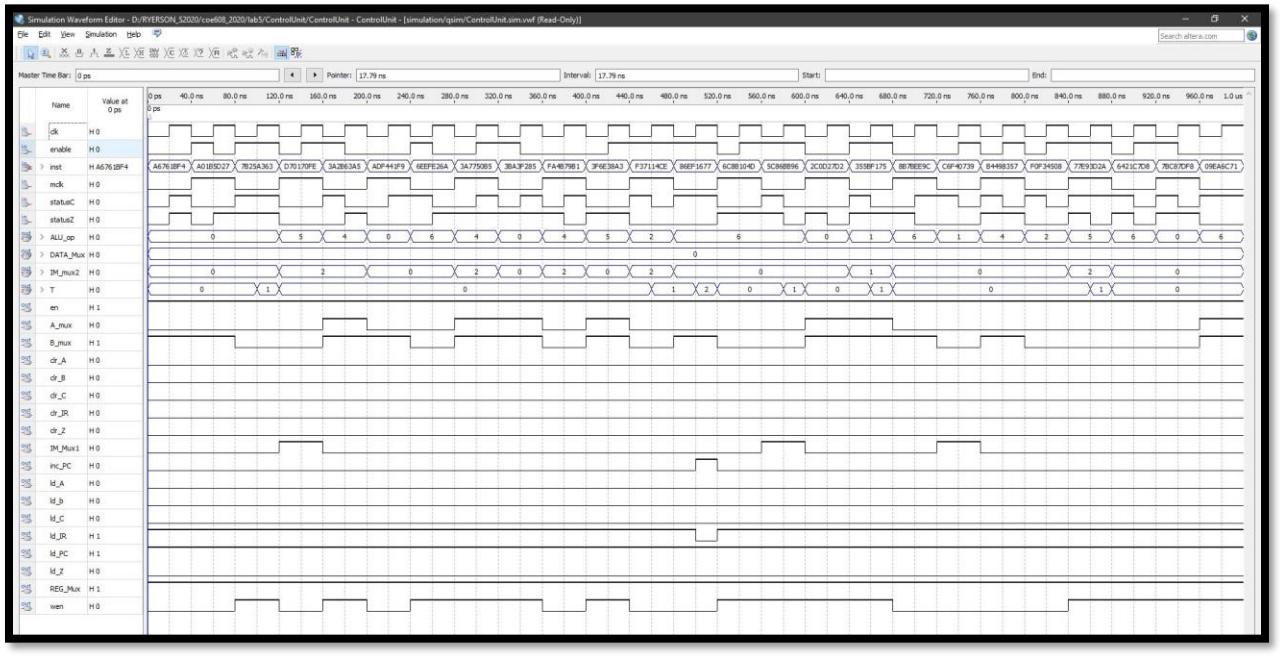


Figure 2: CPU Control Unit Functional Waveform

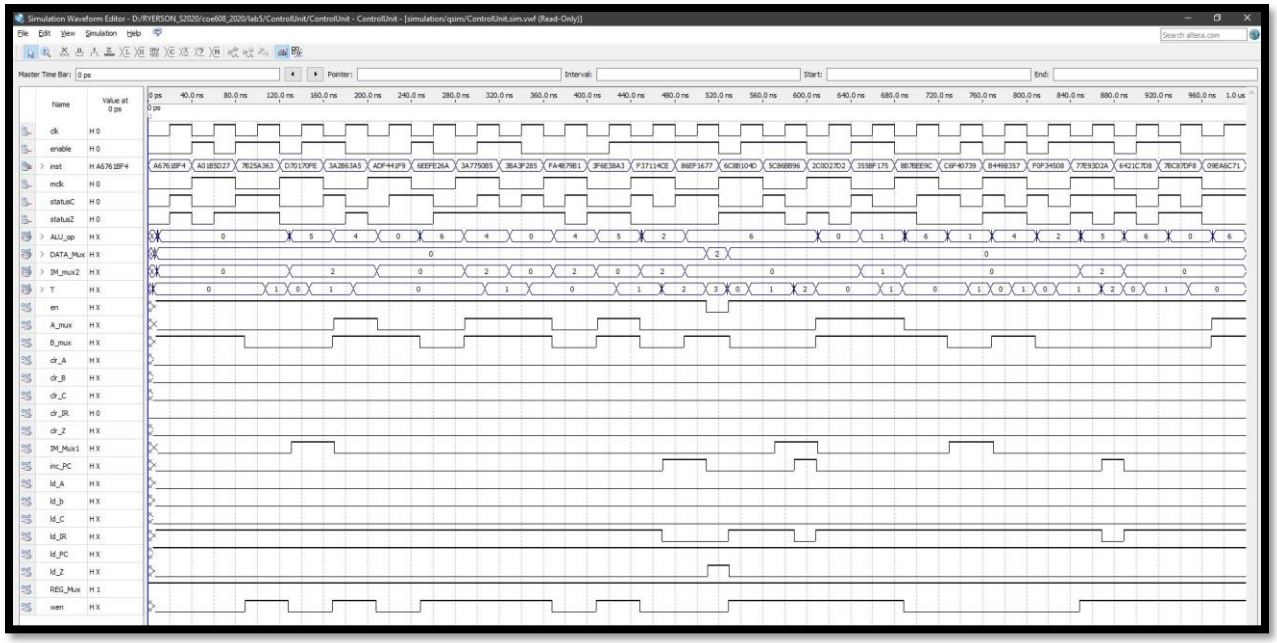


Figure 3: CPU Control Unit Timing Waveform

Appendix: VHDL Codes

The following appendix includes the VHDL code for the CPU control unit and the magnified screenshots of the waveforms for easier reading.

I also include the VHDL code by both of us—both Hadrian and Duan Wei Zhang. I have included the waveforms for the individual operations in a “table of contents” which is a screenshot of the order of the waveforms by order.

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   entity Control_NEW is
4      port(
5            clk, mclk            :  in    std_logic;
6            enable               :  in    std_logic;
7            statusC, statusZ     :  in    std_logic;
8            INST                 :  in    std_logic_vector(31 downto 0);
9            A_Mux, B_Mux         :  out   std_logic;
10           IM_MUX1, REG_Mux     :  out   std_logic;
11           IM_MUX2, DATA_Mux    :  out   std_logic_vector(1 downto 0);
12           ALU_op               :  out   std_logic_vector(2 downto 0);
13           inc_PC, ld_PC        :  out   std_logic;
14           clr_IR               :  out   std_logic;
15           ld_IR                :  out   std_logic;
16           clr_A, clr_B, clr_C, clr_Z :  out   std_logic;
17           ld_A, ld_B, ld_C, ld_Z     :  out   std_logic;
18           T                    :  out   std_logic_vector(2 downto 0);
19           wen, en              :  out   std_logic
20        );
21  end Control_NEW;
22
23  architecture Behaviour of Control_NEW is
24     type state_type is (s0, t0, t1, t2);
25     signal y : state_type;
26     signal Inst_sig: std_logic_vector(3 downto 0);
27     signal Inst_sig2: std_logic_vector(3 downto 0);
28
29  begin
30     Inst_sig <= INST(31 DOWNTO 28);
31     Inst_sig2 <= INST(27 DOWNTO 24);
32     --STATE MACHINE--
33     process (clk, mclk, INST, statusC, statusZ, enable)
34     begin
35        if (enable = '0') then
36           y <= s0;
37        elsif (clk' event and clk = '1') then
38           case (y) is
39              when s0 => y <= t0;
40              when t0 => y <= t1;
41              when t1 => y <= t2;
42              when t2 => y <= t0;
43           end case;
44        end if;
45     end process;
46
47     process (y)
48     begin
49        case (y) is
50           when s0 =>      --IR <= M[INST]
51                 clr_IR      <= '0';
52                 ld_IR       <= '1';
53                 ld_PC       <= '0';
54                 inc_PC      <= '0';
55                 clr_A       <= '0';
56                 ld_A        <= '0';
57                 clr_B       <= '0';
58                 ld_B        <= '0';
59                 clr_C       <= '0';
60                 ld_C        <= '0';
61                 clr_Z       <= '0';
62                 ld_Z        <= '0';
```

```
63                ALU_op      <= "XXX";
64                en          <= 'X';
65                wen         <= 'X';
66                A_Mux       <= 'X';
67                B_Mux       <= 'X';
68                REG_Mux     <= 'X';
69                DATA_Mux    <= "00";
70                IM_MUX1     <= 'X';
71                IM_MUX2     <= "XX";
72          when t0 =>        --IR <= M[INST]
73                clr_IR      <= '0';
74                ld_IR       <= '1';
75                ld_PC       <= '0';
76                inc_PC      <= '0';
77                clr_A       <= '0';
78                ld_A        <= '0';
79                clr_B       <= '0';
80                ld_B        <= '0';
81                clr_C       <= '0';
82                ld_C        <= '0';
83                clr_Z       <= '0';
84                ld_Z        <= '0';
85                ALU_op      <= "XXX";
86                en          <= 'X';
87                wen         <= 'X';
88                A_Mux       <= 'X';
89                B_Mux       <= 'X';
90                REG_Mux     <= 'X';
91                DATA_Mux    <= "00";
92                IM_MUX1     <= 'X';
93                IM_MUX2     <= "XX";
94          when t1 =>        --PC <= PC + 4
95                clr_IR      <= '0';
96                ld_IR       <= '0';
97                ld_PC       <= '1';
98                inc_PC      <= '1';
99                clr_A       <= '0';
100               ld_A        <= '0';
101               clr_B       <= '0';
102               ld_B        <= '0';
103               clr_C       <= '0';
104               ld_C        <= '0';
105               clr_Z       <= '0';
106               ld_Z        <= '0';
107               ALU_op      <= "XXX";
108               en          <= 'X';
109               wen         <= 'X';
110               A_Mux       <= 'X';
111               B_Mux       <= 'X';
112               REG_Mux     <= 'X';
113               DATA_Mux    <= "XX";
114               IM_MUX1     <= 'X';
115               IM_MUX2     <= "XX";
116
117               case (Inst_sig) is      -- MIGHT NEED TO CHANGE PC INC
118
119                  when "0010" =>       --STA
120                        clr_IR      <= '0';
121                        ld_IR       <= '0';
122                        ld_PC       <= '1';
123                        inc_PC      <= '1';
124                        clr_A       <= '0';
```

```
125                     ld_A        <= '0';
126                     clr_B       <= '0';
127                     ld_B        <= '0';
128                     clr_C       <= '0';
129                     ld_C        <= '0';
130                     clr_Z       <= '0';
131                     ld_Z        <= '0';
132                     ALU_op      <= "XXX";
133                     en          <= '1';
134                     wen         <= '1';
135                     A_Mux       <= 'X';
136                     B_Mux       <= 'X';
137                     REG_Mux     <= '0';
138                     DATA_Mux    <= "XX";
139                     IM_MUX1     <= 'X';
140                     IM_MUX2     <= "XX";
141                 when "0011" =>      --STB
142                     clr_IR      <= '0';
143                     ld_IR       <= '0';
144                     ld_PC       <= '1';
145                     inc_PC      <= '1';
146                     clr_A       <= '0';
147                     ld_A        <= '0';
148                     clr_B       <= '0';
149                     ld_B        <= '0';
150                     clr_C       <= '0';
151                     ld_C        <= '0';
152                     clr_Z       <= '0';
153                     ld_Z        <= '0';
154                     ALU_op      <= "XXX";
155                     en          <= '1';
156                     wen         <= '1';
157                     A_Mux       <= 'X';
158                     B_Mux       <= 'X';
159                     REG_Mux     <= '1';
160                     DATA_Mux    <= "XX";
161                     IM_MUX1     <= 'X';
162                     IM_MUX2     <= "XX";
163                 when "1001" =>      --LDA
164                     clr_IR      <= '0';
165                     ld_IR       <= '0';
166                     ld_PC       <= '1';
167                     inc_PC      <= '1';
168                     clr_A       <= '0';
169                     ld_A        <= '1';
170                     clr_B       <= '0';
171                     ld_B        <= '0';
172                     clr_C       <= '0';
173                     ld_C        <= '0';
174                     clr_Z       <= '0';
175                     ld_Z        <= '0';
176                     ALU_op      <= "XXX";
177                     en          <= '1';
178                     wen         <= '0';
179                     A_Mux       <= '0';
180                     B_Mux       <= 'X';
181                     REG_Mux     <= 'X';
182                     DATA_Mux    <= "01";
183                     IM_MUX1     <= 'X';
184                     IM_MUX2     <= "XX";
185                 when "1010" =>      --LDB
186                     clr_IR      <= '0';
```

```
187                         ld_IR       <= '0';
188                         ld_PC       <= '1';
189                         inc_PC      <= '1';
190                         clr_A       <= '0';
191                         ld_A        <= '0';
192                         clr_B       <= '0';
193                         ld_B        <= '1';
194                         clr_C       <= '0';
195                         ld_C        <= '0';
196                         clr_Z       <= '0';
197                         ld_Z        <= '0';
198                         ALU_op      <= "XXX";
199                         en          <= '1';
200                         wen         <= '0';
201                         A_Mux       <= 'X';
202                         B_Mux       <= '0';
203                         REG_Mux     <= 'X';
204                         DATA_Mux    <= "01";
205                         IM_MUX1     <= 'X';
206                         IM_MUX2     <= "XX";
207                      when others =>
208                         clr_IR <= '0';
209                   end case;
210                when t2 =>
211                   case (Inst_sig) is
212                      when "0000" =>       --LDAI
213                         clr_IR      <= '0';
214                         ld_IR       <= '0';
215                         ld_PC       <= '0';
216                         inc_PC      <= '0';
217                         clr_A       <= '0';
218                         ld_A        <= '1';
219                         clr_B       <= '0';
220                         ld_B        <= '0';
221                         clr_C       <= '0';
222                         ld_C        <= '0';
223                         clr_Z       <= '0';
224                         ld_Z        <= '0';
225                         ALU_op      <= "XXX";
226                         en          <= 'X';
227                         wen         <= 'X';
228                         A_Mux       <= '1';
229                         B_Mux       <= 'X';
230                         REG_Mux     <= 'X';
231                         DATA_Mux    <= "XX";
232                         IM_MUX1     <= 'X';
233                         IM_MUX2     <= "XX";
234                      when "0001" =>       --LDBI
235                         clr_IR      <= '0';
236                         ld_IR       <= '0';
237                         ld_PC       <= '0';
238                         inc_PC      <= '0';
239                         clr_A       <= '0';
240                         ld_A        <= '0';
241                         clr_B       <= '0';
242                         ld_B        <= '1';
243                         clr_C       <= '0';
244                         ld_C        <= '0';
245                         clr_Z       <= '0';
246                         ld_Z        <= '0';
247                         ALU_op      <= "XXX";
248                         en          <= 'X';
```

```
249                     wen         <= 'X';
250                     A_Mux       <= 'X';
251                     B_Mux       <= '1';
252                     REG_Mux     <= 'X';
253                     DATA_Mux    <= "XX";
254                     IM_MUX1     <= 'X';
255                     IM_MUX2     <= "XX";
256                 when "0010" =>      --STA
257                     clr_IR      <= '0';
258                     ld_IR       <= '0';
259                     ld_PC       <= '0';
260                     inc_PC      <= '0';
261                     clr_A       <= '0';
262                     ld_A        <= '0';
263                     clr_B       <= '0';
264                     ld_B        <= '0';
265                     clr_C       <= '0';
266                     ld_C        <= '0';
267                     clr_Z       <= '0';
268                     ld_Z        <= '0';
269                     ALU_op      <= "XXX";
270                     en          <= '1';
271                     wen         <= '1';
272                     A_Mux       <= 'X';
273                     B_Mux       <= 'X';
274                     REG_Mux     <= '0';
275                     DATA_Mux    <= "XX";
276                     IM_MUX1     <= 'X';
277                     IM_MUX2     <= "XX";
278                 when "0011" =>      --STB
279                     clr_IR      <= '0';
280                     ld_IR       <= '0';
281                     ld_PC       <= '0';
282                     inc_PC      <= '0';
283                     clr_A       <= '0';
284                     ld_A        <= '0';
285                     clr_B       <= '0';
286                     ld_B        <= '0';
287                     clr_C       <= '0';
288                     ld_C        <= '0';
289                     clr_Z       <= '0';
290                     ld_Z        <= '0';
291                     ALU_op      <= "XXX";
292                     en          <= '1';
293                     wen         <= '1';
294                     A_Mux       <= 'X';
295                     B_Mux       <= 'X';
296                     REG_Mux     <= '1';
297                     DATA_Mux    <= "XX";
298                     IM_MUX1     <= 'X';
299                     IM_MUX2     <= "XX";
300                 when "1001" =>      --LDA
301                     clr_IR      <= '0';
302                     ld_IR       <= '0';
303                     ld_PC       <= '0';
304                     inc_PC      <= '0';
305                     clr_A       <= '0';
306                     ld_A        <= '1';
307                     clr_B       <= '0';
308                     ld_B        <= '0';
309                     clr_C       <= '0';
310                     ld_C        <= '0';
```

```
311                         clr_Z       <= '0';
312                         ld_Z        <= '0';
313                         ALU_op      <= "XXX";
314                         en          <= '1';
315                         wen         <= '0';
316                         A_Mux       <= '0';
317                         B_Mux       <= 'X';
318                         REG_Mux     <= 'X';
319                         DATA_Mux    <= "01";
320                         IM_MUX1     <= 'X';
321                         IM_MUX2     <= "XX";
322                   when "1010" =>        --LDB
323                         clr_IR      <= '0';
324                         ld_IR       <= '0';
325                         ld_PC       <= '0';
326                         inc_PC      <= '0';
327                         clr_A       <= '0';
328                         ld_A        <= '0';
329                         clr_B       <= '0';
330                         ld_B        <= '1';
331                         clr_C       <= '0';
332                         ld_C        <= '0';
333                         clr_Z       <= '0';
334                         ld_Z        <= '0';
335                         ALU_op      <= "XXX";
336                         en          <= '1';
337                         wen         <= '0';
338                         A_Mux       <= 'X';
339                         B_Mux       <= '0';
340                         REG_Mux     <= 'X';
341                         DATA_Mux    <= "01";
342                         IM_MUX1     <= 'X';
343                         IM_MUX2     <= "XX";
344                   when "0100" =>        --LUI
345                         clr_IR      <= '0';
346                         ld_IR       <= '0';
347                         ld_PC       <= '0';
348                         inc_PC      <= '0';
349                         clr_A       <= '0';
350                         ld_A        <= '1';
351                         clr_B       <= '1';
352                         ld_B        <= '0';
353                         clr_C       <= '0';
354                         ld_C        <= '0';
355                         clr_Z       <= '0';
356                         ld_Z        <= '0';
357                         ALU_op      <= "001";
358                         en          <= 'X';
359                         wen         <= 'X';
360                         A_Mux       <= '0';
361                         B_Mux       <= 'X';
362                         REG_Mux     <= 'X';
363                         DATA_Mux    <= "10";
364                         IM_MUX1     <= '1';
365                         IM_MUX2     <= "XX";
366                   when "0101" =>        --JMP
367                         clr_IR      <= '0';
368                         ld_IR       <= '0';
369                         ld_PC       <= '1';
370                         inc_PC      <= '0';
371                         clr_A       <= '0';
372                         ld_A        <= '0';
```

```
373                         clr_B       <= '0';
374                         ld_B        <= '0';
375                         clr_C       <= '0';
376                         ld_C        <= '0';
377                         clr_Z       <= '0';
378                         ld_Z        <= '0';
379                         ALU_op      <= "XXX";
380                         en          <= 'X';
381                         wen         <= 'X';
382                         A_Mux       <= 'X';
383                         B_Mux       <= 'X';
384                         REG_Mux     <= 'X';
385                         DATA_Mux    <= "XX";
386                         IM_MUX1     <= 'X';
387                         IM_MUX2     <= "XX";
388                   when "0111" =>
389                      case (Inst_sig2) is
390                         when "0000" => --ADD
391                               clr_IR      <= '0';
392                               ld_IR       <= '0';
393                               ld_PC       <= '0';
394                               inc_PC      <= '0';
395                               clr_A       <= '0';
396                               ld_A        <= '1';
397                               clr_B       <= '0';
398                               ld_B        <= '0';
399                               clr_C       <= '0';
400                               ld_C        <= '1';
401                               clr_Z       <= '0';
402                               ld_Z        <= '1';
403                               ALU_op      <= "010";
404                               en          <= 'X';
405                               wen         <= 'X';
406                               A_Mux       <= '0';
407                               B_Mux       <= 'X';
408                               REG_Mux     <= 'X';
409                               DATA_Mux    <= "10";
410                               IM_MUX1     <= '0';
411                               IM_MUX2     <= "00";
412                         when "0001" => --ADDI
413                               clr_IR      <= '0';
414                               ld_IR       <= '0';
415                               ld_PC       <= '0';
416                               inc_PC      <= '0';
417                               clr_A       <= '0';
418                               ld_A        <= '1';
419                               clr_B       <= '0';
420                               ld_B        <= '0';
421                               clr_C       <= '0';
422                               ld_C        <= '1';
423                               clr_Z       <= '0';
424                               ld_Z        <= '1';
425                               ALU_op      <= "010";
426                               en          <= 'X';
427                               wen         <= 'X';
428                               A_Mux       <= '0';
429                               B_Mux       <= 'X';
430                               REG_Mux     <= 'X';
431                               DATA_Mux    <= "10";
432                               IM_MUX1     <= '0';
433                               IM_MUX2     <= "01";
434                         when "0010" => --SUB
```

```
435                         clr_IR      <= '0';
436                         ld_IR       <= '0';
437                         ld_PC       <= '0';
438                         inc_PC      <= '0';
439                         clr_A       <= '0';
440                         ld_A        <= '1';
441                         clr_B       <= '0';
442                         ld_B        <= '0';
443                         clr_C       <= '0';
444                         ld_C        <= '1';
445                         clr_Z       <= '0';
446                         ld_Z        <= '1';
447                         ALU_op      <= "110";
448                         en          <= 'X';
449                         wen         <= 'X';
450                         A_Mux       <= '0';
451                         B_Mux       <= 'X';
452                         REG_Mux     <= 'X';
453                         DATA_Mux    <= "10";
454                         IM_MUX1     <= '0';
455                         IM_MUX2     <= "00";
456                     when "0011" => --INCA
457                         clr_IR      <= '0';
458                         ld_IR       <= '0';
459                         ld_PC       <= '0';
460                         inc_PC      <= '0';
461                         clr_A       <= '0';
462                         ld_A        <= '1';
463                         clr_B       <= '0';
464                         ld_B        <= '0';
465                         clr_C       <= '0';
466                         ld_C        <= '1';
467                         clr_Z       <= '0';
468                         ld_Z        <= '1';
469                         ALU_op      <= "010";
470                         en          <= 'X';
471                         wen         <= 'X';
472                         A_Mux       <= '0';
473                         B_Mux       <= 'X';
474                         REG_Mux     <= 'X';
475                         DATA_Mux    <= "10";
476                         IM_MUX1     <= '0';
477                         IM_MUX2     <= "10";
478                     when "0100" => --ROL
479                         clr_IR      <= '0';
480                         ld_IR       <= '0';
481                         ld_PC       <= '0';
482                         inc_PC      <= '0';
483                         clr_A       <= '0';
484                         ld_A        <= '1';
485                         clr_B       <= '0';
486                         ld_B        <= '0';
487                         clr_C       <= '0';
488                         ld_C        <= '1';
489                         clr_Z       <= '0';
490                         ld_Z        <= '1';
491                         ALU_op      <= "100";
492                         en          <= 'X';
493                         wen         <= 'X';
494                         A_Mux       <= '0';
495                         B_Mux       <= 'X';
496                         REG_Mux     <= 'X';
```

```
497                         DATA_Mux    <= "10";
498                         IM_MUX1     <= '0';
499                         IM_MUX2     <= "XX";
500                     when "0101" => --CLRA
501                         clr_IR      <= '0';
502                         ld_IR       <= '0';
503                         ld_PC       <= '0';
504                         inc_PC      <= '0';
505                         clr_A       <= '1';
506                         ld_A        <= '0';
507                         clr_B       <= '0';
508                         ld_B        <= '0';
509                         clr_C       <= '0';
510                         ld_C        <= '0';
511                         clr_Z       <= '0';
512                         ld_Z        <= '0';
513                         ALU_op      <= "XXX";
514                         en          <= 'X';
515                         wen         <= 'X';
516                         A_Mux       <= 'X';
517                         B_Mux       <= 'X';
518                         REG_Mux     <= 'X';
519                         DATA_Mux    <= "XX";
520                         IM_MUX1     <= 'X';
521                         IM_MUX2     <= "XX";
522                     when "0110" => --CLRB
523                         clr_IR      <= '0';
524                         ld_IR       <= '0';
525                         ld_PC       <= '0';
526                         inc_PC      <= '0';
527                         clr_A       <= '0';
528                         ld_A        <= '0';
529                         clr_B       <= '1';
530                         ld_B        <= '0';
531                         clr_C       <= '0';
532                         ld_C        <= '0';
533                         clr_Z       <= '0';
534                         ld_Z        <= '0';
535                         ALU_op      <= "XXX";
536                         en          <= 'X';
537                         wen         <= 'X';
538                         A_Mux       <= 'X';
539                         B_Mux       <= 'X';
540                         REG_Mux     <= 'X';
541                         DATA_Mux    <= "XX";
542                         IM_MUX1     <= 'X';
543                         IM_MUX2     <= "XX";
544                     when "0111" => --CLRC
545                         clr_IR      <= '0';
546                         ld_IR       <= '0';
547                         ld_PC       <= '0';
548                         inc_PC      <= '0';
549                         clr_A       <= '0';
550                         ld_A        <= '0';
551                         clr_B       <= '0';
552                         ld_B        <= '0';
553                         clr_C       <= '1';
554                         ld_C        <= '0';
555                         clr_Z       <= '0';
556                         ld_Z        <= '0';
557                         ALU_op      <= "XXX";
558                         en          <= 'X';
```

```
559                     wen         <= 'X';
560                     A_Mux       <= 'X';
561                     B_Mux       <= 'X';
562                     REG_Mux     <= 'X';
563                     DATA_Mux    <= "XX";
564                     IM_MUX1     <= 'X';
565                     IM_MUX2     <= "XX";
566                 when "1000" => --CLRZ
567                     clr_IR      <= '0';
568                     ld_IR       <= '0';
569                     ld_PC       <= '0';
570                     inc_PC      <= '0';
571                     clr_A       <= '0';
572                     ld_A        <= '0';
573                     clr_B       <= '0';
574                     ld_B        <= '0';
575                     clr_C       <= '0';
576                     ld_C        <= '0';
577                     clr_Z       <= '1';
578                     ld_Z        <= '0';
579                     ALU_op      <= "XXX";
580                     en          <= 'X';
581                     wen         <= 'X';
582                     A_Mux       <= 'X';
583                     B_Mux       <= 'X';
584                     REG_Mux     <= 'X';
585                     DATA_Mux    <= "XX";
586                     IM_MUX1     <= 'X';
587                     IM_MUX2     <= "XX";
588                 when "1001" => --ANDI
589                     clr_IR      <= '0';
590                     ld_IR       <= '0';
591                     ld_PC       <= '0';
592                     inc_PC      <= '0';
593                     clr_A       <= '0';
594                     ld_A        <= '1';
595                     clr_B       <= '0';
596                     ld_B        <= '0';
597                     clr_C       <= '0';
598                     ld_C        <= '1';
599                     clr_Z       <= '0';
600                     ld_Z        <= '1';
601                     ALU_op      <= "000";
602                     en          <= 'X';
603                     wen         <= 'X';
604                     A_Mux       <= '0';
605                     B_Mux       <= 'X';
606                     REG_Mux     <= 'X';
607                     DATA_Mux    <= "10";
608                     IM_MUX1     <= '0';
609                     IM_MUX2     <= "01";
610                     --
611                 when "1011" =>    --AND
612                     clr_IR      <= '0';
613                     ld_IR       <= '0';
614                     ld_PC       <= '0';
615                     inc_PC      <= '0';
616                     clr_A       <= '0';
617                     ld_A        <= '1';
618                     clr_B       <= '0';
619                     ld_B        <= '0';
620                     clr_C       <= '0';
```

```
621                     ld_C        <= '1';
622                     clr_Z       <= '0';
623                     ld_Z        <= '1';
624                     ALU_op      <= "000";
625                     en          <= 'X';
626                     wen         <= 'X';
627                     A_Mux       <= '0';
628                     B_Mux       <= 'X';
629                     REG_Mux     <= 'X';
630                     DATA_Mux    <= "10";
631                     IM_MUX1     <= '0';
632                     IM_MUX2     <= "00";
633                     --
634                 when "1101" => --ORI
635                     clr_IR      <= '0';
636                     ld_IR       <= '0';
637                     ld_PC       <= '0';
638                     inc_PC      <= '0';
639                     clr_A       <= '0';
640                     ld_A        <= '1';
641                     clr_B       <= '0';
642                     ld_B        <= '0';
643                     clr_C       <= '0';
644                     ld_C        <= '1';
645                     clr_Z       <= '0';
646                     ld_Z        <= '1';
647                     ALU_op      <= "001";
648                     en          <= 'X';
649                     wen         <= 'X';
650                     A_Mux       <= '0';
651                     B_Mux       <= 'X';
652                     REG_Mux     <= 'X';
653                     DATA_Mux    <= "10";
654                     IM_MUX1     <= '0';
655                     IM_MUX2     <= "01";
656                 when "1110" => --DECA
657                     clr_IR      <= '0';
658                     ld_IR       <= '0';
659                     ld_PC       <= '0';
660                     inc_PC      <= '0';
661                     clr_A       <= '0';
662                     ld_A        <= '1';
663                     clr_B       <= '0';
664                     ld_B        <= '0';
665                     clr_C       <= '0';
666                     ld_C        <= '1';
667                     clr_Z       <= '0';
668                     ld_Z        <= '1';
669                     ALU_op      <= "110";
670                     en          <= 'X';
671                     wen         <= 'X';
672                     A_Mux       <= '0';
673                     B_Mux       <= 'X';
674                     REG_Mux     <= 'X';
675                     DATA_Mux    <= "10";
676                     IM_MUX1     <= '0';
677                     IM_MUX2     <= "10";
678                 when "1111" => --ROR
679                     clr_IR      <= '0';
680                     ld_IR       <= '0';
681                     ld_PC       <= '0';
682                     inc_PC      <= '0';
```

```
683                                 clr_A       <= '0';
684                                 ld_A        <= '1';
685                                 clr_B       <= '0';
686                                 ld_B        <= '0';
687                                 clr_C       <= '0';
688                                 ld_C        <= '1';
689                                 clr_Z       <= '0';
690                                 ld_Z        <= '1';
691                                 ALU_op      <= "101";
692                                 en          <= 'X';
693                                 wen         <= 'X';
694                                 A_Mux       <= '0';
695                                 B_Mux       <= 'X';
696                                 REG_Mux     <= 'X';
697                                 DATA_Mux    <= "10";
698                                 IM_MUX1     <= '0';
699                                 IM_MUX2     <= "XX";
700                              when others =>
701                                 clr_IR <= '0';
702                           end case;
703                        when others =>
704                           clr_IR <= '0';
705                  end case;
706            end case;
707         end process;
708      with y select
709         T <= "000" when s0,
710              "001" when t0,
711              "010" when t1,
712              "100" when t2,
713              "000" when others;
714   end Behaviour;
```

```
1   library ieee;
2
3   use ieee.std_logic_1164.all;
4   use ieee.std_logic_arith.all;
5   use ieee.std_logic_unsigned.all;
6
7   entity ControlUnit is
8      port (
9         clk, mclk: in std_logic;
10        enable: in std_logic;
11        statusC, statusZ: in std_logic;
12        inst: in std_logic_vector(31 downto 0);
13        A_mux, B_mux, IM_Mux1, REG_Mux : out std_logic;
14        IM_mux2, DATA_Mux: out std_logic_vector (1 downto 0);
15        ALU_op: out std_logic_vector(2 downto 0);
16        inc_PC, ld_PC, clr_IR, ld_IR: out std_logic;
17        clr_A, clr_B, clr_C, clr_Z : out std_logic;
18        ld_A, ld_b, ld_C, ld_Z: out std_logic;
19        T : out std_logic_vector(2 downto 0);
20        wen, en: out std_logic);
21  end ControlUnit;
22
23  architecture description of ControlUnit is
24  --define state types
25     type statetype is (state_0, state_1, state_2, s0);
26     --state signals
27     signal present_state: statetype;
28     signal inst_sig, inst_sig2: std_logic_vector(3 downto 0);
29        begin
30           inst_sig <= inst(31 downto 28);
31           inst_sig2 <= inst(27 downto 24);
32
33           --state machine
34           process(clk, enable, mclk, inst, statusC, statusZ)
35              begin
36                 if (enable = '0') then
37                    present_state <= s0;
38                 elsif (rising_edge(clk)) then
39                    case present_state is
40                       when s0 => present_state <= state_0;
41                       when state_0 => present_state <= state_1;
42                       when state_1 => present_state <= state_2;
43                       when state_2 => present_state <= state_0;
44                    end case;
45                 end if;
46           end process;
47
48           --decoder and memory signal
49              process(present_state)
50                 begin
51                    case present_state is
52                       when s0 => clr_IR <= '0';
53                                  ld_IR <= '1';
54                                  ld_PC <= '1';
55                                  inc_PC <= '0';
56                                  clr_A <= '0';
57                                  ld_A <= '0';
58                                  clr_B <= '0';
59                                  ld_b <= '0';
60                                  ld_C <= '0';
61                                  clr_C <= '0';
62                                  clr_Z <= '0';
```

```
63                                      ld_Z <= '0';
64                                      alu_op <= "XXX";
65                                      en <= 'X';
66                                      wen <= 'X';
67                                      A_mux <= 'X';
68                                      B_mux <= 'X';
69                                      REG_Mux <= 'X';
70                                      DATA_Mux <= "00";
71                                      IM_Mux1 <= 'X';
72                                      IM_mux2 <= "XX";
73
74                              when state_0 => clr_IR <= '0';
75                                      ld_IR <= '1';
76                                      ld_PC <= '1';
77                                      inc_PC <= '0';
78                                      clr_A <= '0';
79                                      ld_A <= '0';
80                                      clr_B <= '0';
81                                      ld_b <= '0';
82                                      ld_C <= '0';
83                                      clr_C <= '0';
84                                      clr_Z <= '0';
85                                      ld_Z <= '0';
86                                      alu_op <= "XXX";
87                                      en <= 'X';
88                                      wen <= 'X';
89                                      A_mux <= 'X';
90                                      B_mux <= 'X';
91                                      REG_Mux <= 'X';
92                                      DATA_Mux <= "00";
93                                      IM_Mux1 <= 'X';
94                                      IM_mux2 <= "XX";
95
96                              when state_1 => clr_IR <= '0';
97                                      ld_IR <= '0';
98                                      ld_PC <= '1';
99                                      inc_PC <= '1';
100                                     clr_A <= '0';
101                                     ld_A <= '0';
102                                     clr_B <= '0';
103                                     ld_b <= '0';
104                                     ld_C <= '0';
105                                     clr_C <= '0';
106                                     clr_Z <= '0';
107                                     ld_Z <= '0';
108                                     alu_op <= "XXX";
109                                     en <= 'X';
110                                     wen <= 'X';
111                                     A_mux <= 'X';
112                                     B_mux <= 'X';
113                                     REG_Mux <= 'X';
114                                     DATA_Mux <= "00";
115                                     IM_Mux1 <= 'X';
116                                     IM_mux2 <= "XX";
117
118                             case inst_sig is --sta
119                                   when "0010" =>
120                                     clr_IR <= '0';
121                                     ld_IR <= '0';
122                                     ld_PC <= '1';
123                                     inc_PC <= '1';
124                                     clr_A <= '0';
```

```
125                     ld_A <= '0';
126                     clr_B <= '0';
127                     ld_b <= '0';
128                     ld_C <= '0';
129                     clr_C <= '0';
130                     clr_Z <= '0';
131                     ld_Z <= '0';
132                     alu_op <= "XXX";
133                     en <= '1';
134                     wen <= '1';
135                     A_mux <= 'X';
136                     B_mux <= 'X';
137                     REG_Mux <= 'X';
138                     DATA_Mux <= "00";
139                     IM_Mux1 <= 'X';
140                     IM_mux2 <= "XX";
141 
142                   when "0011" => --stb
143                     clr_IR <= '0';
144                     ld_IR <= '0';
145                     ld_PC <= '1';
146                     inc_PC <= '1';
147                     clr_A <= '0';
148                     ld_A <= '0';
149                     clr_B <= '0';
150                     ld_b <= '0';
151                     ld_C <= '0';
152                     clr_C <= '0';
153                     clr_Z <= '0';
154                     ld_Z <= '0';
155                     alu_op <= "XXX";
156                     en <= '1';
157                     wen <= '1';
158                     A_mux <= 'X';
159                     B_mux <= 'X';
160                     REG_Mux <= '1';
161                     DATA_Mux <= "00";
162                     IM_Mux1 <= 'X';
163                     IM_mux2 <= "XX";
164 
165                   when "1001" => --lda
166                     clr_IR <= '0';
167                     ld_IR <= '0';
168                     ld_PC <= '1';
169                     inc_PC <= '1';
170                     clr_A <= '0';
171                     ld_A <= '1';
172                     clr_B <= '0';
173                     ld_b <= '0';
174                     ld_C <= '0';
175                     clr_C <= '0';
176                     clr_Z <= '0';
177                     ld_Z <= '0';
178                     alu_op <= "XXX";
179                     en <= '1';
180                     wen <= '0';
181                     A_mux <= 'X';
182                     B_mux <= 'X';
183                     REG_Mux <= '1';
184                     DATA_Mux <= "01";
185                     IM_Mux1 <= 'X';
186                     IM_mux2 <= "XX";
```

```
187
188                         when "1010" => --ldb
189                           clr_IR <= '0';
190                           ld_IR <= '0';
191                           ld_PC <= '1';
192                           inc_PC <= '1';
193                           clr_A <= '0';
194                           ld_A <= '0';
195                           clr_B <= '0';
196                           ld_b <= '1';
197                           ld_C <= '0';
198                           clr_C <= '0';
199                           clr_Z <= '0';
200                           ld_Z <= '0';
201                           alu_op <= "XXX";
202                           en <= '1';
203                           wen <= '0';
204                           A_mux <= 'X';
205                           B_mux <= 'X';
206                           REG_Mux <= '1';
207                           DATA_Mux <= "01";
208                           IM_Mux1 <= 'X';
209                           IM_mux2 <= "XX";
210
211                         when others =>
212                            clr_IR <= '0';
213                      end case; --inst_sig end
214
215                when state_2 =>
216                   case inst_sig is
217                      when "0000" => --ldbi
218                        clr_IR <= '0';
219                        ld_IR <= '0';
220                        ld_PC <= '0';
221                        inc_PC <= '0';
222                        clr_A <= '0';
223                        ld_A <= '1';
224                        clr_B <= '0';
225                        ld_b <= '0';
226                        ld_C <= '0';
227                        clr_C <= '0';
228                        clr_Z <= '0';
229                        ld_Z <= '0';
230                        alu_op <= "XXX";
231                        en <= 'X';
232                        wen <= 'X';
233                        A_mux <= '1';
234                        B_mux <= 'X';
235                        REG_Mux <= 'X';
236                        DATA_Mux <= "XX";
237                        IM_Mux1 <= 'X';
238                        IM_mux2 <= "XX";
239
240                      when "0001" => --sta
241                        clr_IR <= '0';
242                        ld_IR <= '0';
243                        ld_PC <= '0';
244                        inc_PC <= '0';
245                        clr_A <= '0';
246                        ld_A <= '0';
247                        clr_B <= '0';
248                        ld_b <= '1';
```

```
249                     ld_C <= '0';
250                     clr_C <= '0';
251                     clr_Z <= '0';
252                     ld_Z <= '0';
253                     alu_op <= "XXX";
254                     en <= 'X';
255                     wen <= 'X';
256                     A_mux <= 'X';
257                     B_mux <= '1';
258                     REG_Mux <= 'X';
259                     DATA_Mux <= "XX";
260                     IM_Mux1 <= 'X';
261                     IM_mux2 <= "XX";
262 
263                   when "0010" => --stb
264                     clr_IR <= '0';
265                     ld_IR <= '0';
266                     ld_PC <= '0';
267                     inc_PC <= '0';
268                     clr_A <= '0';
269                     ld_A <= '0';
270                     clr_B <= '0';
271                     ld_b <= '1';
272                     ld_C <= '0';
273                     clr_C <= '0';
274                     clr_Z <= '0';
275                     ld_Z <= '0';
276                     alu_op <= "XXX";
277                     en <= '1';
278                     wen <= '1';
279                     A_mux <= 'X';
280                     B_mux <= 'X';
281                     REG_Mux <= 'X';
282                     DATA_Mux <= "XX";
283                     IM_Mux1 <= 'X';
284                     IM_mux2 <= "XX";
285 
286                   when "0011" => --lda
287                     clr_IR <= '0';
288                     ld_IR <= '0';
289                     ld_PC <= '0';
290                     inc_PC <= '0';
291                     clr_A <= '0';
292                     ld_A <= '0';
293                     clr_B <= '0';
294                     ld_b <= '1';
295                     ld_C <= '0';
296                     clr_C <= '0';
297                     clr_Z <= '0';
298                     ld_Z <= '0';
299                     alu_op <= "XXX";
300                     en <= '1';
301                     wen <= '1';
302                     A_mux <= 'X';
303                     B_mux <= 'X';
304                     REG_Mux <= '1';
305                     DATA_Mux <= "XX";
306                     IM_Mux1 <= 'X';
307                     IM_mux2 <= "XX";
308 
309                   when "1001" => --ldab
310                     clr_IR <= '0';
```

```
311                     ld_IR <= '0';
312                     ld_PC <= '0';
313                     inc_PC <= '0';
314                     clr_A <= '0';
315                     ld_A <= '1';
316                     clr_B <= '0';
317                     ld_b <= '0';
318                     ld_C <= '0';
319                     clr_C <= '0';
320                     clr_Z <= '0';
321                     ld_Z <= '0';
322                     alu_op <= "XXX";
323                     en <= '1';
324                     wen <= '0';
325                     A_mux <= '0';
326                     B_mux <= 'X';
327                     REG_Mux <= '1';
328                     DATA_Mux <= "01";
329                     IM_Mux1 <= 'X';
330                     IM_mux2 <= "XX";
331 
332                   when "1010" => --lui
333                     clr_IR <= '0';
334                     ld_IR <= '0';
335                     ld_PC <= '0';
336                     inc_PC <= '0';
337                     clr_A <= '0';
338                     ld_A <= '0';
339                     clr_B <= '0';
340                     ld_b <= '1';
341                     ld_C <= '0';
342                     clr_C <= '0';
343                     clr_Z <= '0';
344                     ld_Z <= '0';
345                     alu_op <= "XXX";
346                     en <= '1';
347                     wen <= '0';
348                     A_mux <= '0';
349                     B_mux <= 'X';
350                     REG_Mux <= 'X';
351                     DATA_Mux <= "01";
352                     IM_Mux1 <= 'X';
353                     IM_mux2 <= "XX";
354 
355                   when "0100" => --jmp
356                     clr_IR <= '0';
357                     ld_IR <= '0';
358                     ld_PC <= '0';
359                     inc_PC <= '0';
360                     clr_A <= '1';
361                     ld_A <= '0';
362                     clr_B <= '0';
363                     ld_b <= '0';
364                     ld_C <= '0';
365                     clr_C <= '0';
366                     clr_Z <= '0';
367                     ld_Z <= '0';
368                     alu_op <= "001";
369                     en <= 'X';
370                     wen <= 'X';
371                     A_mux <= '0';
372                     B_mux <= 'X';
```

```
373                     REG_Mux <= 'X';
374                     DATA_Mux <= "10";
375                     IM_Mux1 <= '1';
376                     IM_mux2 <= "XX";
377
378                   when "0101" => --bne
379                     clr_IR <= '0';
380                     ld_IR <= '0';
381                     ld_PC <= '1';
382                     inc_PC <= '0';
383                     clr_A <= '0';
384                     ld_A <= '0';
385                     clr_B <= '0';
386                     ld_b <= '0';
387                     ld_C <= '0';
388                     clr_C <= '0';
389                     clr_Z <= '0';
390                     ld_Z <= '0';
391                     alu_op <= "XXX";
392                     en <= 'X';
393                     wen <= 'X';
394                     A_mux <= '0';
395                     B_mux <= 'X';
396                     REG_Mux <= 'X';
397                     DATA_Mux <= "XX";
398                     IM_Mux1 <= 'X';
399                     IM_mux2 <= "XX";
400
401                    when "1000" => --beq
402                     clr_IR <= '0';
403                     ld_IR <= '0';
404                     ld_PC <= '0';
405                     inc_PC <= '0';
406                     clr_A <= '0';
407                     ld_A <= '0';
408                     clr_B <= '0';
409                     ld_b <= '0';
410                     ld_C <= '0';
411                     clr_C <= '0';
412                     clr_Z <= '0';
413                     ld_Z <= '1';
414                     alu_op <= "110";
415                     en <= 'X';
416                     wen <= 'X';
417                     A_mux <= '0';
418                     B_mux <= 'X';
419                     REG_Mux <= 'X';
420                     DATA_Mux <= "XX";
421                     IM_Mux1 <= '0';
422                     IM_mux2 <= "00";
423                      if statusZ = '0' then
424                         ld_PC <= '1';
425                      else
426                         ld_PC <= '0';
427                      end if;
428
429                   when "0110" => --add - check multiplexer A
430                     clr_IR <= '0';
431                     ld_IR <= '0';
432                     ld_PC <= '0';
433                     inc_PC <= '0';
434                     clr_A <= '0';
```

```
435                         ld_A <= '0';
436                         clr_B <= '0';
437                         ld_b <= '0';
438                         ld_C <= '0';
439                         clr_C <= '0';
440                         clr_Z <= '0';
441                         ld_Z <= '1';
442                         alu_op <= "110";
443                         en <= 'X';
444                         wen <= 'X';
445                         A_mux <= '0';
446                         B_mux <= 'X';
447                         REG_Mux <= 'X';
448                         DATA_Mux <= "XX";
449                         IM_Mux1 <= '0';
450                         IM_mux2 <= "00";
451                          if statusZ = '1' then
452                             ld_PC <= '1';
453                          else
454                             ld_PC <= '0';
455                          end if;
456
457                      when "0111" =>
458                         case inst_sig2 is
459                            when "0000" => --add
460                              clr_IR <= '0';
461                              ld_IR <= '0';
462                              ld_PC <= '0';
463                              inc_PC <= '0';
464                              clr_A <= '0';
465                              ld_A <= '1';
466                              clr_B <= '0';
467                              ld_b <= '0';
468                              ld_C <= '0';
469                              clr_C <= '0';
470                              clr_Z <= '1';
471                              ld_Z <= '0';
472                              alu_op <= "010";
473                              en <= 'X';
474                              wen <= 'X';
475                              A_mux <= '0';
476                              B_mux <= 'X';
477                              REG_Mux <= 'X';
478                              DATA_Mux <= "10";
479                              IM_Mux1 <= '0';
480                              IM_mux2 <= "00";
481
482                            when "0001" => --addi
483                              clr_IR <= '0';
484                              ld_IR <= '0';
485                              ld_PC <= '0';
486                              inc_PC <= '0';
487                              clr_A <= '0';
488                              ld_A <= '1';
489                              clr_B <= '0';
490                              ld_b <= '0';
491                              ld_C <= '1';
492                              clr_C <= '0';
493                              clr_Z <= '1';
494                              ld_Z <= '0';
495                              alu_op <= "010";
496                              en <= 'X';
```

```
497                 wen <= 'X';
498                 A_mux <= '0';
499                 B_mux <= 'X';
500                 REG_Mux <= 'X';
501                 DATA_Mux <= "10";
502                 IM_Mux1 <= '0';
503                 IM_mux2 <= "01";
504 
505               when "0010" => --sub
506                 clr_IR <= '0';
507                 ld_IR <= '0';
508                 ld_PC <= '0';
509                 inc_PC <= '0';
510                 clr_A <= '0';
511                 ld_A <= '1';
512                 clr_B <= '0';
513                 ld_b <= '0';
514                 ld_C <= '1';
515                 clr_C <= '0';
516                 clr_Z <= '1';
517                 ld_Z <= '0';
518                 alu_op <= "110";
519                 en <= 'X';
520                 wen <= 'X';
521                 A_mux <= '0';
522                 B_mux <= 'X';
523                 REG_Mux <= 'X';
524                 DATA_Mux <= "10";
525                 IM_Mux1 <= '0';
526                 IM_mux2 <= "00";
527 
528               when "0011" => --inca
529                 clr_IR <= '0';
530                 ld_IR <= '0';
531                 ld_PC <= '0';
532                 inc_PC <= '0';
533                 clr_A <= '0';
534                 ld_A <= '1';
535                 clr_B <= '0';
536                 ld_b <= '0';
537                 ld_C <= '1';
538                 clr_C <= '0';
539                 clr_Z <= '1';
540                 ld_Z <= '0';
541                 alu_op <= "010";
542                 en <= 'X';
543                 wen <= 'X';
544                 A_mux <= '0';
545                 B_mux <= 'X';
546                 REG_Mux <= 'X';
547                 DATA_Mux <= "10";
548                 IM_Mux1 <= '0';
549                 IM_mux2 <= "10";
550 
551               when "0100" => --rol
552                 clr_IR <= '0';
553                 ld_IR <= '0';
554                 ld_PC <= '0';
555                 inc_PC <= '0';
556                 clr_A <= '0';
557                 ld_A <= '1';
558                 clr_B <= '0';
```

```
559                                 ld_b <= '0';
560                                 ld_C <= '1';
561                                 clr_C <= '0';
562                                 clr_Z <= '1';
563                                 ld_Z <= '0';
564                                 alu_op <= "100";
565                                 en <= 'X';
566                                 wen <= 'X';
567                                 A_mux <= '0';
568                                 B_mux <= 'X';
569                                 REG_Mux <= 'X';
570                                 DATA_Mux <= "10";
571                                 IM_Mux1 <= '0';
572                                 IM_mux2 <= "XX";
573 
574                             when "0101" => --clra
575                                 clr_IR <= '0';
576                                 ld_IR <= '0';
577                                 ld_PC <= '0';
578                                 inc_PC <= '0';
579                                 clr_A <= '0';
580                                 ld_A <= '1';
581                                 clr_B <= '0';
582                                 ld_b <= '0';
583                                 ld_C <= '0';
584                                 clr_C <= '0';
585                                 clr_Z <= '0';
586                                 ld_Z <= '0';
587                                 alu_op <= "XXX";
588                                 en <= 'X';
589                                 wen <= 'X';
590                                 A_mux <= 'X';
591                                 B_mux <= 'X';
592                                 REG_Mux <= 'X';
593                                 DATA_Mux <= "XX";
594                                 IM_Mux1 <= 'X';
595                                 IM_mux2 <= "XX";
596 
597                             when "0110" => --clrb
598                                 clr_IR <= '0';
599                                 ld_IR <= '0';
600                                 ld_PC <= '0';
601                                 inc_PC <= '0';
602                                 clr_A <= '0';
603                                 ld_A <= '0';
604                                 clr_B <= '1';
605                                 ld_b <= '0';
606                                 ld_C <= '0';
607                                 clr_C <= '0';
608                                 clr_Z <= '0';
609                                 ld_Z <= '0';
610                                 alu_op <= "XXX";
611                                 en <= 'X';
612                                 wen <= 'X';
613                                 A_mux <= 'X';
614                                 B_mux <= 'X';
615                                 REG_Mux <= 'X';
616                                 DATA_Mux <= "XX";
617                                 IM_Mux1 <= 'X';
618                                 IM_mux2 <= "XX";
619 
620                             when "0111" => --clrc
```

```
621                 clr_IR <= '0';
622                 ld_IR <= '0';
623                 ld_PC <= '0';
624                 inc_PC <= '0';
625                 clr_A <= '0';
626                 ld_A <= '0';
627                 clr_B <= '0';
628                 ld_b <= '0';
629                 ld_C <= '0';
630                 clr_C <= '1';
631                 clr_Z <= '0';
632                 ld_Z <= '0';
633                 alu_op <= "XXX";
634                 en <= 'X';
635                 wen <= 'X';
636                 A_mux <= 'X';
637                 B_mux <= 'X';
638                 REG_Mux <= 'X';
639                 DATA_Mux <= "XX";
640                 IM_Mux1 <= 'X';
641                 IM_mux2 <= "XX";
642 
643               when "1000" => --clrz
644                 clr_IR <= '0';
645                 ld_IR <= '0';
646                 ld_PC <= '0';
647                 inc_PC <= '0';
648                 clr_A <= '0';
649                 ld_A <= '0';
650                 clr_B <= '0';
651                 ld_b <= '0';
652                 ld_C <= '0';
653                 clr_C <= '0';
654                 clr_Z <= '1';
655                 ld_Z <= '0';
656                 alu_op <= "XXX";
657                 en <= 'X';
658                 wen <= 'X';
659                 A_mux <= 'X';
660                 B_mux <= 'X';
661                 REG_Mux <= 'X';
662                 DATA_Mux <= "XX";
663                 IM_Mux1 <= 'X';
664                 IM_mux2 <= "XX";
665 
666               when "1001" => --andi
667                 clr_IR <= '0';
668                 ld_IR <= '0';
669                 ld_PC <= '0';
670                 inc_PC <= '0';
671                 clr_A <= '0';
672                 ld_A <= '1';
673                 clr_B <= '0';
674                 ld_b <= '0';
675                 ld_C <= '1';
676                 clr_C <= '0';
677                 clr_Z <= '0';
678                 ld_Z <= '1';
679                 alu_op <= "000";
680                 en <= 'X';
681                 wen <= 'X';
682                 A_mux <= 'X';
```

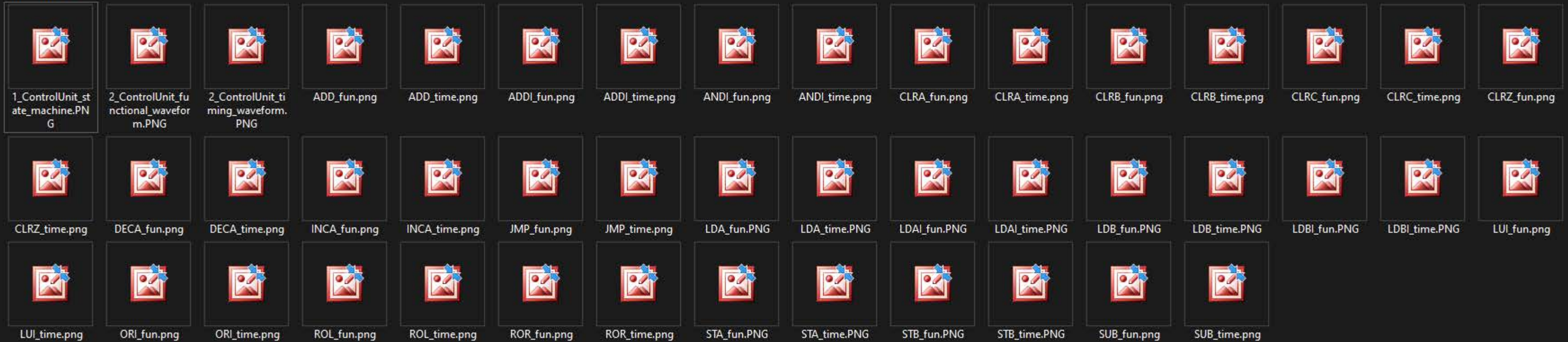
```
683                 B_mux <= 'X';
684                 REG_Mux <= 'X';
685                 DATA_Mux <= "10";
686                 IM_Mux1 <= '0';
687                 IM_mux2 <= "01";
688 
689               when "1011" => --and
690                 clr_IR <= '0';
691                 ld_IR <= '0';
692                 ld_PC <= '0';
693                 inc_PC <= '0';
694                 clr_A <= '0';
695                 ld_A <= '1';
696                 clr_B <= '0';
697                 ld_b <= '0';
698                 ld_C <= '1';
699                 clr_C <= '0';
700                 clr_Z <= '0';
701                 ld_Z <= '1';
702                 alu_op <= "000";
703                 en <= 'X';
704                 wen <= 'X';
705                 A_mux <= '0';
706                 B_mux <= 'X';
707                 REG_Mux <= 'X';
708                 DATA_Mux <= "10";
709                 IM_Mux1 <= '0';
710                 IM_mux2 <= "00";
711 
712               when "1101" => --ori
713                 clr_IR <= '0';
714                 ld_IR <= '0';
715                 ld_PC <= '0';
716                 inc_PC <= '0';
717                 clr_A <= '0';
718                 ld_A <= '1';
719                 clr_B <= '0';
720                 ld_b <= '0';
721                 ld_C <= '1';
722                 clr_C <= '0';
723                 clr_Z <= '0';
724                 ld_Z <= '1';
725                 alu_op <= "001";
726                 en <= 'X';
727                 wen <= 'X';
728                 A_mux <= '0';
729                 B_mux <= 'X';
730                 REG_Mux <= 'X';
731                 DATA_Mux <= "10";
732                 IM_Mux1 <= '0';
733                 IM_mux2 <= "01";
734 
735               when "1110" => --deca
736                 clr_IR <= '0';
737                 ld_IR <= '0';
738                 ld_PC <= '0';
739                 inc_PC <= '0';
740                 clr_A <= '0';
741                 ld_A <= '1';
742                 clr_B <= '0';
743                 ld_b <= '0';
744                 ld_C <= '1';
```

```
                                    clr_C <= '0';
                                    clr_Z <= '0';
                                    ld_Z <= '1';
                                    alu_op <= "110";
                                    en <= 'X';
                                    wen <= 'X';
                                    A_mux <= '0';
                                    B_mux <= 'X';
                                    REG_Mux <= 'X';
                                    DATA_Mux <= "10";
                                    IM_Mux1 <= '0';
                                    IM_mux2 <= "10";

                                  when "1111" => --ror
                                    clr_IR <= '0';
                                    ld_IR <= '0';
                                    ld_PC <= '0';
                                    inc_PC <= '0';
                                    clr_A <= '0';
                                    ld_A <= '1';
                                    clr_B <= '0';
                                    ld_b <= '0';
                                    ld_C <= '1';
                                    clr_C <= '0';
                                    clr_Z <= '0';
                                    ld_Z <= '1';
                                    alu_op <= "101";
                                    en <= 'X';
                                    wen <= 'X';
                                    A_mux <= '0';
                                    B_mux <= 'X';
                                    REG_Mux <= 'X';
                                    DATA_Mux <= "10";
                                    IM_Mux1 <= '0';
                                    IM_mux2 <= "XX";

                                  when others =>
                                     clr_IR <= '0';
                                  end case;
                               when others =>
                                  clr_IR <= '0';
                            end case;
                         end case;
                end process;
        with present_state select
           T <= "000" when s0,
                "001" when state_0,
                "010" when state_1,
                "011" when state_2,
                "111" when others;
   end description;
```

PNG File (45)

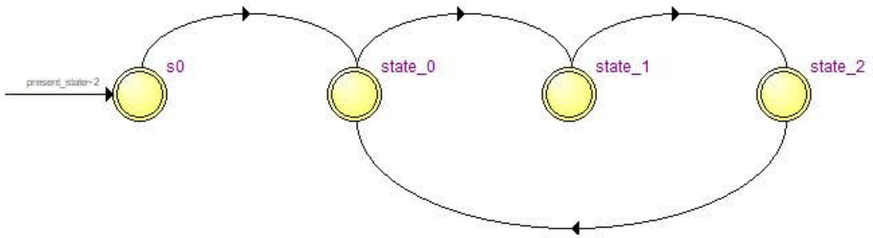

1_ControlUnit_state_machine.PNG
2_ControlUnit_functional_waveform.PNG
2_ControlUnit_timing_waveform.PNG
ADD_fun.png
ADD_time.png
ADDI_fun.png
ADDI_time.png
ANDI_fun.png
ANDI_time.png
CLRA_fun.png
CLRA_time.png
CLRB_fun.png
CLRB_time.png
CLRC_fun.png
CLRC_time.png
CLRZ_fun.png
CLRZ_time.png
DECA_fun.png
DECA_time.png
INCA_fun.png
INCA_time.png
JMP_fun.png
JMP_time.png
LDA_fun.PNG
LDA_time.PNG
LDAI_fun.PNG
LDAI_time.PNG
LDB_fun.PNG
LDB_time.PNG
LDBI_fun.PNG
LDBI_time.PNG
LUI_fun.png
LUI_time.png
ORI_fun.png
ORI_time.png
ROL_fun.png
ROL_time.png
ROR_fun.png
ROR_time.png
STA_fun.PNG
STA_time.PNG
STB_fun.PNG
STB_time.PNG
SUB_fun.png
SUB_time.png

State Machine Viewer - D:/RYERSON_S2020/coe608_2020/lab5/ControlUnit/ControlUnit - ControlUnit

File Edit View Tools Window Help

Search altera.com

State Machine: |ControlUnit|present_state



State Table

	Source State	Destination State	Condition
1	s0	state_0	
2	state_0	state_1	
3	state_1	state_2	
4	state_2	state_0	

Transitions Encoding

0% 00:00:00

ENG 6:02 PM

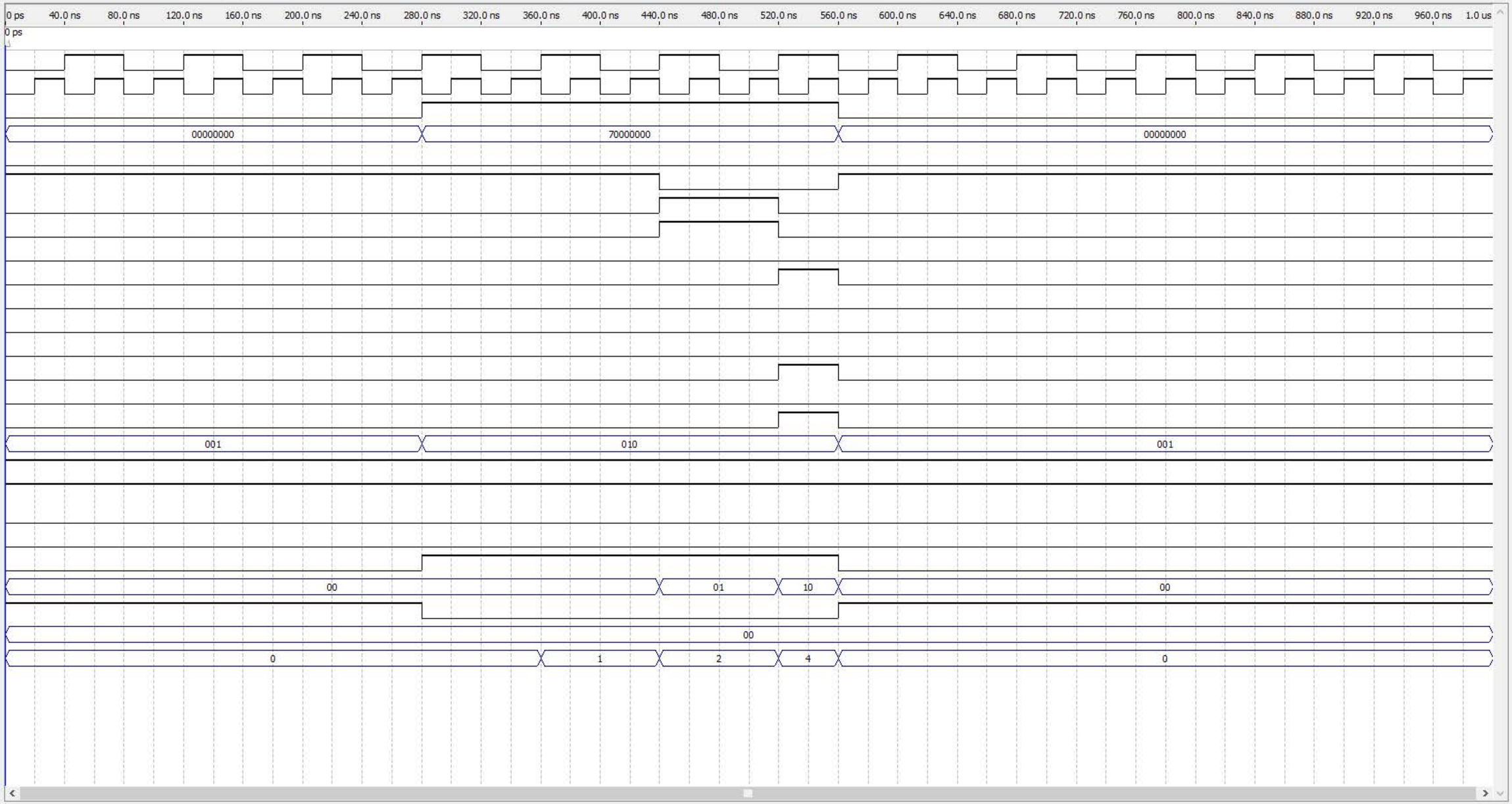
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 228.9 ns | Interval: 228.9 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



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ENG 5:15 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 609.01 ns | Interval: 609.01 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 70000000 | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:15 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

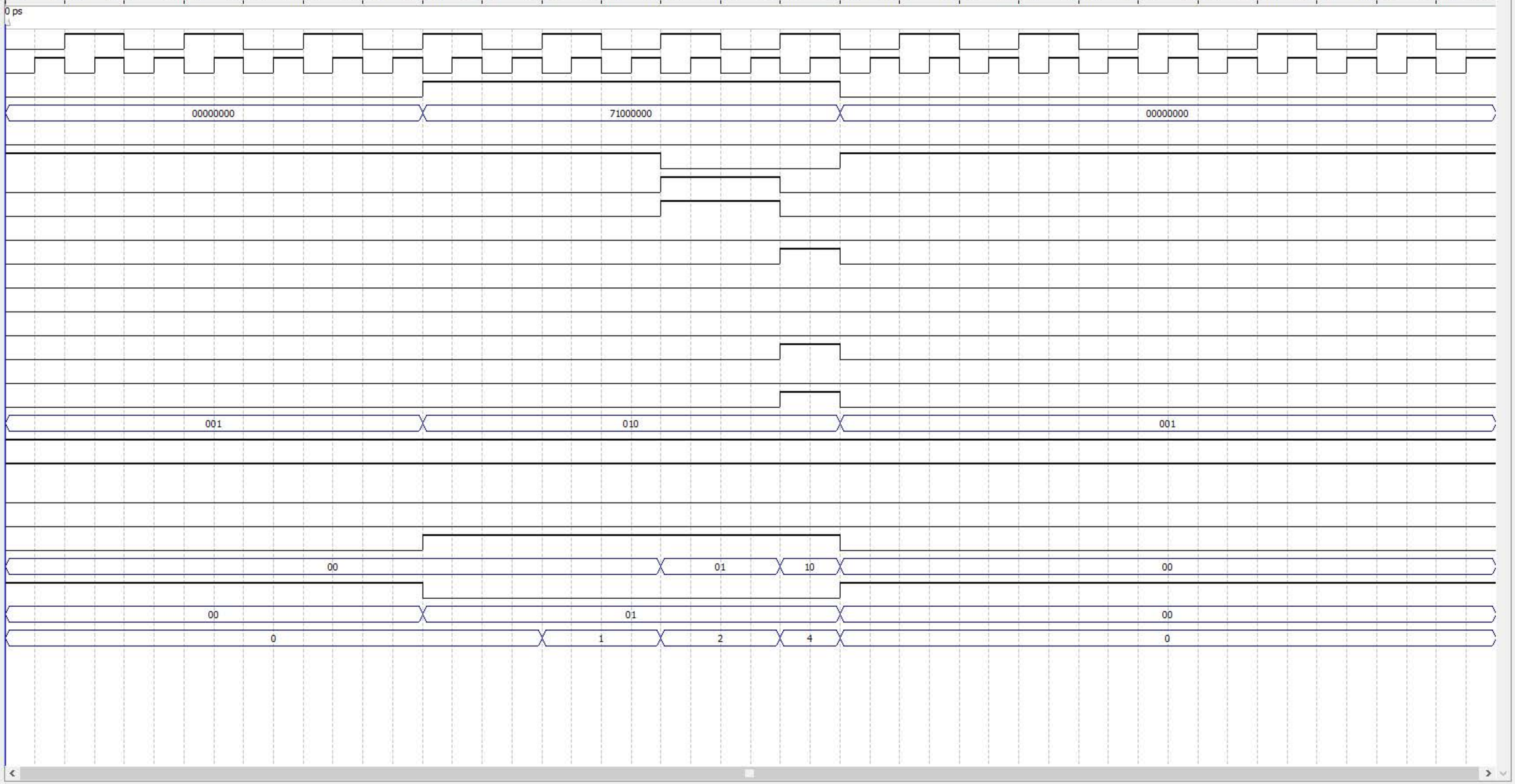
File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 123.34 ns | Interval: 123.34 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us



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ENG 5:16 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

00000000 71000000 00000000

001 010 001

00 01 10 00

00 01 00

0 1 2 4 1 0

0% 00:00:00

ENG 5:16 PM

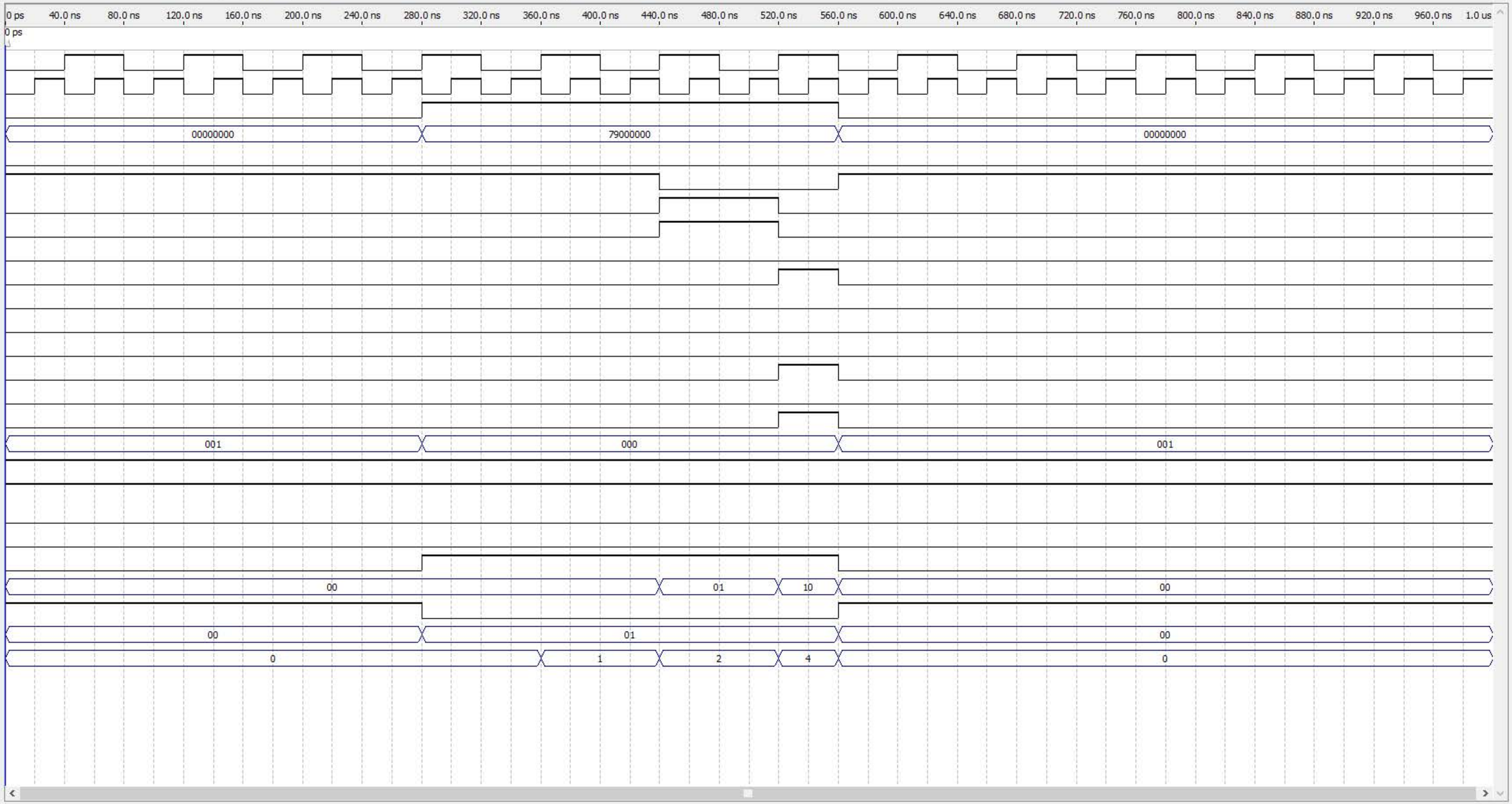
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 432.89 ns | Interval: 432.89 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



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ENG 5:23 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 79000000 | 00000000

ALU_op: 001 | 000 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00 | 01 | 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:23 PM

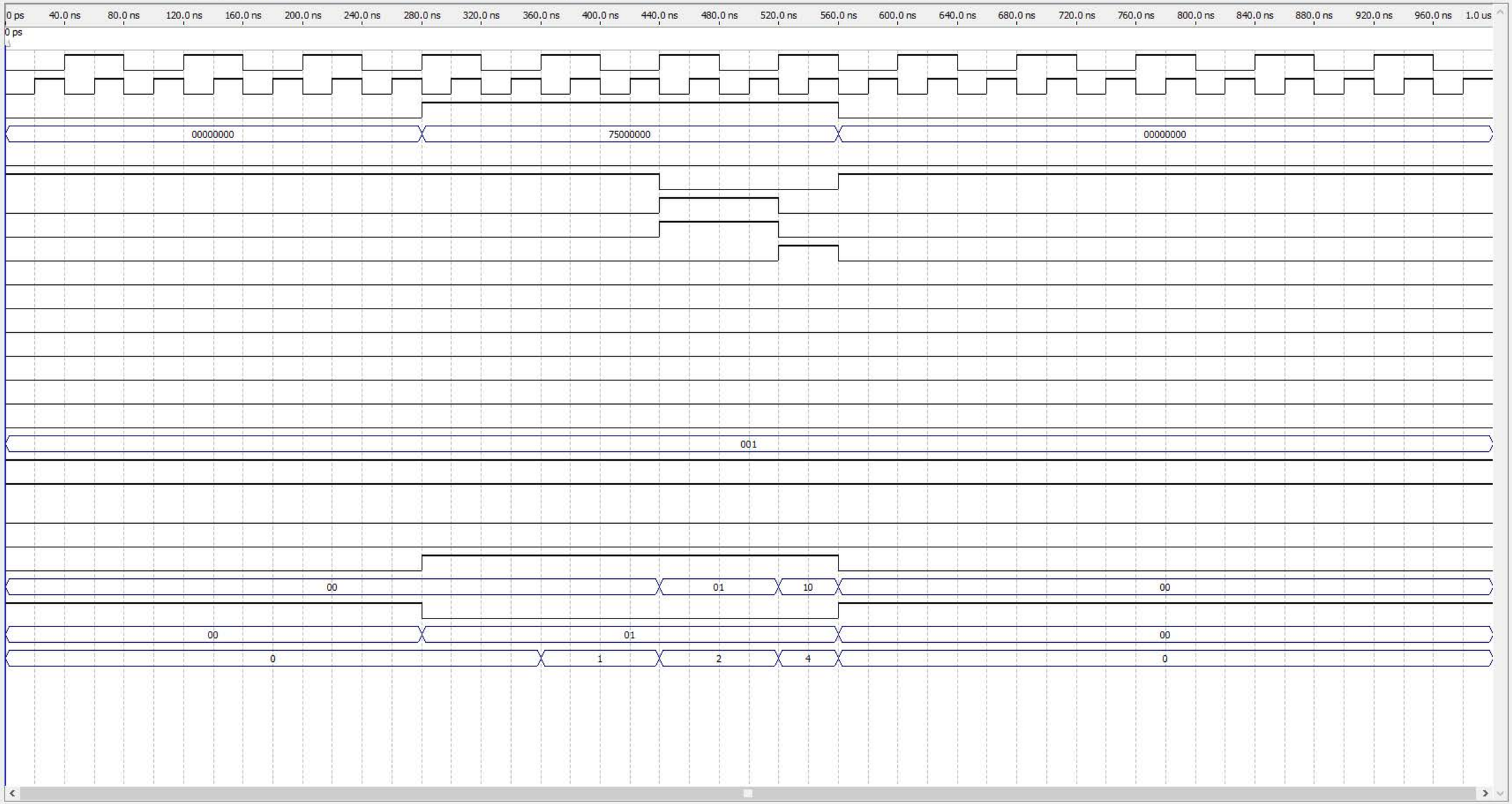
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



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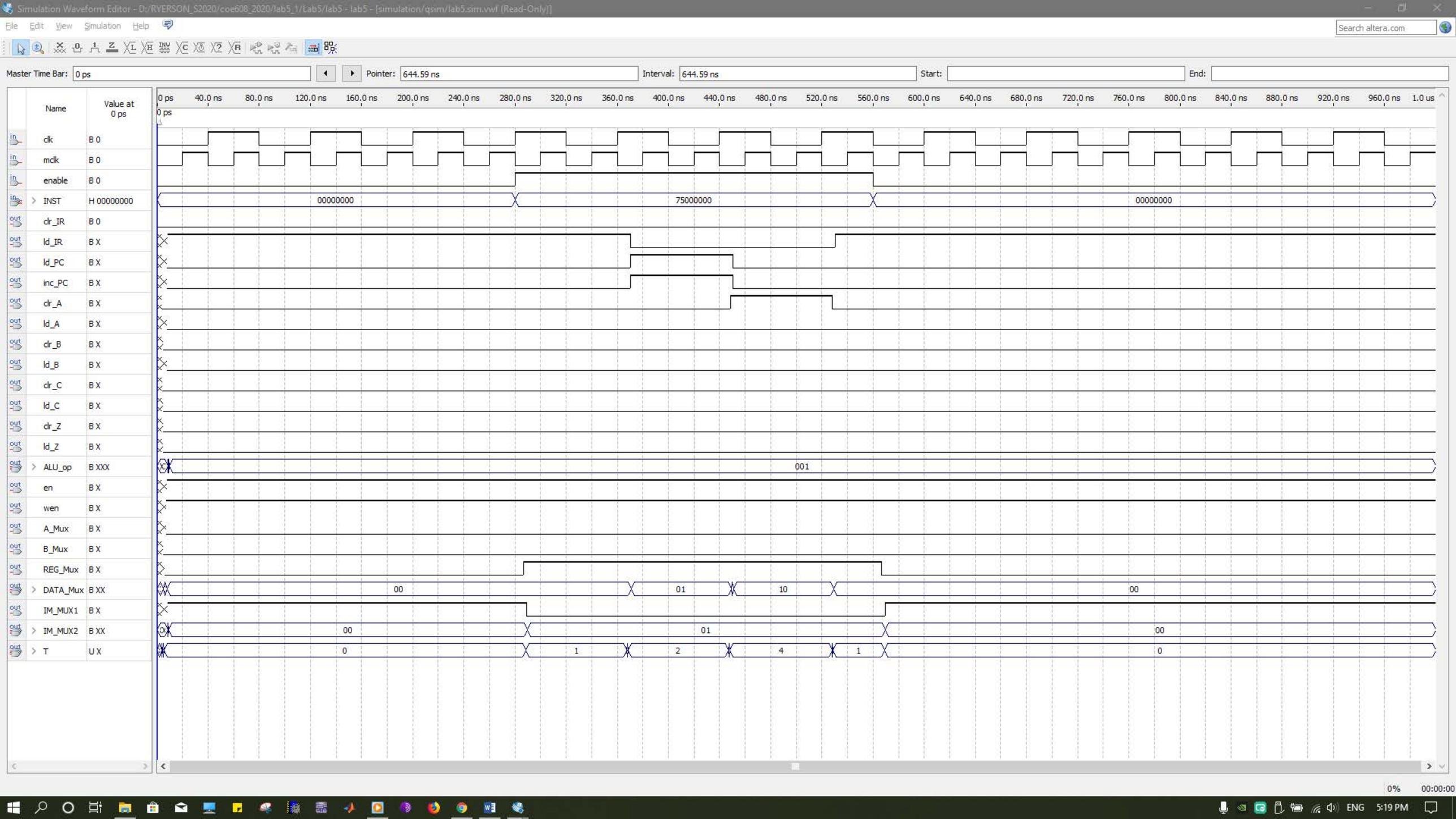
ENG 5:19 PM


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 644.59 ns
Interval: 644.59 ns
Start:
End:
Name
Value at 0 ps
clk B 0
mclk B 0
enable B 0
INST H 00000000
clr_IR B 0
ld_IR B X
ld_PC B X
inc_PC B X
clr_A B X
ld_A B X
clr_B B X
ld_B B X
clr_C B X
ld_C B X
clr_Z B X
ld_Z B X
ALU_op B XXX
en B X
wen B X
A_Mux B X
B_Mux B X
REG_Mux B X
DATA_Mux B XX
IM_MUX1 B X
IM_MUX2 B XX
T U X
0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us
00000000
75000000
00000000
001
00
01
10
00
00
01
00
0
1
2
4
1
0
0%
00:00:00
ENG
5:19 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 370.63 ns | Interval: 370.63 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 76000000 | 00000000

ALU_op: 001 | 100 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 5:20 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 76000000 | 00000000

ALU_op: 001 | 100 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:20 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

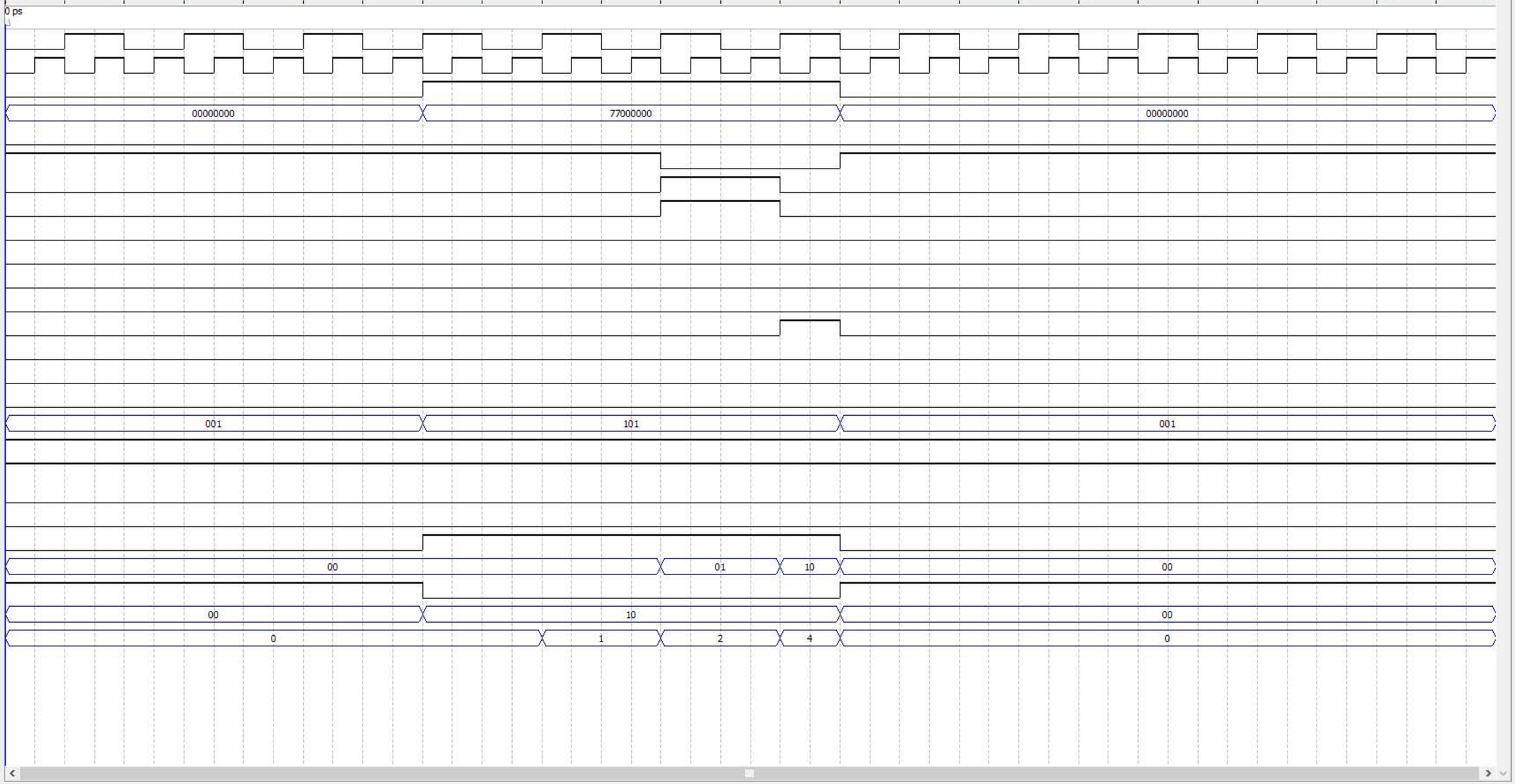
File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 11.86 ns | Interval: 11.86 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us



Start

0% 00:00:00

ENG 5:21 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 706.86 ns | Interval: 706.86 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 77000000 | 00000000

ALU_op: 001 | 101 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00 | 10 | 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:21 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

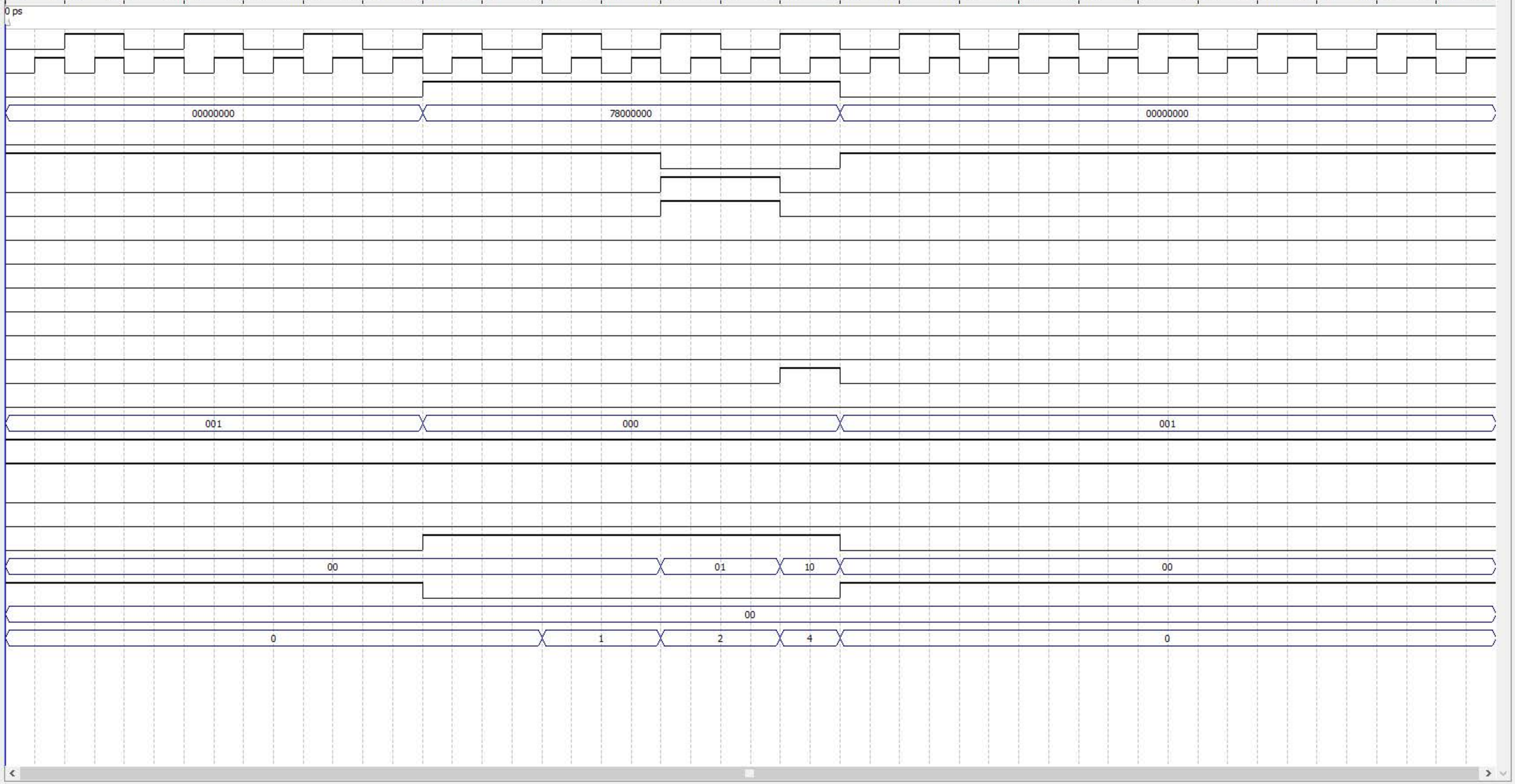
File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 675.43 ns | Interval: 675.43 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us



0% 00:00:00

ENG 5:21 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 78000000 | 00000000

ALU_op: 001 | 000 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:22 PM

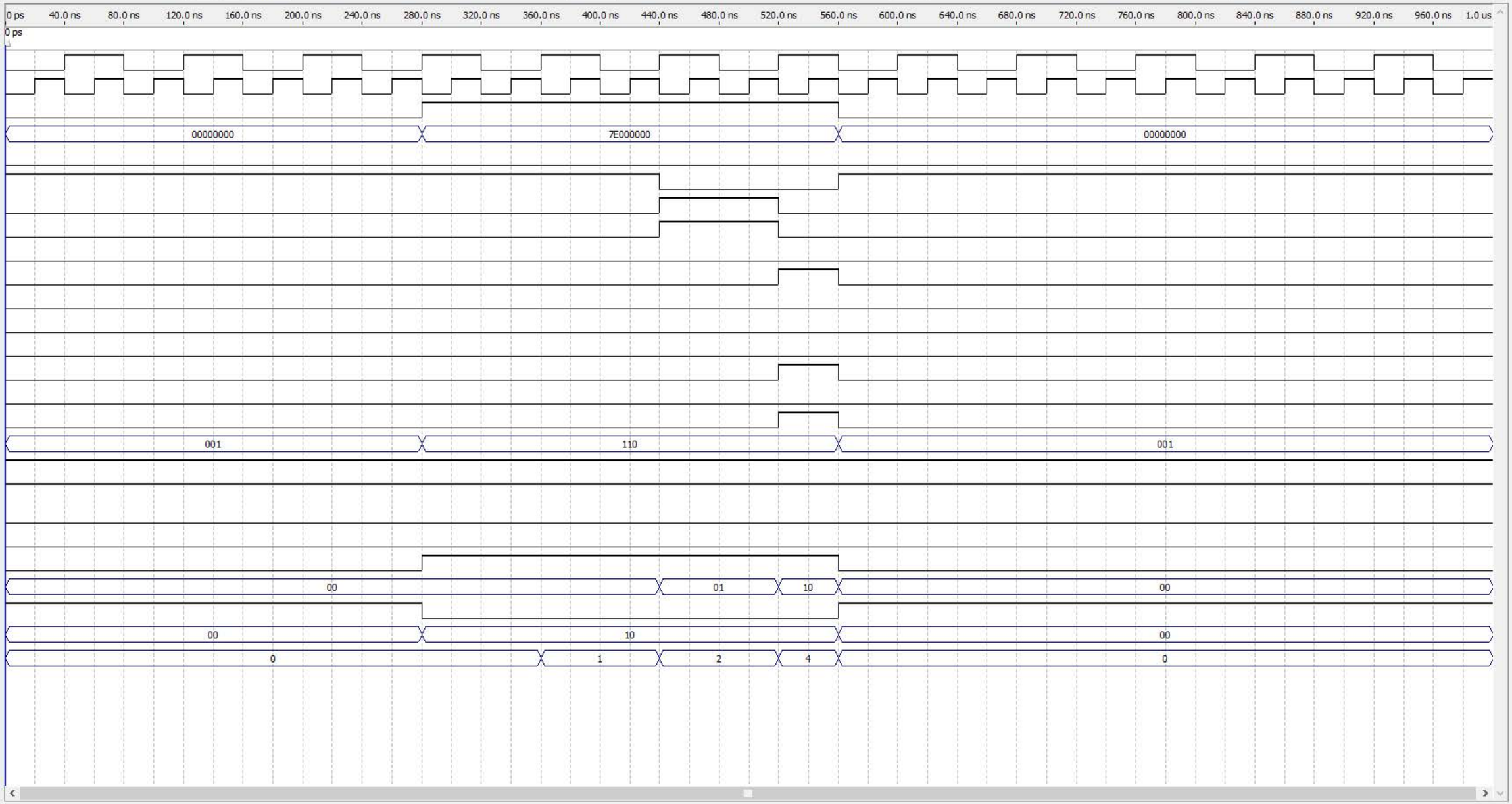
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



Start

0% 00:00:00

ENG 5:25 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 976.67 ns | Interval: 976.67 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 7E000000 | 00000000

ALU_op: 001 | 110 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00 | 10 | 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:25 PM

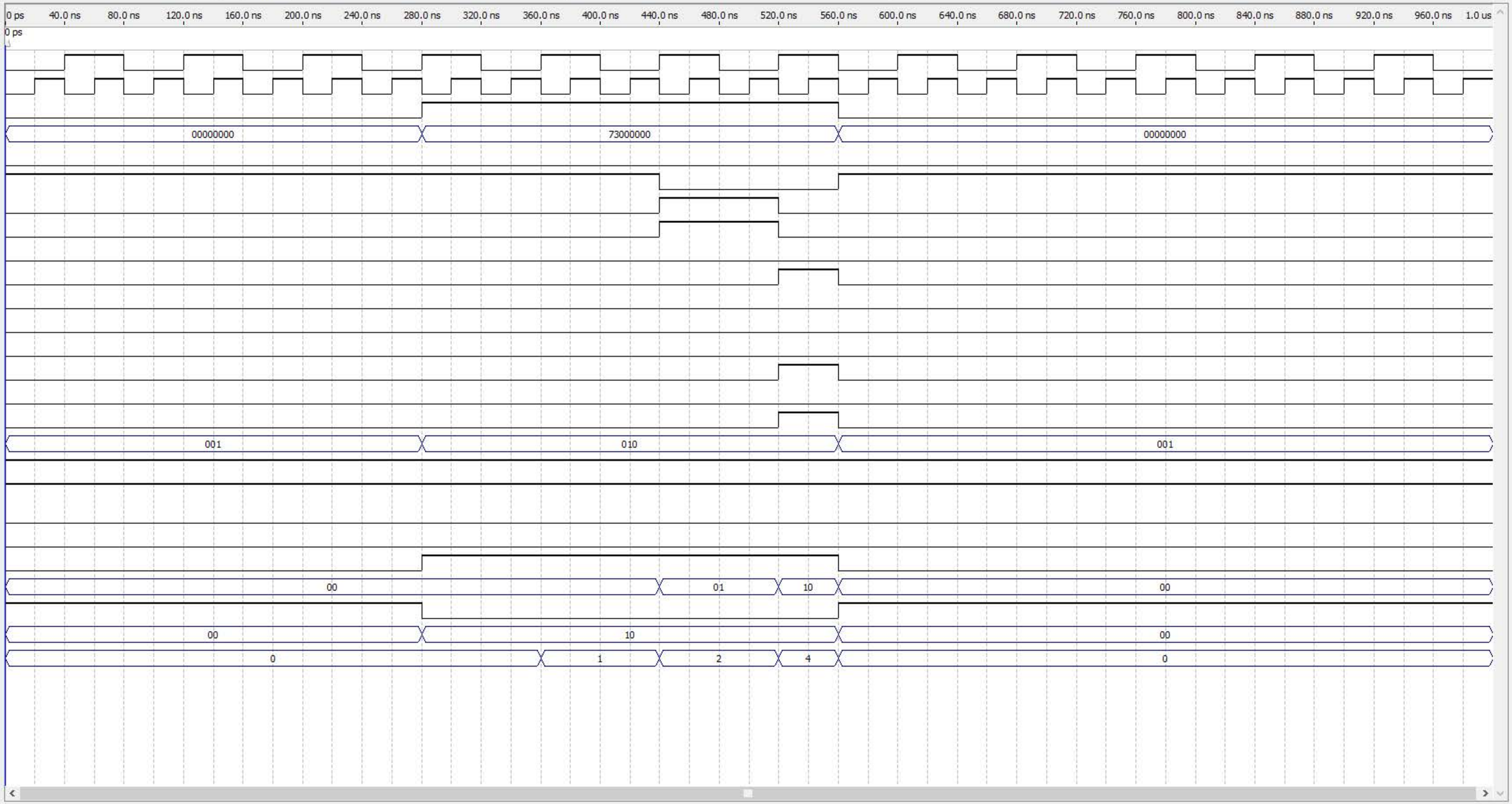
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



0% 00:00:00

ENG 5:18 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 73000000 | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00 | 10 | 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:18 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

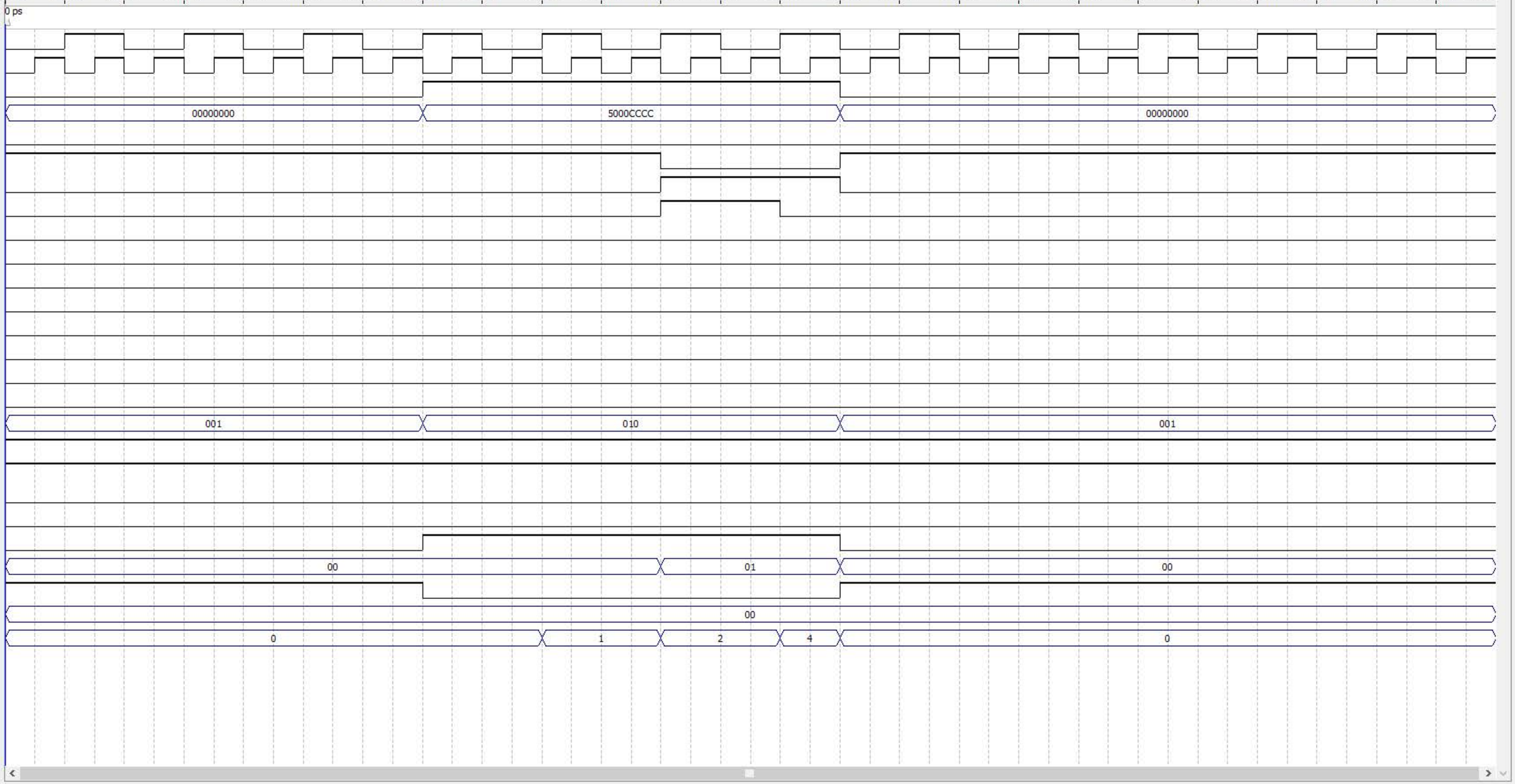
File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 437.63 ns | Interval: 437.63 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us



0% 00:00:00

ENG 5:14 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 511.76 ns | Interval: 511.76 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 5000CCCC | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:14 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

00000000 A000BBBB 00000000

001

00 01 00

00

0 1 2 4 1 0

0% 00:00:00

ENG 5:58 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 976.67 ns | Interval: 976.67 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 9000AAAA | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 5:56 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 881.2 ns | Interval: 881.2 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 9000AAAA | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:56 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 993.28 ns | Interval: 993.28 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

00000000 0000AAAA 00000000

001

00 01 10 00

00

0 1 2 4 0

0% 00:00:00

ENG 5:52 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 308.36 ns | Interval: 308.36 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 0000AAAA | 00000000

ALU_op: 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:53 PM

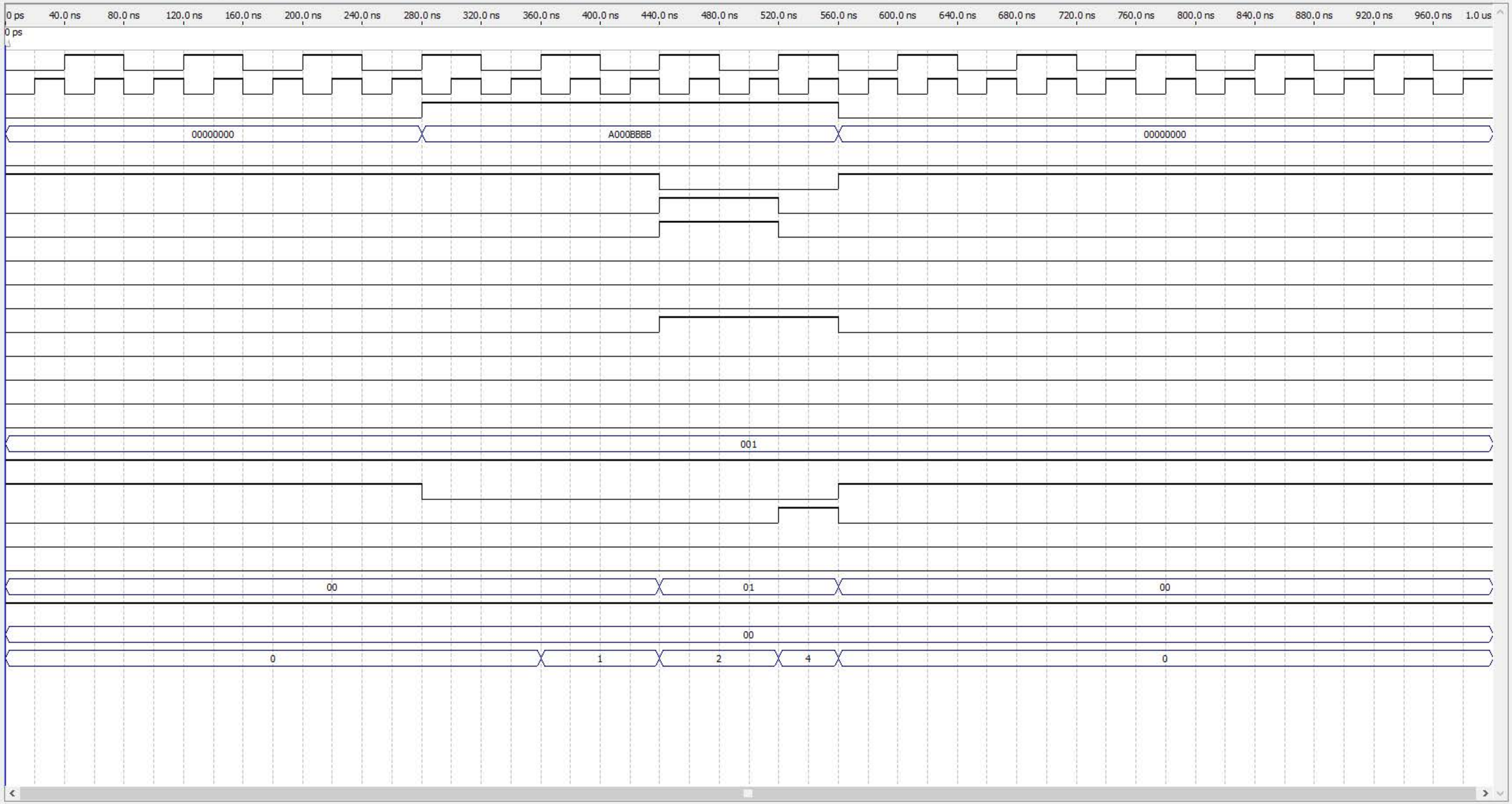
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



0% 00:00:00

ENG 5:58 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 442.97 ns | Interval: 442.97 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 1000BBBB | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 5:53 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 1000BBBB | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:54 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 996.24 ns | Interval: 996.24 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 4000CCCC | 00000000

ALU_op: 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 5:59 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

00000000 4000CCCC 00000000

001

00 01 10 00

00

0 1 2 4 1 0

0% 00:00:00

ENG 5:59 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 440.6 ns | Interval: 440.6 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 7D000000 | 00000000

ALU_op: 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00 | 01 | 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 5:24 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 7D000000 | 00000000

ALU_op: 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00 | 01 | 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:24 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

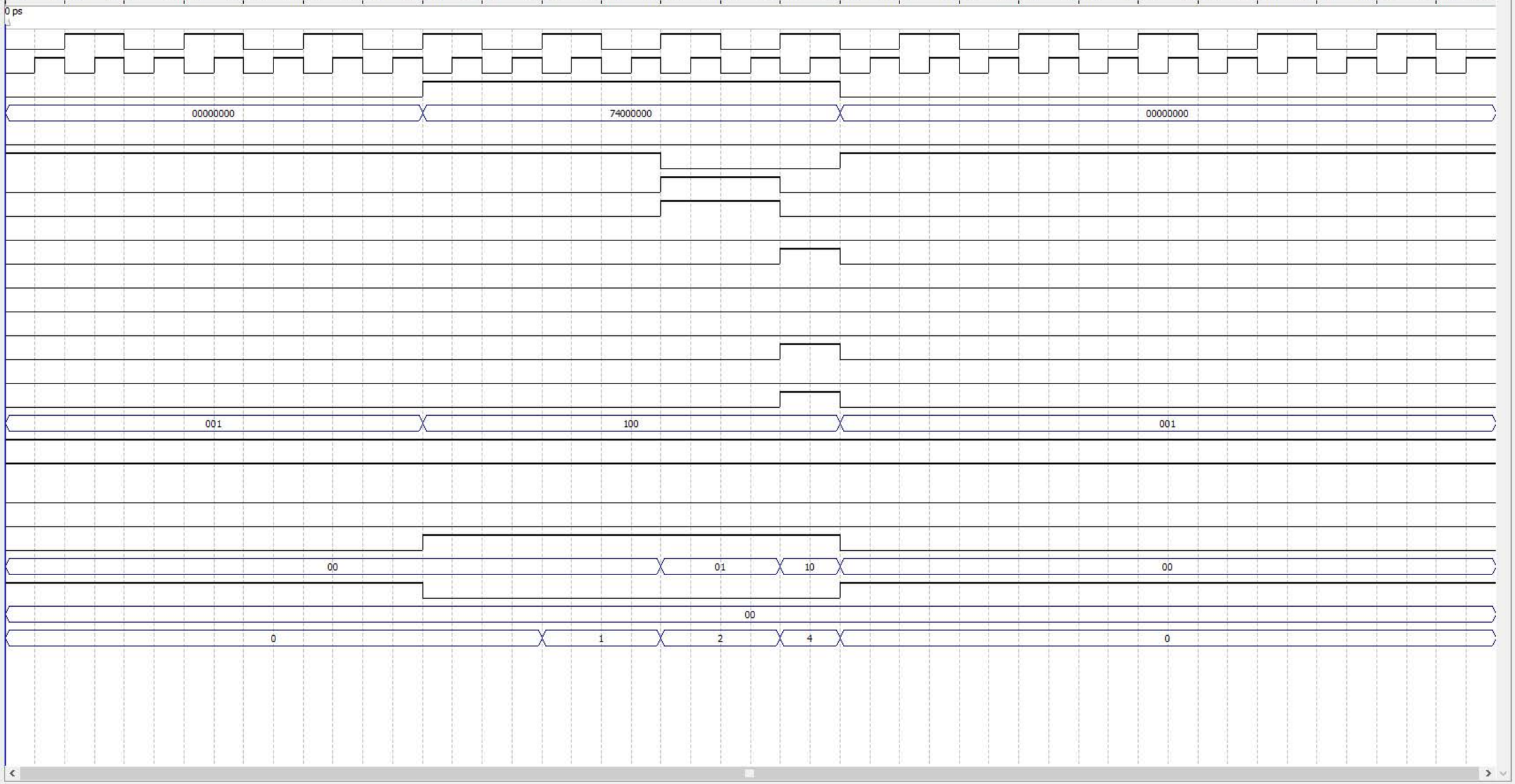
File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 61.67 ns | Interval: 61.67 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us



0% 00:00:00

ENG 5:18 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 230.68 ns | Interval: 230.68 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 74000000 | 00000000

ALU_op: 001 | 100 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:18 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 913.81 ns | Interval: 913.81 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 7F000000 | 00000000

ALU_op: 001 | 101 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 5:27 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 7F000000 | 00000000

ALU_op: 001 | 101 | 001

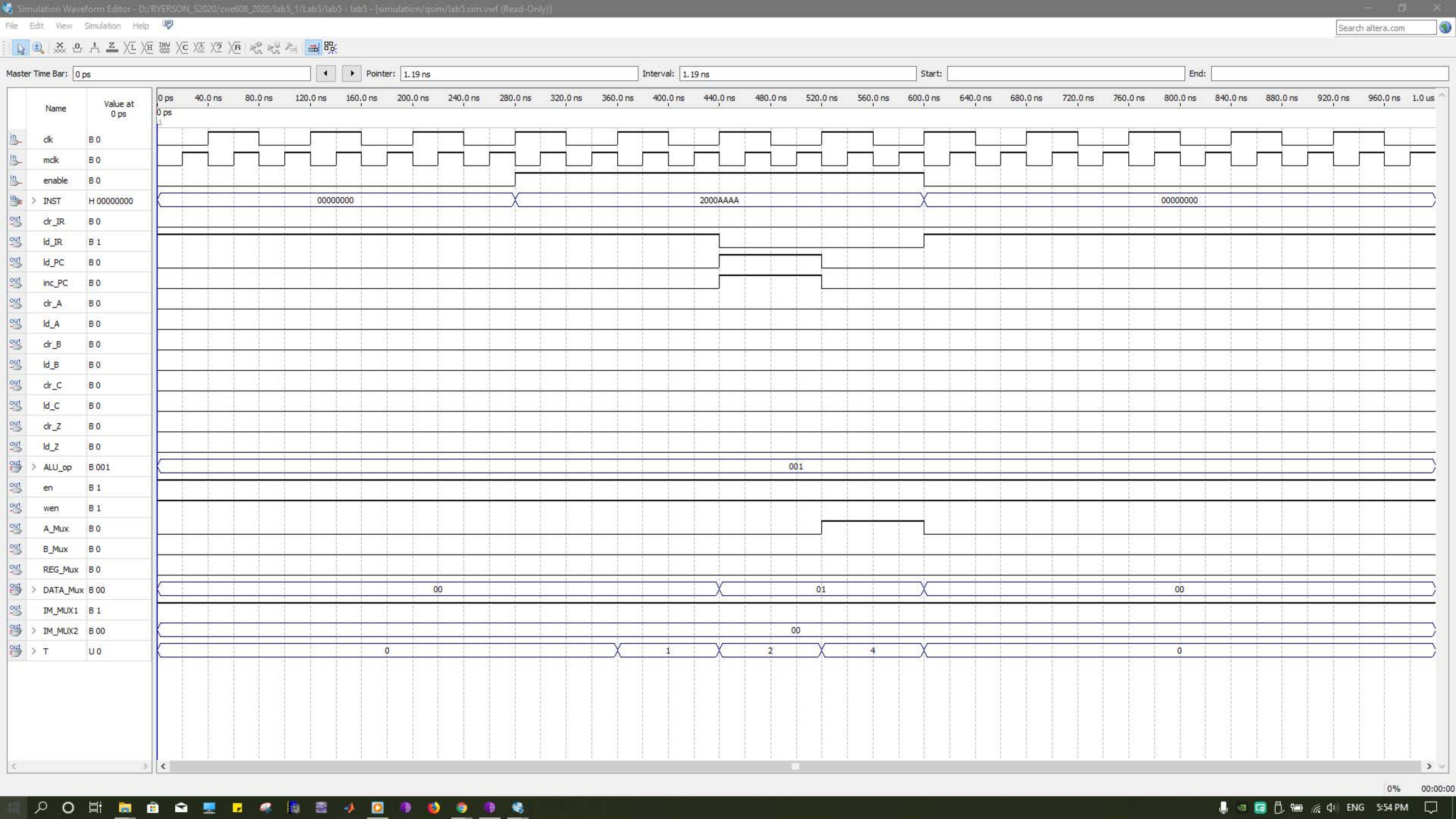
DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:27 PM


Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 1.19 ns
Interval: 1.19 ns
Start:
End:
Name
Value at 0 ps
clk B 0
mclk B 0
enable B 0
INST H 00000000
clr_IR B 0
ld_IR B 1
ld_PC B 0
inc_PC B 0
clr_A B 0
ld_A B 0
clr_B B 0
ld_B B 0
clr_C B 0
ld_C B 0
clr_Z B 0
ld_Z B 0
ALU_op B 001
en B 1
wen B 1
A_Mux B 0
B_Mux B 0
REG_Mux B 0
DATA_Mux B 00
IM_MUX1 B 1
IM_MUX2 B 00
T U 0
0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us
00000000
2000AAAA
00000000
001
00
01
00
00
0
1
2
4
0
0%
00:00:00
ENG 5:54 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 732.95 ns Interval: 732.95 ns Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

00000000 2000AAAA 00000000

001

00 01 00

00

0 1 2 4 1 0

0% 00:00:00

ENG 5:54 PM

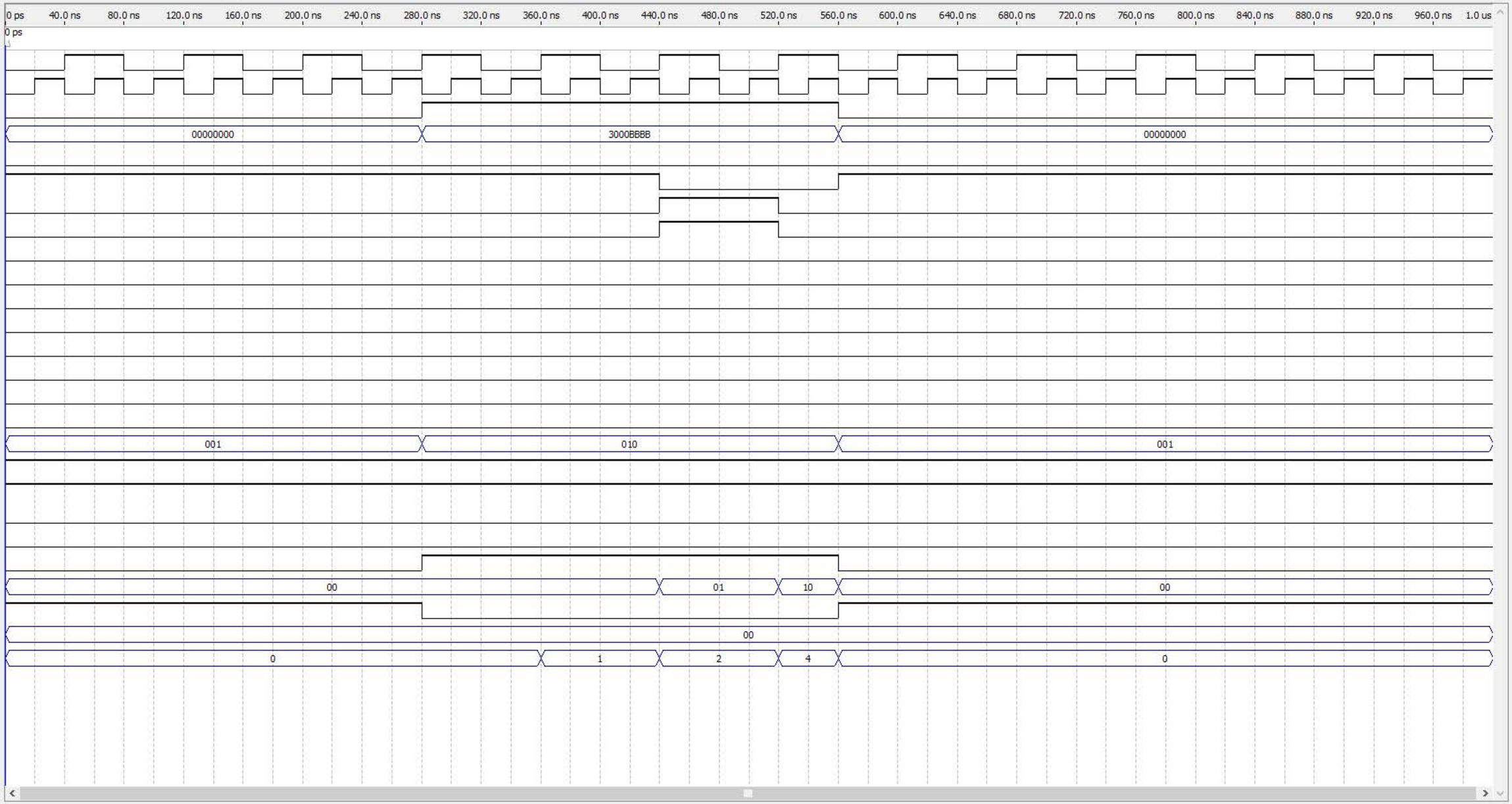
Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 709.23 ns | Interval: 709.23 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0



0% 00:00:00

ENG 5:55 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 3000BBBB | 00000000

ALU_op: 001 | 010 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:55 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

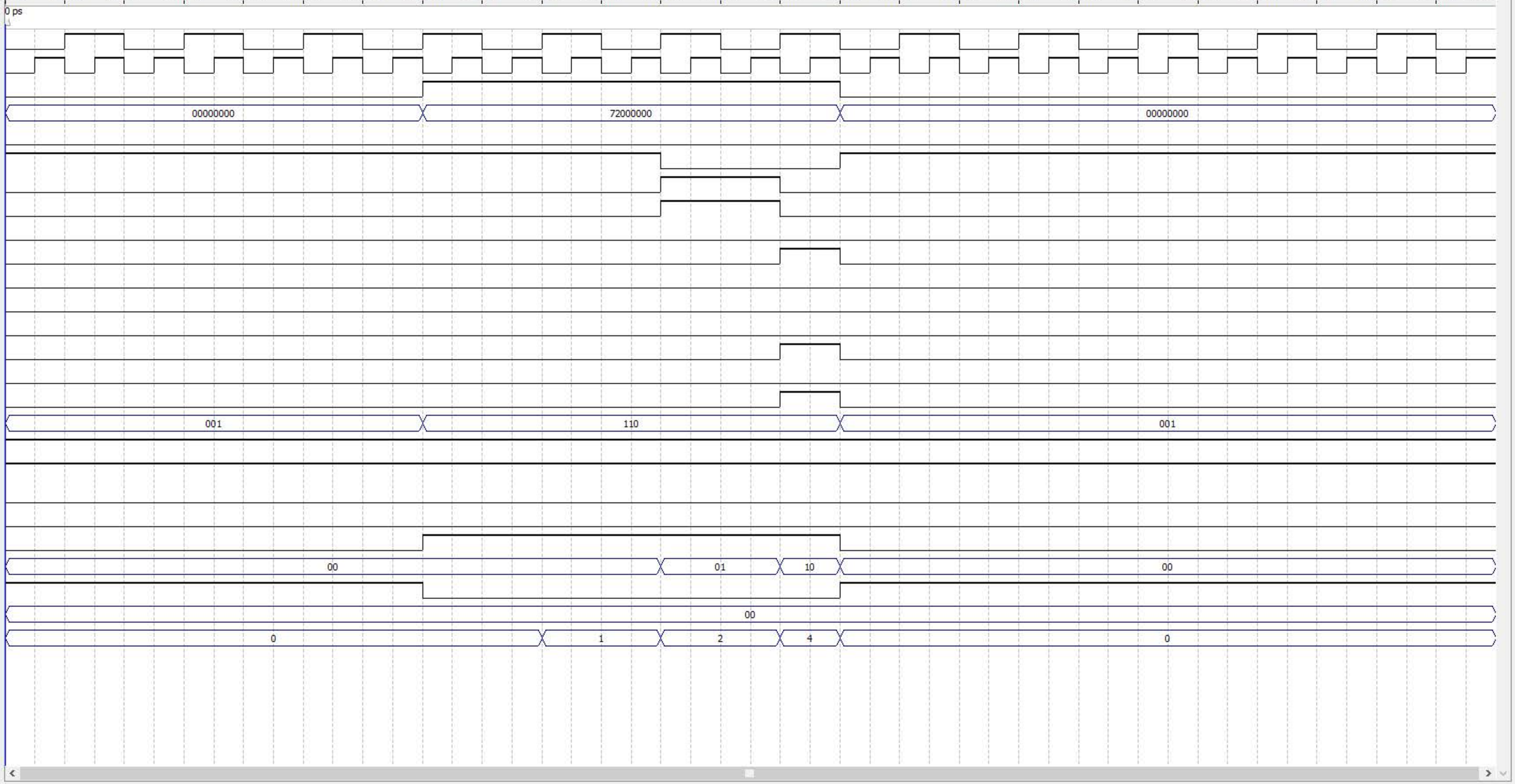
File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 512.35 ns | Interval: 512.35 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us



0% 00:00:00

ENG 5:17 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

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Master Time Bar: 0 ps Pointer: Interval: Start: End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | 72000000 | 00000000

ALU_op: 001 | 110 | 001

DATA_Mux: 00 | 01 | 10 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 1 | 0

0% 00:00:00

ENG 5:17 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 982.6 ns | Interval: 982.6 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B 1
ld_PC	B 0
inc_PC	B 0
clr_A	B 0
ld_A	B 0
clr_B	B 0
ld_B	B 0
clr_C	B 0
ld_C	B 0
clr_Z	B 0
ld_Z	B 0
ALU_op	B 001
en	B 1
wen	B 1
A_Mux	B 0
B_Mux	B 0
REG_Mux	B 0
DATA_Mux	B 00
IM_MUX1	B 1
IM_MUX2	B 00
T	U 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

INST: 00000000 | A000BBBB | 00000000

ALU_op: 001

DATA_Mux: 00 | 01 | 00

IM_MUX2: 00

T: 0 | 1 | 2 | 4 | 0

0% 00:00:00

ENG 6:05 PM

Simulation Waveform Editor - D:/RYERSON_S2020/coe608_2020/lab5_1/Lab5/lab5 - lab5 - [simulation/qsim/lab5.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps | Pointer: 474.99 ns | Interval: 474.99 ns | Start: | End:

Name	Value at 0 ps
clk	B 0
mclk	B 0
enable	B 0
INST	H 00000000
clr_IR	B 0
ld_IR	B X
ld_PC	B X
inc_PC	B X
clr_A	B X
ld_A	B X
clr_B	B X
ld_B	B X
clr_C	B X
ld_C	B X
clr_Z	B X
ld_Z	B X
ALU_op	B XXX
en	B X
wen	B X
A_Mux	B X
B_Mux	B X
REG_Mux	B X
DATA_Mux	B XX
IM_MUX1	B X
IM_MUX2	B XX
T	U X

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns 520.0 ns 560.0 ns 600.0 ns 640.0 ns 680.0 ns 720.0 ns 760.0 ns 800.0 ns 840.0 ns 880.0 ns 920.0 ns 960.0 ns 1.0 us

0 ps

00000000 A000BBBB 00000000

001

00 01 00

00

0 1 2 4 1 0

0% 00:00:00

ENG 6:05 PM