```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_unsigned.all;
4
5   entity lze is
6      port(
7         lze_in: in std_logic_vector(31 downto 0);
8         lze_out: out std_logic_vector(31 downto 0));
9   end lze;
10
11  architecture behavior of lze is
12     signal zeros : std_logic_vector(31 downto 16) := (others => '0');
13        begin
14           lze_out <= zeros & lze_in(15 downto 0);
15  end behavior;
16
17
```