```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity two_bit_asu is
   port (
   a, b: in std_logic_vector(1 downto 0);
   add_sub: in std_logic;
   result: out std_logic_vector(1 downto 0));
end two_bit_asu;

architecture behavior of two_bit_asu is
   begin
      process(a,b,add_sub)
         begin
            if add_sub = '0' then --adding
               result <= a or b;
            elsif add_sub = '1' then --subtracting
               result <= (a or (not b))+ 1;
            end if;
      end process;
end behavior;
```