```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   entity pc is
7      port(
8      clr, clk, ld, inc: in std_logic;
9      d: in std_logic_vector(31 downto 0);
10     q: inout std_logic_vector(31 downto 0));
11  end pc;
12
13  architecture description of pc is
14     begin
15        process(clk,clr,ld,inc)
16           begin
17              if clr = '0' then
18                 q <= (others => '0');
19                 elsif rising_edge(clk) then
20                    if ld = '1' then
21                       if inc = '0' then
22                       q <= d;
23                          if ld = '1' and inc = '1' then
24                             q <= q+4;
25                          end if;
26                       end if;
27                    end if;
28             end if;
29       end process;
30  end description;
```