```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   entity lab1_light is
4      port
5      (x1, x2 : in std_logic;
6      f : out std_logic);
7   end lab1_light;
8
9   architecture logicfunction of lab1_light is
10     begin
11        f <= ((x1 and (not x2)) or ((not x1) and x2));
12     end logicfunction;
13
14
15
```