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1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5
6  ENTITY adder32 IS
7      PORT(cin          :IN STD_LOGIC;
8           mode         :IN STD_LOGIC; -- 1 = sub , 0 = add
9           x             : in std_logic_vector(31 downto 0);
10          y             : in std_logic_vector(31 downto 0);
11          s             : out std_logic_vector(31 downto 0);
12          cout          :OUT STD_LOGIC
13      );
14  end adder32;
15
16  ARCHITECTURE description of adder32 IS
17      SIGNAL c31,c30,c29,c28,c27,c26,c25,c24,c23,c22,c21,c20,c19,c18,c17,c16,c15,c14,c13,c12,
18      c11,c10,c9,c8,c7,c6,c5,c4,c3,c2,c1,c0 : STD_LOGIC;
19      COMPONENT adder
20          port(
21              x : in std_logic;
22              y : in std_logic;
23              mode : in std_logic;
24              cin : in std_logic;
25              cout : out std_logic;
26              s : out std_logic
27          );
28      END COMPONENT;
29  BEGIN
30      --st0: adder port map (x(0), y(0), mode, cin, c1, s(0));
31      st0: adder port map (x(0), y(0), mode, mode, c1, s(0));
32      st1: adder port map (x(1), y(1), mode, c1, c2, s(1));
33      st2: adder port map (x(2), y(2), mode, c2, c3, s(2));
34      st3: adder port map (x(3), y(3), mode, c3, c4, s(3));
35      st4: adder port map (x(4), y(4), mode, c4, c5, s(4));
36      st5: adder port map (x(5), y(5), mode, c5, c6, s(5));
37      st6: adder port map (x(6), y(6), mode, c6, c7, s(6));
38      st7: adder port map (x(7), y(7), mode, c7, c8, s(7));
39      st8: adder port map (x(8), y(8), mode, c8, c9, s(8));
40      st9: adder port map (x(9), y(9), mode, c9, c10, s(9));
41      st10: adder port map (x(10), y(10), mode, c10, c11, s(10));
42      st11: adder port map (x(11), y(11), mode, c11, c12, s(11));
43      st12: adder port map (x(12), y(12), mode, c12, c13, s(12));
44      st13: adder port map (x(13), y(13), mode, c13, c14, s(13));
45      st14: adder port map (x(14), y(14), mode, c14, c15, s(14));
46      st15: adder port map (x(15), y(15), mode, c15, c16, s(15));
47      st16: adder port map (x(16), y(16), mode, c16, c17, s(16));
48      st17: adder port map (x(17), y(17), mode, c17, c18, s(17));
49      st18: adder port map (x(18), y(18), mode, c18, c19, s(18));
50      st19: adder port map (x(19), y(19), mode, c19, c20, s(19));
51      st20: adder port map (x(20), y(20), mode, c20, c21, s(20));
52      st21: adder port map (x(21), y(21), mode, c21, c22, s(21));
53      st22: adder port map (x(22), y(22), mode, c22, c23, s(22));
54      st23: adder port map (x(23), y(23), mode, c23, c24, s(23));
55      st24: adder port map (x(24), y(24), mode, c24, c25, s(24));
56      st25: adder port map (x(25), y(25), mode, c25, c26, s(25));
57      st26: adder port map (x(26), y(26), mode, c26, c27, s(26));
58      st27: adder port map (x(27), y(27), mode, c27, c28, s(27));
59      st28: adder port map (x(28), y(28), mode, c28, c29, s(28));
60      st29: adder port map (x(29), y(29), mode, c29, c30, s(29));
61      st30: adder port map (x(30), y(30), mode, c30, c31, s(30));
62      st31: adder port map (x(31), y(31), mode, c31, cout, s(31));
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62     end description;  
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