```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5  use ieee.numeric_std.all;
6  use ieee.numeric_bit.all;
7
8  entity bcd7seg is
9     port(
10       bcd_in: in std_logic_vector(3 downto 0);
11       sevenseg: out std_logic_vector(6 downto 0));
12 end bcd7seg;
13
14 architecture behavior of bcd7seg is
15    begin
16       process(bcd_in)
17          begin
18             case bcd_in is
19                when "0000" => sevenseg <= "0000001"; --0
20                when "0001" => sevenseg <= "1001111"; --1
21                when "0010" => sevenseg <= "0010010"; --2
22                when "0011" => sevenseg <= "0000110"; --3
23                when "0100" => sevenseg <= "1001100"; --4
24                when "0101" => sevenseg <= "0100100"; --5
25                when "0110" => sevenseg <= "0100000"; --6
26                when "0111" => sevenseg <= "0001111"; --7
27                when "1000" => sevenseg <= "0000000"; --8
28                when "1001" => sevenseg <= "0000100"; --9
29                when "1010" => sevenseg <= "0001000"; --A
30                when "1011" => sevenseg <= "1100000"; --b
31                when "1100" => sevenseg <= "0110001"; --C
32                when "1101" => sevenseg <= "1000010"; --d
33                when "1110" => sevenseg <= "0110000"; --E
34                when "1111" => sevenseg <= "0111000"; --F
35             end case;
36       end process;
37 end behavior;
38
39
```