

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5  entity register32 is
6      port (
7          d: in std_logic_vector(31 downto 0);
8          ld,clr,clk: in std_logic;
9          Q: out std_logic_vector(31 downto 0));
10 end register32;
11
12 architecture description of register32 is
13     begin
14         process (ld, clr,clk)
15             begin
16                 if ld = '0' or clr = '1' then
17                     Q <= (others => '0');
18                 elsif rising_edge(clk) then
19                     Q <= d;
20                 end if;
21             end process;
22         end description;
23
```