```
1
   library ieee;
 2 use ieee.std_logic_1164.all;
 3 use ieee.numeric_std.all;
 4
 5
   entity red is
 6
     port(
7
          red_in : in std_logic_vector(31 downto 0);
8
          red_out : out unsigned(7 downto 0));
9
   end red;
10
11
    architecture behavior of red is
12
      begin
13
          red_out <= unsigned (red_in(7 downto 0));</pre>
14
   end behavior;
15
16
```