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COE 608: Computer Architecture and Design

COE 608: Lab 3, Part 1 Report

Purpose

The purpose of this lab is to generate the components of a 32-bit ALU, with six different operations. The addition and subtraction units must be done in structural form of VHDL.

Design and Implementation

The goal of the 32-bit ALU is to perform the following operations:



Figure 1: ALU Operations

The first step is to create the adder, since it is not possible to use behavioral model in this lab to create the adder circuit.



Figure 2: Full Adder Circuit with logical functions

Next, the operation of the two-to-one multiplexer is illustrated below:



Figure 3: Two-to-one multiplexer

Next, the binary-coded-decimal to seven-segment converter is shown below. It is assumed that the seven-segment display is cathode-active.



Figure 4: BCD to 7 segment display Truth Table

One-bit Adder: Functional and Timing Waveforms

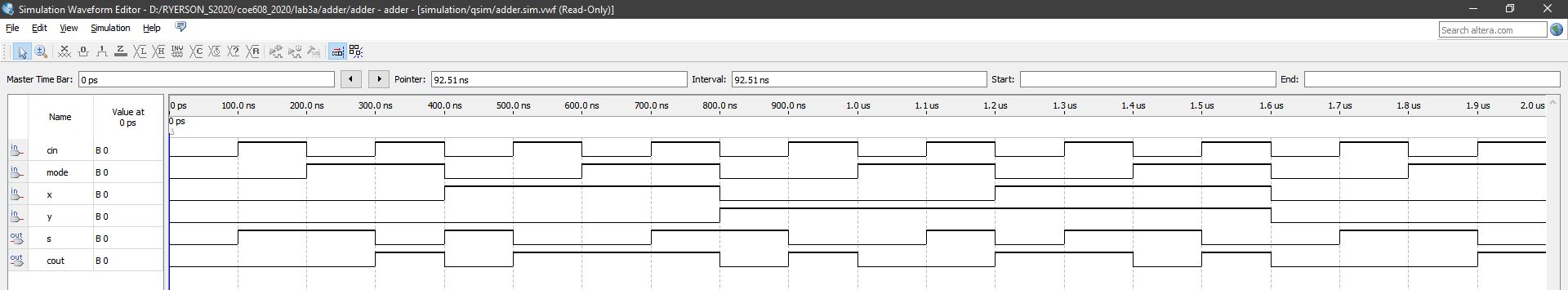


Figure 5: 1-bit Adder Functional Waveform

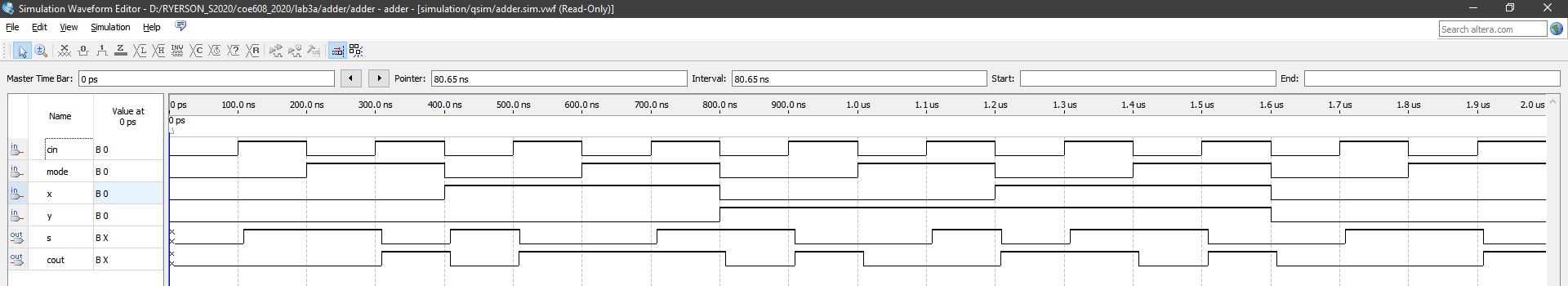


Figure 6: 1-bit Adder Timing Waveform

32-bit Adder: Functional and Timing Waveforms

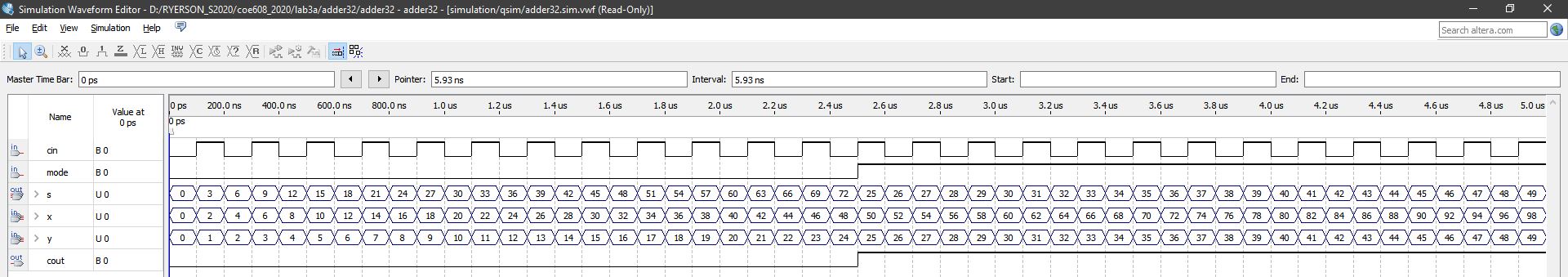


Figure 7: 32-bit Adder Functional Waveform

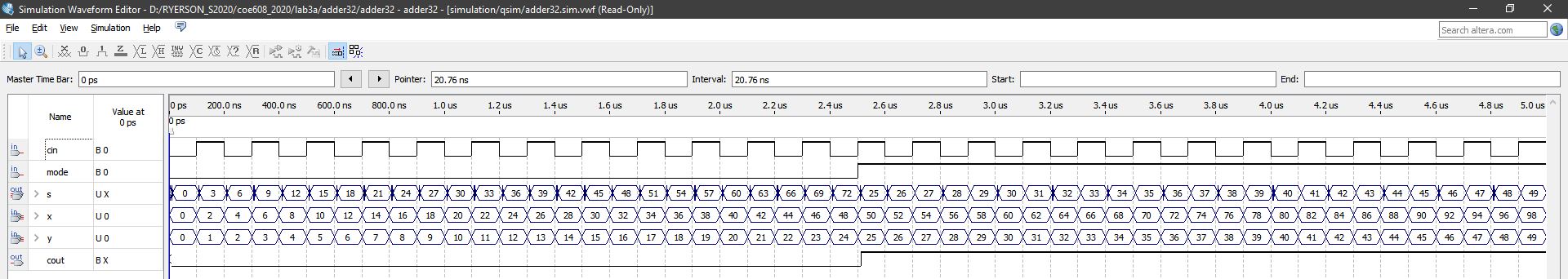


Figure 8: 32-bit Adder Timing Waveform

2 to 1 Multiplexer: Functional and Timing Waveforms

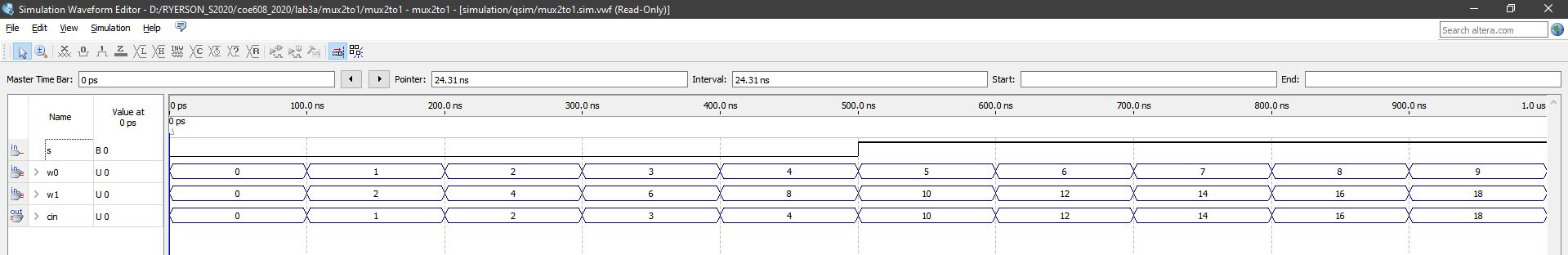


Figure 9: 2-to1 Multiplexer Functional Waveform

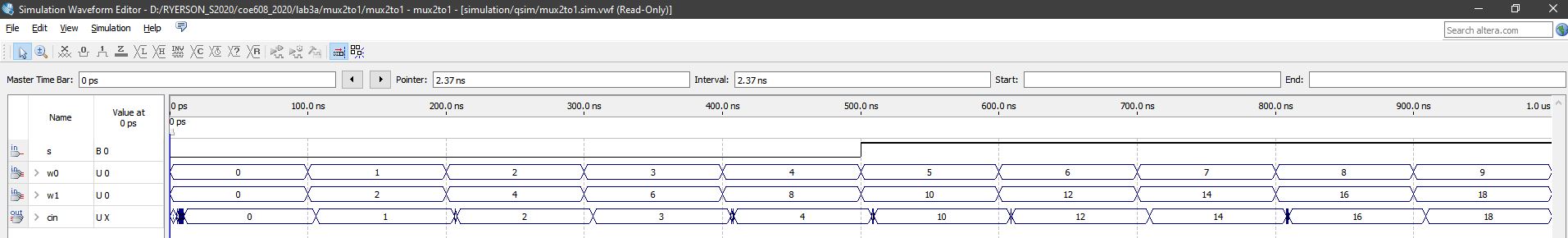


Figure 10: 2-to-1 Multiplexer Timing Waveform

32-bit ALU: Functional and Timing Waveforms

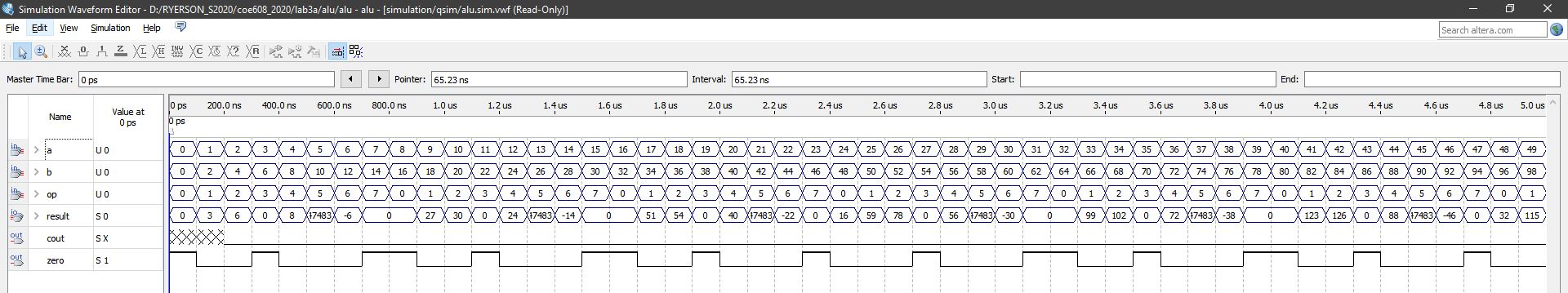


Figure 11: 32-bit ALU Functional Waveform

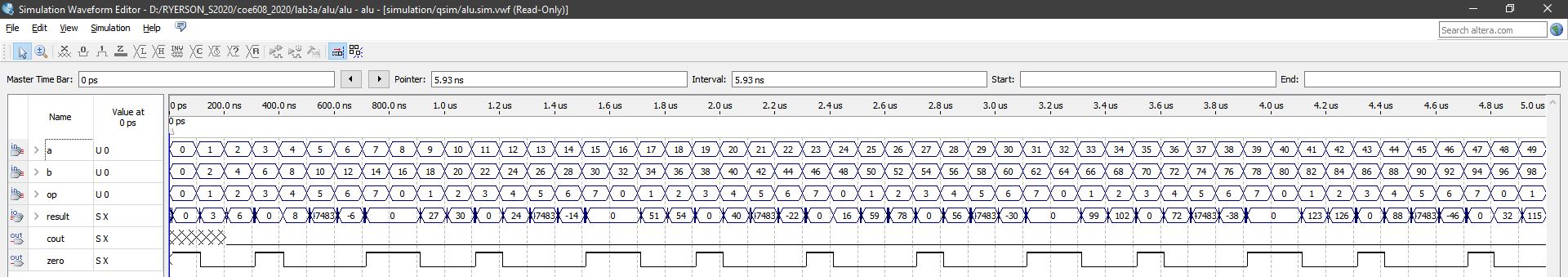


Figure 12: 32-bit ALU Timing Waveform

Discussions and Conclusions

All of the above devices work as expected. The worst-case delay of the 32-bit ALU is 1 ns, for most outputs. The longest delay occurs at the positive or negative signs of the output. The worst delay for the negative output symbol is 40 ns.

Appendices: VHDL Codes for the ALU and other Supporting Devices

The files are attached as PDF to make this document easier to read.