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COE 608: Computer Architecture and Design

COE 608: Lab 4, Part 1 Report

Objective

The purpose of this lab is to create a memory module for the 32-bit ALU, and later the instruction set architecture (ISA) for the million instructions per second (MIPS) ISA.

Design and Implementation

Provided below is the truth table for the memory module. The address is an 8-bit data, and the data-in and data-outs are 32-bit data. See Figure 1: Memory Module Truth Table.



Figure 1: Memory Module Truth Table

Observations and Results

Below are the observations from functional and timing waveforms: See Figure 2: Memory Module Functional Waveform and Figure 3: Memory Module Timing Waveform.

Memory Module: Functional and Timing

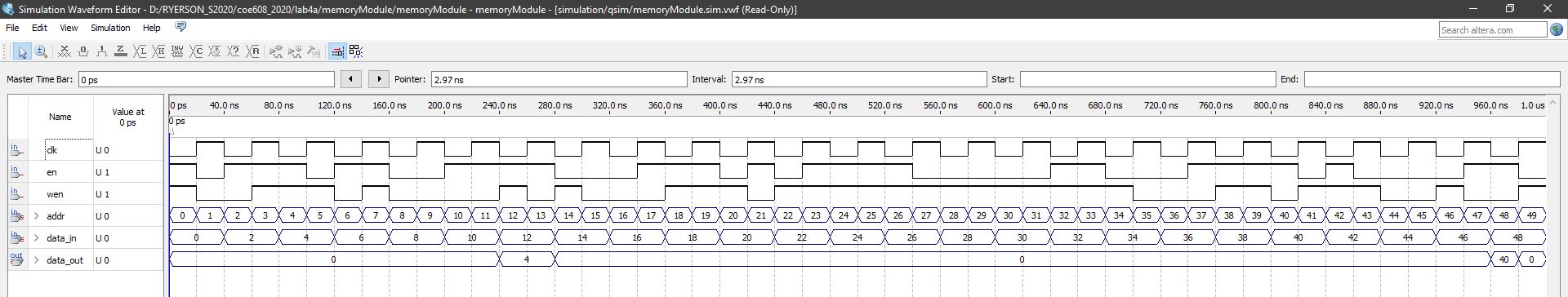


Figure 2: Memory Module Functional Waveform

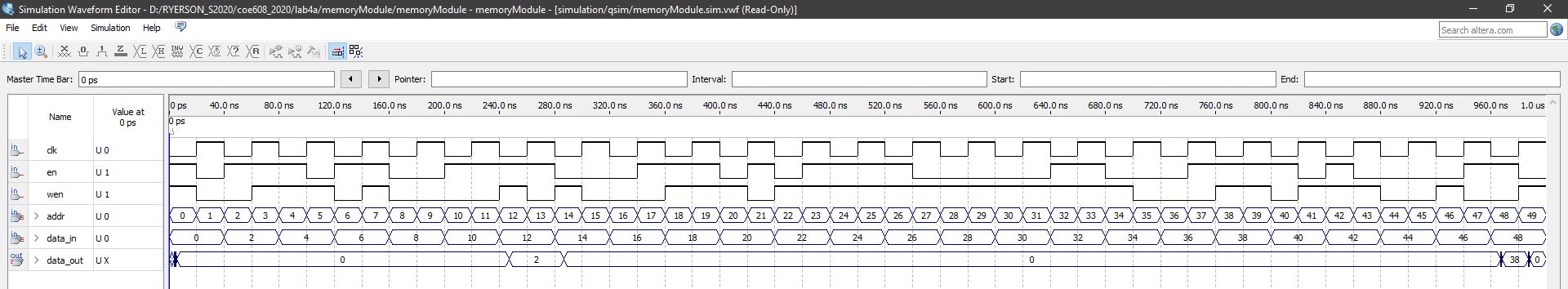


Figure 3: Memory Module Timing Waveform

Discussions and Conclusions

The memory module works as intended. The worst case delays for the memory module is 5 ns, as can be observed from the timing simulation waveform.

Appendix: VHDL Codes and Screenshots of Waveforms

I have provided the VHDL and screenshots of the waveforms for easier reading.