Ryerson University
Department of Electrical & Computer Engineering
ELE328 — Digital Systems

# F2004 Final Examination

**Name:** _____ **ID No.:** _____ **Section:** _____

**Time Limit:** 2 hour and 50 minutes **Professors:** Chen, Y.C., Mekhiel, N., Sedaghat, R.

- Closed-book examination, no calculator or any other aids allowed.
- Answer all questions in the space provided and show all steps for full credit.
- Circle the name of your Professor shown above.

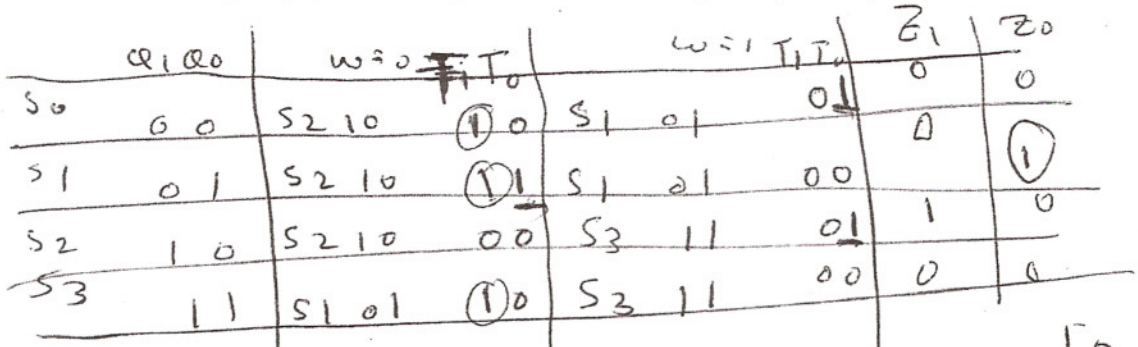
1. The state table of a finite-state machine (FSM) with one input $w$ and 2 outputs $z_1$ and $z_0$ is given below:

| Present State | Next State | | Outputs | |
|---|---|---|---|---|
| | $w=0$ | $w=1$ | $z_1$ | $z_0$ |
| S0 | S2 | S1 | 0 | 0 |
| S1 | S2 | S1 | 0 | 1 |
| S2 | S2 | S3 | 1 | 0 |
| S3 | S1 | S3 | 0 | 0 |

(a) (1 mark) Explain whether the given FSM is a Moore-type or Mealy-type state machine?

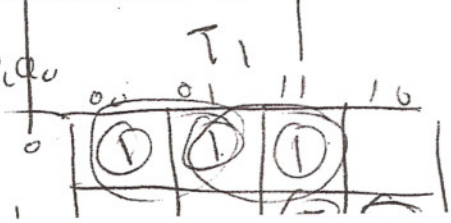
$z_1, z_0$ depend on P. State only.
It is a Moore type.

(b) (9 marks) The given FSM is to be implemented as a synchronous sequential circuit with T flip-flops using the state assignments: S0=00, S1=01, S2=10, S3=11. Derive the equations for the inputs to the T flip-flops, and the equations for the outputs $z_1$ and $z_0$.

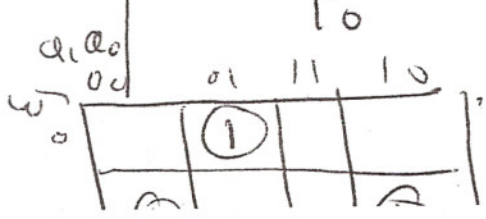



$Z_0 = \bar{Q}_1 Q_0$

$Z_1 = Q_1 \bar{Q}_0$

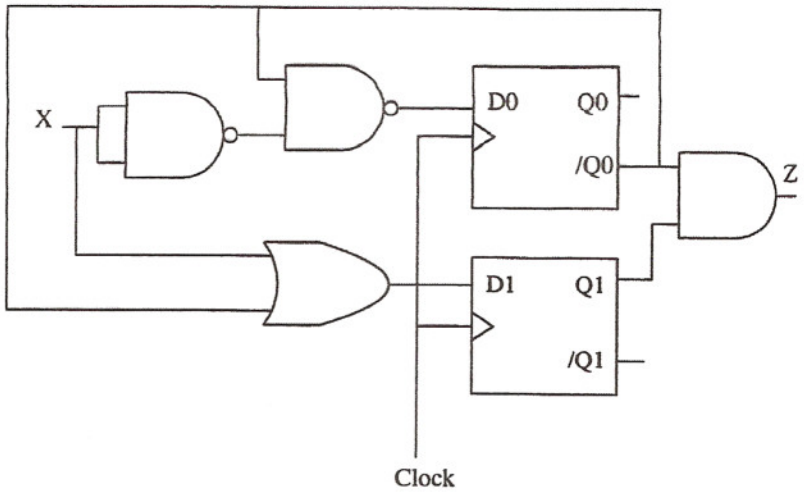



$T_1 = \bar{w} \bar{Q}_1$




$T_0 = w \bar{Q}_1 \bar{Q}_0 + \bar{w} \bar{Q}_1 Q_0$

2. Consider the following circuit which implements a finite-state machine (FSM):




(a) (4 marks) Derive the state assigned table for the FSM.

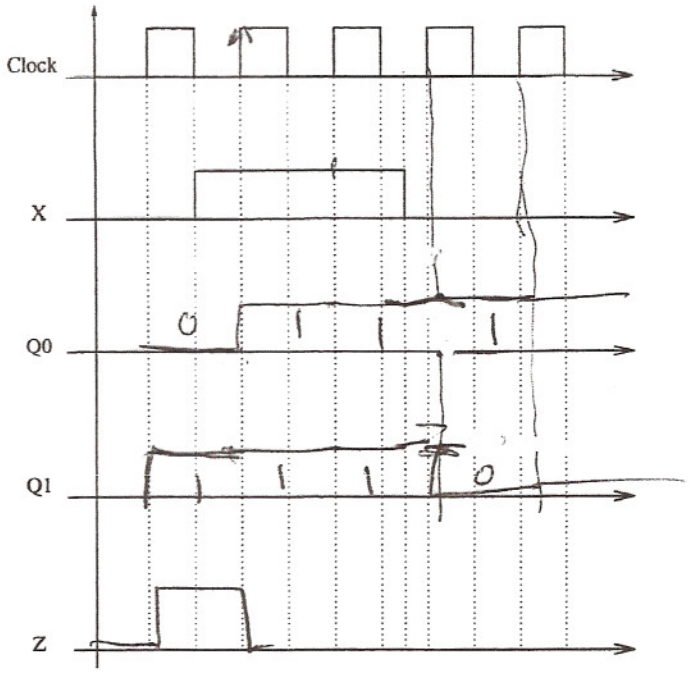
$D_0 = \overline{\overline{X} \cdot \overline{Q_0}} = X + Q_0$

$D_1 = X + \overline{Q_0}$

$Z = Q_1 \cdot \overline{Q_0}$

| P.S $Q_1Q_0$ | N.S $X=0$ $D_1D_0$ | $X=1$ $D_1D_0$ | Z |
|---|---|---|---|
| 0 00 | $S_2$ 1 0 | $S_3$ 1 1 | 0 |
| 1 01 | $S_1$ 0 1 | $S_3$ 1 1 | 0 |
| 2 10 | $S_2$ 1 0 | $S_3$ 1 1 | 1 |
| 3 11 | $S_1$ 0 1 | $S_3$ 1 1 | 0 |

(b) (4 marks) Complete the following timing diagram for the circuit by assuming $Q_1 = Q_0 = 0$ at the beginning.



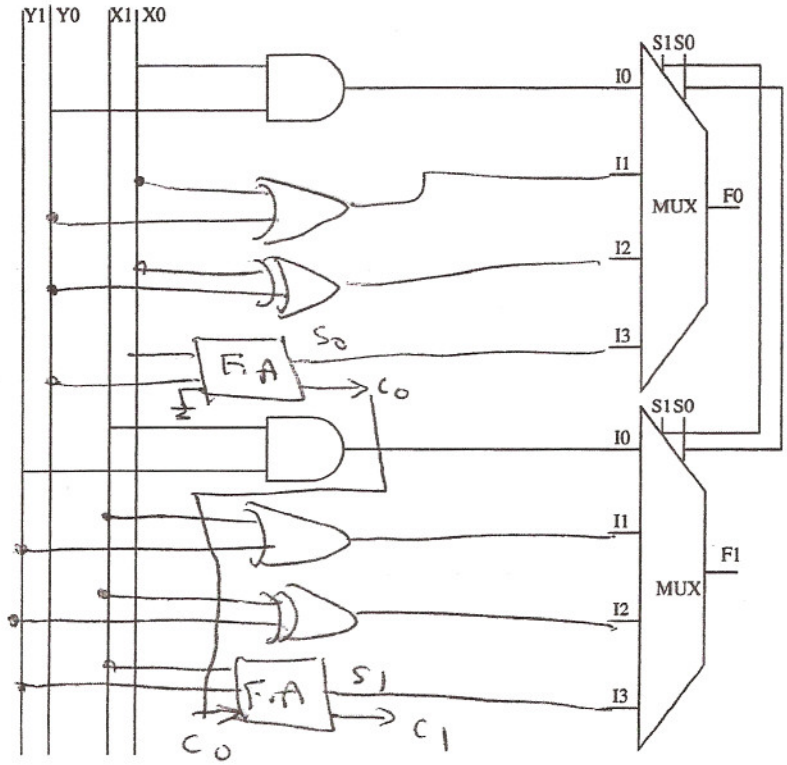

(c) (4 marks) Derive the state assigned table if JK flip-flops (instead of D flip-flips) are to be used to implement the FSM.

| $Q_1Q_0$ | $X=0$ N.S | $J_1K_1$ $J_0K_0$ | $X=1$ | $J_1K_1$ $J_0K_0$ | Z |
|---|---|---|---|---|---|
| 00 | 10 | 1X 0X | 11 | 1X 1X | 0 |
| 01 | 01 | 0X X0 | 11 | 1X X0 | 0 |
| 10 | 10 | X0 0X | 11 | X0 1X | 1 |
| 11 | 01 | X1 X0 | 11 | X0 X0 | 0 |

3. (10 marks) The circuit below is used as a part of an ALU to perform logical and arithmetic operations on the 2-bit inputs $X = X_1X_0$ and $Y = Y_1Y_0$. The operation to be performed is determined by the function select input $S_1S_0$ to produce the output $F = F_1F_0$ according to the following table:

| $S_1S_0$ | Operations |
|---|---|
| 00 | F = X AND Y |
| 01 | F = X OR Y |
| 10 | F = X XOR Y |
| 11 | F = X + Y (addition) |

Complete the implementation of the circuit shown below according to the given requirements:



4. Consider the following VHDL code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY fsm IS
  PORT( Clock,Resetn,w   : IN STD_LOGIC;
        Z    : OUT STD_LOGIC );
END fsm;

ARCHITECTURE Behavior OF fsm IS
  TYPE State_type IS (A,B,C);
  SIGNAL y: State_type;
BEGIN
  PROCESS(Resetn, Clock)
  BEGIN
     IF Resetn = '0' THEN
              y<=A;
     ELSEIF (Clock'EVENT AND Clock = '1') THEN
       CASE y IS
           WHEN A =>
              IF w='0' THEN
                  y<=A;
              ELSE
                  y<=B;
              END IF;
           WHEN B =>
              IF w='0' THEN
                  y<=A;
              ELSE
                  y<=C;
              END IF;
           WHEN C =>
              IF w='0' THEN
                  y<=A;
              ELSE
                  y<=C;
              END IF;
       END CASE;
     ENDIF;
  END PROCESS;
       z<= '1' WHEN y=C ELSE '0';
END Behavior;
```

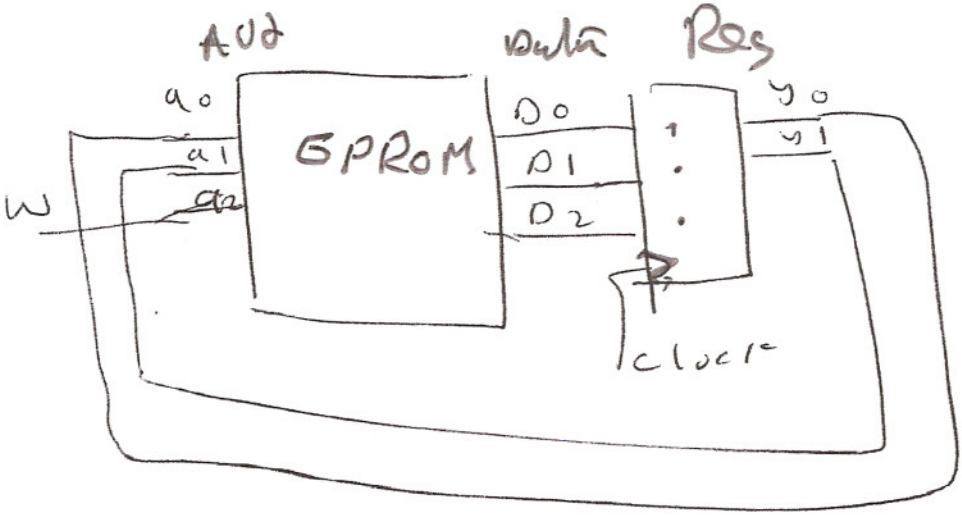
(a) (3 marks) Describe the behavior of the given FSM using a state diagram.

(b) Assume that an 8x4-bit EPROM is available, provide a programmable implementation of the FSM in Part (a):

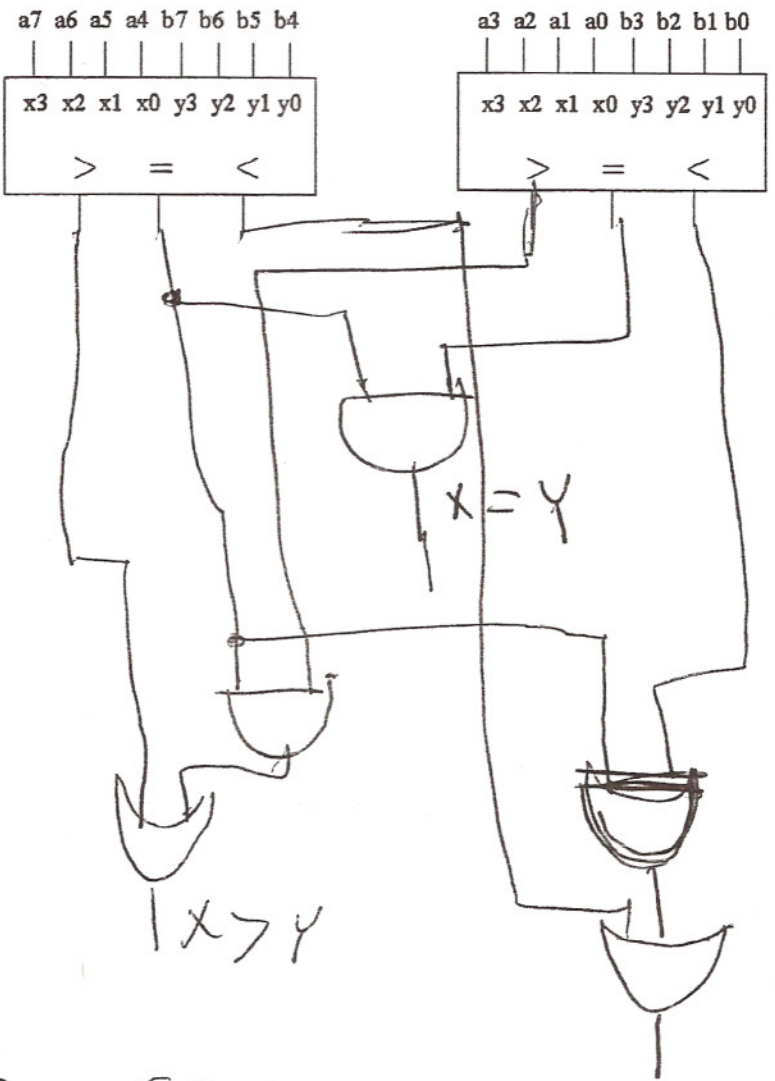
i. (4 marks) Fill in the contents of the EPROM in the table below by setting up the addresses of the EPROM as follow: $a_2 = w$, $a_1a_0 = y_1y_0$ (present state), and explain what the contents of the EPROM represents.

| Address $a_2a_1a_0$ | Contents $d_3d_2d_1d_0$ |
|---|---|
| 0 0 0 | 0 0 0 |
| 0 0 1 | 0 0 0 |
| 0 1 0 | 0 0 0 |
| 0 1 1 | 0 0 0 |
| 1 0 0 | 0 0 1 |
| 1 0 1 | 0 1 0 |
| 1 1 0 | 1 1 0 |
| 1 1 1 | 0 0 0 |

ii. (3 marks) Draw a schematic diagram for the implementation.



5. (10 marks) Two comparators for 4-bit unsigned numbers are available. Each comparator has two 4-bit inputs: $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$, and 3 logical outputs: $X$ greater than $Y$ (>), $X$ equal to $Y$ (=), and $X$ less than $Y$ (<). Construct a comparator for two 8-bit unsigned numbers $A = a_7a_6a_5a_4a_3a_2a_1a_0$ and $B = b_7b_6b_5b_4b_3b_2b_1b_0$ using the two 4-bit comparators and any additional logic gates, and draw the resulting circuit.




Examples:

- 53, 53 (=, =)
- 57, 53 (=, >)
- 37, 29 (>)
- 52, 57 (<)
- 37, 52 (<)

6. This question deals with the programmable processor module used in Lab 7. The function table of the 74181 ALU, and the instruction set of the processor are given in the Appendix.

(a) (5 marks) Determine the contents of the Program Counter (PC), Accumulator (ACCA), and the Carry Bit (C) *after* the execution of each of the following instructions using the given initial values of the Input Switches (Sw), Carry Bit (C), Program Counter (PC), Accumulator (ACCA) and content of the Memory Location 2 (M(2)).

Each of the following instructions has initial conditions as given:

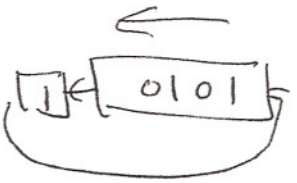
Sw = 1011 C = 0 PC = 0010 ACCA=0110 M(2) = 1010

| | PC | ACCA | C |
|---|---|---|---|
| (i) ADDA S | 0011 | 0001 | 1 |

1011 Sw
0110 AC
10001

Sw = 1100 C = 1 PC = 1100 ACCA=0101 M(2) = 0101

| | PC | ACCA | C |
|---|---|---|---|
| (ii) ROLA | 1101 | 1011 | 0 |




Sw = 0110 C = 1 PC = 1010 ACCA=0110 M(2) = 1010

| | PC | ACCA | C |
|---|---|---|---|
| (iii) JEQ 0011 | 0011 | 0110 | 1 |

Sw=0110 ?
A = 0110 ?
JMP ✓

Sw = 1011 C = 0 PC = 0010 ACCA=1111 M(2) = 1010

| | PC | ACCA | C |
|---|---|---|---|
| (iv) INCA | 0011 | 0000 | 1 |

1111
1
(1)0000

Sw = 1000 C = 0 PC = 0010 ACCA=0110 M(2) = 0111

| | PC | ACCA | C |
|---|---|---|---|
| (v) SUBA 2 | 0011 | 0110 | 0 |

0110
0111

0110
0111
−1 } = −2
1110

A = A − M(2)
= A + −M(2)
= 0110 − 01

(b) (2 marks) Fill in the microcode table for the following instructions:

| | EPROMs 1&2 Address Lines | | | | | | | EPROM1 | | | | | | | | EPROM2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | EPROM3 | | | | | | | PAL | ACCA | | ALU 181 | | | | | | DATA PATH | | | 161 | | EPROMs | |
| | JP | N0 | OP Code | | | | Mic Code | NCC | S1 | S0 | M | S3 | S2 | S1 | S0 | | /AS | WR | SM | /PE | CNT | A1+ | A0+ |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SUBA S | | | | | | | 0 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| | | | | | | | 0 1 | | | | | | | | | | | | | | | | |
| | | | | | | | 1 0 | | | | | | | | | | | | | | | | |
| | | | | | | | 1 1 | | | | | | | | | | | | | | | | |
| STAA N | | | | | | | 0 0 | 1 | 0 | 0 | X | 1 | X | X | X | X | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | | | | | | 0 1 | | | | | | | | | | | | | | | | |
| | | | | | | | 1 0 | | | | | | | | | | | | | | | | |
| | | | | | | | 1 1 | | | | | | | | | | | | | | | | |

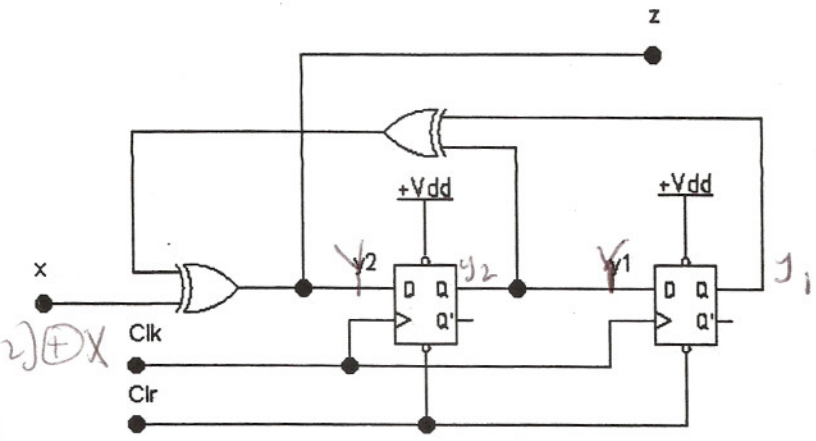
(c) (4 marks) Suppose that the STSW N instruction is required to be changed to a new instruction STEZ N. The new instruction STEZ N is used to compare the contents of the accumulator (ACCA) to the data from the Input Switches (Sw). If they are equal, a value of zero will be stored in the memory location N; otherwise, the next program instruction following the STEZ N instruction will be executed. Fill in the microcode for the STEZ N instruction in the following table:

| | EPROMs 1&2 Address Lines | | | | | | | EPROM1 | | | | | | | | EPROM2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | EPROM3 | | | | | | | PAL | ACCA | | ALU 181 | | | | | | DATA PATH | | | 161 | | EPROMs | |
| | JP | N0 | OP Code | | | | Mic Code | NCC | S1 | S0 | M | S3 | S2 | S1 | S0 | | /AS | WR | SM | /PE | CNT | A1+ | A0+ |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| STEZ N | 0 | 0 | | | | | 0 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | X | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| | 0 | 0 | | | | | 0 1 | 1 | 0 | 0 | X | X | X | X | X | X | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| | 0 | 0 | | | | | 1 0 | | | | | | | | | | | | | | | | |
| | 0 | 0 | | | | | 1 1 | | | | | | | | | | | | | | | | |
| STEZ N | 1 | 0 | | | | | 0 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | X | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| | 1 | 0 | | | | | 0 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | X | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | 1 | 0 | | | | | 1 0 | | | | | | | | | | | | | | | | |
| | 1 | 0 | | | | | 1 1 | | | | | | | | | | | | | | | | |

(d) (3 marks) Write a program (not to exceed 16 instructions) to swap the data that are already stored at memory locations 2 and 3. You may use other memory locations as temporary storage.

1 - LDA 2
2 - STA 4
3 - LDA 3
4 - STA 2
5 - LDA 4
6 - STA 3

1. Given the following logic circuit, derive its state table and state diagram. If the following sequence 1010110101 is applied to the $x$ input of the circuit with initial sate 01, determine the resulting output sequence on $z$ output. **(8 marks)**




(2)

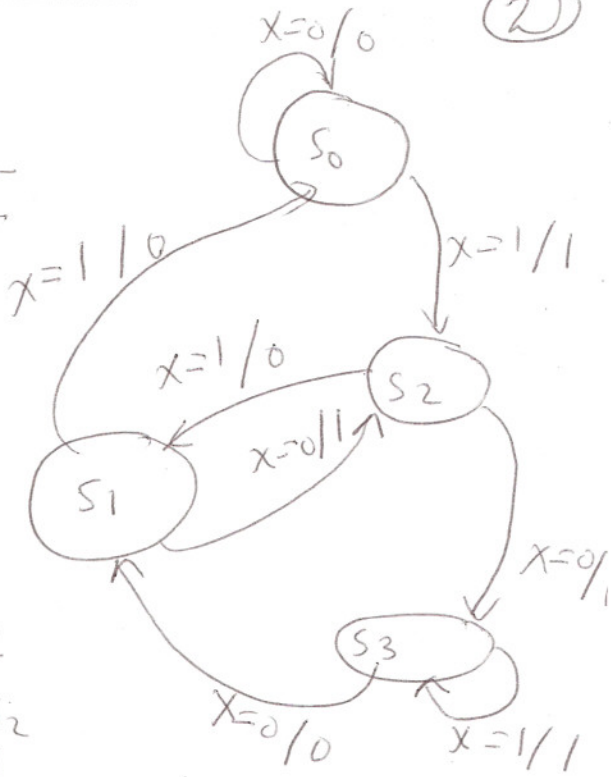
$Y_1 = y_2$

$Z = Y_2 = (y_1 \oplus y_2) \oplus X$

(2)

| $y_2y_1$ | $x=0$ | | $x=1$ | | $Z$ $x=0$ | $Z$ $x=1$ |
|---|---|---|---|---|---|---|
| $S_0$ 00 | $S_0$ | 00 | $S_2$ | 10 | 0 | 1 |
| $S_1$ 01 | $S_2$ | 10 | $S_0$ | 00 | 1 | 0 |
| $S_2$ 10 | $S_3$ | 11 | $S_1$ | 01 | 1 | 0 |
| $S_3$ 11 | $S_1$ | 01 | $S_3$ | 11 | 0 | 1 |

(2)




| X | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| $S_1$ | $S_0$ | $S_0$ | $S_2$ | $S_3$ | $S_3$ | $S_3$ | $S_1$ | $S_0$ | $S_0$ | $S_2$ |
| Z | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

(2)