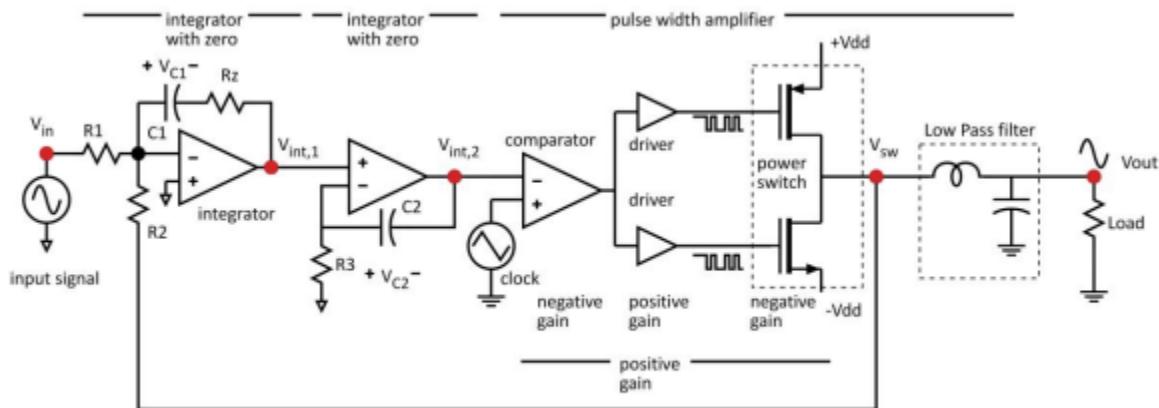


## 1. Objectives

The goal of this project is to design a digital audio power amplifier. These types of devices are often used for audio purposes, as the name suggests. Examples of their inclusion in devices might be loudspeakers or headphones. There are various steps regarding the construction of the device. For this portion of the project, our group is expected to have a complete circuit: soldered and fully tested. In doing so, conducting Matlab tests and running experiments with the provided software would help such that feasible performance as a function of loop bandwidth is understood. The design will include everything from the prior lab (pulse width modulation, driver module, and a low pass filter) plus other various modules that will complete the design.

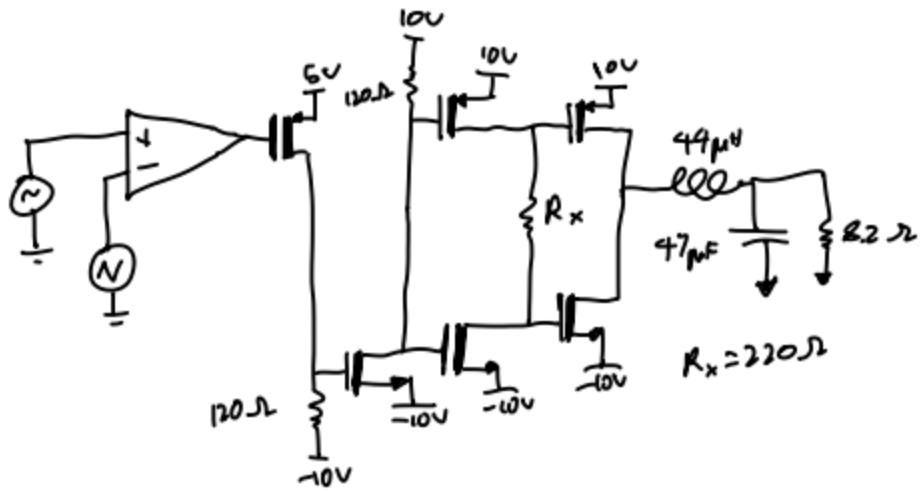
## 2. Circuit Diagram

For our circuit, we will be using the basic approach with sophisticated feedback

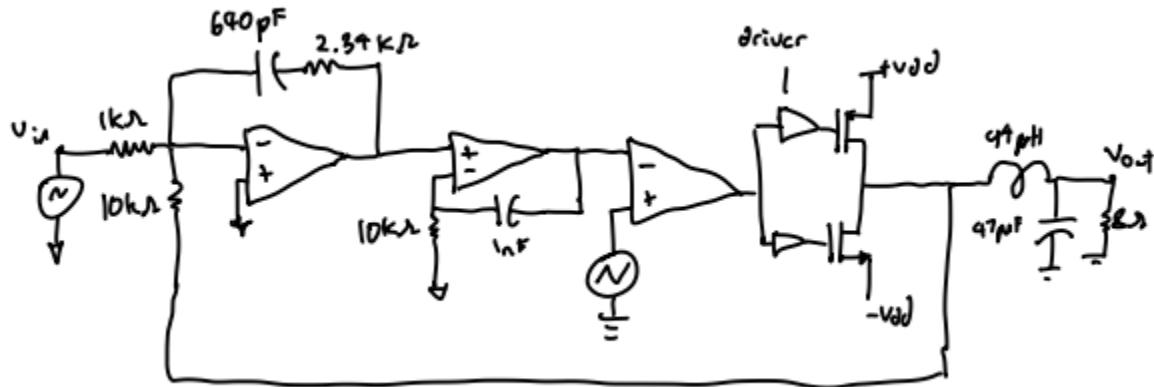


**Figure 7:** Pulse-width-modulation amplifier with more sophisticated negative feedback

**Anticipated Completed Design**



Driver Circuit from Part 2



Circuit with Values in Place

### 3. Design Discussion

The circuit must be optimized such that the wasted switching energy is low while maintaining high clock frequency and output power. The amplifier is a multi-stage design that is built with a triangle wave generator, a comparator-based PWM modulator, a power stage, and an output filter. The triangle wave generator will provide a high-frequency signal to ensure an accurate PWM generation. The comparator converts analog signals into a PWM signal. The power stage is effectively the switch, which needs to be power efficient to prevent too much wasted power. The low pass filter will remove much of the high-frequency switching components, as a filter might do, and recover the base analog signal. Ultimately the circuit will empower that same

analog signal. We anticipate utilizing the two integrator design to reduce distortion. Indeed we may need to resolve the driver module as well. Our initial soldered design seemed to have issues with efficiency, however, it produced the correct results.

#### 4. Bias Analysis

Feedback Loop Analysis:

$$V_{DD} = 10V$$

$$f_2 = \text{user-defined} \rightarrow 10\text{kHz} \quad f_{loop} = \text{user-defined} \rightarrow 50\text{kHz}$$

$$A_{climb} = 10$$

$$R_1 = \frac{R_2}{A_{climb}} = \frac{10\text{ k}\Omega}{10} = 1\text{k}\Omega$$

$$f_{i1} = f_{loop} \left( \frac{V_A}{V_{DD}} \right) = (50\text{kHz}) \left( \frac{5}{10} \right) = 25\text{kHz}$$

$$C_1 = \frac{1}{2\pi f_{i1} R_1} = \frac{1}{2\pi (25 \times 10^3) (10 \times 10^3)} \approx 636 \text{ pF} \\ \rightarrow 640 \text{ pF}$$

$$f_{z1} = 2(50\text{kHz}) = 100\text{kHz}$$

$$R_2 = \frac{1}{2\pi f_{z1} R_1} \approx 2.34\text{k}\Omega$$

$$R_3 = \text{user-defined} \rightarrow 10\text{k}\Omega$$

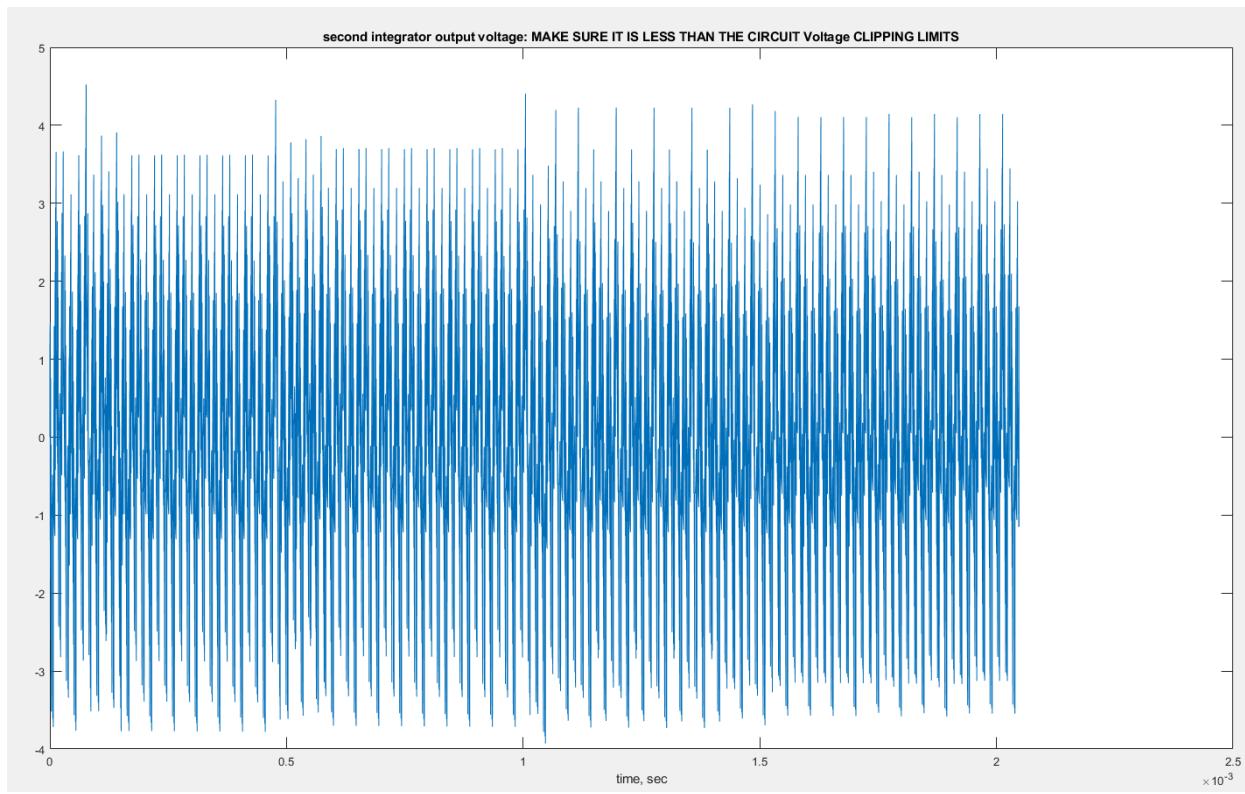
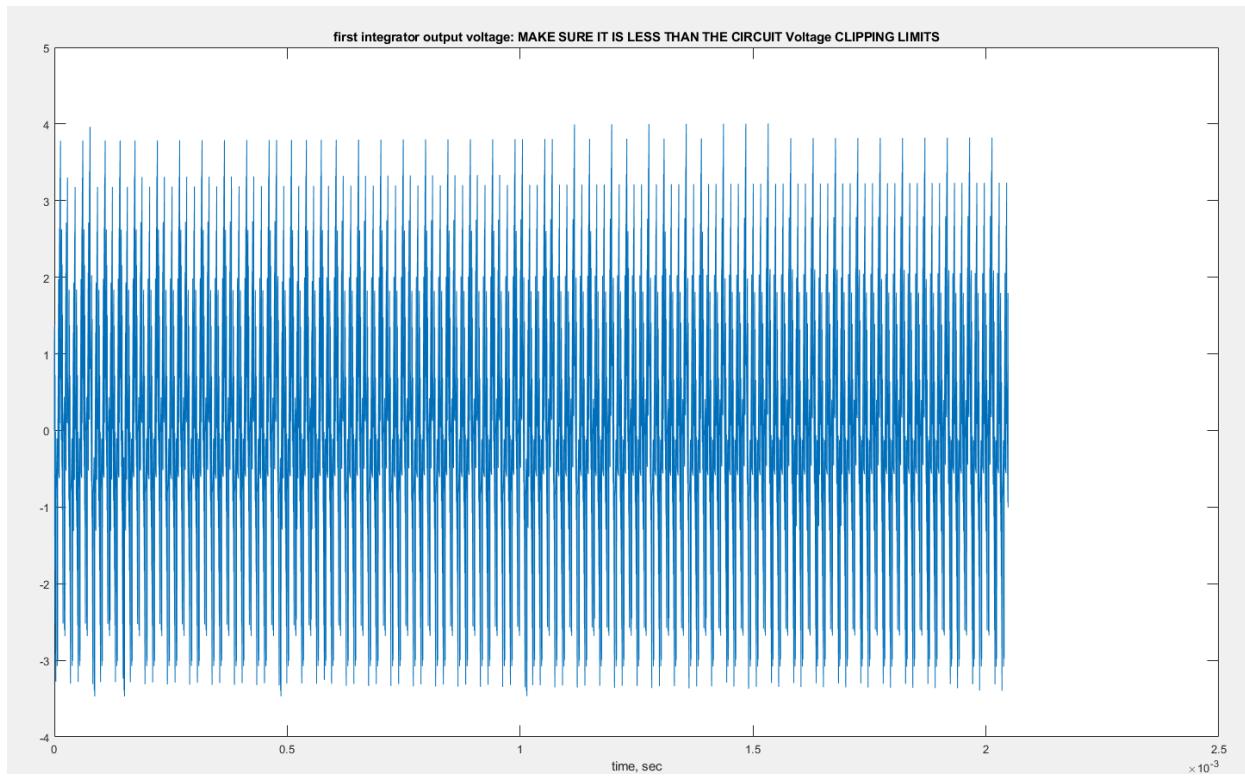
$$f_{i2} = \frac{80\text{kHz}}{3} = 16.7\text{kHz}$$

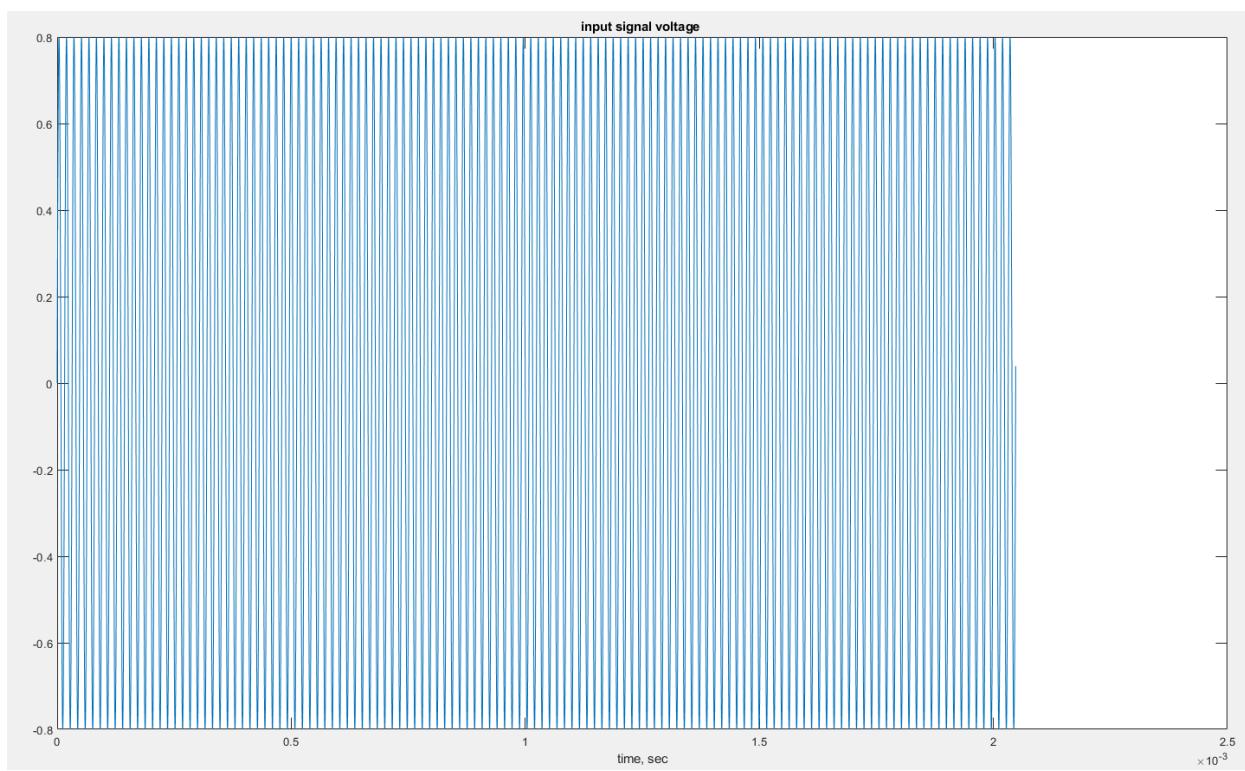
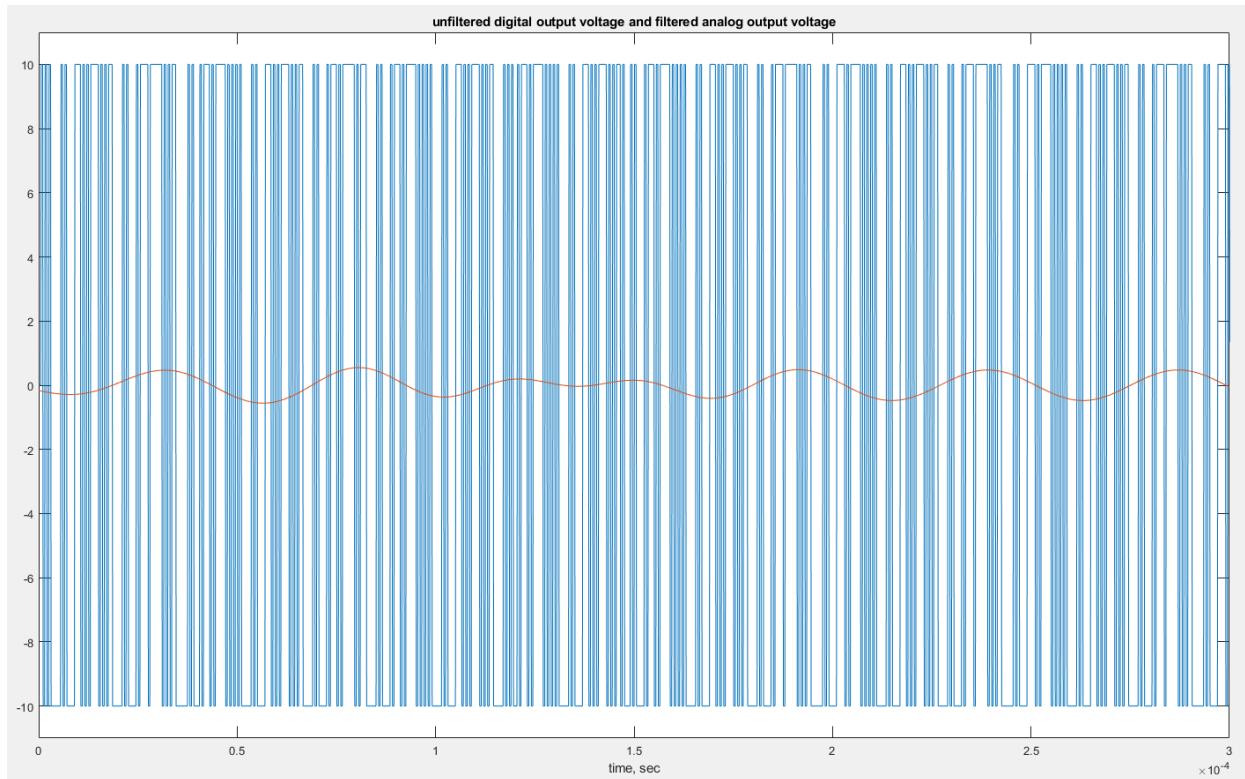
$$C_2 = \frac{1}{2\pi f_{i2} R_3} = \left( \frac{1}{2\pi (16.7\text{kHz}) (10\text{k})} \right) \approx 1\text{nF}$$

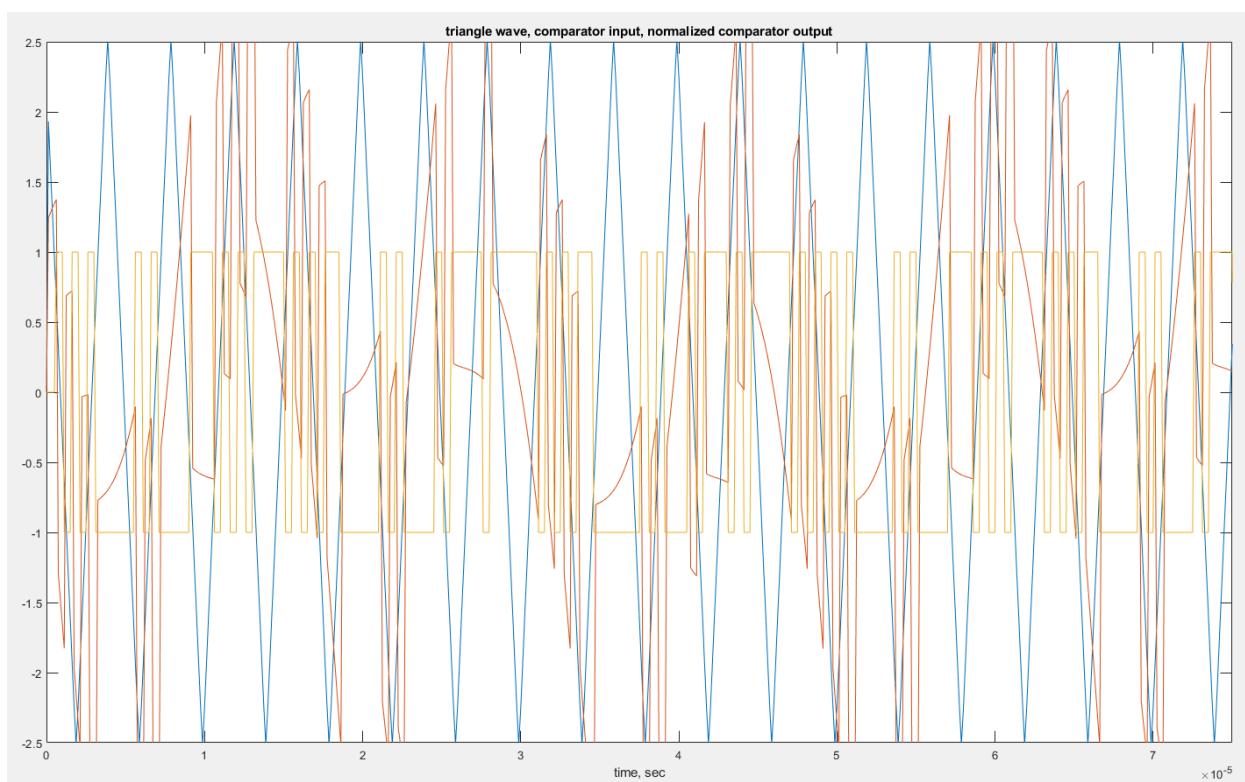
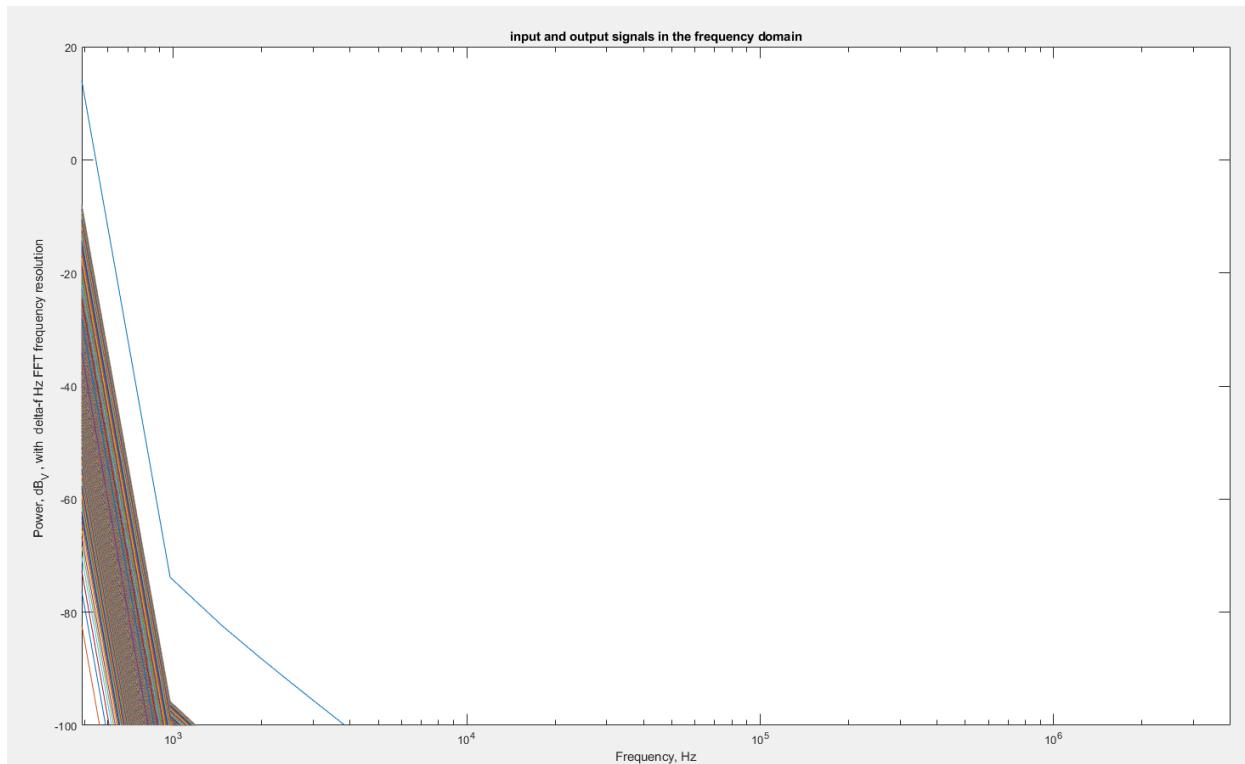
#### 5. Performance Analysis

The following are the Matlab experimentation done to test our values and observe simulated results. The following values are the conditions we set in place outside of the calculated/user-defined values:

```
N=2^14
f_tri=250E3
v_in_mag = 0.8
```



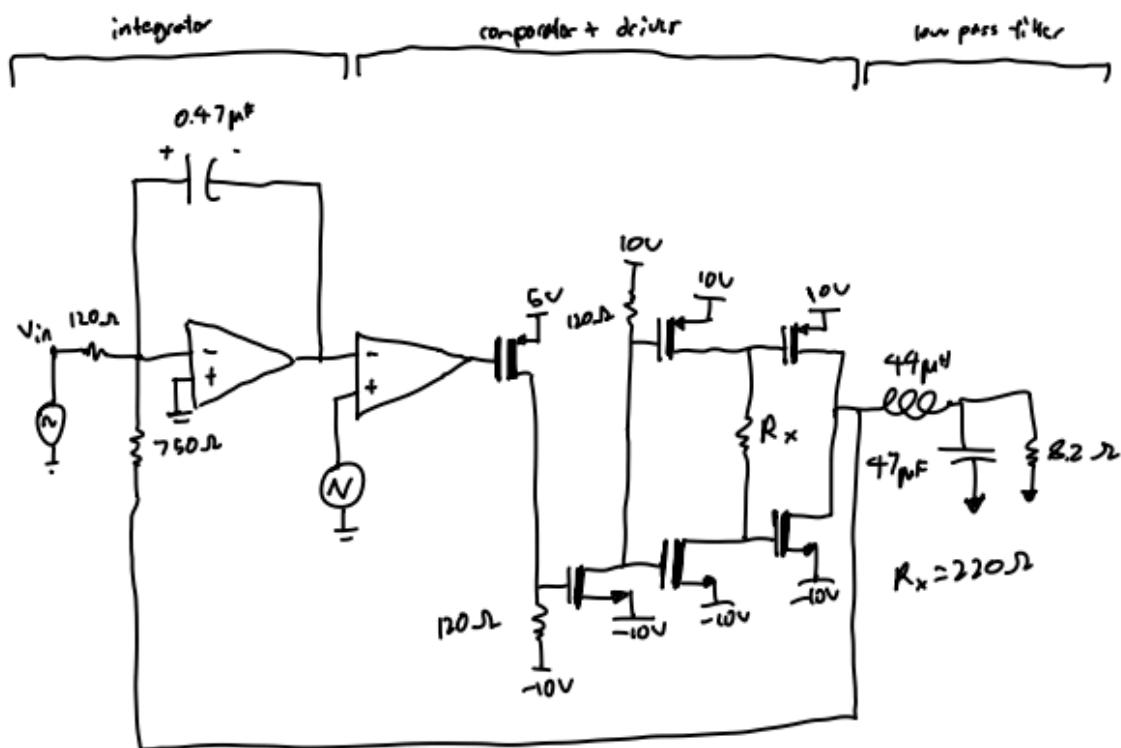




The results are around what we should expect provided our values and circuit. However, there is observed clipping which can potentially cause problems for our design. This can be mitigated by slight tweaks to the R2/R3 values, as it is seen in the integrator section of the waveforms.

# Digital Audio Power Amplifier Final Report

## 1. Circuit Diagram



**Final Circuit Design**

### Parts Acquired:

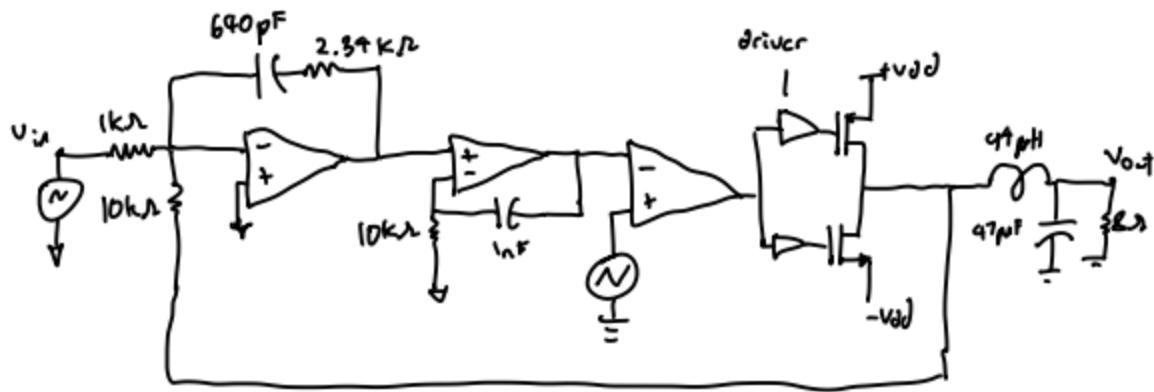
- $\frac{1}{4}$  Watt Resistors
  - 120  $\Omega$  x1
  - 750  $\Omega$  x1
- $\frac{1}{2}$  Watt Resistors
  - 120  $\Omega$  x2
  - 220  $\Omega$  x1
- 5 Watt Resistor (Load resistor)
  - 8.2  $\Omega$  x1
- Capacitors
  - 47  $\mu$ F Electrolytic Capacitor x1
  - 0.476  $\mu$ F Electrolytic Capacitor x1
- Inductor
  - 22  $\mu$ H Inductor x2

- Integrator Op-Amp
  - TL074 Op-Amp x1
- Comparator
  - AD790 Comparator x1
- MOSFETS
  - VN0104 x2
  - VP0104 x2
  - IRFU9014 x2
  - IRFU014 x2

## 2. Design Discussion

The circuit must be optimized such that the wasted switching energy is low while maintaining high clock frequency and output power. The amplifier is a multi-stage design that is built with a triangle wave generator, a comparator-based PWM modulator, a power stage, and an output filter. The triangle wave generator will provide a high-frequency signal to ensure an accurate PWM generation. The comparator converts analog signals into a PWM signal. The power stage is effectively the switch, which needs to be power efficient to prevent too much wasted power. The low pass filter will remove much of the high-frequency switching components, as a filter might do, and recover the base analog signal. Ultimately the circuit will empower that same analog signal. We anticipate utilizing the two integrator design to reduce distortion. Indeed we may need to resolve the driver module as well. Our initial soldered design seemed to have issues with efficiency, however, it produced the correct results.

Following initial testing with the driver, comparator, and low pass filter stages, we decided to resolder the circuit for a better waveform, which could provide better results in efficiency, expected peak-to-peak values, and distortion (derived from poor soldering or damaged components). In our initial design, we anticipated using two integrators (shown below) to produce better results. However, through various iterations and testing, this design proved unsuccessful.



### Two Integrator Initial Design

As shown in our final circuit design, we opted to develop a circuit with a singular integrator.

### 3. General Analysis

$$T(s) = \frac{1 + sR_1C}{sR_1C} \quad \text{single integrator}$$

$$f_z = \frac{1}{2\pi R_1 C}$$

$$R_1 = 120 \Omega$$

$$A_2 = 750$$

$$C = 0.47 \mu F$$

$$f_i = \frac{1}{2\pi (120)(0.47 \times 10^{-6})} = 2.62 \text{ kHz}$$

$$f_z = \frac{1}{2\pi (750)(0.47 \times 10^{-6})} = 452 \text{ Hz}$$

low pass filter

$$R = 8.2 \Omega$$

$$C = 2.2 \mu F$$

$$L = 44 \mu H$$

need 0.6 damping factor

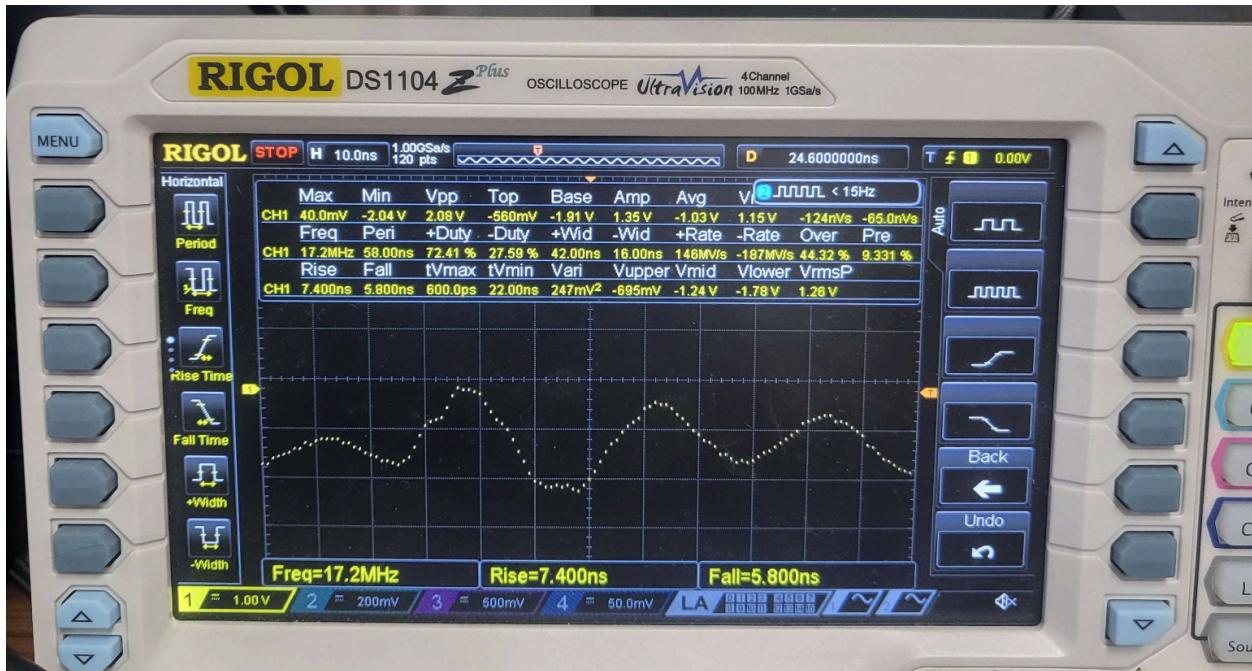
$$\zeta = \frac{R}{2} \sqrt{\frac{2.2 \times 10^{-6}}{44 \times 10^{-6}}} \approx 0.917 \checkmark$$

## 4. Performance Analysis

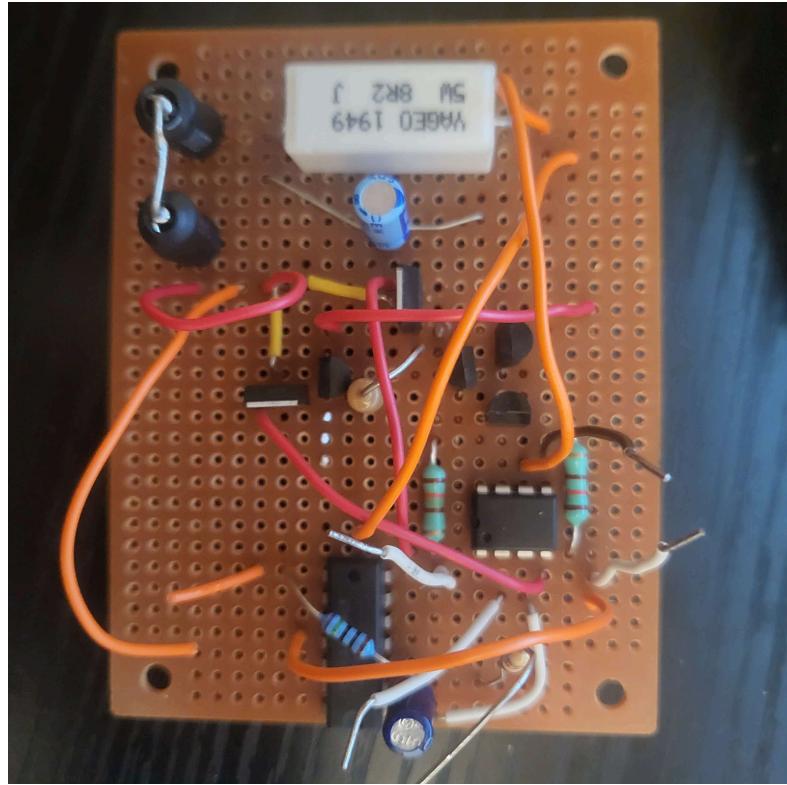
While we were able to produce some results, we failed to meet the specifications of the design.



$V_{load(pp)}$  at 100 Hertz



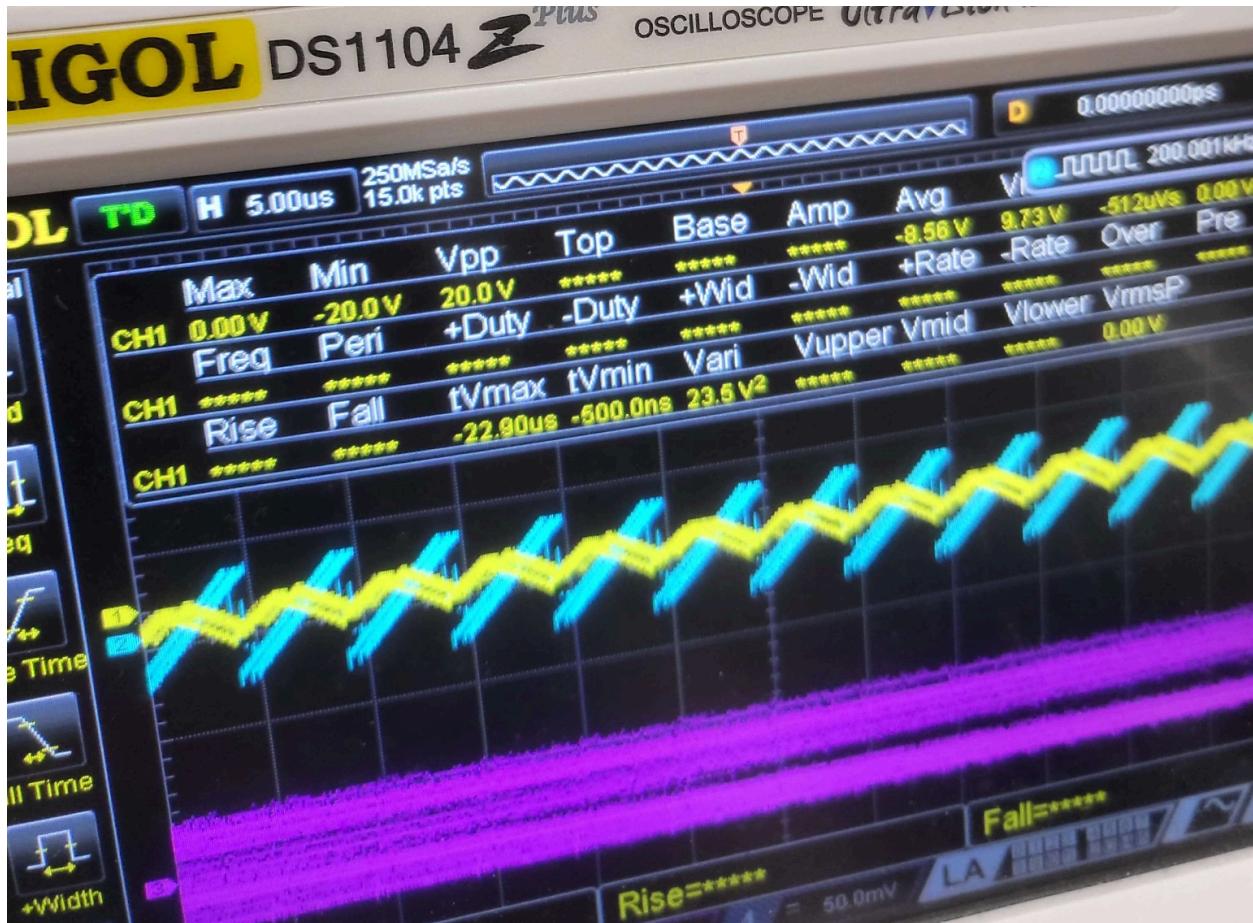
$V_{load(pp)}$  at 10 Hertz



**Final Circuit**

The above images show our final result for the project. The oscilloscope readings were the  $V_{out}$  signals at the provided frequencies that the board managed to produce, however, they were far from the specification requirements. Interestingly, they still output some kind of peak to peak voltage value and a somewhat constructed sinusoidal wave.

Ultimately, our design generally proved unsuccessful. The root cause of the design's flaws can be attributed to mostly poor construction quality. However, despite the design's critical flaws, the schematic and values are expected to work assuming the construction was better quality. In fact, the expectation of at least the comparator, driver, and low pass filter was already met in initial progress of the project as demonstrated here.



**Comparator + Driver + Low Pass Filter Stages Results (Yellow =  $V_{out}$ )**

In the above image, the settings inputted into the system was a 0.3 volt peak to peak sinusoidal signal running at 1000 Hz. Along with that input, a ramp clock signal of 200 kHz at 3 volts peak to peak was run through the comparator, creating this result. With a voltage peak-to-peak of 20, it can be concluded that these stages were relatively stable and optimal. In addition, the  $V_{out}$  signal demonstrates a fairly accurate representation of the input wave, a sinusoidal wave. The rise and fall times, despite not being shown, were also solid for this iteration.

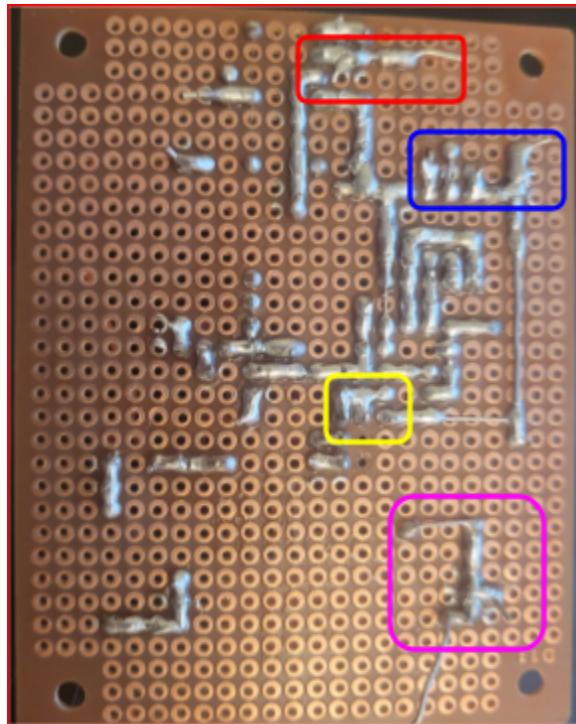
The first problem that we faced was the addition of the integrator stage. Unfortunately, after implementing the integrator stage that we had previously shown, the circuit was unable to maintain stability in the power supplies and became severely damaged. Notably, the -10 DC power supply was reading 12 Watts, which is much above what was anticipated for the design and would definitely destroy the integrity of the components. As such, that board was lost.

Following that iteration, we decided to start anew with a new board. The new board would be wired and layed out almost identically to the previous board. However, the board faced the same

problem when implementing the integrator, where the DC supplies would somehow short, causing large power draws and current, thus destroying the circuit again.

The final iteration of the design, however, was thoroughly tested. The results of everything besides the integrator stage were successful, however, the circuit broke after implementing the integrator stage.

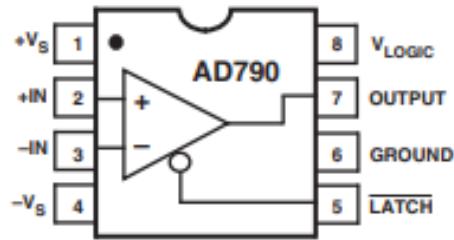
### Possible sources of error



**Final Board Soldering**

As shown above, the circuit has some areas that could be the root cause of the short. In the red box is the integrator and its various inputs. There is a distinctly poor soldering job that connects the various components (120 ohm, 750 ohm, and capacitor), which could have possibly resulted in the integrator causing a failure. If observed closely, there is some solder leaking to the nearby pad as well, which can cause problems, however, it's unlikely that it was a significant contributor.

In blue are all the inputs of the comparator. Shown below is the layout of the AD790 comparator that was used for this project.



### AD 790 Comparator

The circled area of the blue is the  $+V_s$ ,  $+IN$ ,  $-IN$ , and  $-V_s$  area of the comparator. This zone could be particularly volatile to erroneous soldering/wiring as all four of the legs of the comparator are not separated by any pads. As such, the solder job must prevent solder from leaking to nearby legs/pads to prevent shorting two of the inputs. This is especially important as the  $+V_s$  and the  $-V_s$  are the main DC supplies of the project, which can cause a major short.

The yellow area is a possible area of error as well. While soldering, I actually soldered the wrong leg of a MOSFET, but removed it off the board. While it is soldered correctly, the separation into the removed leg of the MOSFET could be nonoptimal.

Finally, in pink, is possibly where it caused problems. That solder joint is the joint where all the grounds were binded. After soldering this specific area, we noticed that the results immediately started breaking and the circuit began breaking. As a result, something in the feedback loop that was incorrectly built or soldered could have ended in a short.