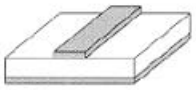
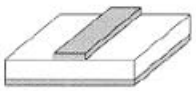


Noise Margins-Noise Budgets EMC &EMI and ESD, Shielding, and Typical Foundry Tolerance Parameters

Rashad.M.Ramzan, Ph.D

FAST-NU, Islamabad



Today's Topic

- Noise Margins
- Noise Budgets
- EMI and EMC
- Shielding against EMI
- ESD
- Typical Foundry Tolerance Parametres

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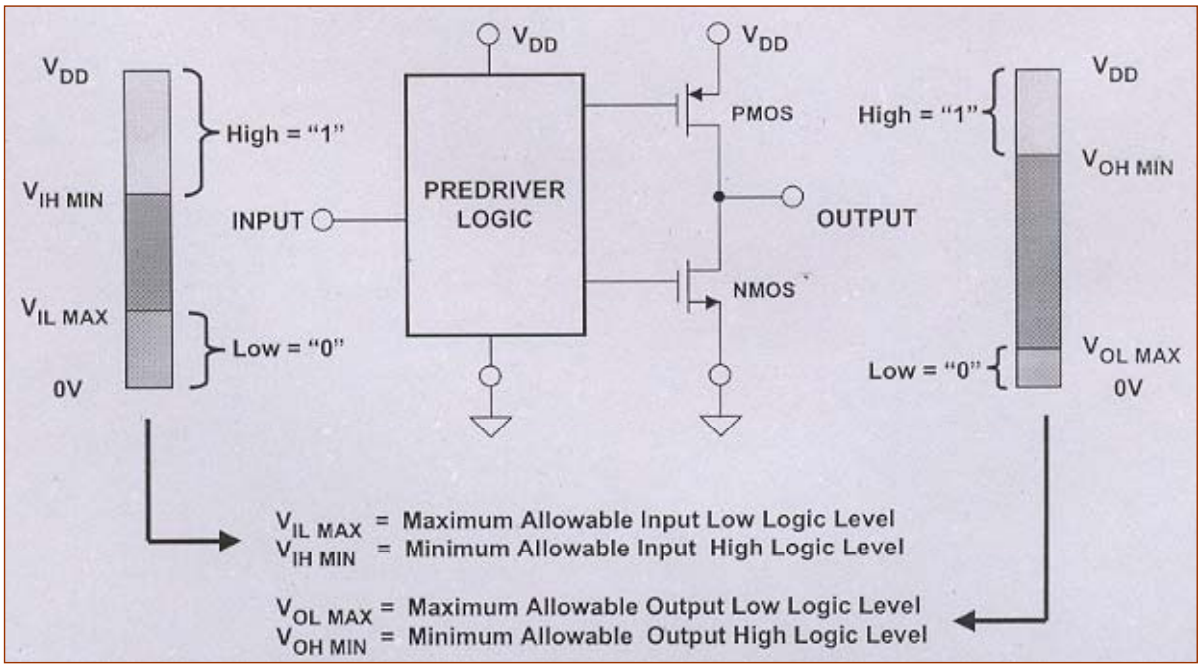
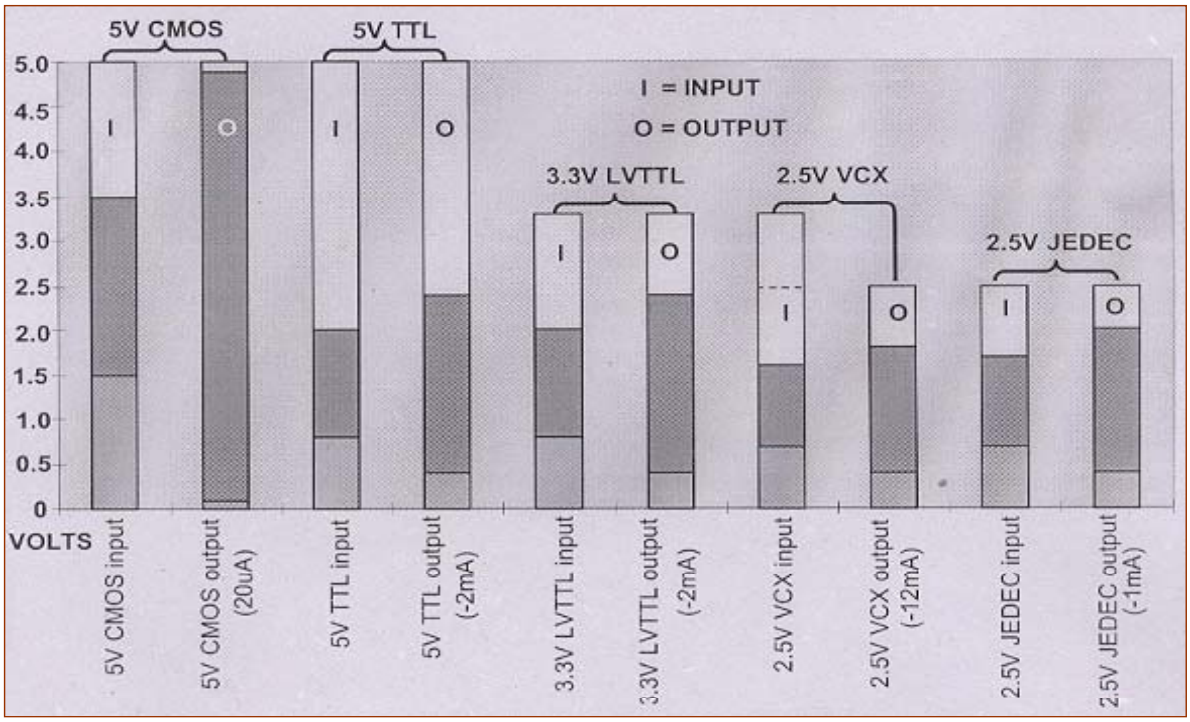
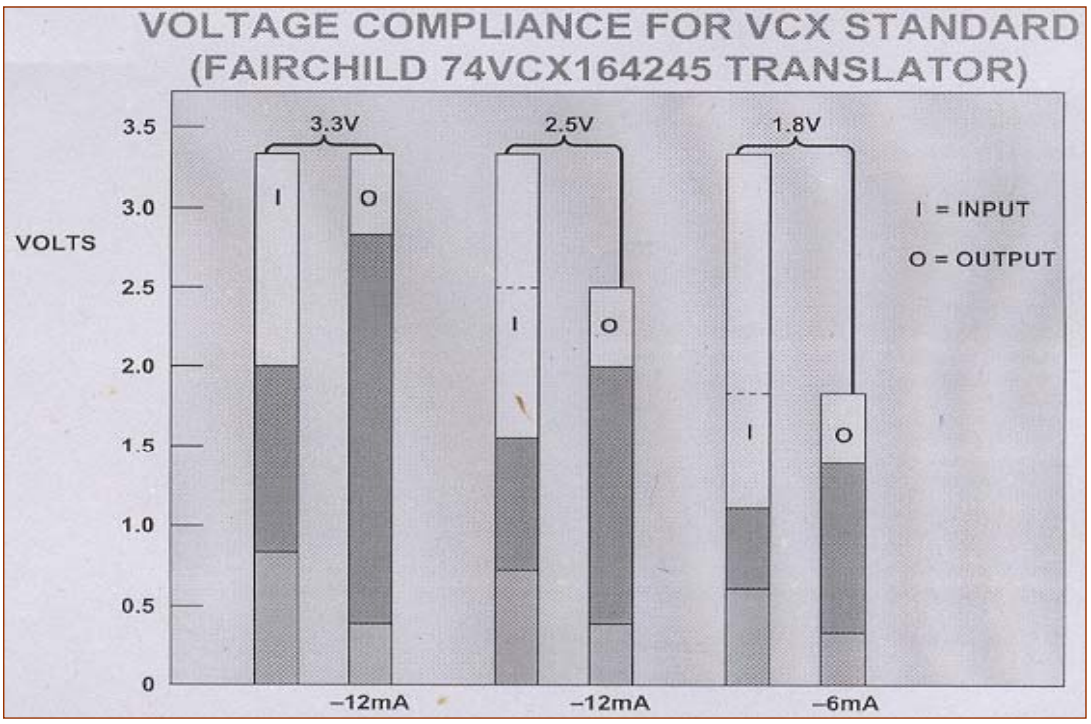
Typical CMOS IC Noise Margins



Low Voltage Logic Standards



VCX Standard Logic



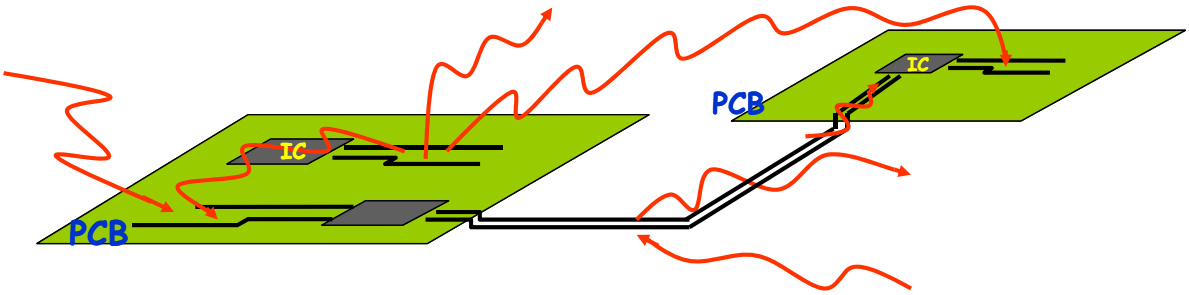
Noise Budget

- Determine the BER (Bit Error Rate) if receiver can detect the signal with amplitude of 250mV. We are using 500mV signaling.
  - 15% High frequency attenuation
  - 5% cross talk from adjacent traces
  - 5% ISI from reflection
  - 20mV receiver offset and sensitivity
  - 10mV Gaussian Noise

Signal Swing (dp-dn)		500
Gross Margin		250
Crosstalk	0.05	25
Reflections	0.05	25
Attenuation	0.15	75
KN	0.25	125
Receiver offset+sensitivity		20
Bounded noise		145
Net Margin		105
Gaussian Noise		10
VSNR		10.5
BER		1.15E-24

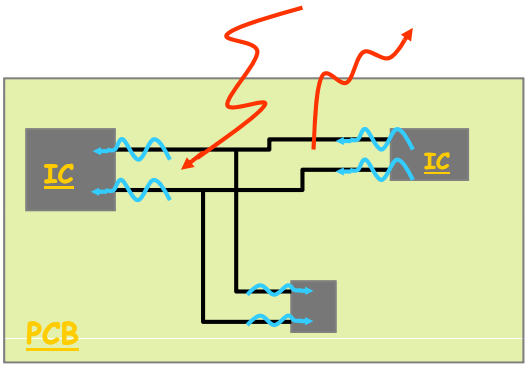
The Electromagnetic Interference (EMI)

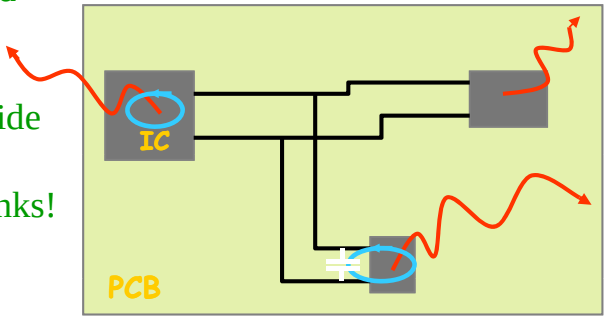
- Electronic circuits produce and are subject to Electromagnetic Interference (EMI).
  - in particular when wavelengths ~ wire lengths
- EMI is a problem because it can severely and randomly affect analog and digital circuit functionality!!!



EMI at board, package and IC level

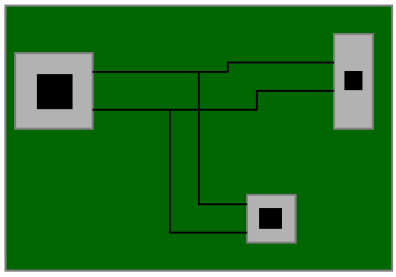
- Traces on PCB can pick up EMI and transmit it to IC's
- IC's can produce high frequency conducted emissions that can radiate from PCB's
- IC's themselves can directly produce radiated emissions
  - high-frequency current loops Vdd-decap-gnd on package or inside IC's.
  - high-frequency current loops inside IC (near future)
  - IC radiation amplified by heat sinks!





EMI a problem for ICs design?

- So far: dimensions too small and wavelengths too large
- Trend: larger chip dies and higher frequencies



Today's PCB:

• clocks	~ 300MHz
• harmonics	~ 3GHz
• wavelengths	~ 10cm
• dimensions	~ 10cm

$\lambda \cong d$

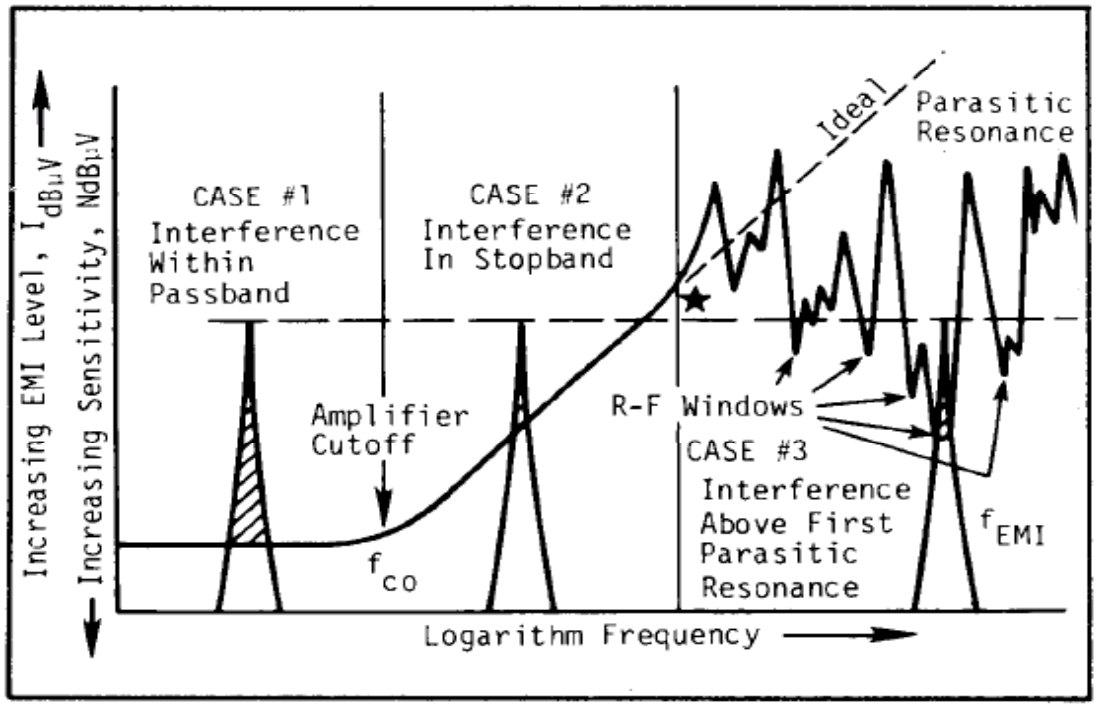
this gives resonances on PCB today, hence it might on IC tomorrow!

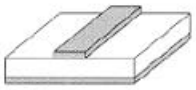
Future's IC:

• clocks	~ 3GHz
• harmonics	~ 30GHz
• wavelengths	~ 1cm
• dimensions	~ 1cm

$\lambda \cong d$

Parasitic resonance Windows for RF Coupling





EMC/EMC Definitions

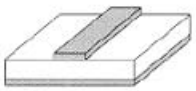
- Emissions: propagation of electromagnetic interference (EMI) from non-compliant devices and in particular radiated and conducted radio frequency interference (RF)
- Susceptibility: The detrimental effects on susceptible devices (victims) of EMI in forms that include electrostatic discharge (ESD) and other forms of electrical overstress (EOS)

EMC Regulatory:

North American –
FCC (Federal Communication Commission, US),
DOC (Department of Communication, Canada)

Worldwide —
IEC (International Electrotechnical Commission)

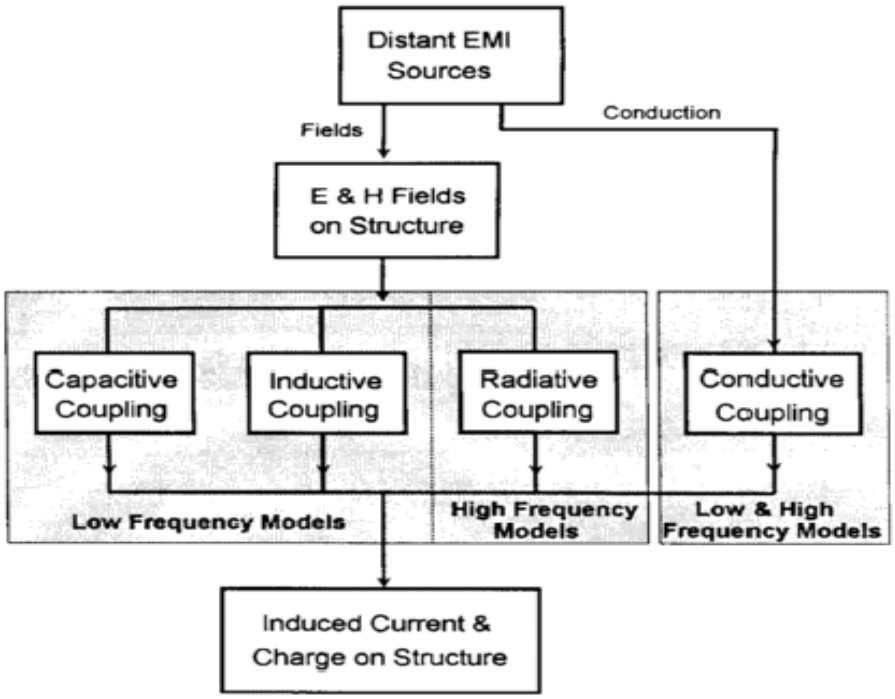
European Union: IEC and CISPR (International Special Committee on Radio Interference)



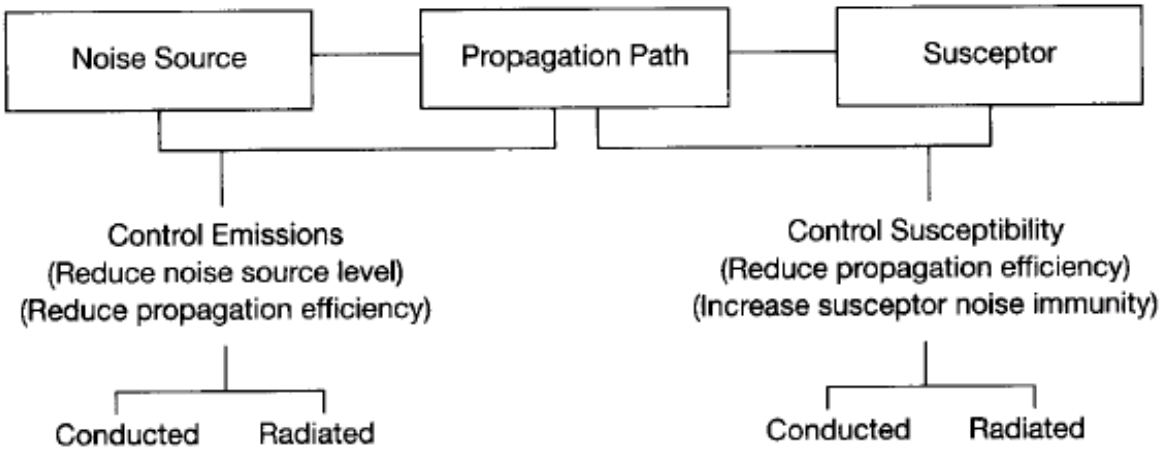
EMC/EMC Definitions

- EMC (Electromagnetic Compatibility)
  - The ability of product to co-exist in electromagnetic environment with out causing or suffering functional degradation or damage.
- EMI (Electromagnetic Interference)
  - A process by with disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths. EMI can occur from DC to day light frequencies.
- Susceptibility
  - A relative measure to be disrupted or damaged by EMI exposure
- Radiated Emissions
  - A relative measure to be disrupted or damaged by EMI exposure that arrive via free space propagation.
- Conducted Emissions
  - A relative measure to be disrupted or damaged by EMI exposure that arrive via external cables, power cords and IO Connectors

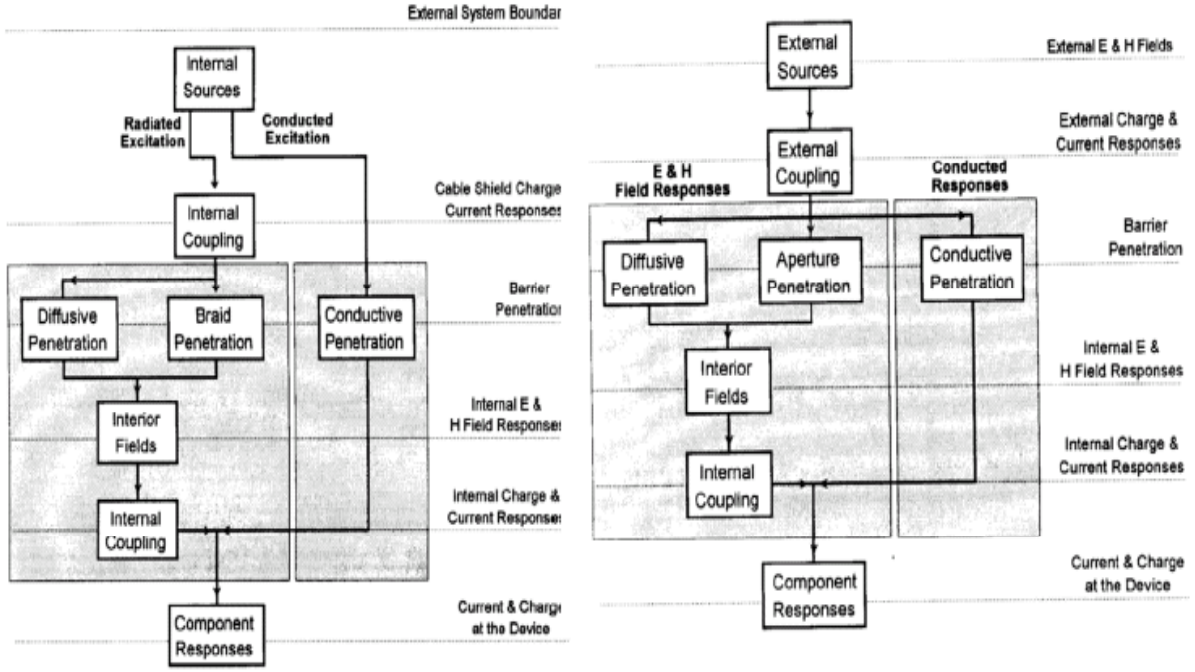
EMI Coupling Process



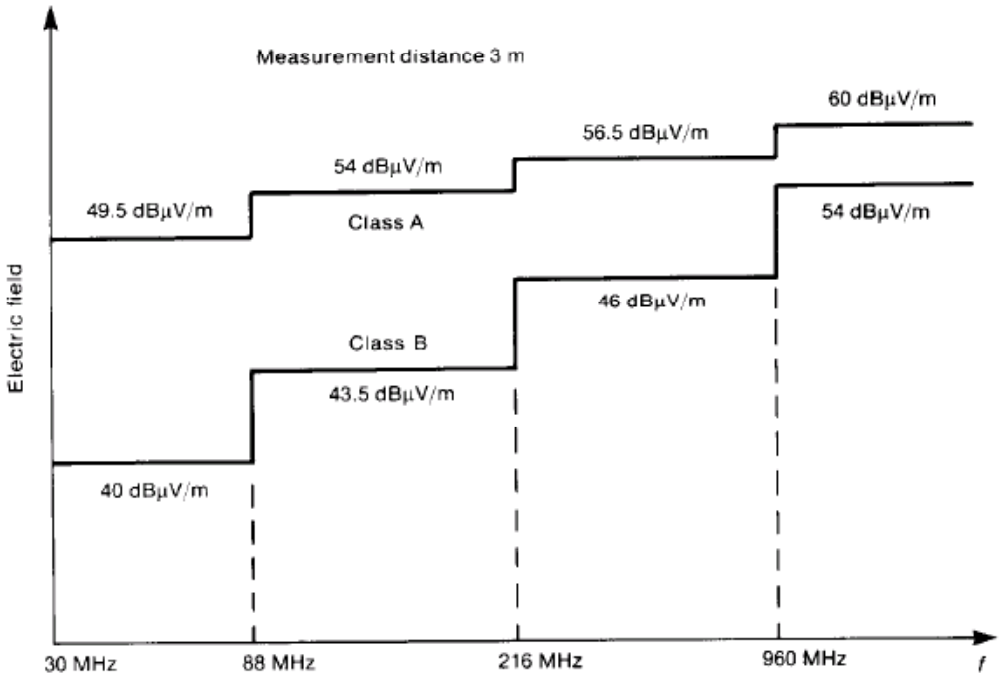
EMC Control



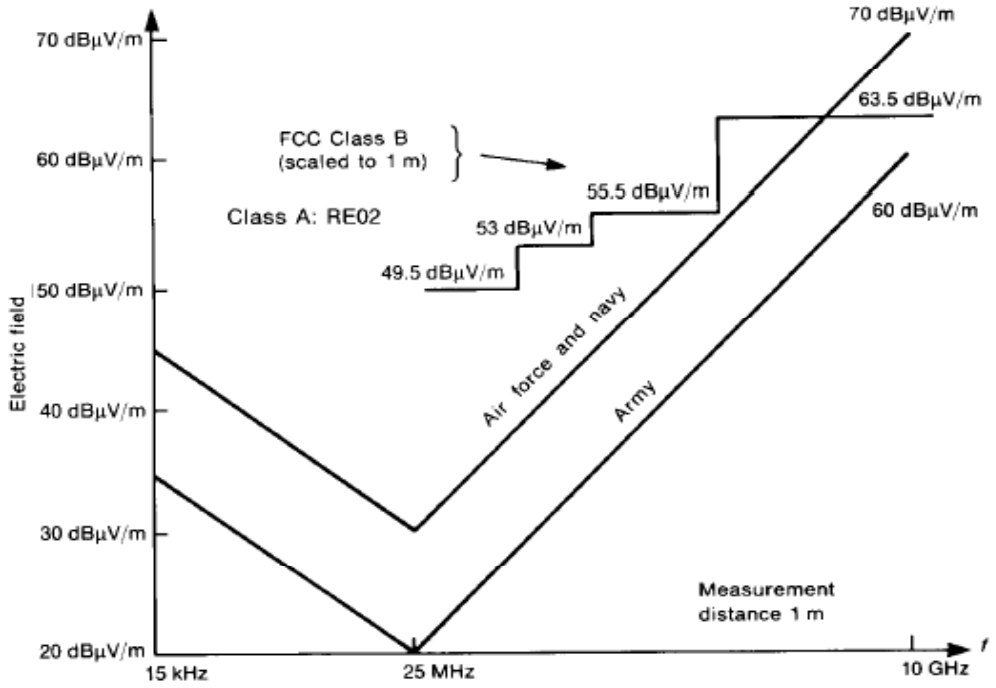
Internal vs. External EMI Process



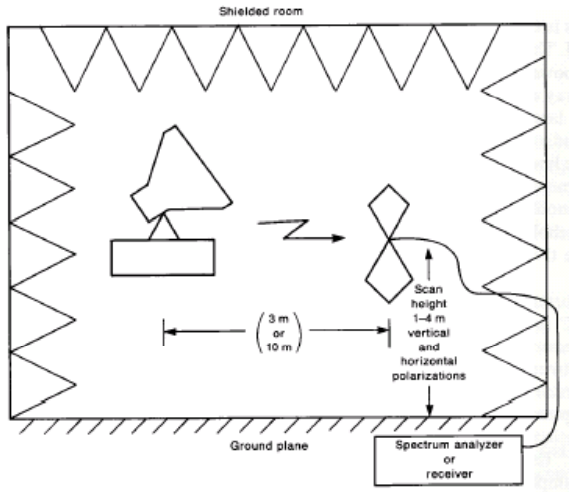
FCC Class A and B Emission Limit at 3m

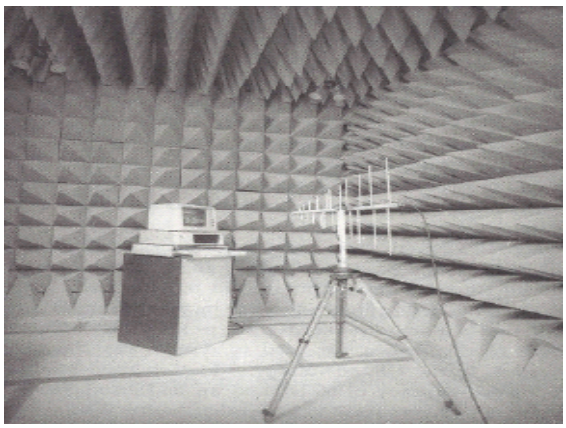


Emission Limit at 1m



Semi-anechoic Chamber





Radiation Pattern of a Circuit

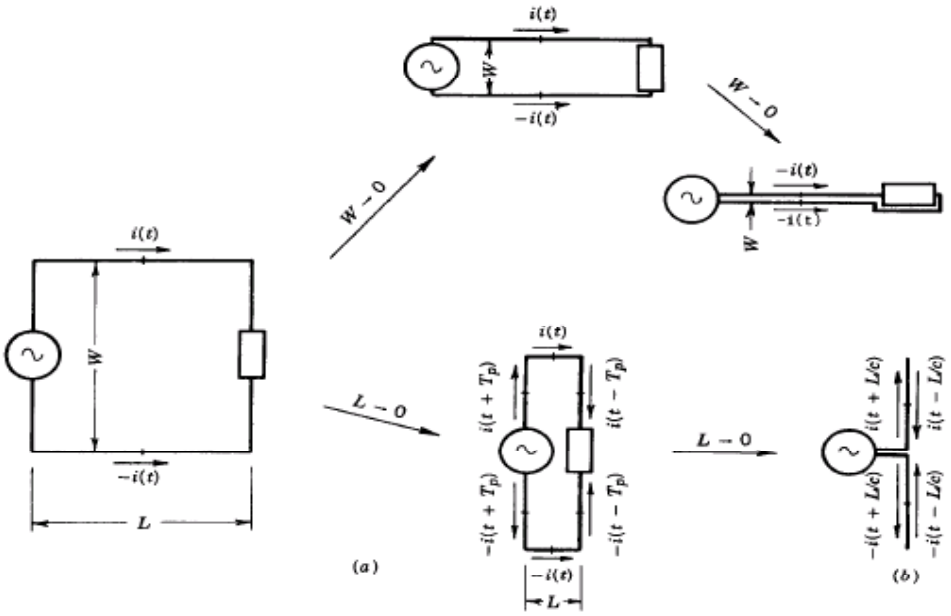
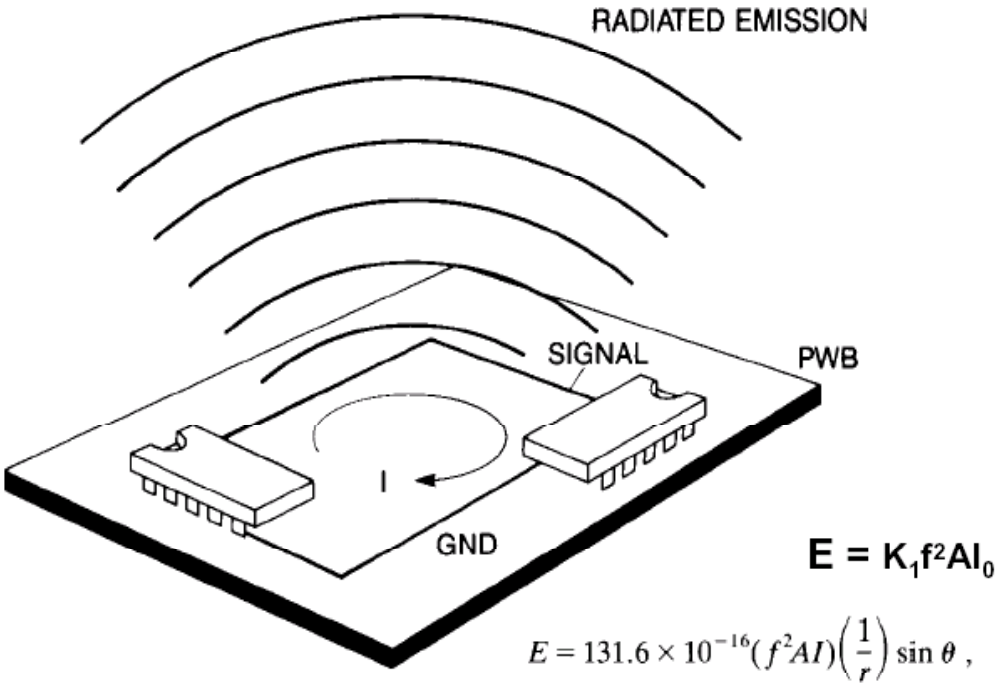


Figure 3-4. As W is made smaller, connecting-current radiations cancel each other more and more; as L is made smaller, the circuit current path becomes more and more like that of a dipole antenna: (a) several circuits of length L and width W; (b) dipole antenna.

Differential Mode Radiation from PCB



$$E = K_1 f^2 A I_0$$

$$E = 131.6 \times 10^{-16} (f^2 A I) \left(\frac{1}{r}\right) \sin\theta \,,$$

Far Field and Near Field Radiation

For near field, $r < \lambda/2\pi$

$$E_{dm\ near} = \frac{\eta_0 IA}{\lambda 2r^2} = \frac{\mu_0 IAf}{2r^2}$$

$$= 6.3\times10^{-7}\left(\frac{IAf}{r^2}\right)\ (V/m)$$

$$H_{dm near} = \frac{IA}{4\pi r^3}\ (A/m)$$

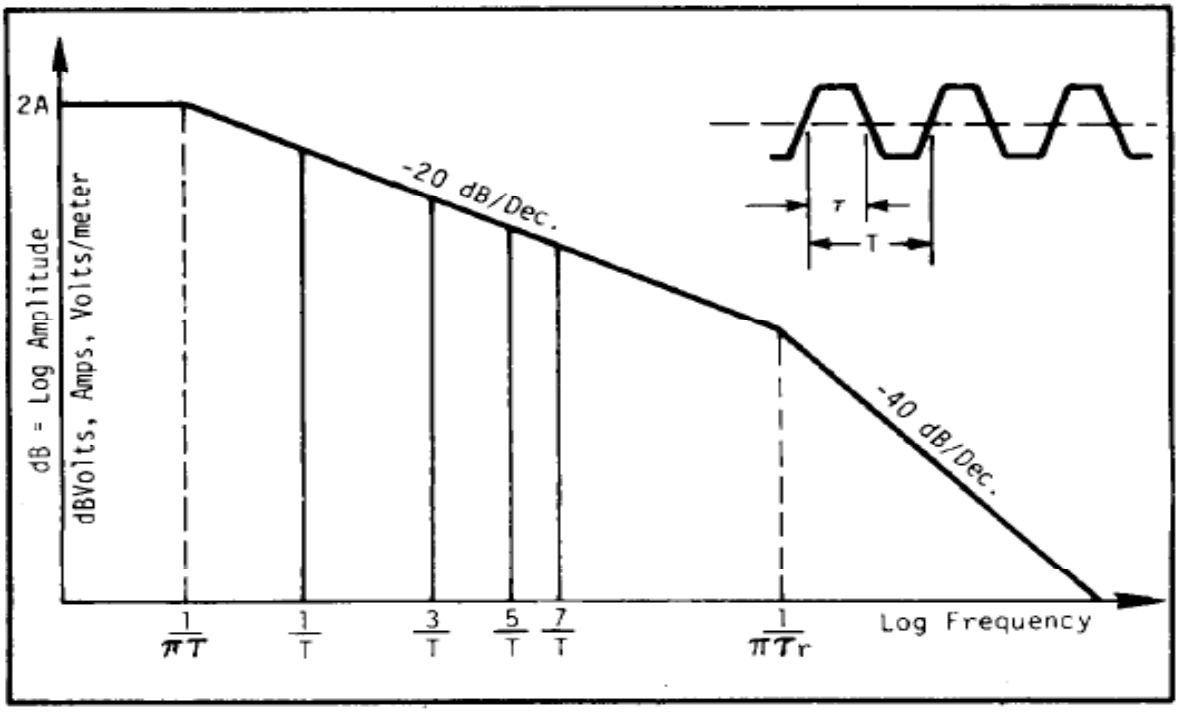
For far field, $r > \lambda/2\pi$

$$E_{dm\ far} = \frac{\eta_0 \pi IA}{\lambda^2 r} = \frac{\eta_0 \pi IAf^2}{c^2 r}$$

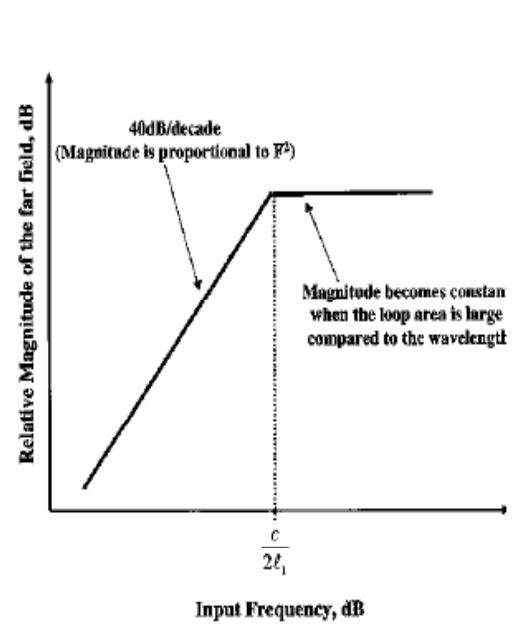
$$= 1.32\times10^{-14}\left(\frac{IAf^2}{r}\right)\ (V/m)$$

$$H_{dm far} = \frac{\pi IA}{\lambda^2 r} = \frac{\pi IAf^2}{c^2 r}\ (A/m)$$

Input Signals in PCB: Spectrum



Radiated Differential Mode Radiation



10.4 Relative magnitude of far-field radiation as a function of frequency.

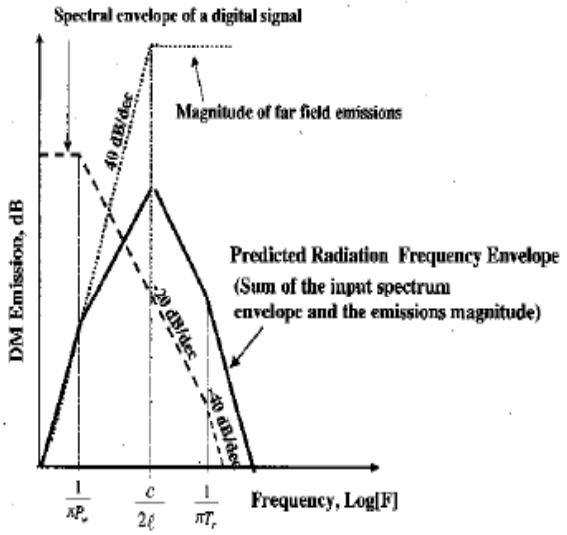


FIGURE 10.5 Resultant differential radiation behavior when far-field characteristics are combined with spectral input.

Radiation Control By Timing

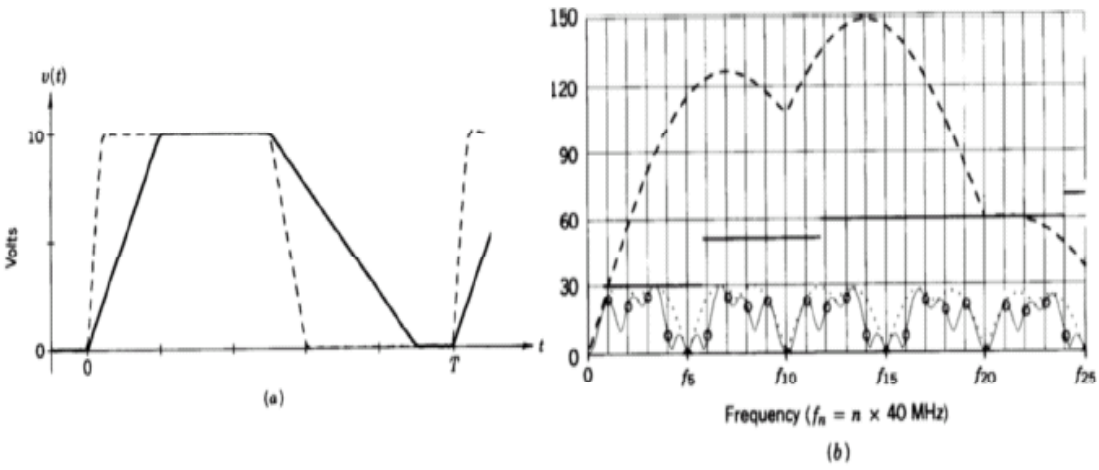


Figure 6-4. The first modified source voltage waveform considered in Example 6-1, and predicted values of measured radiated electric field strength: (*a*) voltage waveform with $t_R = T/5$, $t_F = 2T/5$, and $t_d = T/2$; (*b*) meas$|E_n|$ (○) and Max(meas$|E_n|$) (···) for this voltage waveform, Max(meas$|E_n|$) (---) for the initial voltage waveform, and regulatory limits (—).

Radiation Control by Geometry

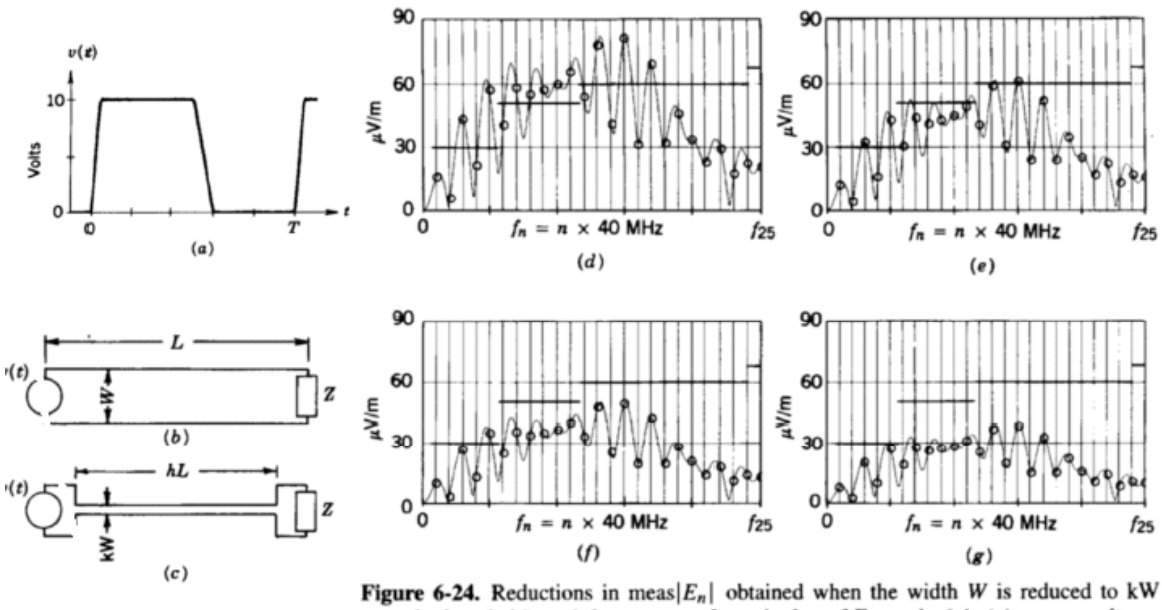


Figure 6-24. Reductions in meas$|E_n|$ obtained when the width W is reduced to kW over the length hL, and the source voltage is that of Example 6-1: (a) source voltage; (b) initial circuit; (c) modified circuit; (d) meas$|E_n|$ when $h = 0.6$ and $k = 0.3$; (e) meas$|E_n|$, when $h = 0.7$ and $k = 0.2$; (f) meas$|E_n|$, when $h = 0.8$ and $k = 0.2$; (g) meas$|E_n|$, when $h = 0.9$ and $k = 0.1$.

Radiation Control by Geometry

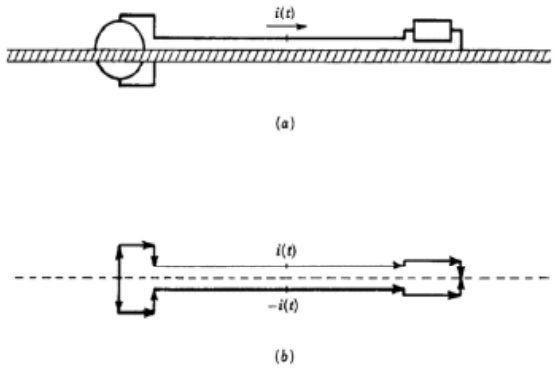


Figure 6-29. Circuit width can be effectively reduced with a finite ground plane, if negative symmetry of the connecting currents can be obtained: (a) circuit implementation to obtain connecting-current symmetry; (b) desired symmetrical current pattern.

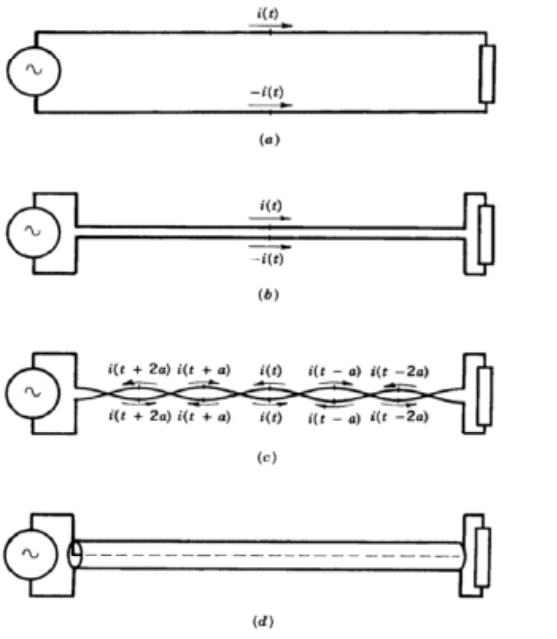
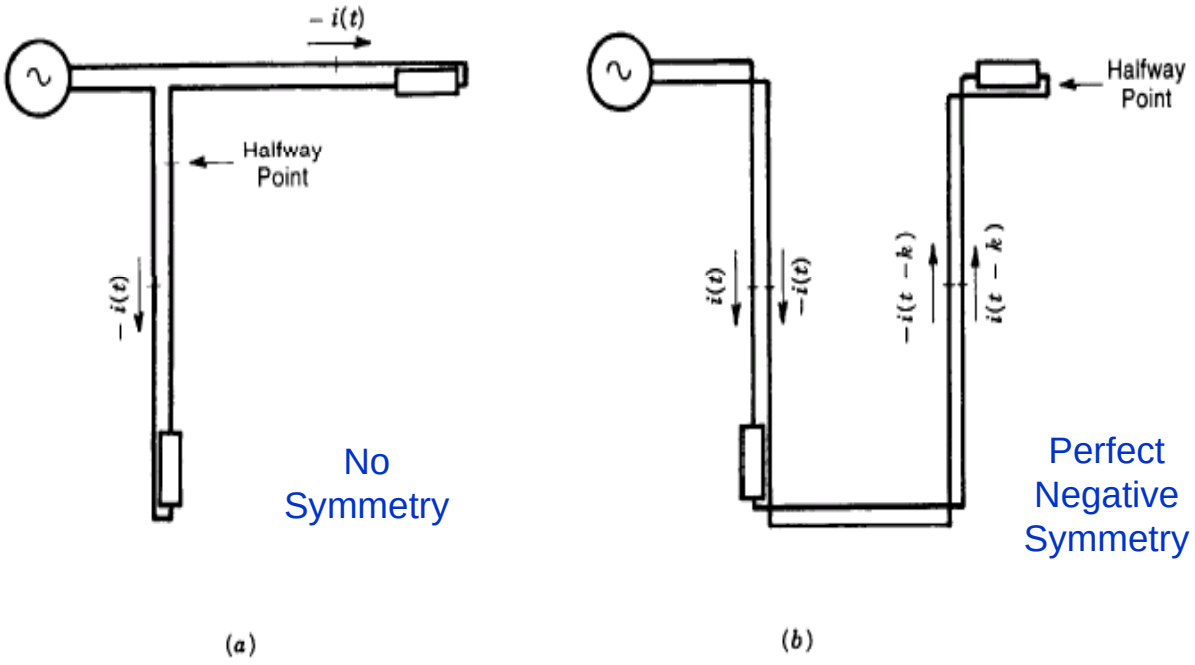
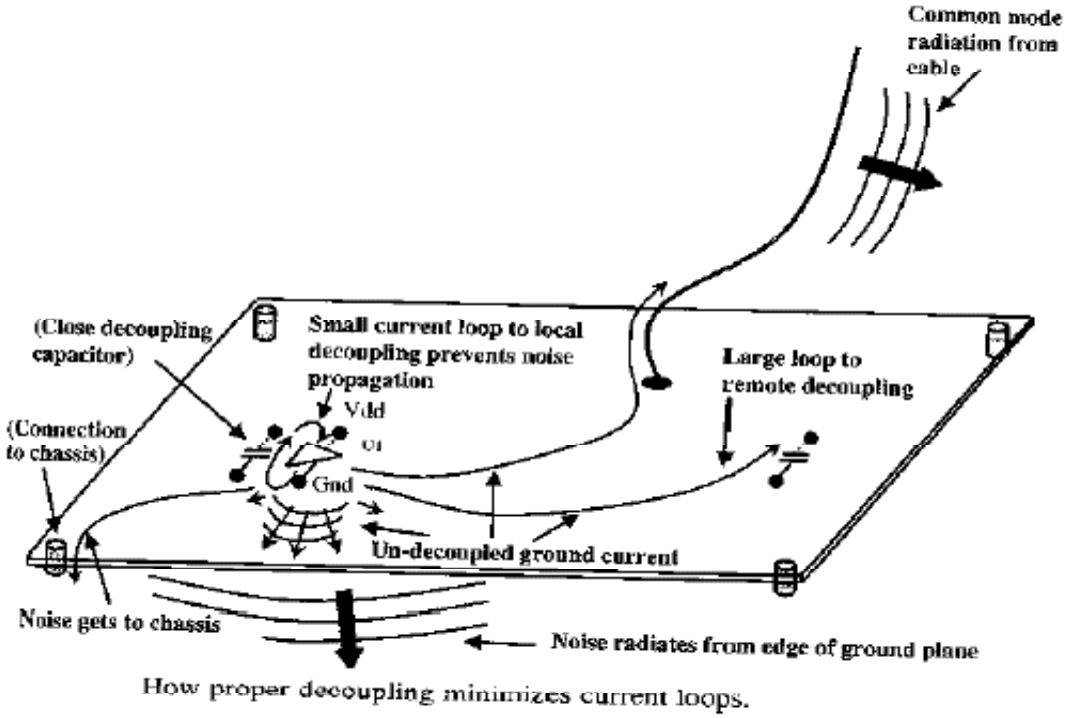


Figure 6-30. Progressively more effective methods of reducing connecting current radiations: (a) unmodified circuit; (b) closely parallel connecting currents; (c) closely twisted connecting currents; (d) coaxial connecting currents.

By Negative Symmetry



Radiation Control by Decoupling Capacitor



How proper decoupling minimizes current loops.

Controlling Differential Mode radiation

- Clock lines most critical. All clock leads must have adjacent ground-return lead. The total clock loop area should not exceed 1 cm^2. Homogenous ground plane close by.
- Clock circuitry must be located away from all I/O leads or circuitry
- Clock lines should not run parallel with data/address buses or other signal leads for minimized crosstalk.
- Line and bus drivers typically generate broad band noise due to random nature of data; teach will require at least one ground-return lead per 8 signal leads placed closed to least significant bit.
- Transient power supply currents are controlled by decoupling capacitors for minimized loop areas.

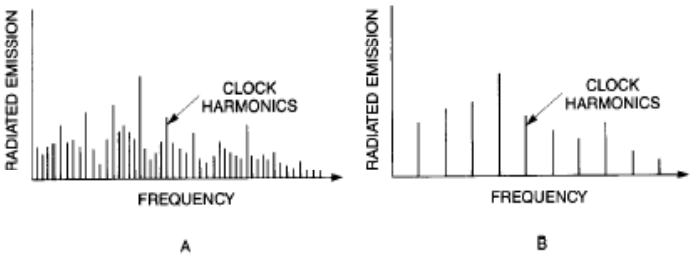
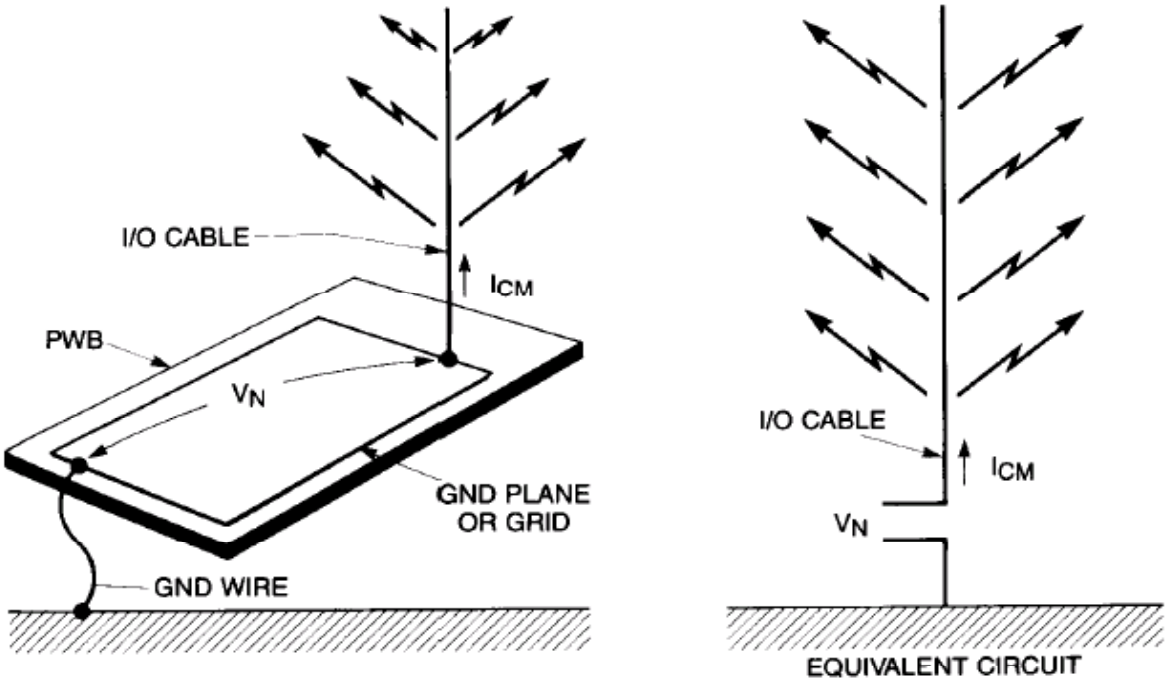
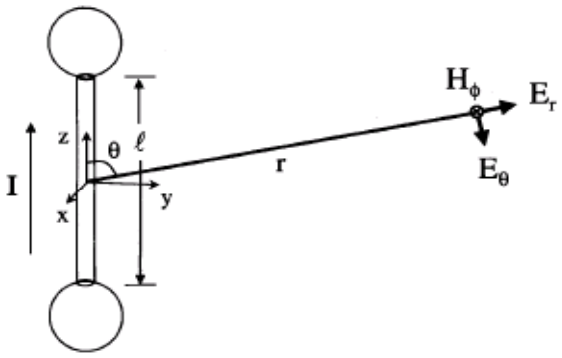


Figure 11-9. *Typical radiated emission spectrum from a digital circuit: (A) with all circuits operational; (B) with only clock circuits operational.*

Common Mode Radiation



Near and Far End CM Radiation



$$E_{\text{cm near}} = \frac{I\ell\eta_0\lambda}{8\pi^2 r^3} = 4.8\left(\frac{I\ell\lambda}{r^3}\right) \quad \text{V/m}$$

$$H_{\text{cm near}} = \frac{I\ell}{4\pi r^2} \quad \text{A/m}$$

For far field, $r > \lambda/2\pi$

$$E_{cm\ far} = \frac{\eta_0 Il}{2\lambda r}$$

$$= 6.28\times10^{-7}\left(\frac{Ilf}{r}\right) \ (V/m)$$

$$H_{cm\ far} = \frac{Il}{2\lambda r} = \frac{Ilf}{2cr} \ (A/m)$$

Diff and CM Radiation

Differential mode and common mode currents

$$\hat{I}_D = \frac{\hat{I}_1 - \hat{I}_2}{2}$$

$$\hat{I}_C = \frac{\hat{I}_1 + \hat{I}_2}{2}$$

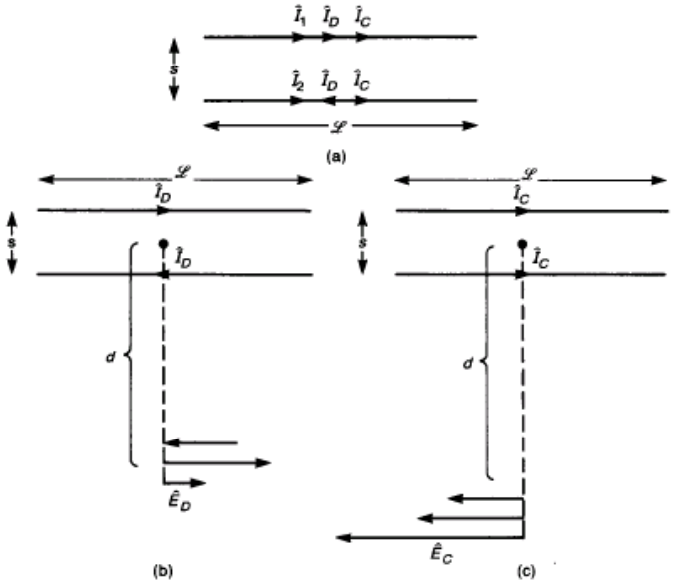


FIGURE 8.1 Illustration of the relative effects of differential-mode currents $\hat{I}_D$ and common-mode currents $\hat{I}_C$ on radiated emissions for parallel conductors: (a) decomposition of the total currents into differential-mode and common-mode components; (b) radiated emissions of differential-mode currents; (c) radiated emissions of common-mode currents.

Common Mode Current Generation

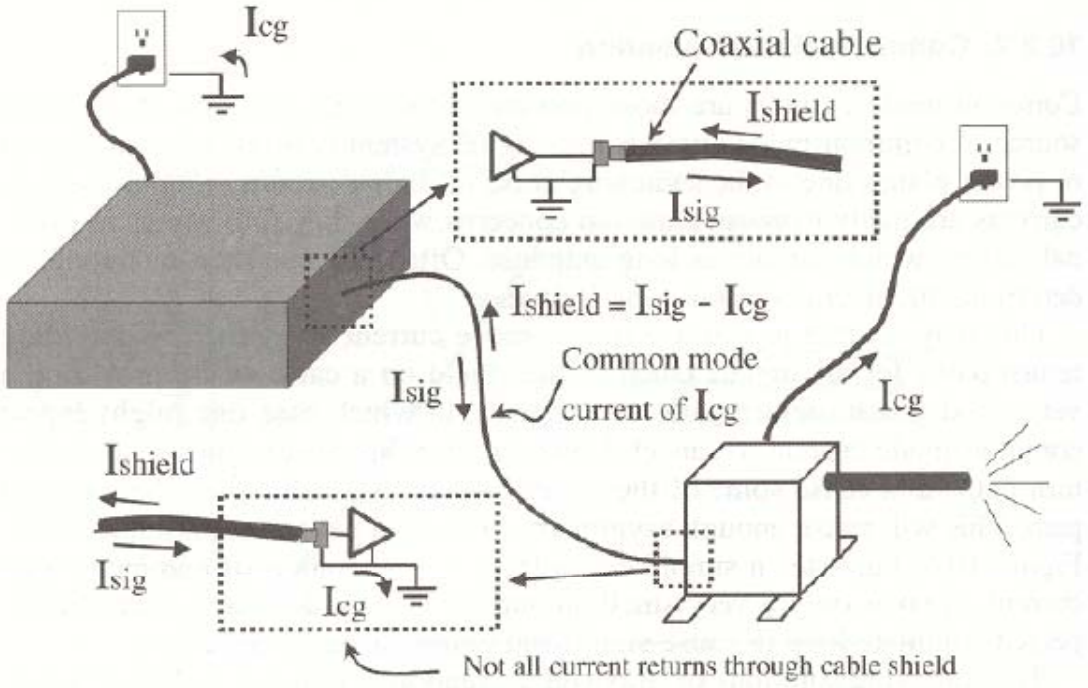
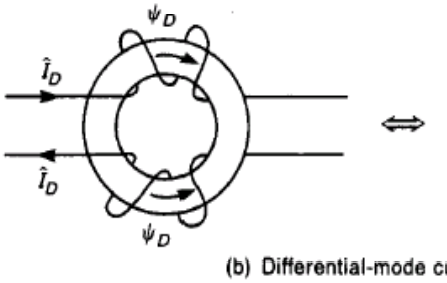
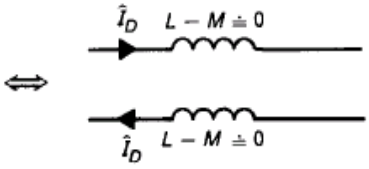


FIGURE 10.6 Common-mode current generation.

Common Mode Chokes

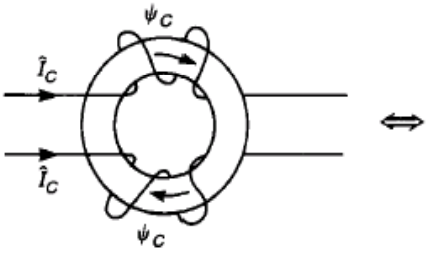


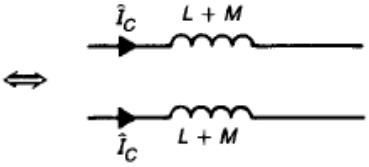


(b) Differential-mode currents

$Z_{DM} = j\omega(L - M)$

For ideal case, L=M
so $Z_{DM}=0$





$Z_{CM} = j\omega(L + M)$,
For ideal case, L=M
so $Z_{CM}=2j\omega L$

Ferrite Beads: Chokes off HF Noise

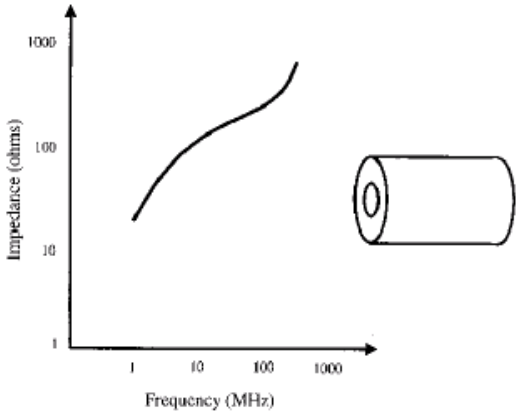


FIGURE 10.18 Impedance variation of a ferrite core. Ferrite dimensions: inner diameter, 8.0 mm; outer diameter, 16 mm; length, 28.5 mm.

Choking cables and localize power and ground planes. Reduce conductive emission

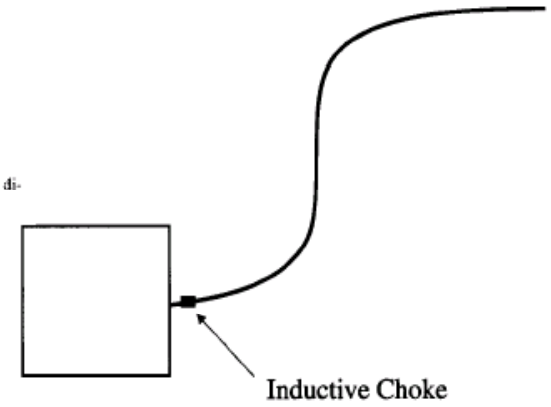
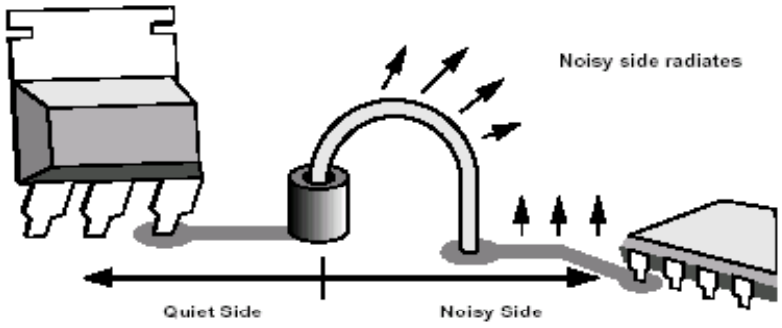
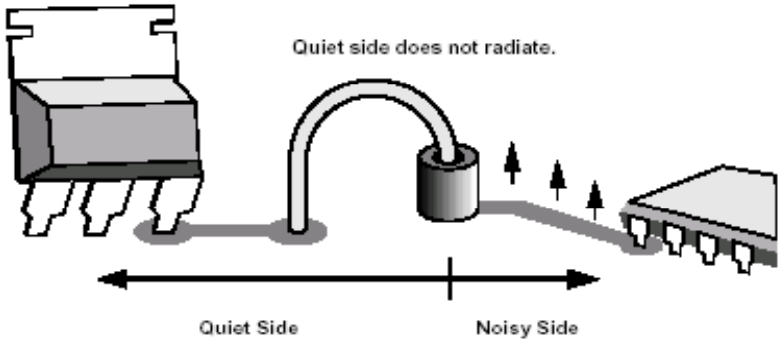


FIGURE 10.17 Choking off noise coupled onto a cable.

Ferrite Beads: Chokes off HF Noise



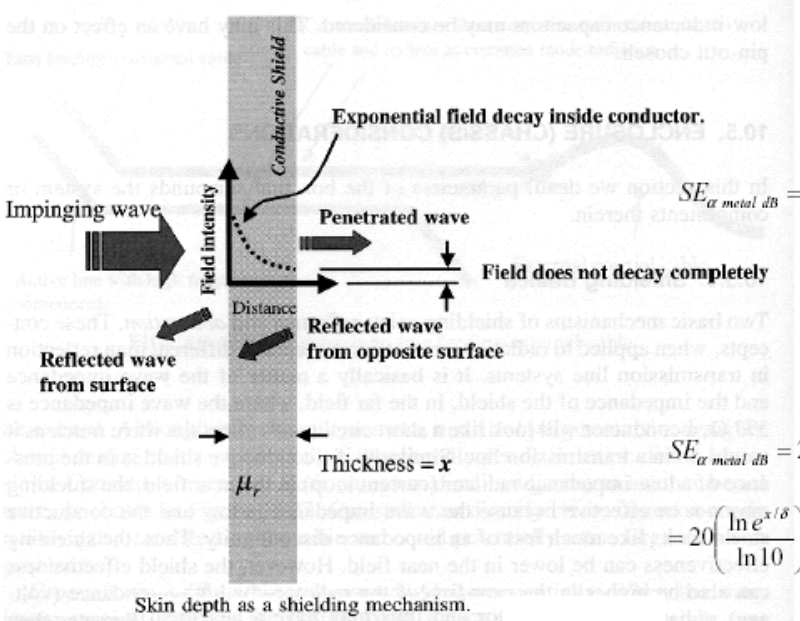


Controlling Common Mode Radiation

- Common mode radiation is generated by wires/cables. The radiated frequencies are determined by the common-mode potential, usually the ground potential and its variations. I/O wires radiates these common mode signals (instead of signal!). Primary method is to decrease the common mode current
- Common mode radiation is more dominant than differential mode for the same conditions (typically 1000 time!)
- Keep all cables and wires short. However, from one quarter wavelength longer cables the emission is not increasing
- Common mode current is controlled by
  - Minimizing the source voltage that drive the antenna (mainly ground potential)
  - Providing a large common mode impedance (choke, e.g. ferrite beats) in series with cable
  - Shunting the current to ground
  - Shielding the cables
  - Reducing high frequency components in wires and interconnects

Shielding: Basic Mechanism

Basic mechanisms: Reflection and absorption



Skin depth as a shielding mechanism.

Reflection:

$$SE_{\alpha\ metal\ dB} = 20\log\left(\frac{(1+Z_{wave}/Z_{shield})^2}{4(Z_{wave}/Z_{shield})}\right)\ (decibels)$$

Absorption:

$$SE_{\alpha\ metal\ dB} = 20\log\left(\frac{E_{inc}}{E_{tunnel}}\right) = 20\log\frac{E_{inc}}{E_{inc}e^{-x/\delta}}$$

$$= 20\left(\frac{\ln e^{x/\delta}}{\ln 10}\right) = 8.7\sqrt{\frac{\pi f\mu}{\rho}} = 0.0172x\sqrt{\frac{f\mu_r}{\rho}}\ (decibels$$

Holes in Boxes

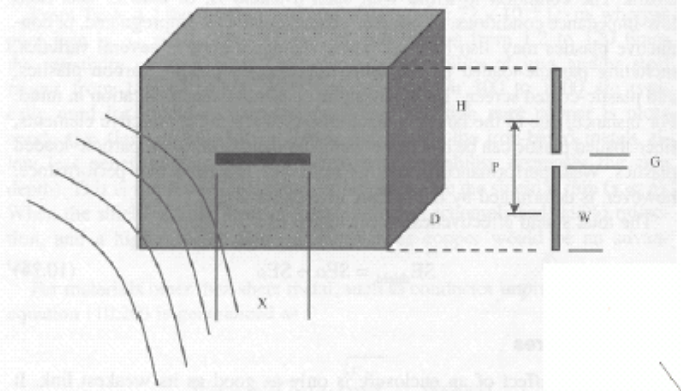
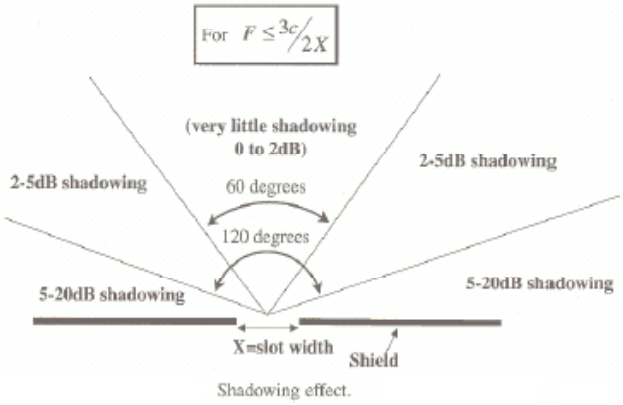


FIGURE 10.24 Chassis with a hole in it.

SE_{shadow} : shadow effect. When f>2c/X, no shadow effect should be considered



Shadowing effect.

Shielding Summery

•Usually iron-based metal sheet is much better than copper for shielding materials because μ_r of that is 110-14800, though resistivity of copper is lower.

•Near field electrical field is easier to be shielded due to higher wave impedance (the wave see metal as short circuits).

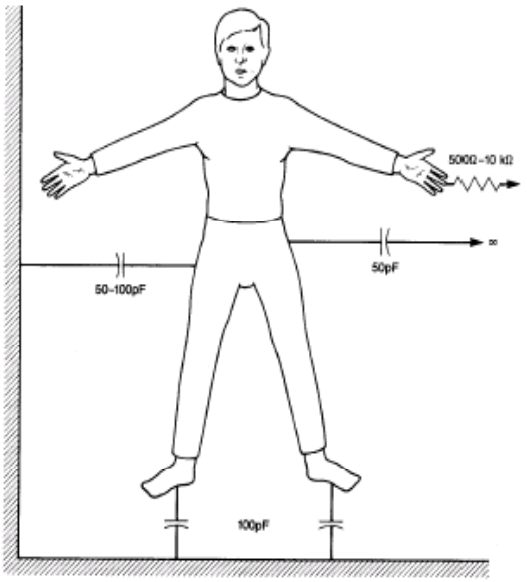
•Near field magnetic field is very difficult to be shielded because of it's lower wave impedance.

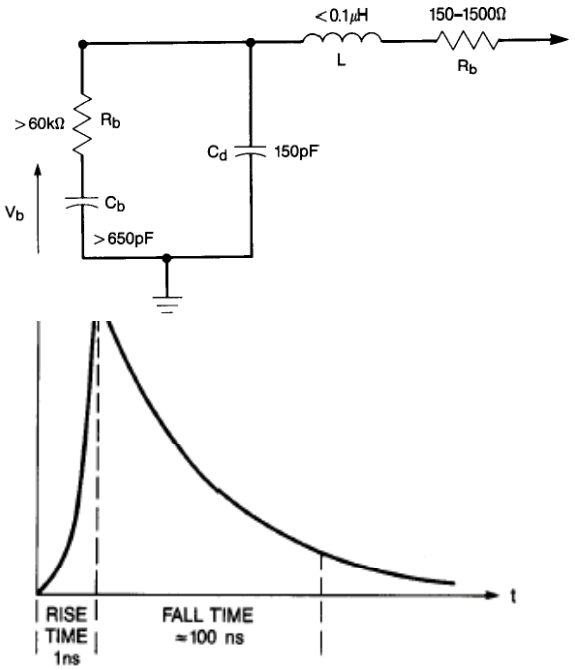
• For far field, both electrical field and magnetic field have the same wave impedance $120\pi = 370\ \Omega$.

•Holes in the chassis will often be the dominant variable in shielding effectiveness. Common holes are viewing screens, thermal air flow, switch holes, cables holes etc.

• Apertures are usually difficult to estimate the exact shielding effect, but the amount can be reasonably predicted.

ESD (Electrostatic Discharge)





ESD Protection in Equipment

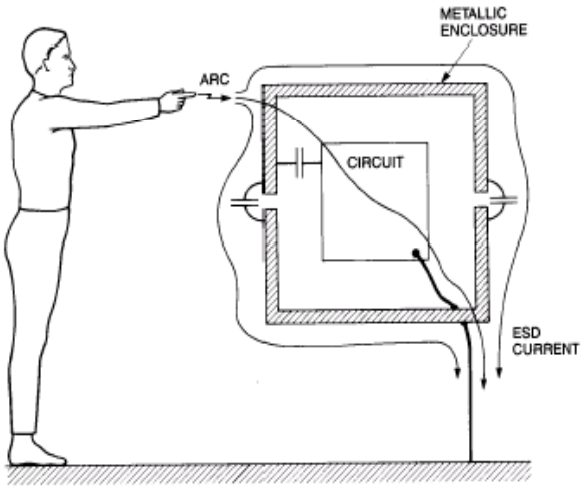


Figure 12-7. *Electrostatic discharge to a metallic enclosure that does not have electrical contact across the seams.*

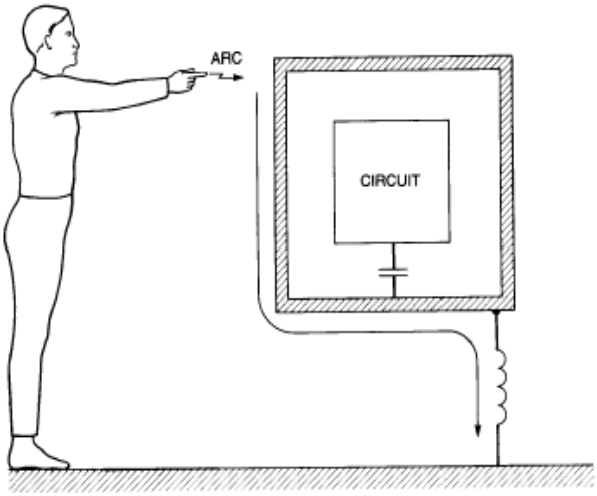
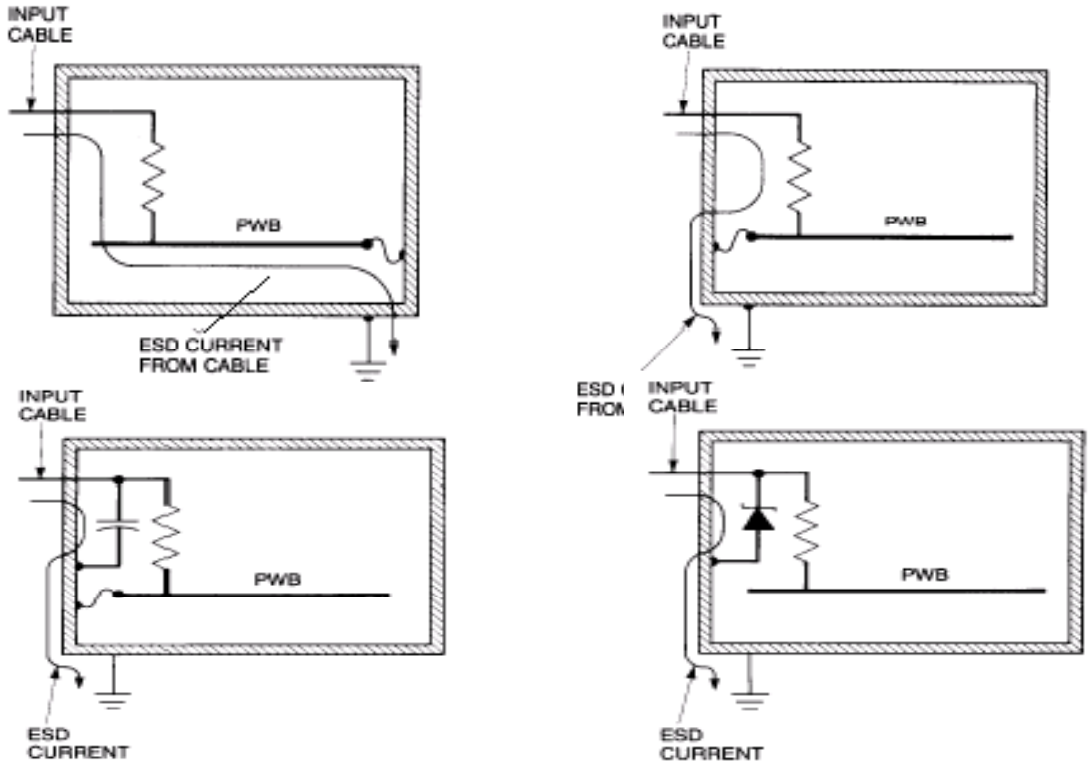


Figure 12-8. *Electrostatic discharge to a metallic enclosure that completely encloses a circuit. The circuit has no external connections.*

ESD Protection in Equipment



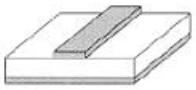
EMC and ESD

ESD is a special case of the overall subject of EMC control. The primary difference between ESD and general EMC control is that with ESD much larger currents and voltages are involved; however, both can be controlled by the same techniques. Notice the similarities between the methods used to provide ESD protection, discussed in this chapter, and those used to control common-mode emissions from I/O cables

1. All I/O cables should be in one area.
2. A separate I/O ground should be used.
3. The I/O ground should have a low-impedance connection to the earth.
4. Cables should be bypassed to this separate I/O ground.
5. All loop areas should be kept as small as possible.

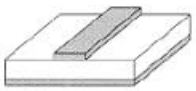
A system properly designed for ESD control will usually perform well with respect to EMC susceptibility. Furthermore ESD testing can often be used to find flaws in the EMC design of a product (Mardiguian, 1985).

ESD Summery



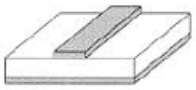
- ESD protection should be part of original system design (not aftertought)
- ESD hardening of a system involves the electrical, mechanical, and software design (error correction codes, recovery, fault tolerance)
- All exposed metal must be grounded to chassis ground
- Multipoint ground should be used where ESD current flow is desired and single-point ground should be sued where discharge current flow is not acceptable
- Secondary shields may be needed between sensitive circuits and the chassis to prevent capacitive coupling from upsetting the circuits
- Inputs should not be edge triggered, but latched and strobed
- All shielded cables must be treated for ESD protection and 360 degree contact is necessary
- Cable bypassing must be done to the chassis or a separate I/O ground, not to a circuit ground
- Loop areas must be kept as small as possible on PCB layout
- A hardware timer can be used to check the sanity of microprocessor. Software filtering can be used to reduce input errors. Avoid unused interrupts
- EDS immune is almost equal to RF immune!

Typical Foundry Parameters



Description	Standard Inch (mm)	Advanced Inch (mm)
Material	FR-4/POLYIMIDE/BT-Resin/High Tg FR-4/Lead Free FR-4	
Max. Number of Layers	70 layer	
Min. Copper Thickness	1/3 oz (12㎛)	
Min. Dielectric Thickness	0.004" (0.100mm)	0.002" (0.051mm)
Min. Board Thickness (a)	0.019"(0.48mm)	
Max. Board Thickness (b)	0.190" (4.8mm)	0.283" (7.2mm)
Board Thickness Tolerance(%)	±10% ~ ±5%	
Layer to Layer Registration	±0.0035" (±0.089mm)	±0.0025" (±0.063mm)
Impedance Control	±8%	±5%
Warpage (inch per inch)	0.008"	0.006"

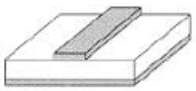
Typical Foundry Parameters



Imaging	Standard Inch (mm)	Advanced Inch (mm)
Min. Trace Width (a)	0.0035" (0.089mm)	0.0028" (0.071mm)
Min. Trace Space (b)	0.058	0.0023"
Min. Annular Ring	0.065	0.00255"
BGA Pitch (b)	0.058	0.0023"

Solder Mask	Standard Inch (mm)	Advanced Inch (mm)
Min. Soldermask Dam (a)	0.004" (0.100mm)	0.003" (0.076mm)
Soldermask Clearance (b)	0.006" (0.150mm)	0.0035" (0.089mm)
Min. SMT Pad Spacing (c)	0.006" (0.150mm)	0.004" (0.100mm)
SokderMask Thickness	0.0007"(0.018mm)	

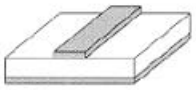
Typical Foundry Parameters



Hole	Standard Inch (mm)	Advanced Inch (mm)
Min. Hole Size (a)	0.0039" (0.10mm)	0.005" (0.127mm)
Max. Hole Size (a)	0.250" (6.35mm)	0.257" (6.50mm)
Hole Tolerance (±)	±0.003" (±0.0762mm)	±0.002" (±0.051mm)
Aspect Ratio	18 : 1	21 : 1
Hole Registration	0.00253"(0.076mm)	

Surface Finishing	Standard Inch (mm)	Advanced Inch (mm)
H A S L	300μ" ~340μ" (7.0㎛ ~ 8.0㎛)	
Immersion Tin	30μ" ~ 50μ" (0.762㎛ ~ 1.27㎛)	
Immersion Gold	2μ" ~3μ" (0.05㎛ ~ 0.076㎛)	
Gold Finger	30μ" ~ 50μ" (0.762㎛ ~ 1.27㎛)	
Nickel Plating	150μ" ~ 300μ" (3.81㎛ ~ 7.62㎛)	
Electrolytic Hard Gold	50μ" (1.27㎛)	

Typical Foundry Parameters

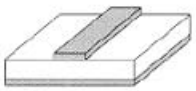


Outline	Standard Inch (mm)	Advanced Inch (mm)
Board Outline Tolerance(±)	±0.008"(±0.200mm)	
Guide Rail	0.400" ~ 0.300"(10.0mm ~ 7.6mm)	
Beveling	20", 30", 45"	

Panel	Standard Inch (mm)	Advanced Inch (mm)
Panel Size	24.0" × 27.5"(609mm x 700mm)	

Refrence :http://www.koreapcb.com/board/index.html

Typical Foundry Parameters



Max. board size (Double-sided): 475 x 533 mm (18" x 21")
Max. board size (Multi-layer): 406 x 254 mm (16" x 10")
Board thickness : 0.5 - 3.0 mm
Min. track between tracks : 100 microns
Min. via/hole dia. : 300 microns

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Summary

- Noise Margins
- Noise Budgets
- EMI and EMC
- Shielding against EMI
- ESD
- Typical Foundry Tolerance Parameters

Wakeup Please lets have Some Food....