# **Type 2, 2nd-Order Sigma Delta Modulator**

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***Abstract –* The Type II, 2nd Order Sigma Delta is a quantizer single bit mixed signal circuit for averaging input signals. The topology covered within the project includes an active loop filter topology that feeds into a one bit quantizer digital circuit. This paper will cover each stage of the sigma delta with time and frequency domain analysis of the outputs of each stage.**

1. **High Level Explanation**

Conceptually, there will be two integrators utilized in the sigma delta loop filter. This determines that the implemented delta sigma is a type 2 topology because the open loop transfer function has two poles at the origin in the Laplace domain.

The sigma-delta ADC is clocked with an internal and external sampling clock. Due to the non-linear behavior of the comparator used in the ADC, the linear model of the sigma-delta ADC uses a summing amplifier structure as the input impedances with an integrating feedback impedance to create the summing junction and the integrator all at once.

The feedback of the digital output has to be turned back into an analog signal that is either Vref or 0V. This analog output is used to compare the error in the physical adjustment and whether or not it needs more 1 or 0 digital output to average out the digital waveform to sum into a decimal analog value. Is that true?

The loop filter of the ADC provides noise shaping because of its ability to adjust for lower frequencies faster, and since the loop filter’s two integrators can’t catch up to higher frequency signals nearly as fast, more errors (which shows up as noise) begin to arise in the higher frequencies. This gives the seemingly high-pass noise shaping characteristic of the ADC, making noise filtering with a low-pass filter following the ADC’s output really effective.

1. **Conceptual Loop Filter Design** In figures 3-6 there are various integrators. Figure 3 the simplest integrator is the basis of how the loop filter will operate in the system. The final loop filter design consists of combining two integrators with a left hand plane zero. In figure 4 and 5 the two integrators cascaded results in the desired system but utilizes a lot of components compared to the figure 6 design that operated with the same functionality but with minimal components.

The Sigma-Delta-based loop filter design has the following characteristics. The circuit has a center frequency of 5kHz, a -3dB cutoff point of 15kHz, and an unity open loop gain. with a center frequency of 5kHz and a -3dB cut-off frequency of 15kHz with an open loop gain of 1.

*A. Loop Filter Design*

The desired transfer function of the filter is from equation (1) below.

(1)

The configurations (to be explained later) to emulate this transfer function were Design 1 and Design 2.

After finding the transfer functions of the 4 individual integrator configurations, two designs were made to fit the desired transfer function in equation (1).

Given that two poles and a zero are needed for this transfer function, the first design uses a first-order inverting integrator with one pole in series (equation (2)) with a non-inverting first-order integrator with another pole and zero (equation (8)). The first design yields a negative output while the second design yields a positive output.

Meanwhile, the second design uses three inverting integrators in series. The first stage is a summing junction with the feedback at the input of the first order inverting op amp from figure 3. The second stage is a first order inverting op amp from Fig. 4. The third stage is an inverting unity-gain op amp whose output feeds back into the input of the first stage summing junction.

Both designs utilize split rail supply so the circuit operates centered at ground, and both designs utilize voltage dividers as voltage references.

In the end, the first design was chosen to be built as it had less op amps and points of failure.

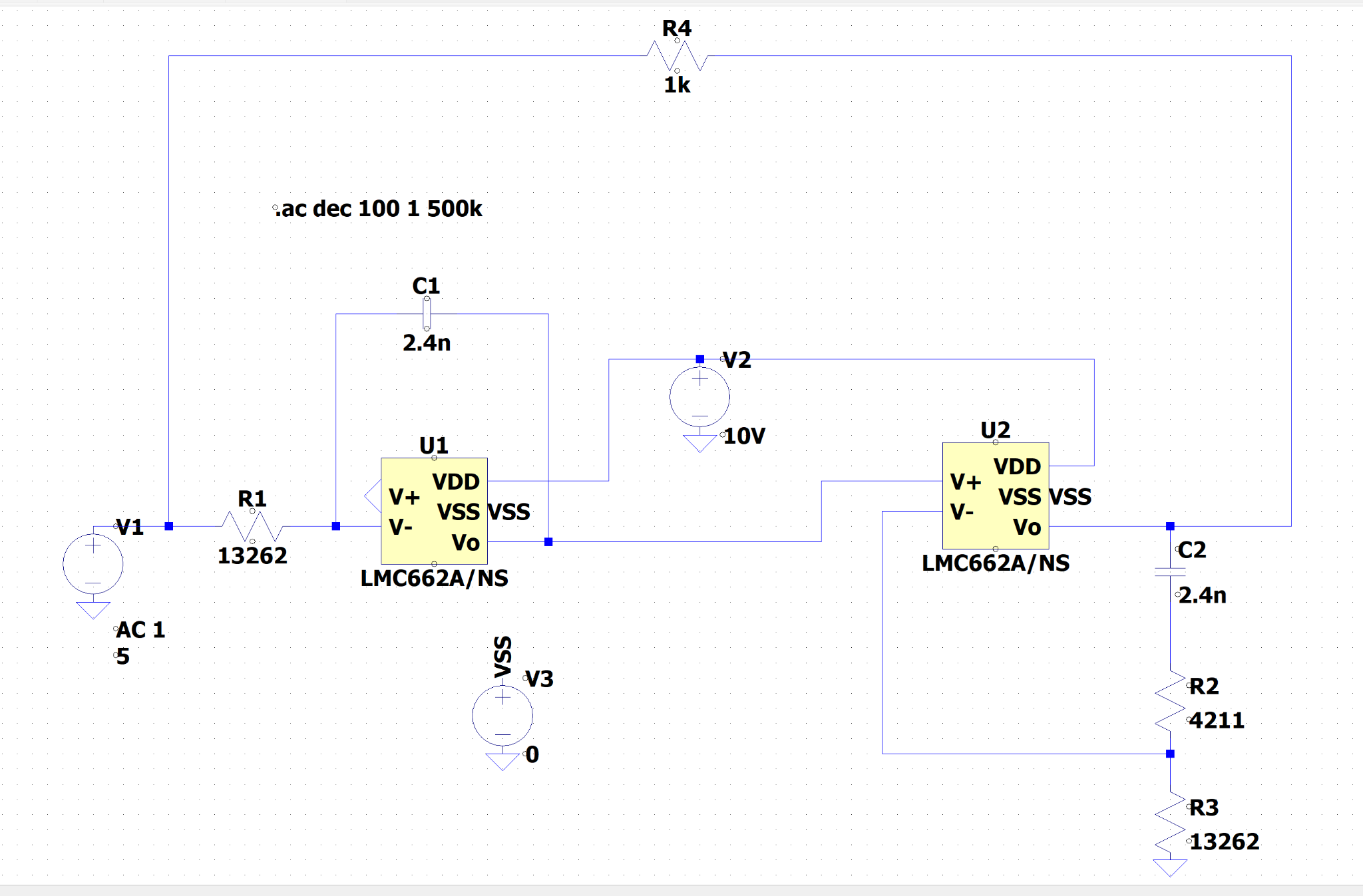


Fig. 1 First Loop Filter Design Schematic.

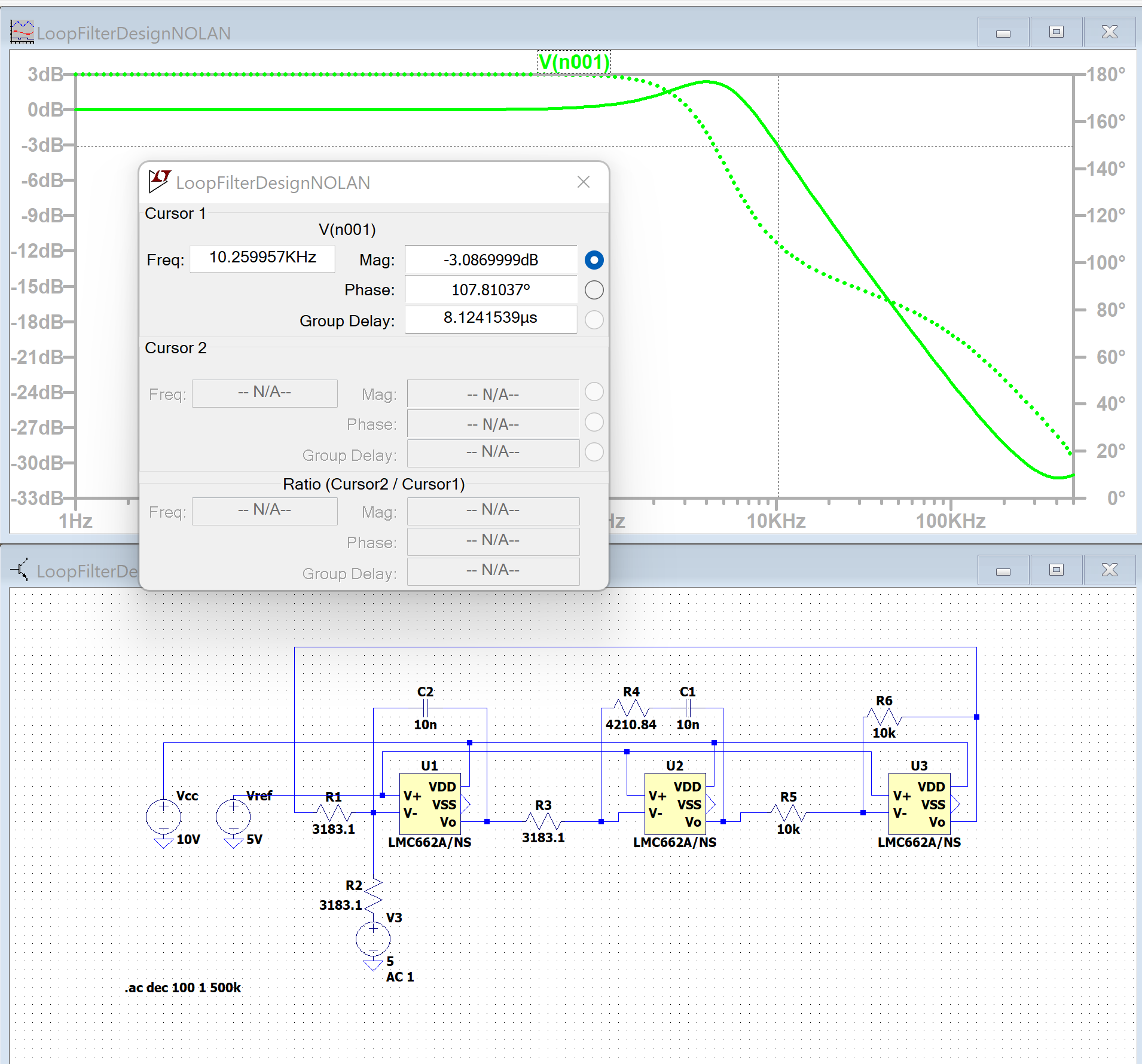


Fig. 2 Second Loop Filter Design Schematic.

1. **Integrators Used for Loop Filter Design**

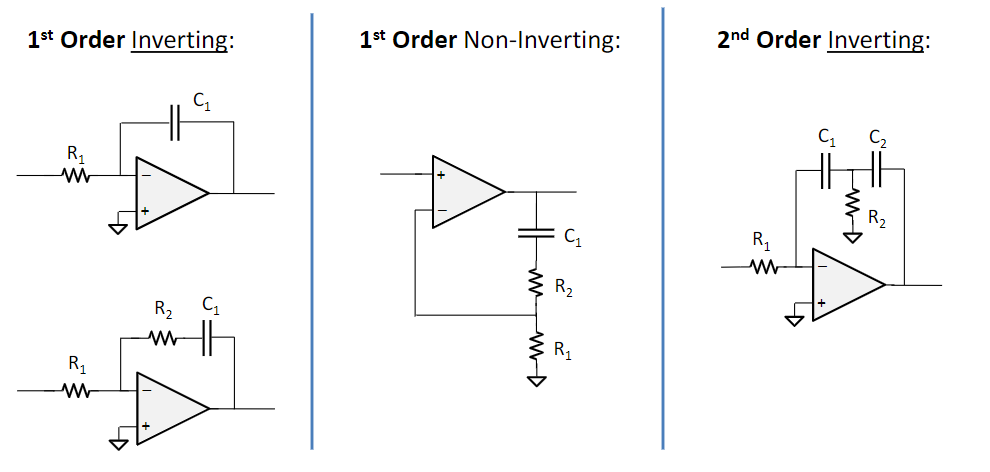
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Fig. 3 1st Order Inverting Integrator.

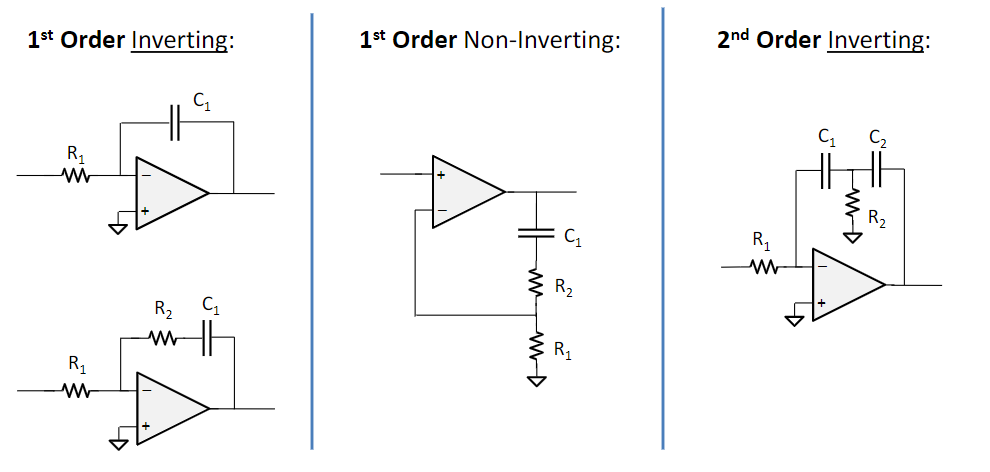


Fig. 4 Another 1st order inverting integrator.

Note: C1 = C2, but R1 != R2

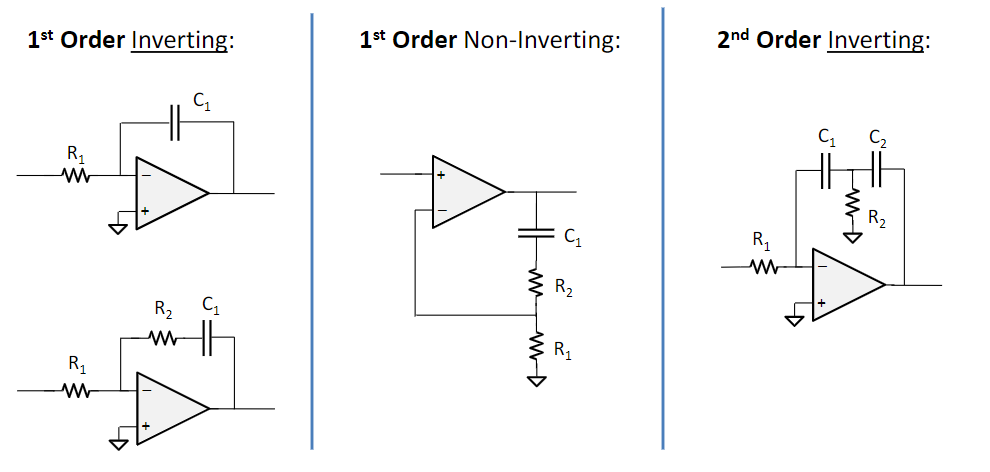


Fig. 5 1st-order non-inverting integrator.

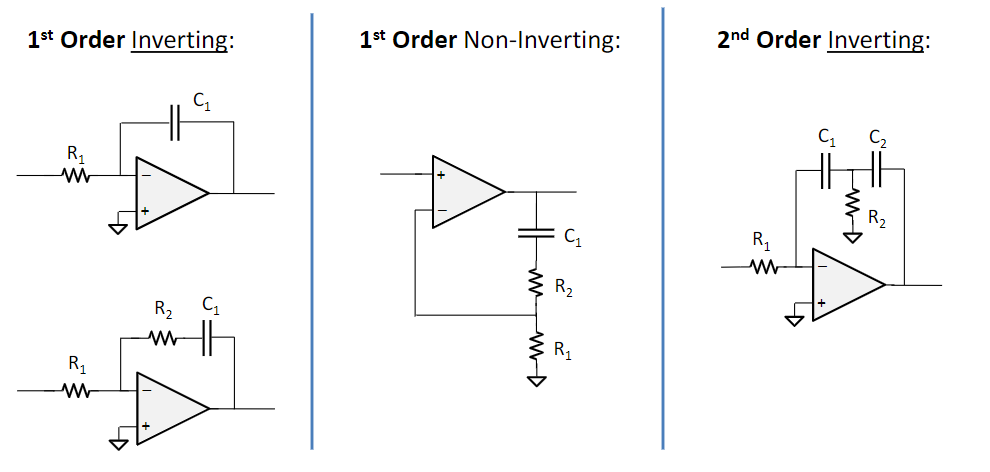


Fig. 6 2nd Order Inverting Integrator.

Equations 2-13 detail the specifics for filter characteristics of each design. Taking a closer look at equation 13 reveals that the left hand plane zero ωz determines the primary NEED TO CALC THEN DETERMINE ITS ROLE

1. **One Bit Quantizer**

*A. Comparator*

The comparator used in the One Bit Quantizer is the TLV3501AID from Texas Instruments. The suggested comparator was not available, but the TLV3501AID is a suitable replacement. The comparator has a relatively high speed of 4.5 nanoseconds and split rail operation. In this application a split rail of positive and negative 2.5V was used. The comparator was tested individually with DC inputs to ensure correct operation before interfacing with other components. The figure below shows a square wave input to the comparator and the resulting waveform is a positive and negative 2.5V output on the scope.

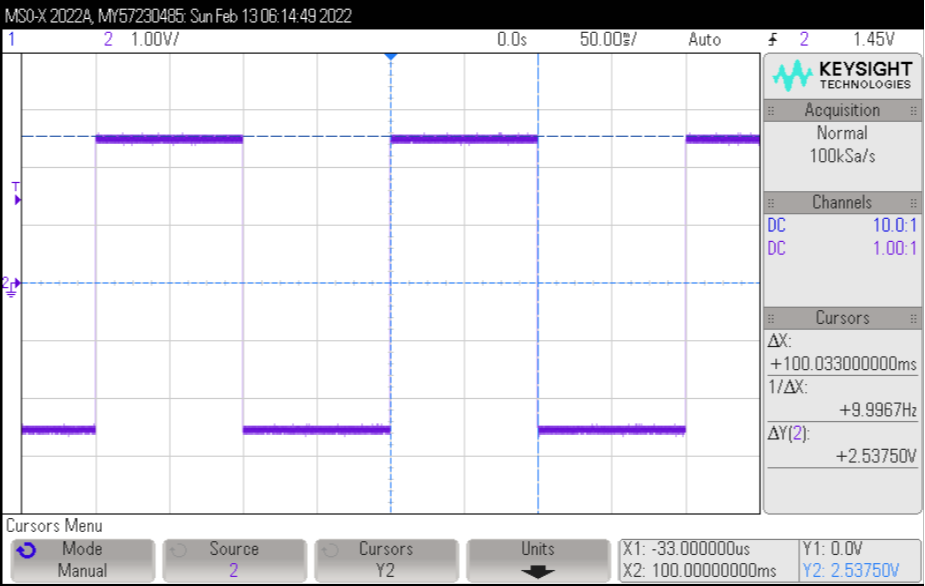


Fig. X Comparator Square Wave Test

*B. D-Flip-Flop*

The D-Flip-Flop was the CD74HC74 from Texas Instruments. The CD74HC74 is a dual channel D-Flip-Flop that has both Q and Q-Bar outputs. In the project only one channel was used. The following figure shows the CD74HC74 in operation with a positive and negative 1V square wave. The CMOS flip flop output is pulled from Q-Bar and shows full rail operation.

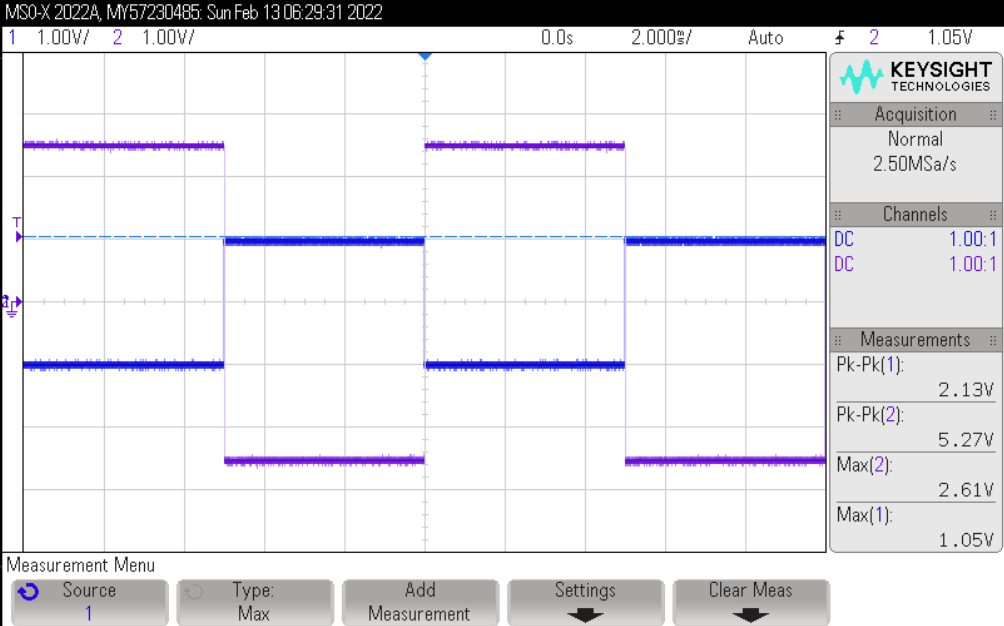


Fig. X Comparator Square Wave Test

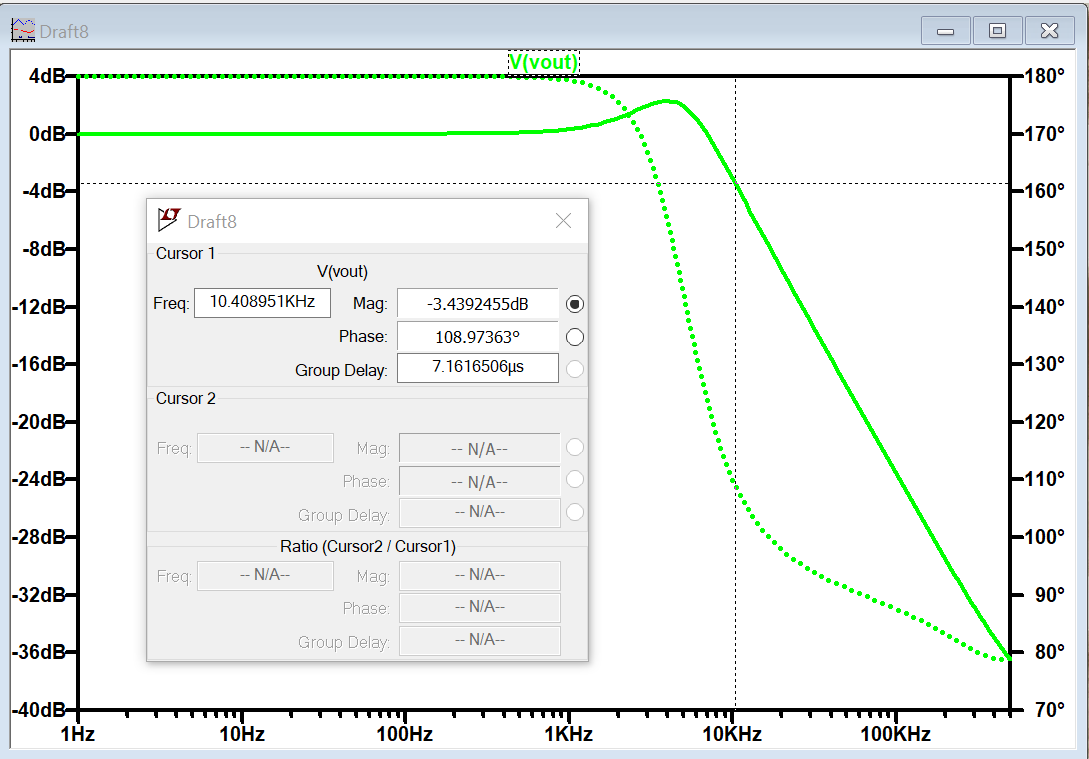
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Fig. 7 Loop Filter I Design Simulated Freq. -3dB point.

**VI. Deliverables for Performance of the ΣΔ Modulator**

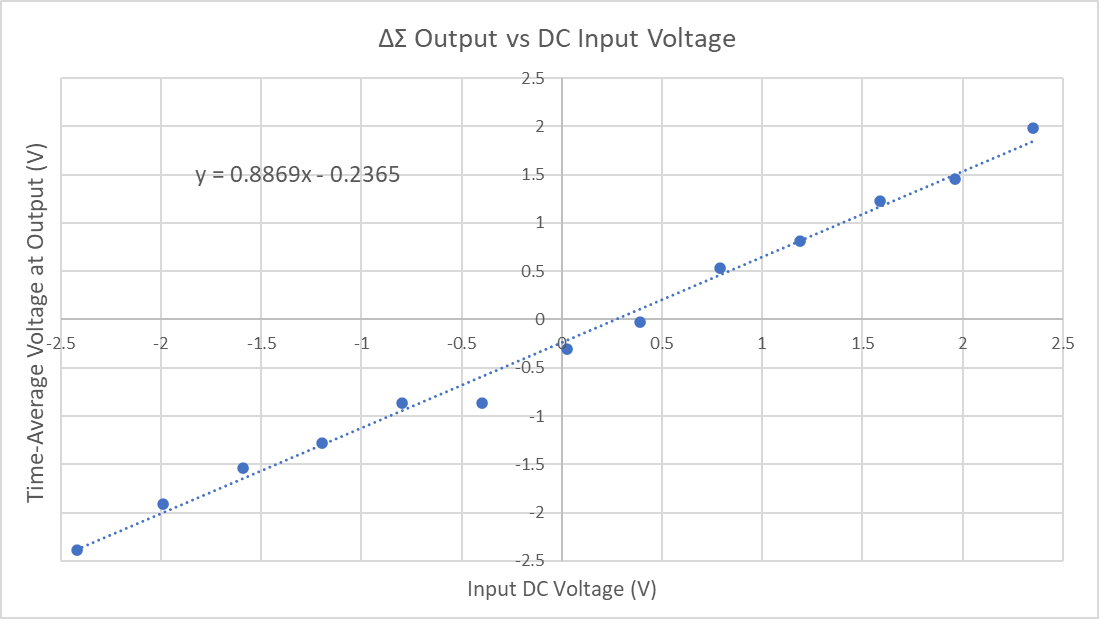


Fig. x Modulator output compared to its input.

Figure X depicts different input DC levels and how the system reacts. The plot reveals an apparent linear relationship between the input signal and output signal which is to be expected due to the nature of the device. Due to there being discrete quantization levels an input signal can only increase output average voltage by increasing the input voltage. In the same figure there are two distinct points that have nearly the same y-value. This phenomenon is due to the input signal not being of high enough value for the system to respond and raise the output voltage. If that value was to increase by a small margin the output voltage would be expected to lie on the expected linear relationship.

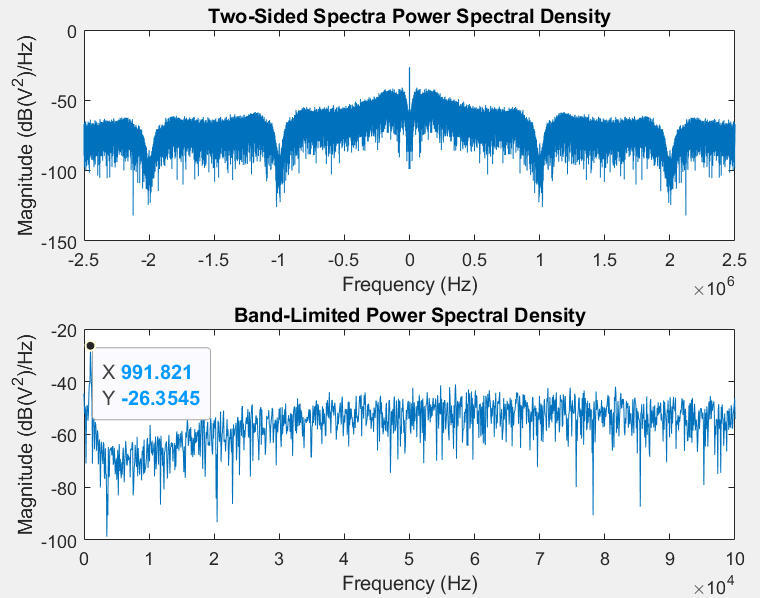


Fig. x 1kHz, 2Vpp Sine wave PSD, fs = 5MHz.

In figure X, the power spectral density is concentrated at the 1kHz input sine waveform while the quantization noise due to the comparator and flip-flop is shaped at approximately 20 dB/dec up to approximately 40kHz. This shaping is due to the two integrators and the left hand plane zero resulting in the 20dB/dec shape.

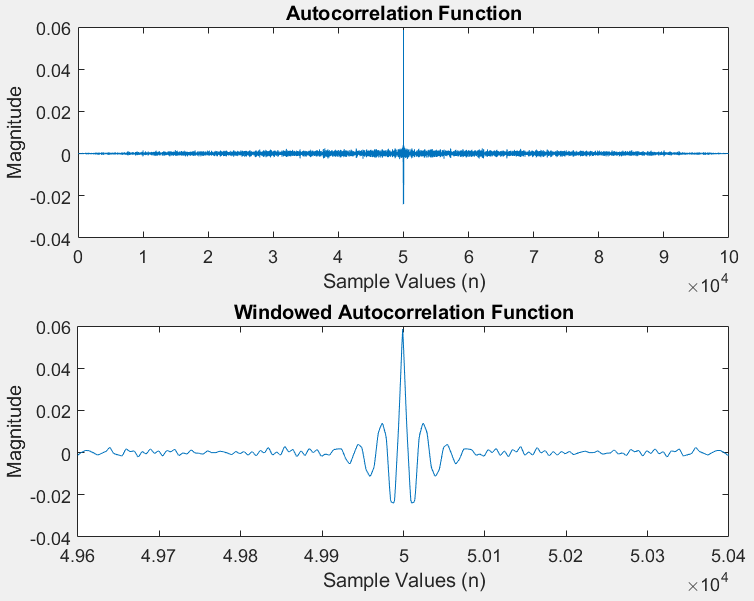


Fig. x ACF of 0V input, fs = 5MHz

IDK WHY THIS THING LOOKS LIKE A SINC

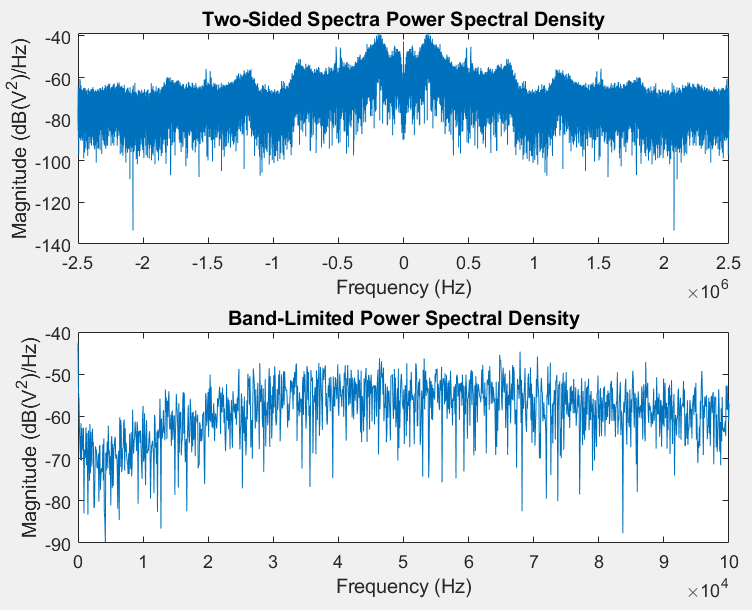


Fig. x 0V PSD, fs = 5MHz

Similar to the test sine waveform, the DC input waveform seen in figure x also experiences noise shaping close to DC of approximately 20dB/dec as predicted by the system. Additionally, compared to the previous sine waveform the frequencies that experience this trend are within a tighter bandwidth of 30kHz rather than 40kHz in figure x.

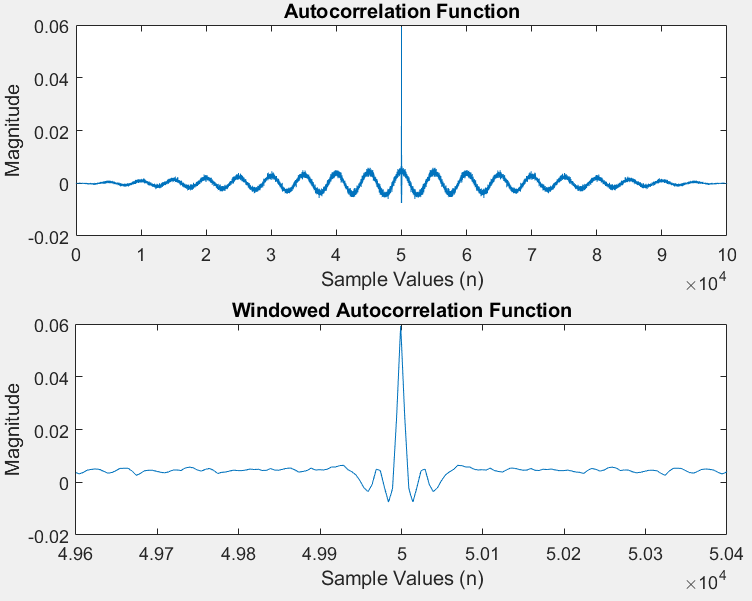


Fig. x 1kHz, 2Vpp, Sine wave ACF, fs = 5MHz.

FUCKING LOST. The autocorrelation fucntion reveals a sinusoidal relationship with a frequency of 1kHz as well as a modulated signal within that sinusoid of approximately 1MHz which is the same value of the clock that is used to drive the system.

**VI. Finalization of Design**

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REFERENCES

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Recommend: MAX4234, LT1711, and CD74HC74.

(or circuits with similar voltage, current, and speed capability)

[4] F. Ohnhauser. Analog-Digital Converters for Industrial Applications Including an Introduction to

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