

*Greetings from  
IEEE EMC Society & Georgia Tech*

# **Designing for Power Integrity Status, Challenges and Opportunities**

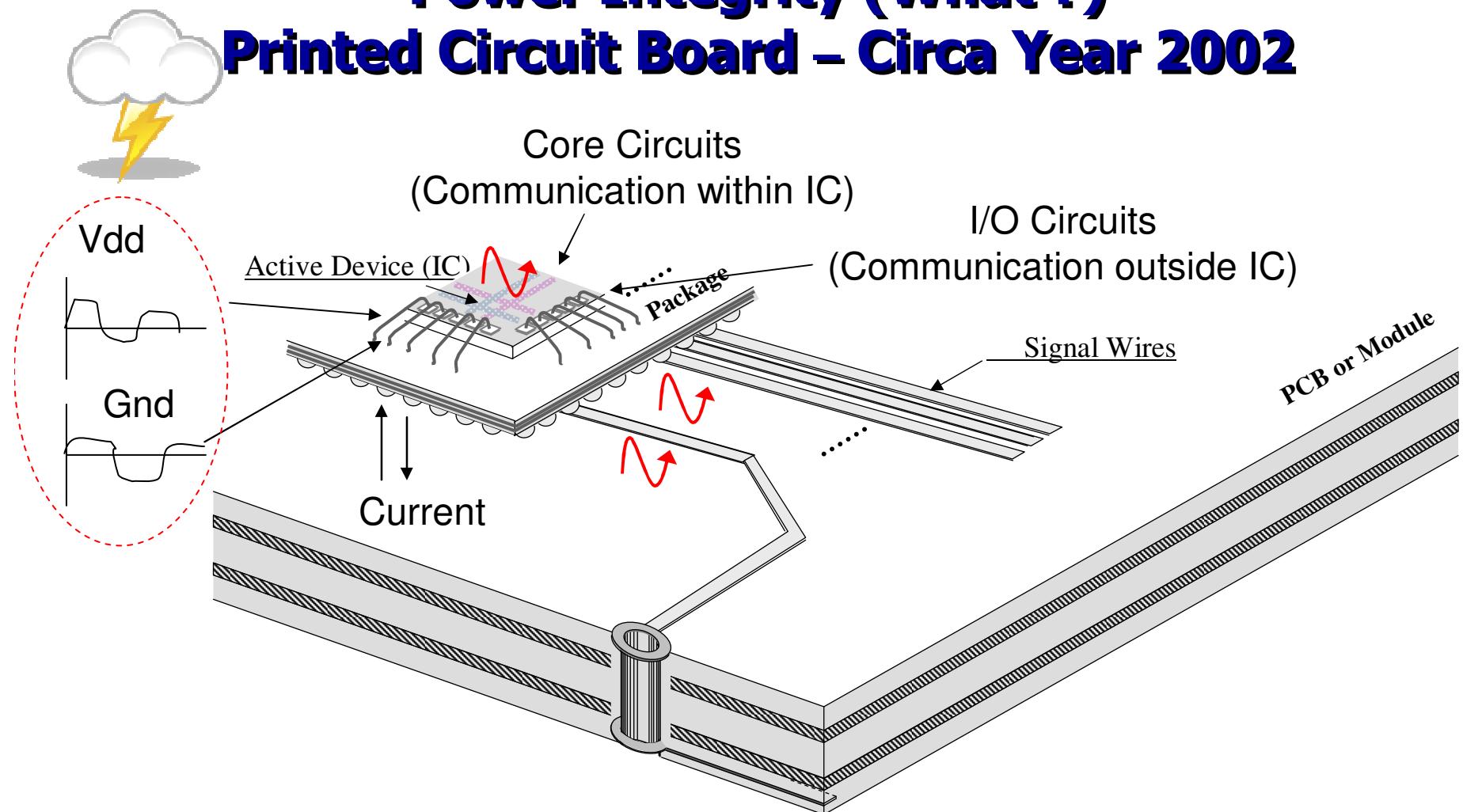
*Madhavan Swaminathan, IEEE Fellow  
Distinguished Lecturer, IEEE EMC Society  
John Pippin Chair in Electromagnetics  
School of Electrical and Computer Engg.  
Director, Interconnect and Packaging Center*



# Outline

- Power Integrity – What and Why ?
- Case for Low Impedance Power Distribution (Status)
- Return Path Discontinuities (Challenges)
- Innovation in EDA
- Some Wild Ideas.....(Opportunities)
- Summary

# Power Integrity (What ?) Printed Circuit Board – Circa Year 2002

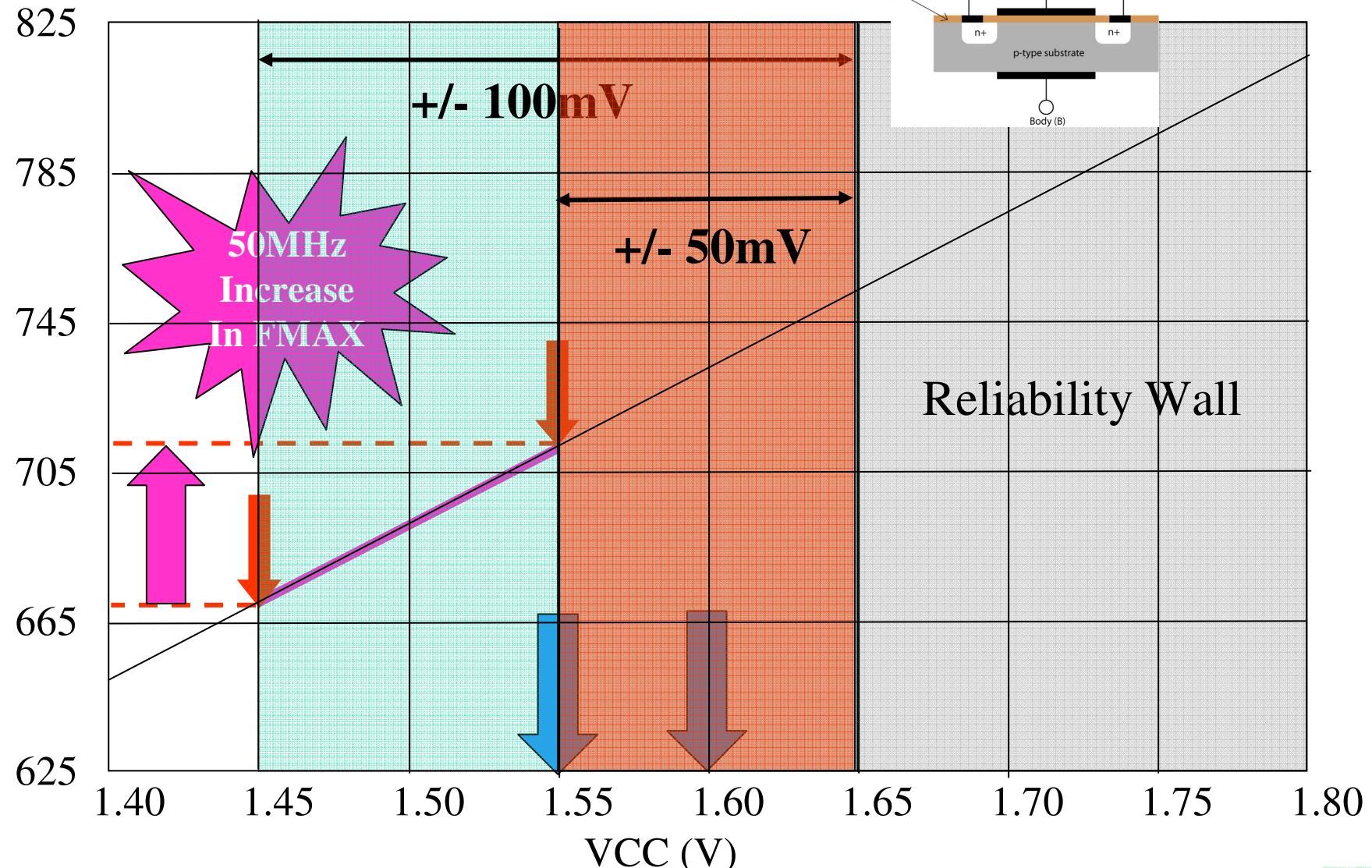


- ❑ Power needs to be supplied to two kinds of circuits – Core & I/O
- ❑ While keeping the Vdd and Gnd nodes at zero fluctuation (DC & AC)

# Power Integrity (Why ?)

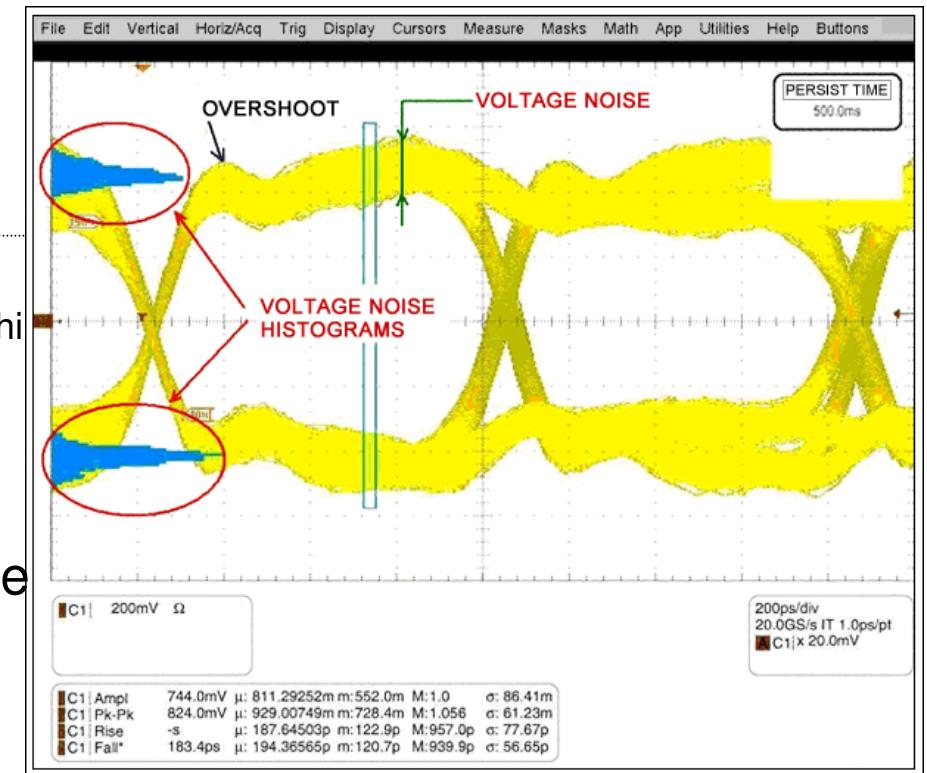
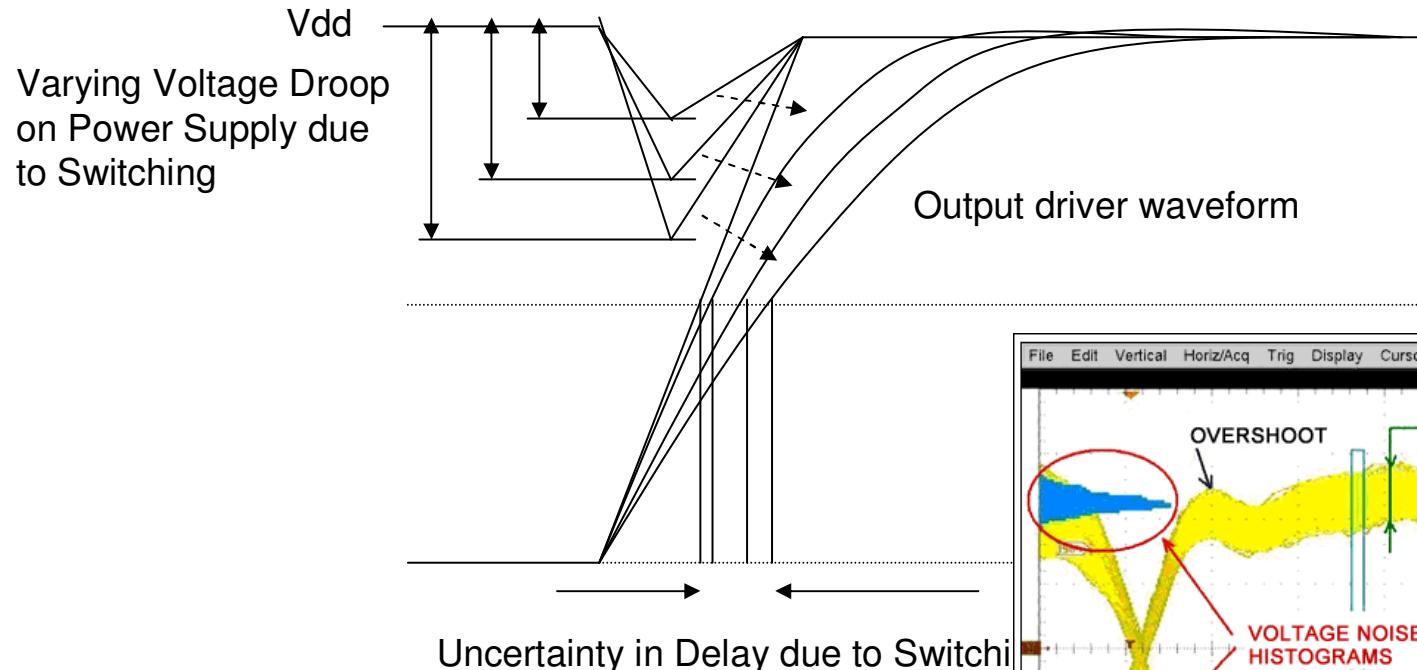
## Power Distribution Affects Operating Frequency

FMAX (MHz)



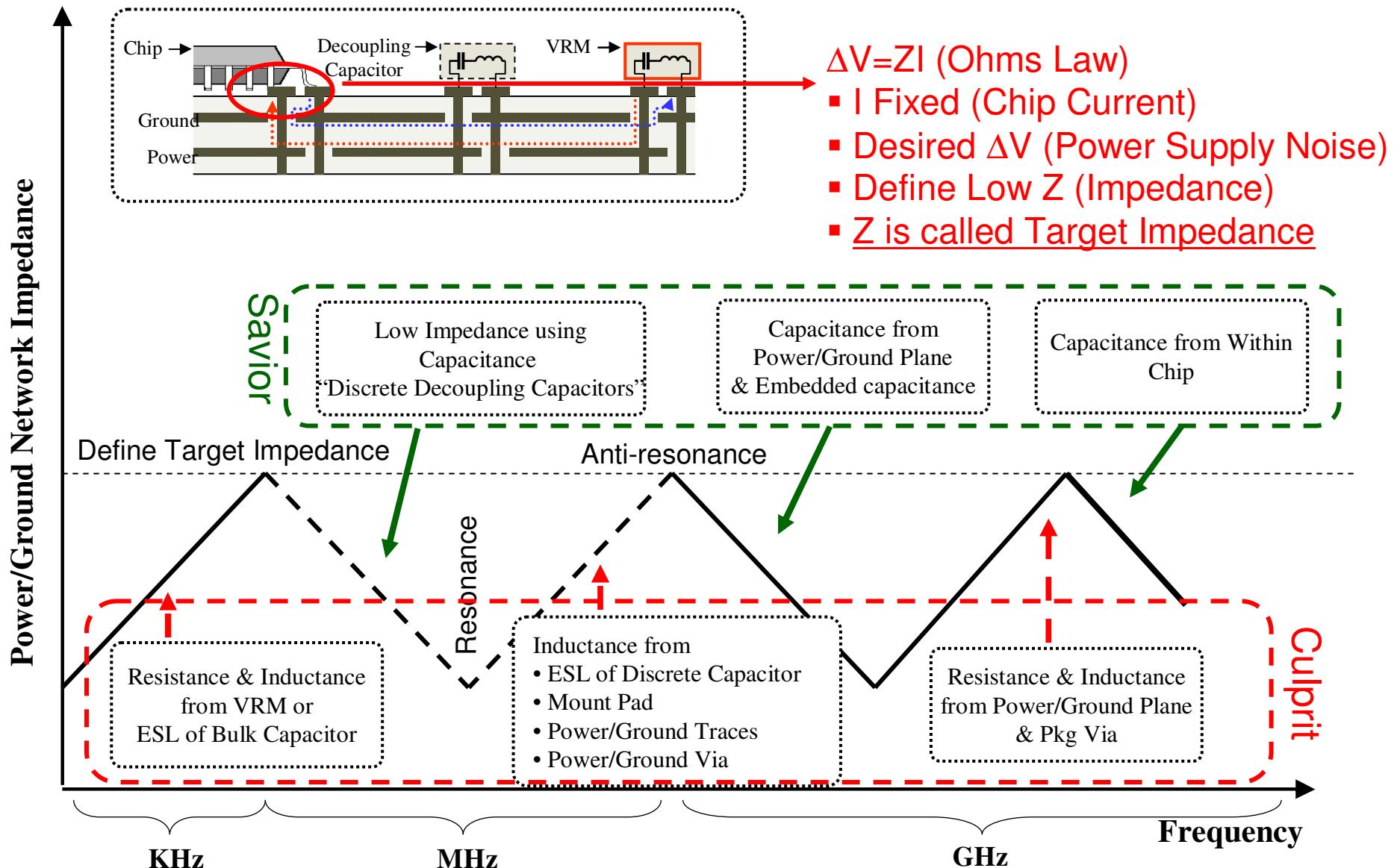
# Power Integrity (Why ?)

## Power Distribution Affects the Eye



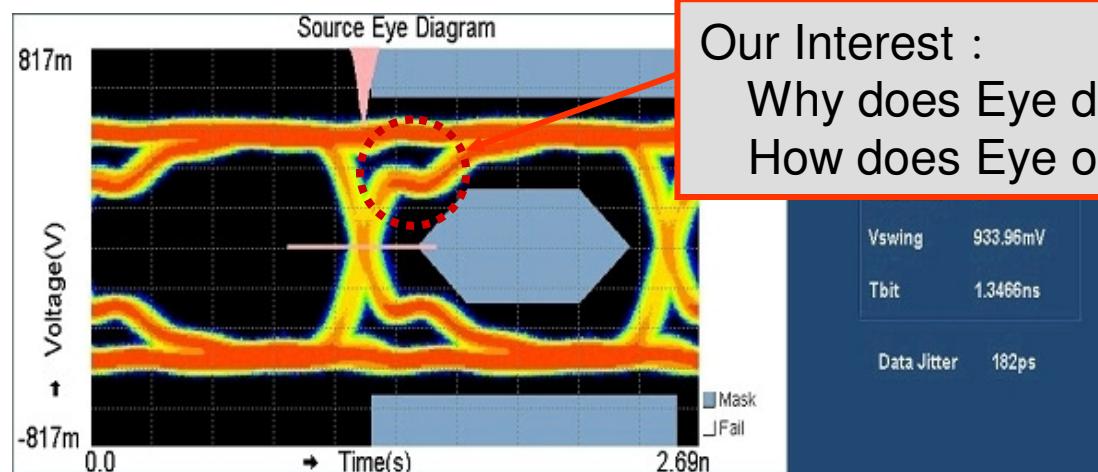
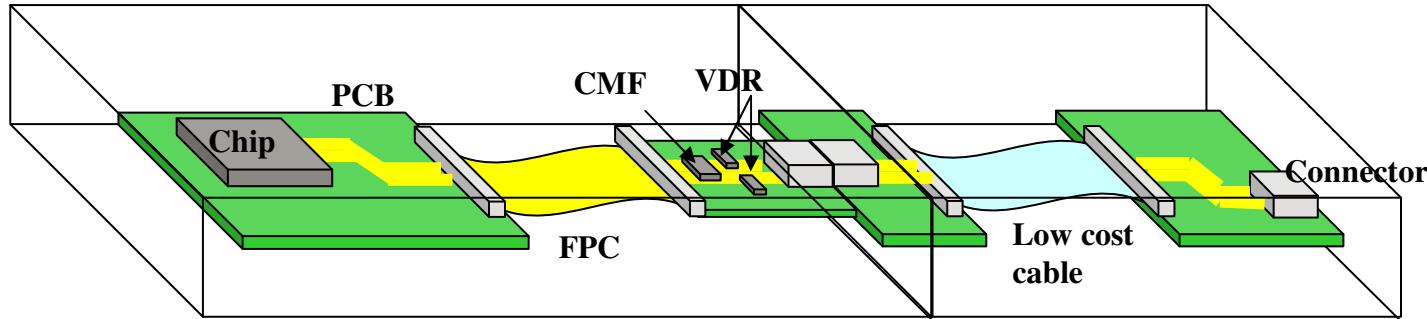
- Random bits generate random power supply noise
- Leading to Random Rising/Falling Edge & Ringing
- Causing Data Dependent Jitter & Eye Closure

# Case for Low Impedance Power Distribution



M. Swaminathan and E. Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", Prentice Hall, 2007

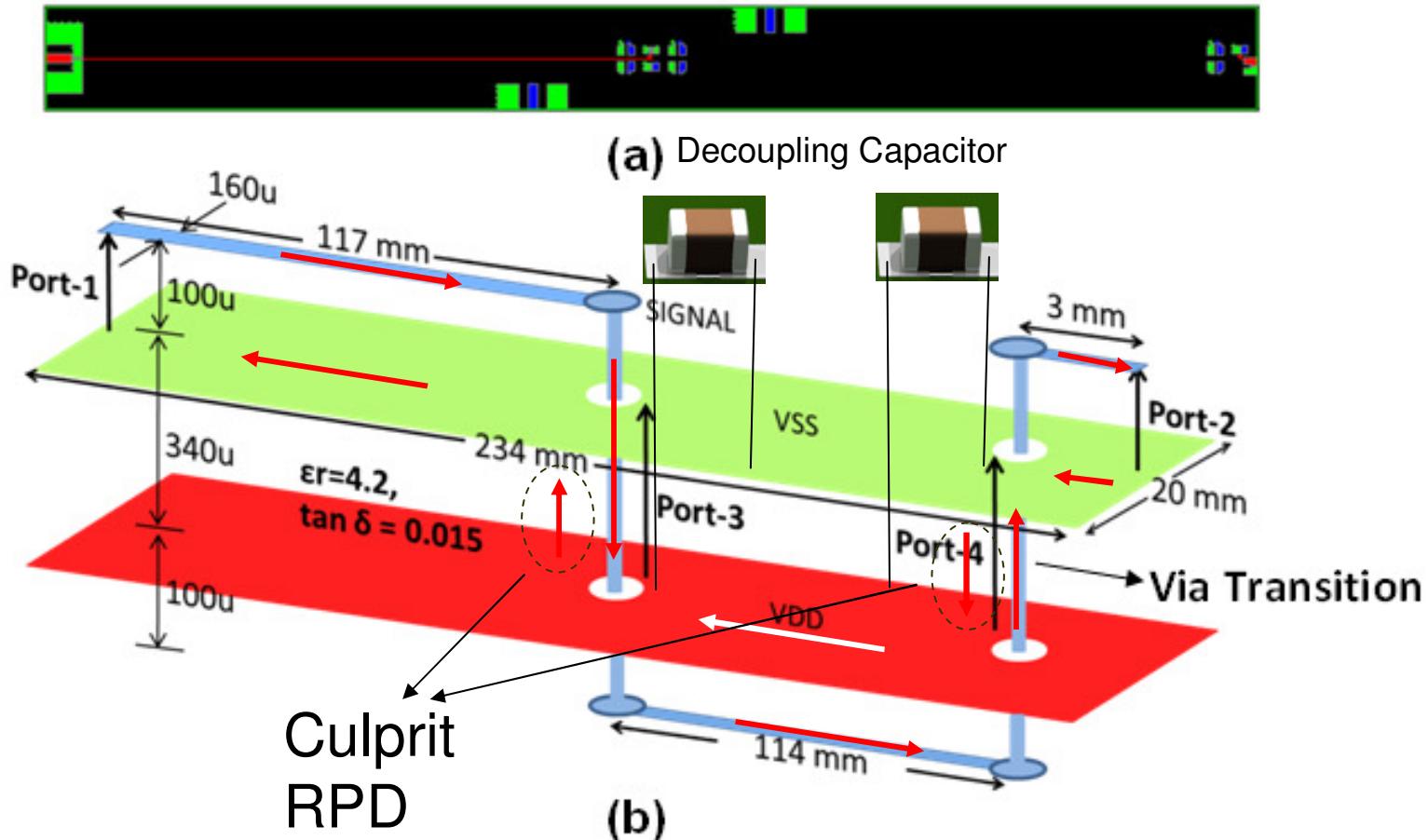
# Let's Focus on I/O – The High Speed Channel



Our Interest :  
Why does Eye degenerate?  
How does Eye open?

- What causes the eye to degrade in high speed systems ?
- Is it the Signal, the Power, or a combination of the two ?

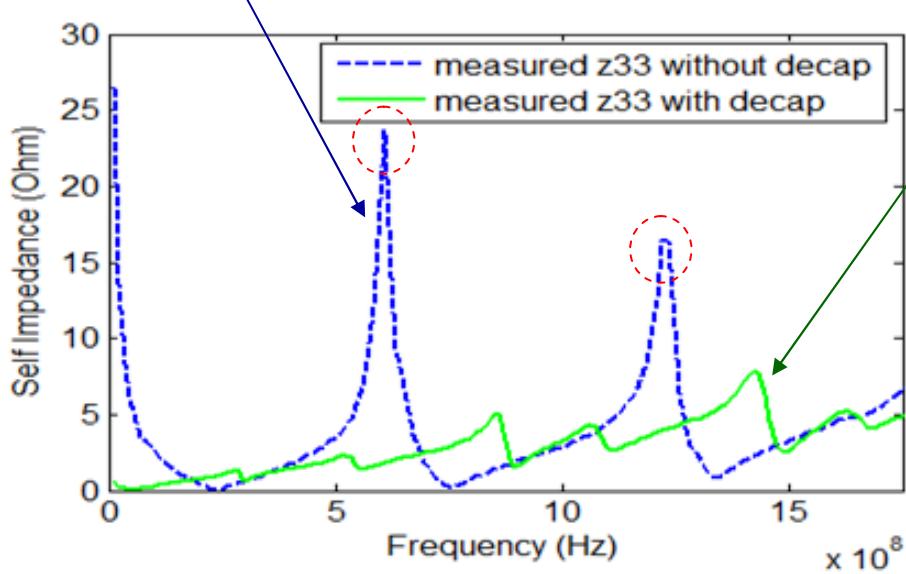
# Let's Start with a Simple Example



- Follow the Return Current
- Discontinuity occurs at the Via
- We call this as the Return Path Discontinuity (RPD)

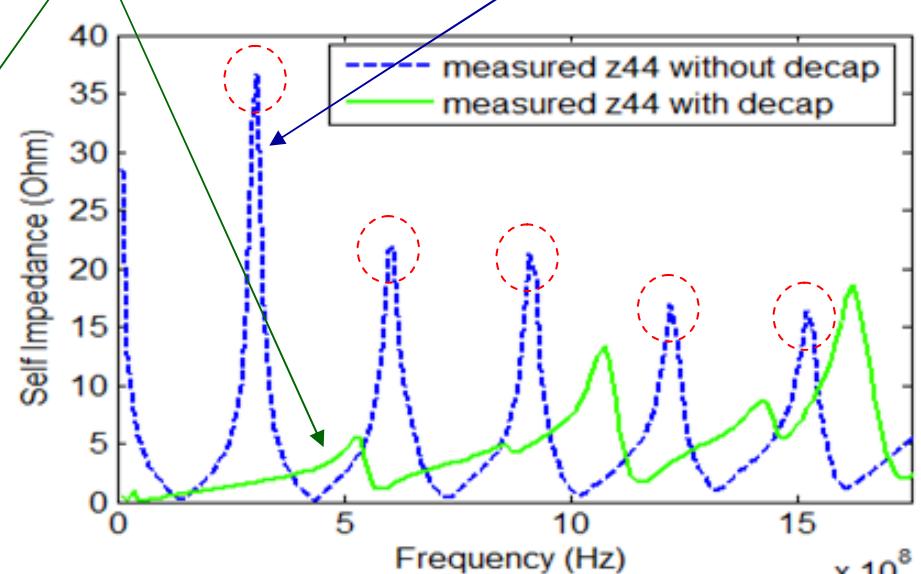
# Self Impedance between Power and Ground at Via Discontinuity

No caps



Port 3 (Z33)

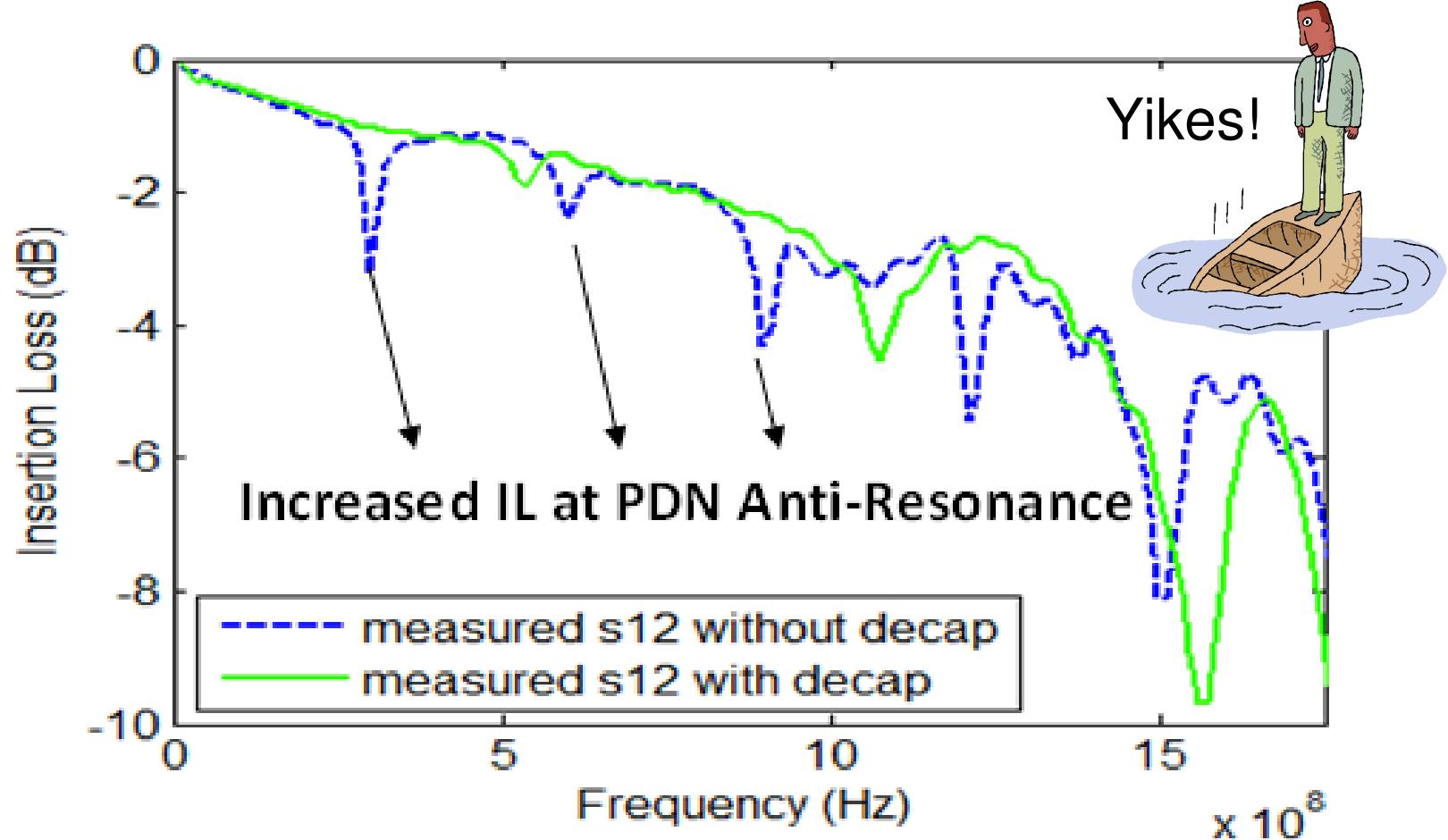
With caps



Port 4 (Z44)

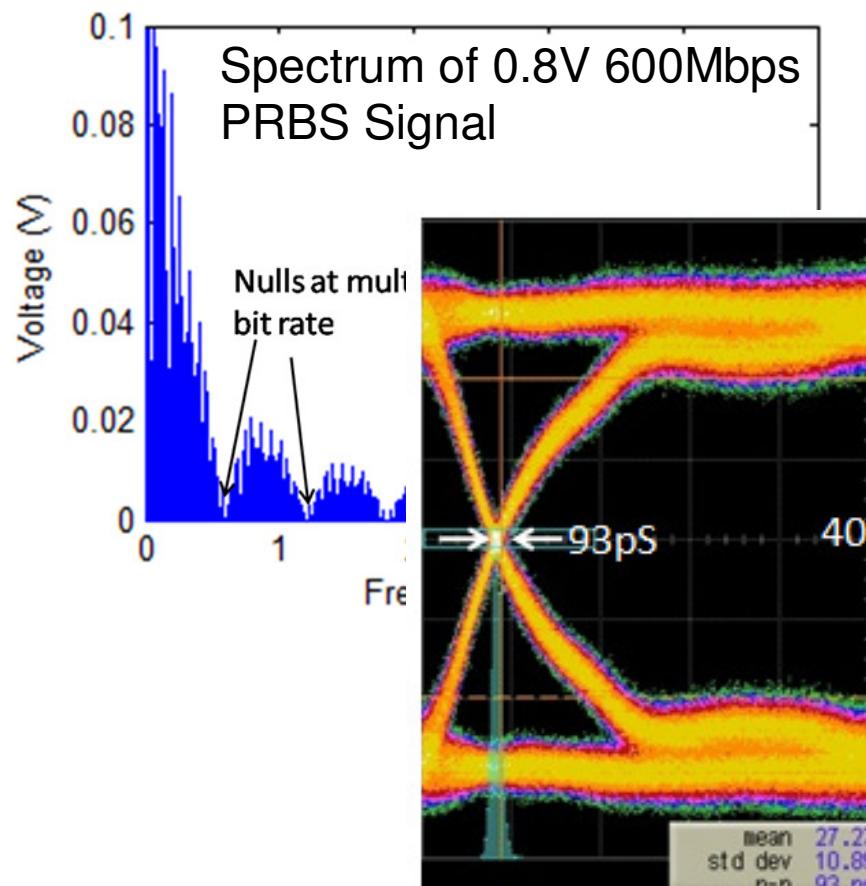
- ❑ Impedance peaks (anti-resonance) is due to cavity resonances between planes
- ❑ Port 4 has more closely spaced anti-resonances than Port 3 due to proximity to Edge
- ❑ Impedance magnitudes are similar with and without caps at high frequencies

# Does Impedance between Power and Ground Planes Affect Insertion Loss ?

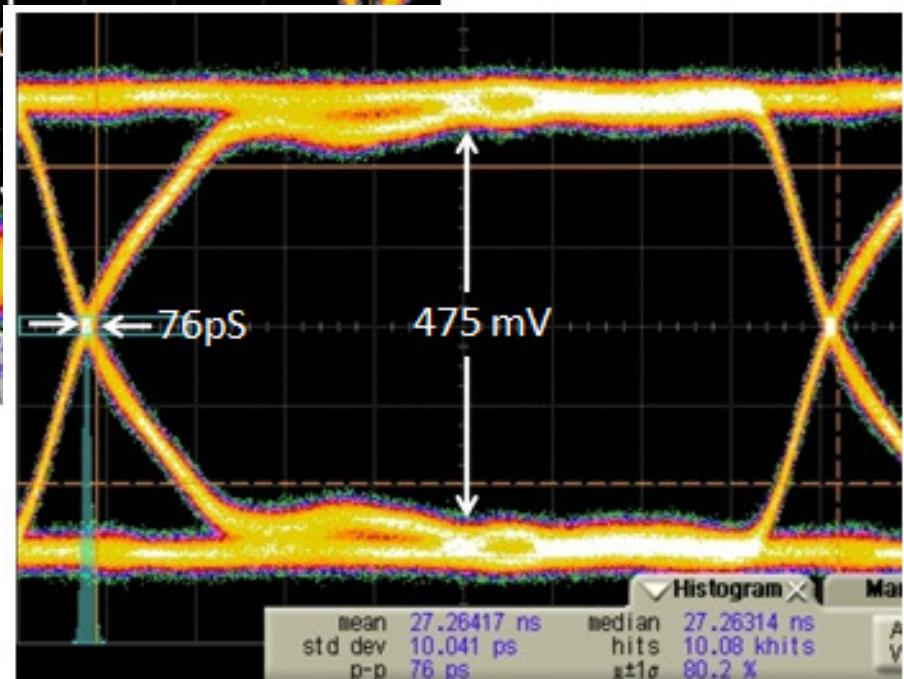


- ❑ Increased Insertion Loss at discrete frequencies can cause excessive attenuation and jitter
- ❑ Very commonly occurs in both packages and PCBs due to RPDs

# Response to 600Mbps PRBS



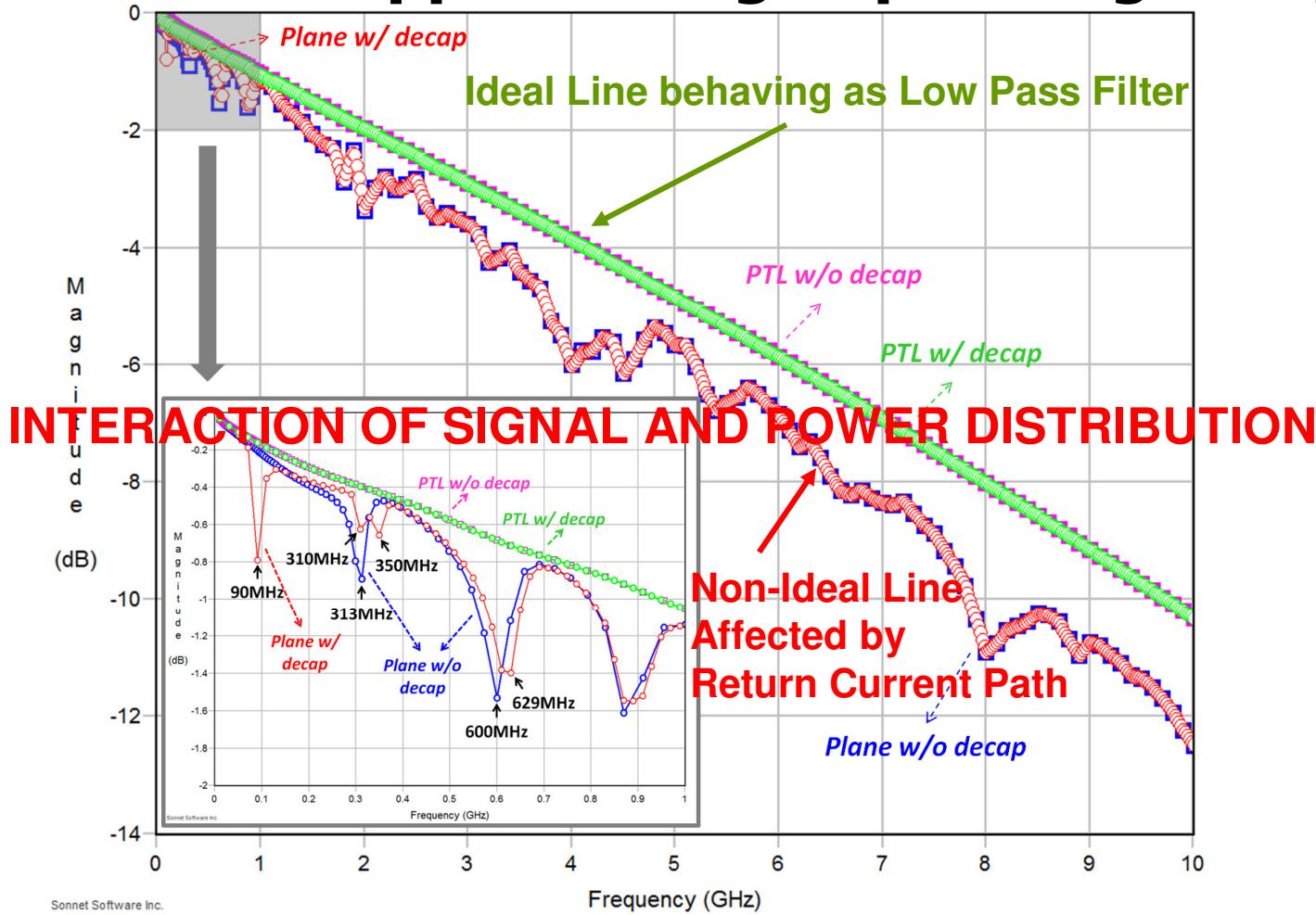
- Spectrum is a  $\text{Sinc}^2$  function
- Nulls occur at multiples of bit rate
- Without Decoupling Capacitors
- With Decoupling Capacitors



- Decoupling capacitors increase amplitude of signals (~20% improvement)
- Significant jitter introduced, which is reduced with decoupling capacitor (~20% improvement)

# Return Path Discontinuities

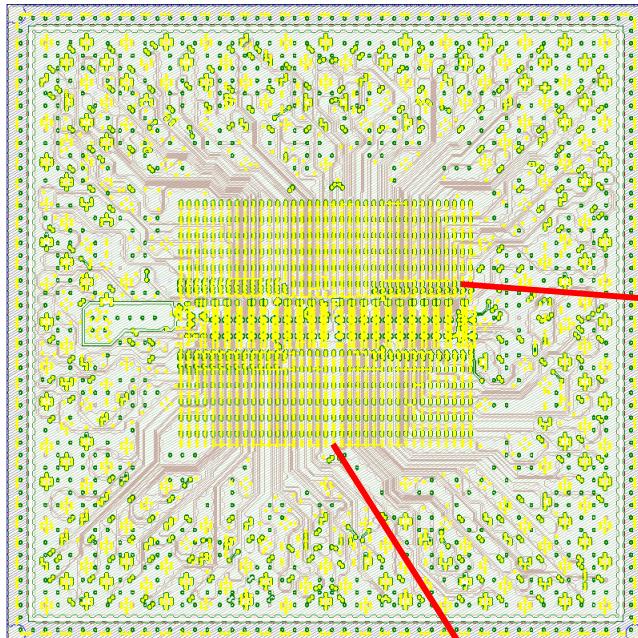
## The Show Stopper for High Speed Signaling



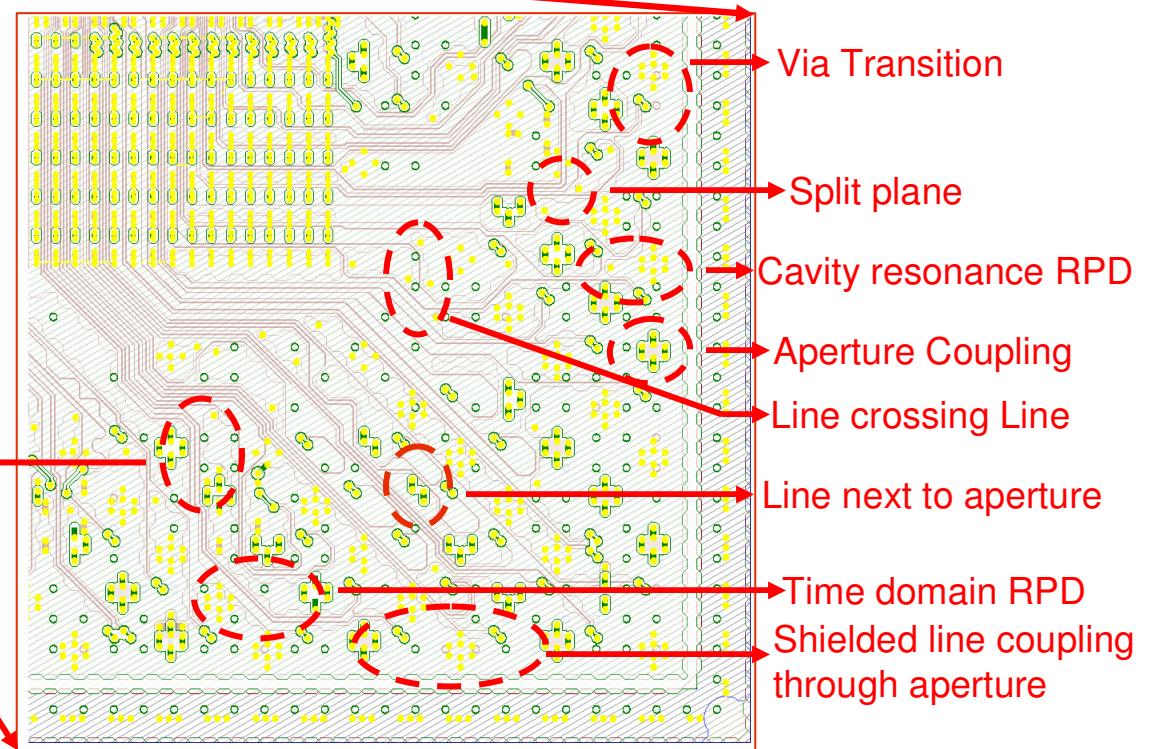
- ❑ Due to non-ideal current return path !
- ❑ Some of you may say: But we have known this for years – so why is this so difficult to manage ?

*M. Swaminathan, D. Chung, S. G. Talocia, K. Bharath and J. Xie, "Designing and Modeling for Power Integrity", IEEE Transactions on Electromagnetic Compatibility, Special Issue, Invited Paper, Vol. 52, Issue: 2, pp: 288-310, 2010*

## Reason: RPDs are many in a High Speed Design – Identifying and mitigating them can be Challenging

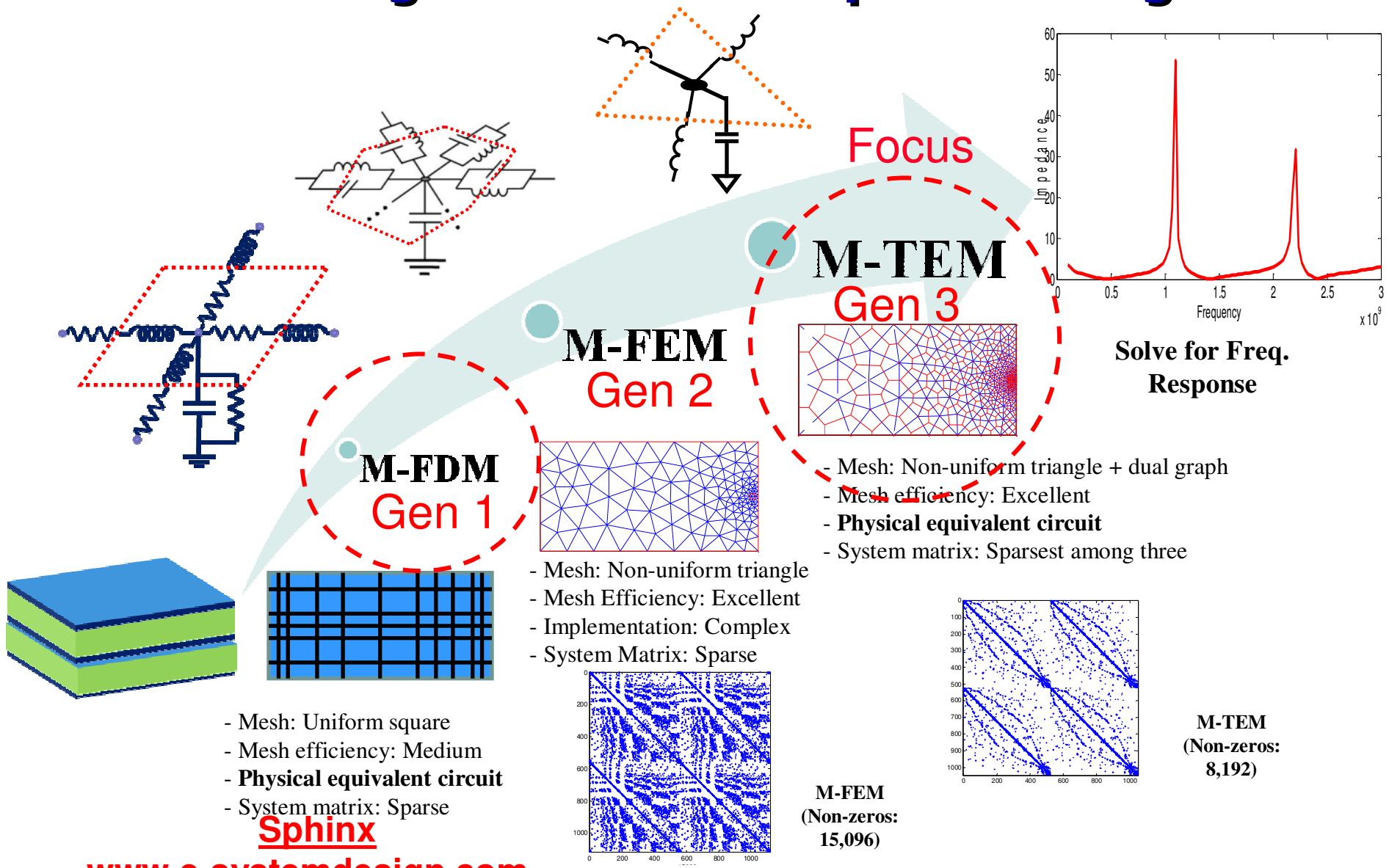


- Very difficult** to identify and gauge effects
- RPD effects are **both local and global**
- Have to rely on an SI/PI tool to enable their identification & mitigation
- Needless to say, the tool has to be reasonably accurate, fast and provide **feedback** on the sources of RPD



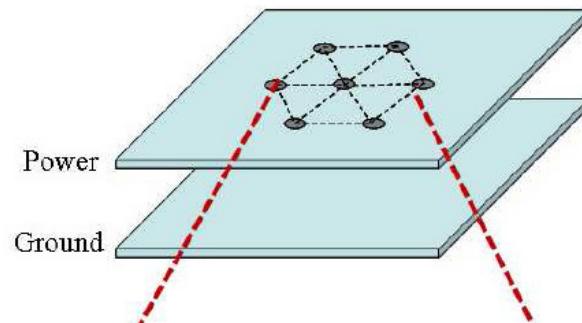
Sub-set of RPDs in a package  
• Full list can be exhaustive

# RPD Modeling Methods Developed at Georgia Tech



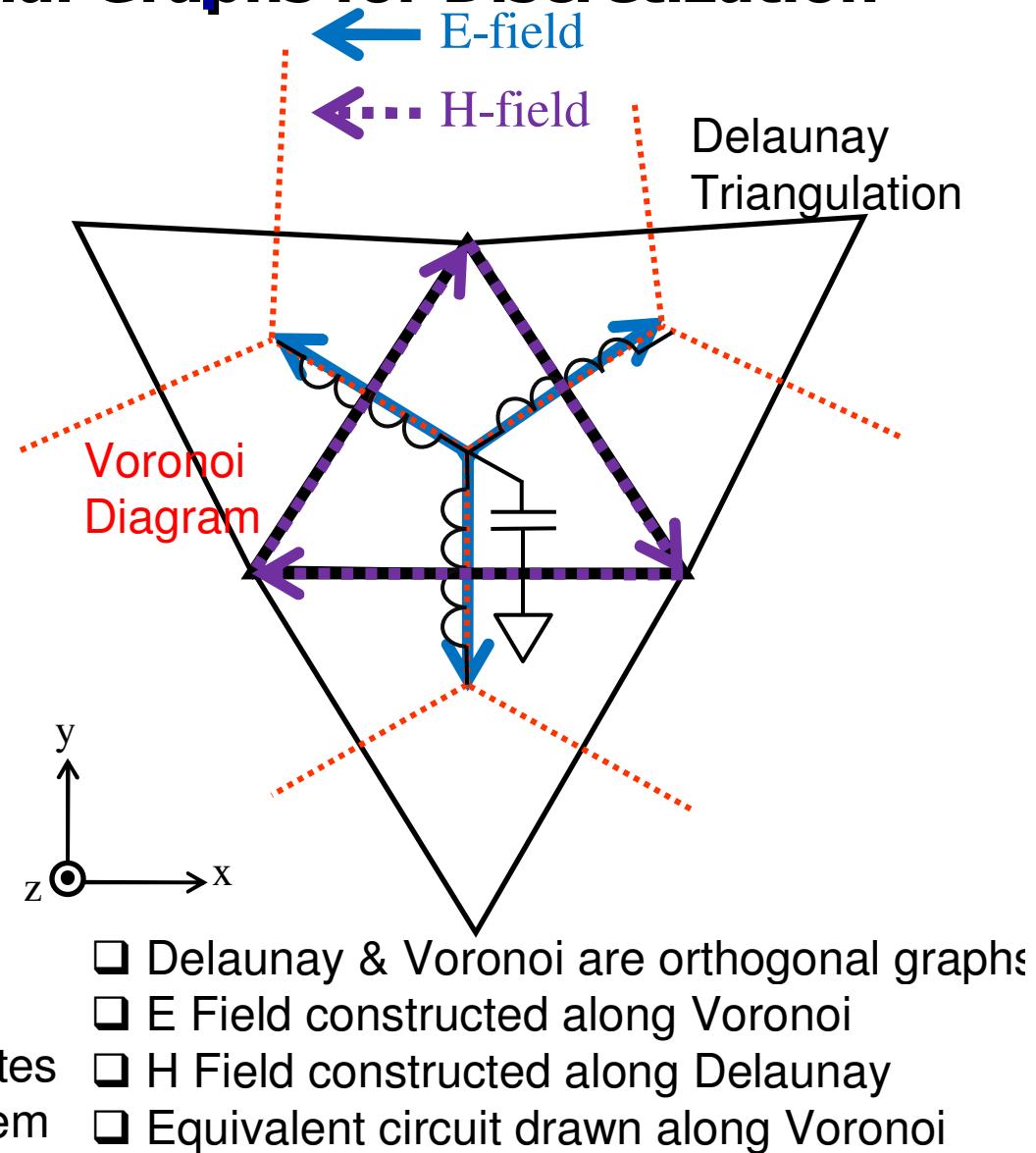
# Finite Difference Frequency Domain Method

## Use of Dual Orthogonal Graphs for Discretization



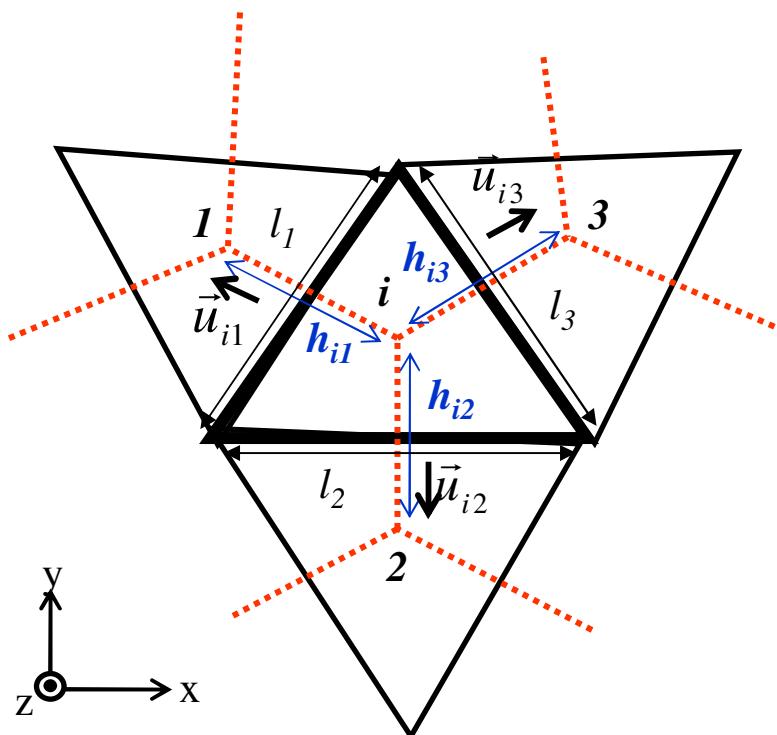
$$(\nabla_t^2 + k^2) u = -j\omega\mu d J_z$$

- Large planar structures
- Small dielectric thickness
- Wave propagation governed by Helmholtz Equation (2D)
- Structures can have large and small apertures
- Can have 15 – 20 layers
- Standing waves create resonances
- Due to High Q of the cavity, generates noise that propagates across the system

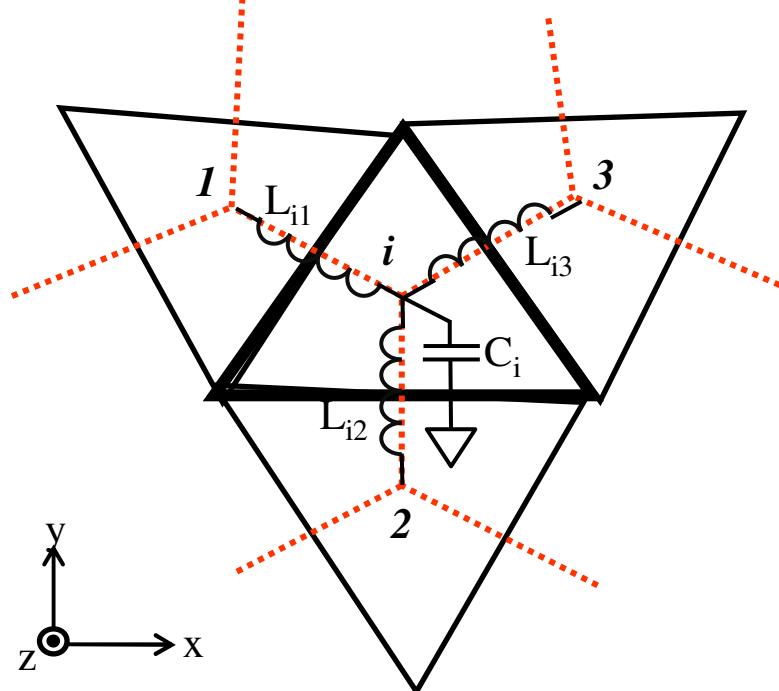


# Multi-layered Triangular Element Formulation (MTEM)

Applying Maxwell-Ampere's  
Circuital Law



Applying Analogy between  
Maxwell-Ampere's Law &  
Kirchoff's Current Law



$$\oint_C \vec{H} \bullet d\vec{l} = \iint_S (\vec{J} + j\omega\epsilon\vec{E}) \bullet d\vec{s}$$

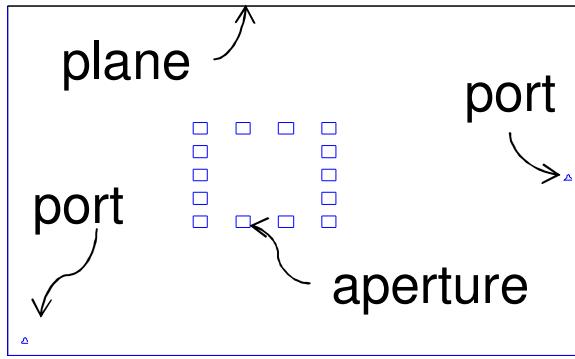
$$-\frac{1}{j\omega\mu d} \sum_{k=1}^3 \left\{ (V_i - V_k) \frac{l_k}{h_{ik}} \right\} = j\omega\epsilon \frac{V_i}{d} A_i$$

$$j\omega C_i + \frac{1}{j\omega} \sum_{k=1}^3 \frac{(V_i - V_k)}{L_{ik}} = 0$$

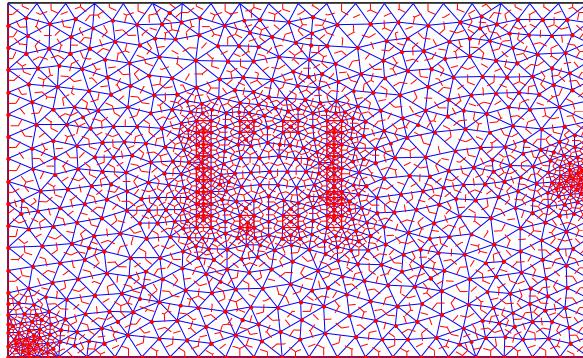
$$C_i = \epsilon \frac{A_i}{d}; L_{ik} = \mu d \frac{h_{ik}}{l_k}$$

# Mesh Generation for Metal Planes with Apertures

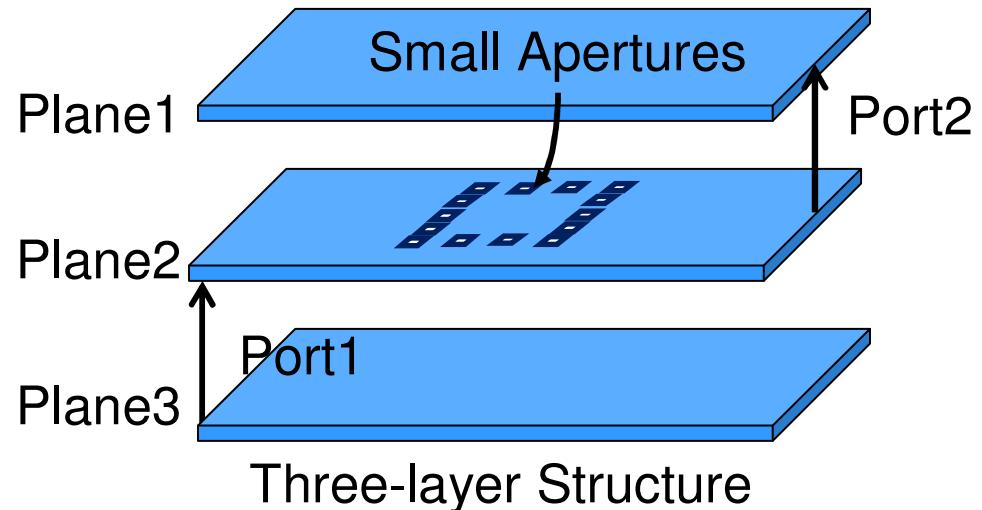
- To generate a mesh, collect all the geometries on one plane.
- Generate a mesh on the plane.
- Classify sub-domains for solid planes and apertures.



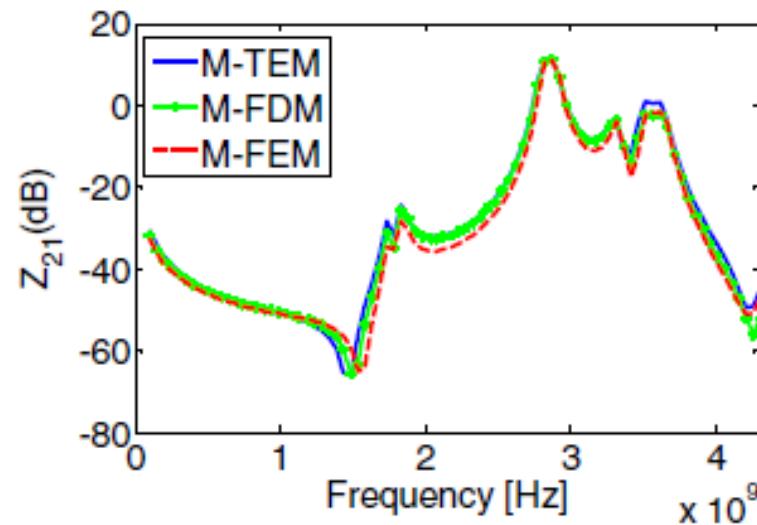
Sub-domain Assignments



Triangulation and Dual graph



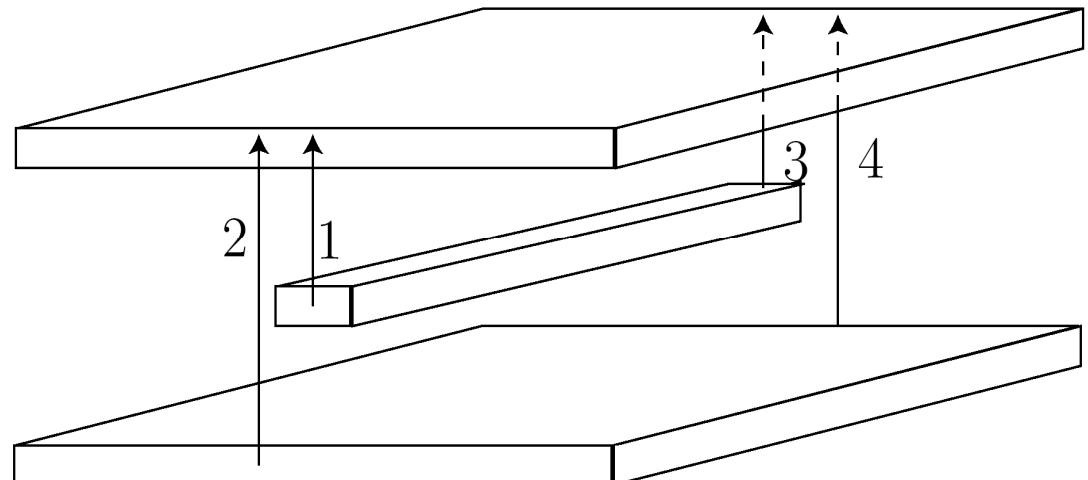
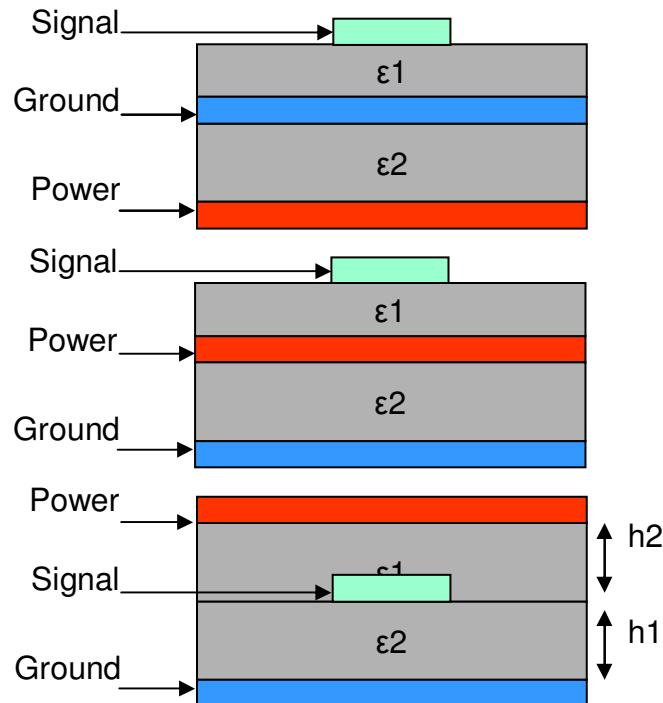
Three-layer Structure



J. Choi and M. Swaminathan, "Modeling Methods for Power/Ground Plane Structures in Electronic Packages", ICEAA, Torino, Italy, Sep 2011

# Coupling to Signal lines

- Based on Modal Decomposition
- Preserves sparse matrix
- Model return currents and coupling



M. Swaminathan and E. Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", Prentice Hall, 2007

# Absorbing Boundary Condition

Apply 1<sup>st</sup> order ABC to boundary cells (node  $i$  and  $b$ ):

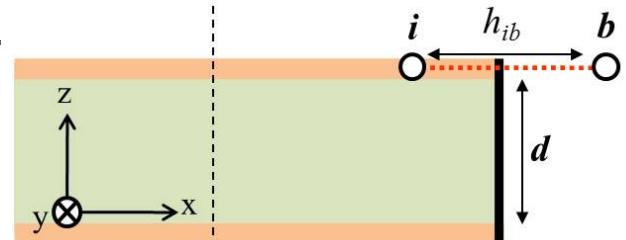
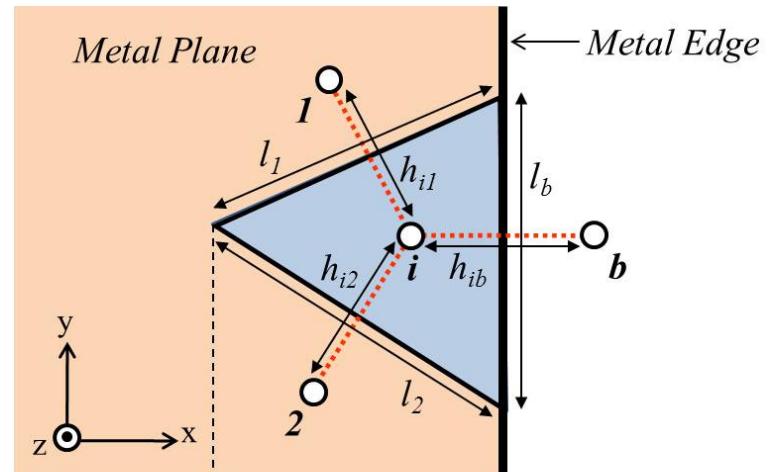
$$\frac{V_i - V_b}{h_{ib}} \rightarrow jkV_i$$


MTEM equation

$$j\omega\epsilon \frac{V_i}{d} A_i + \frac{1}{j\omega\mu d} \sum_{k=1}^2 \left\{ (V_i - V_k) \frac{l_k}{h_{ik}} \right\} + \frac{1}{j\omega\mu d} (V_i - V_b) \frac{l_i}{h_{ib}} = 0.$$

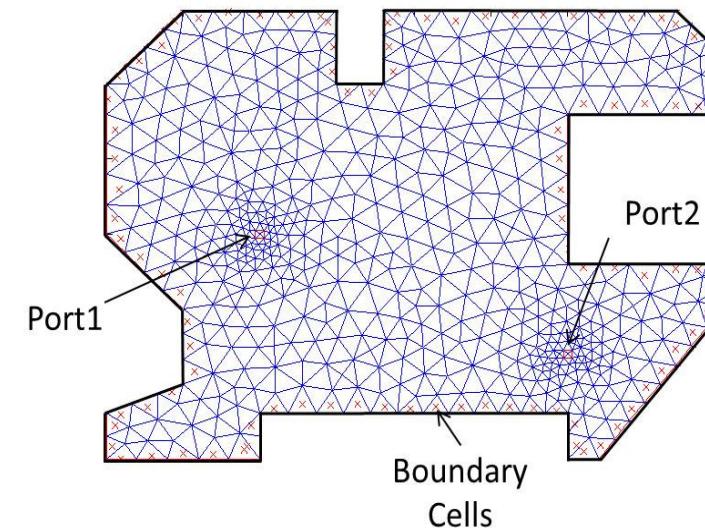
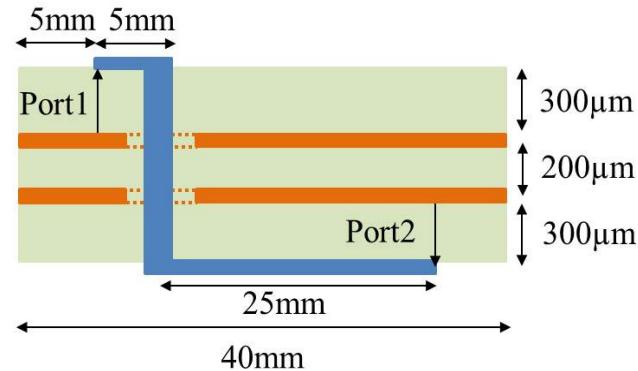
$$(j\omega C_i + G_i)V_i + \frac{V_i - V_1}{j\omega L_{i1}} + \frac{V_i - V_2}{j\omega L_{i2}} = 0.$$

$$G_i = \frac{k l_b}{\omega \mu d} = \frac{l_b}{d} \sqrt{\frac{\epsilon}{\mu}}.$$

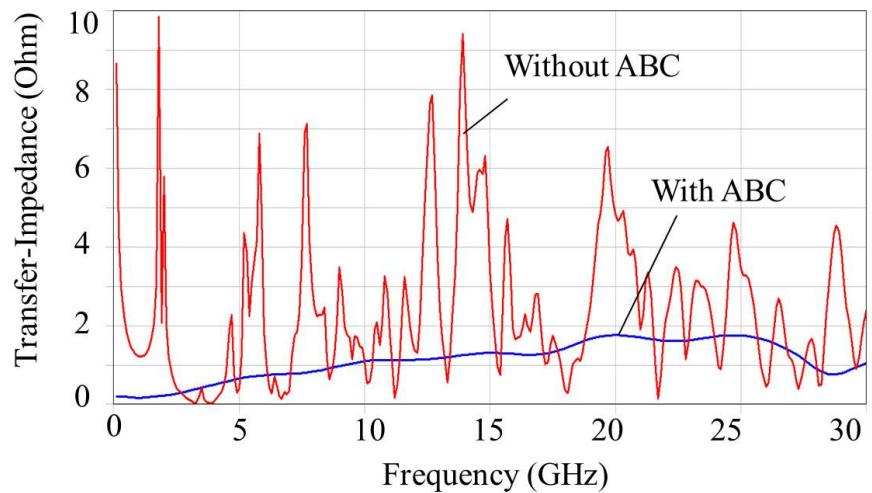
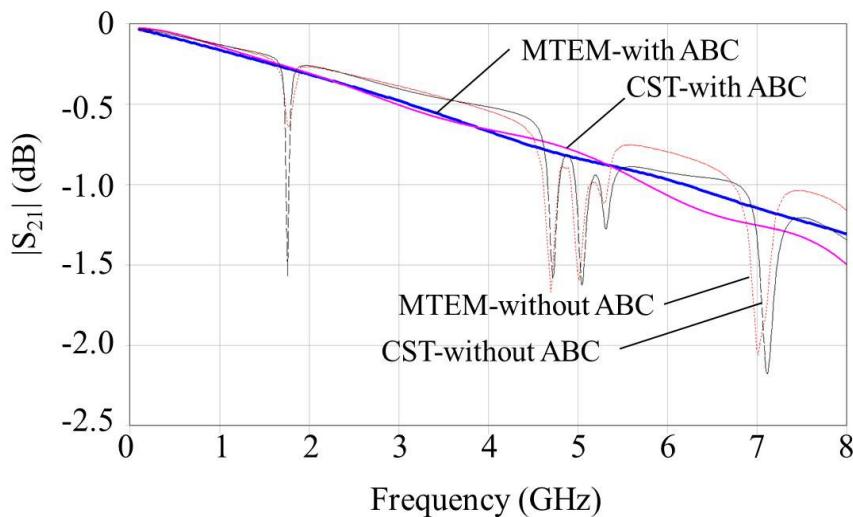


Top and cross-sectional views of a plane-pair at the boundary

# Why Absorbing Boundary Condition ?

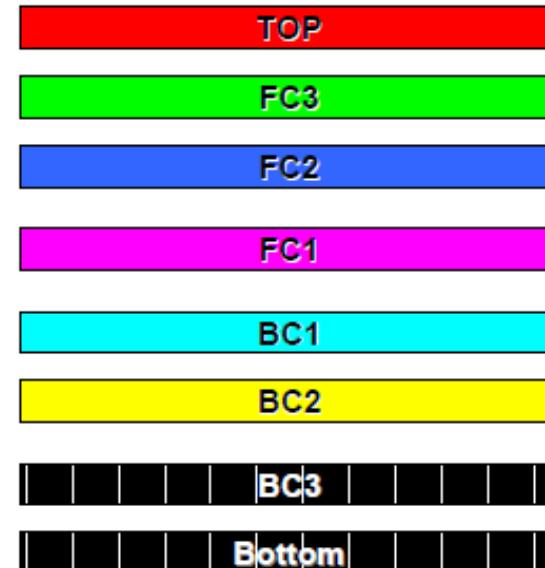
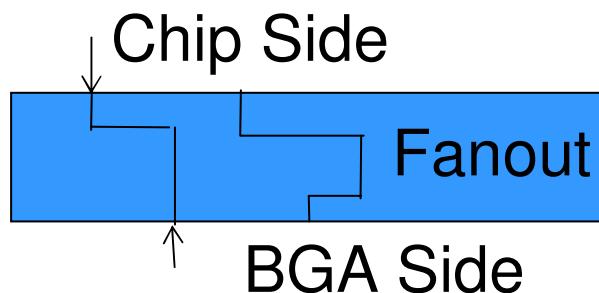
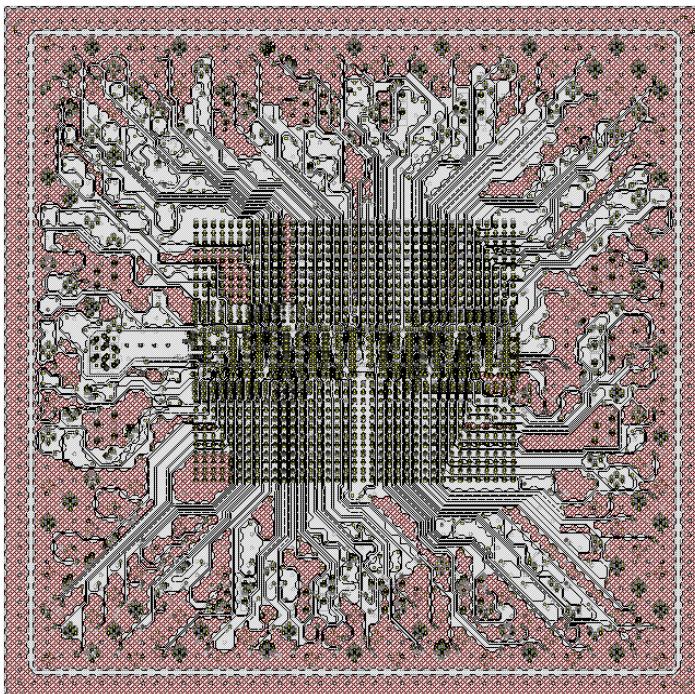


Dielectric Thickness= 200 $\mu$ m  $\epsilon_r=4.5$   $\tan\delta=0.02$



- Provides insight into the impact of resonances on Signal or Power Integrity

# Complex Example: IBM Eight Layer Flip Chip Package



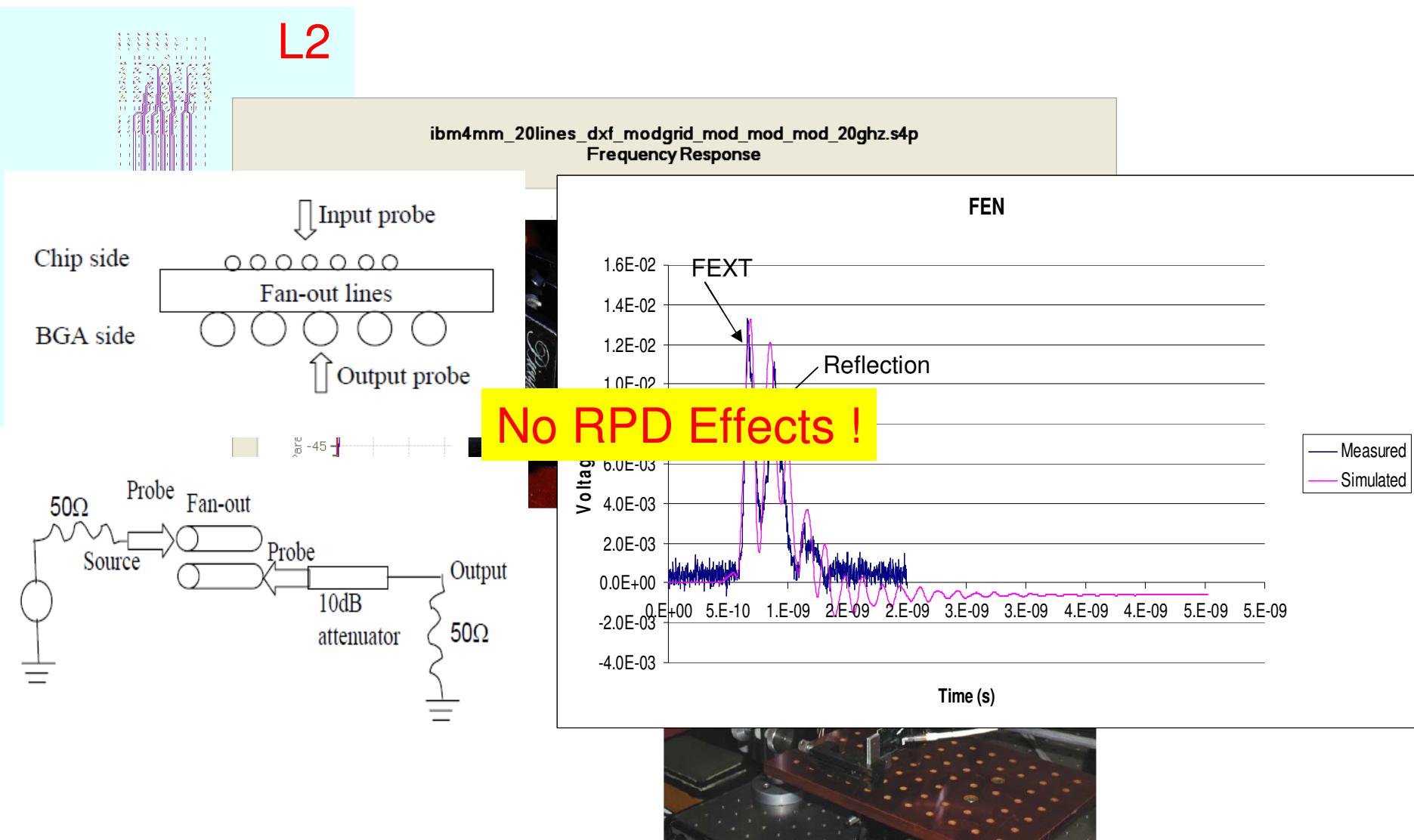
## Metal Layer Stack

- Top
- FC3 (fanout layer)
- FC2
- FC1
- BC1
- BC2
- BC3
- Bottom

- Identify RPD effects using EM Tools
- Understand effect of RPD on Insertion Loss and Coupling

Courtesy: IBM and E-System Design ([www.e-systemdesign.com](http://www.e-systemdesign.com))

# Response of Two Good Nets – Near Field Coupling

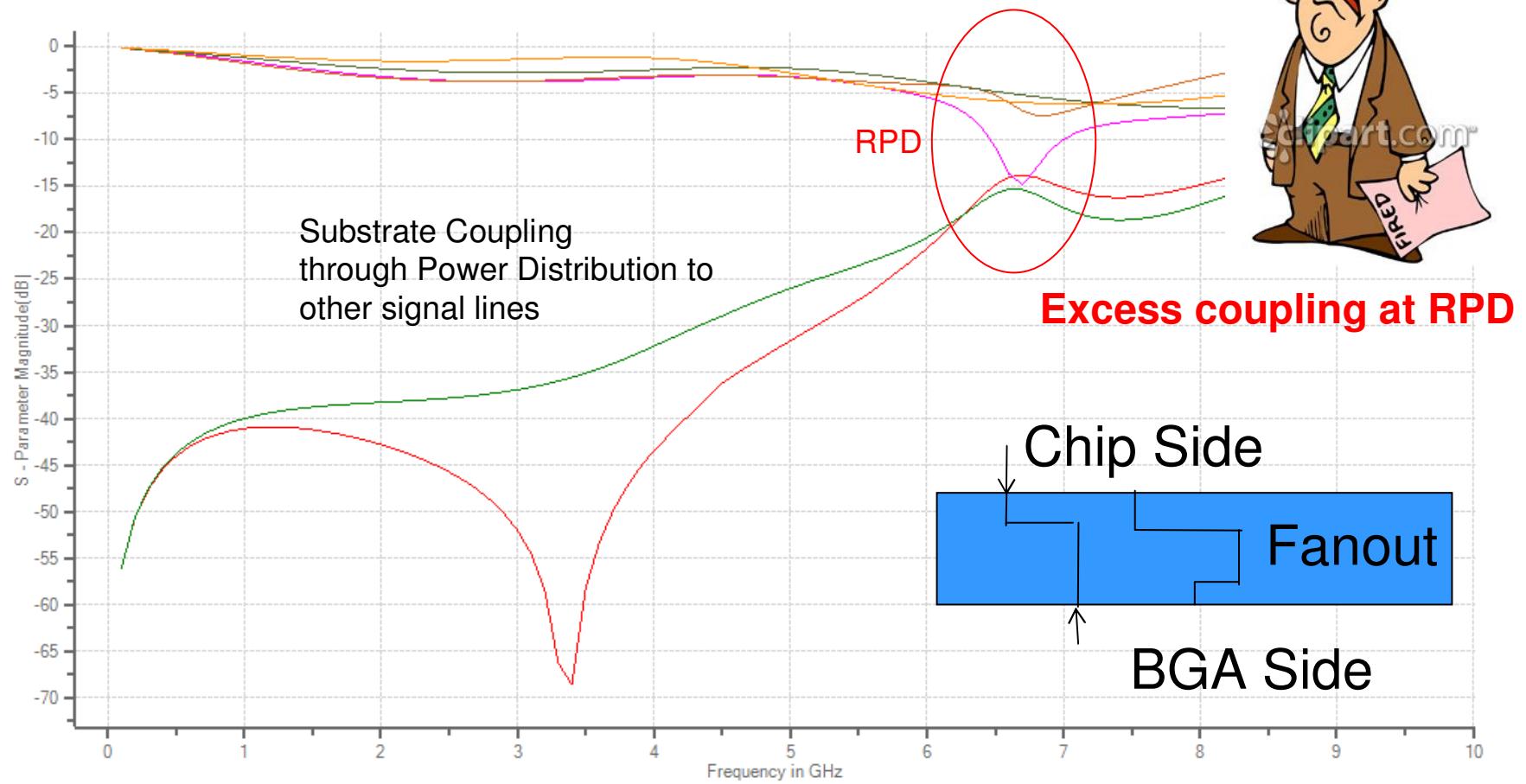


Courtesy: Alina Deutsch and Jason Morse, IBM Yorktown Heights and E-System Design ([www.e-systemdesign.com](http://www.e-systemdesign.com))

# Response of Two Nets Far Apart – Substrate Coupling

What to do ?

ibm-dxf\_file2\_dxf\_2\_mod.s8p and ibm-dxf\_file2\_dxf\_2.s8p  
Frequency Response



- Large increase in Insertion Loss due to RPD
- Large increase in coupling due to RPD

# Low, Lower and Lowest Impedance Power Distribution The Competition is ON!

Achieve a low-impedance path from the power supply to the die

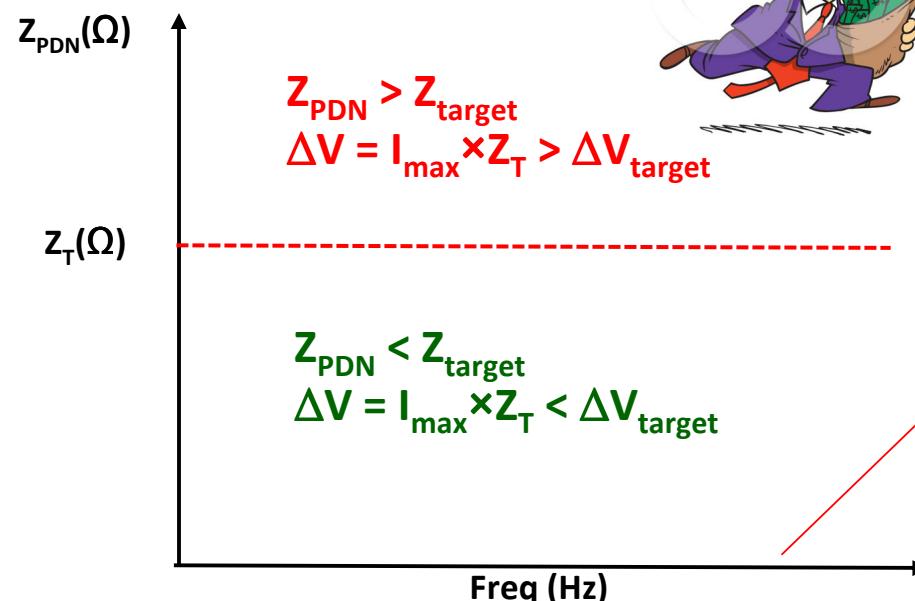
$$I_{\text{avg}} = \frac{P_{\text{avg}}}{V_{\text{DD}}}$$
$$Z_{\text{target}} = \frac{V_{\text{ripple}}}{I_{\text{avg}}}$$



$$Z_{\text{PDN}} < Z_{\text{target}}$$

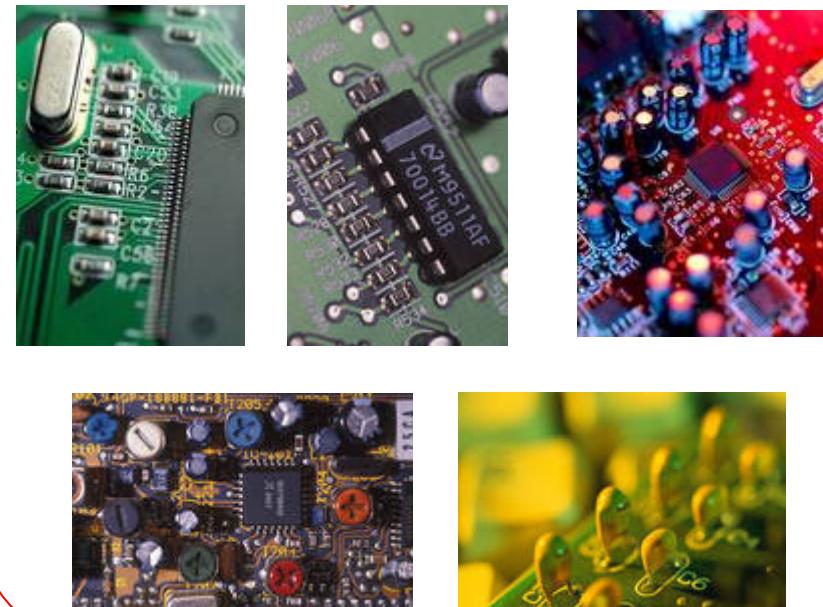


$$\Delta V (\text{noise voltage}) < \Delta V_{\text{target}}$$

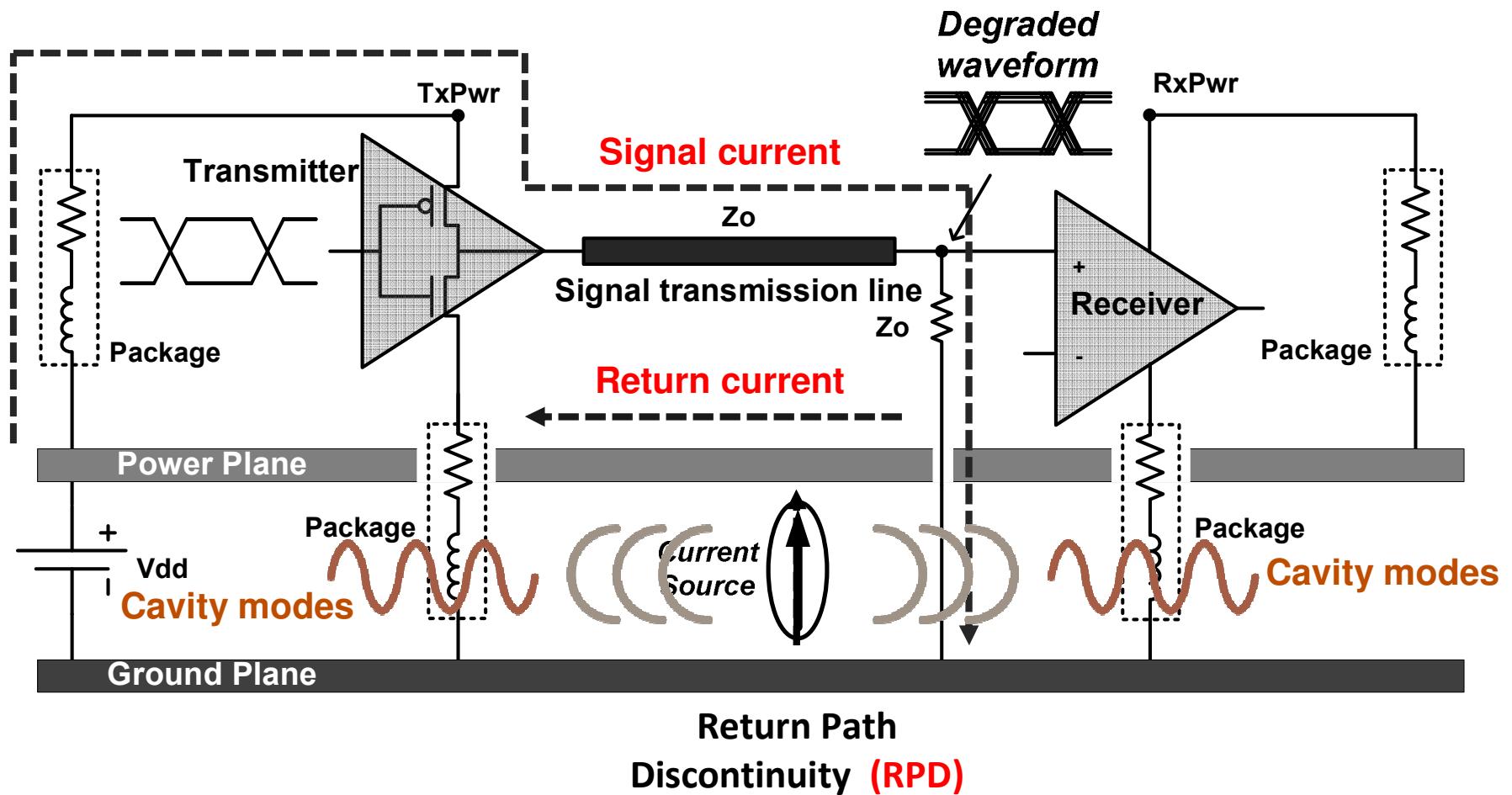


© Ron Leishman - www.CartoonStock.com/439968

## Capacitors

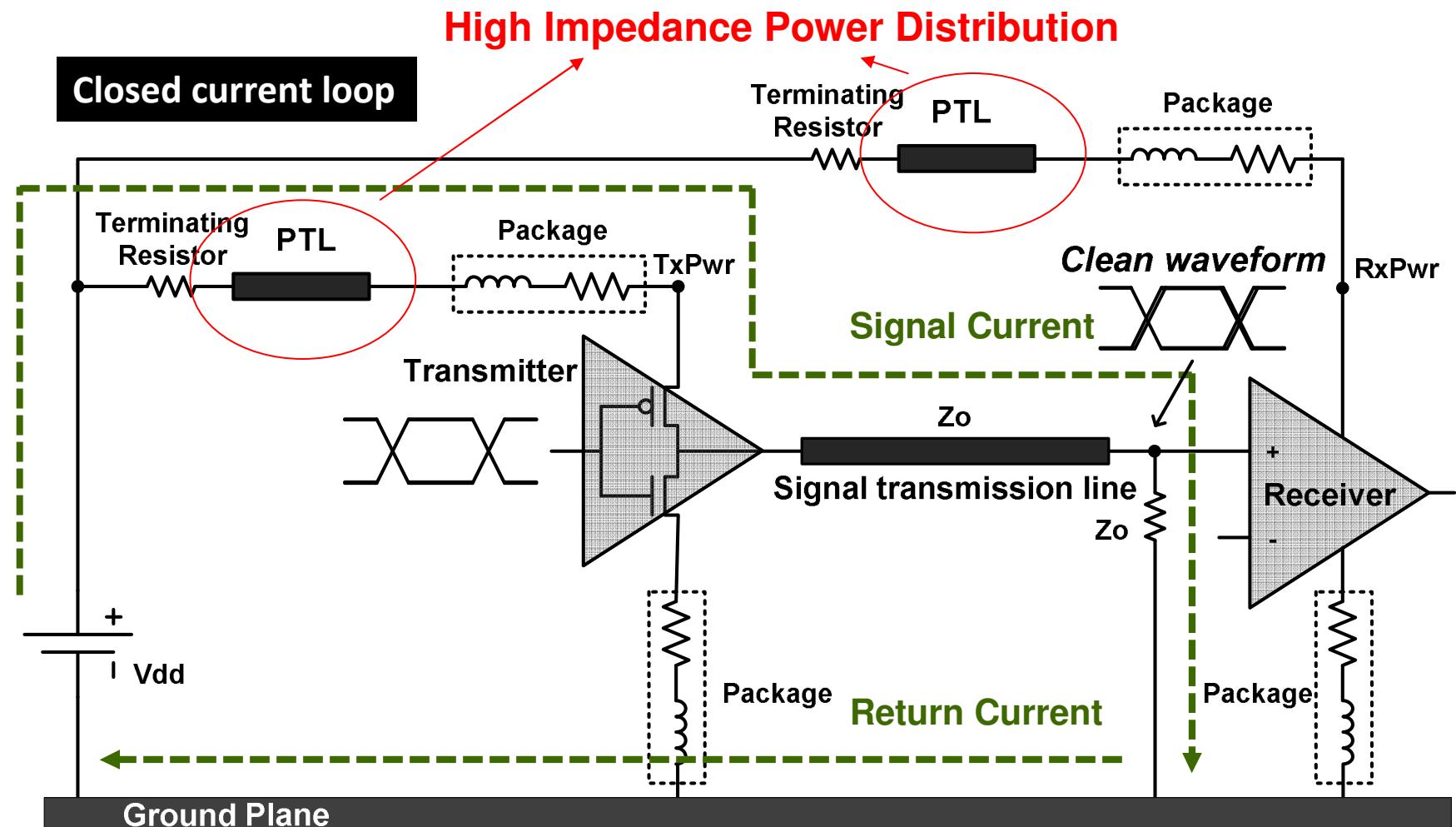


# Let's Revisit our Current Strategy for I/O Power Distribution



Maybe new methods for Power Distribution Design are required in the future – An Opportunity to Innovate !

# Power Transmission Line - Can this be the Game Changer ?

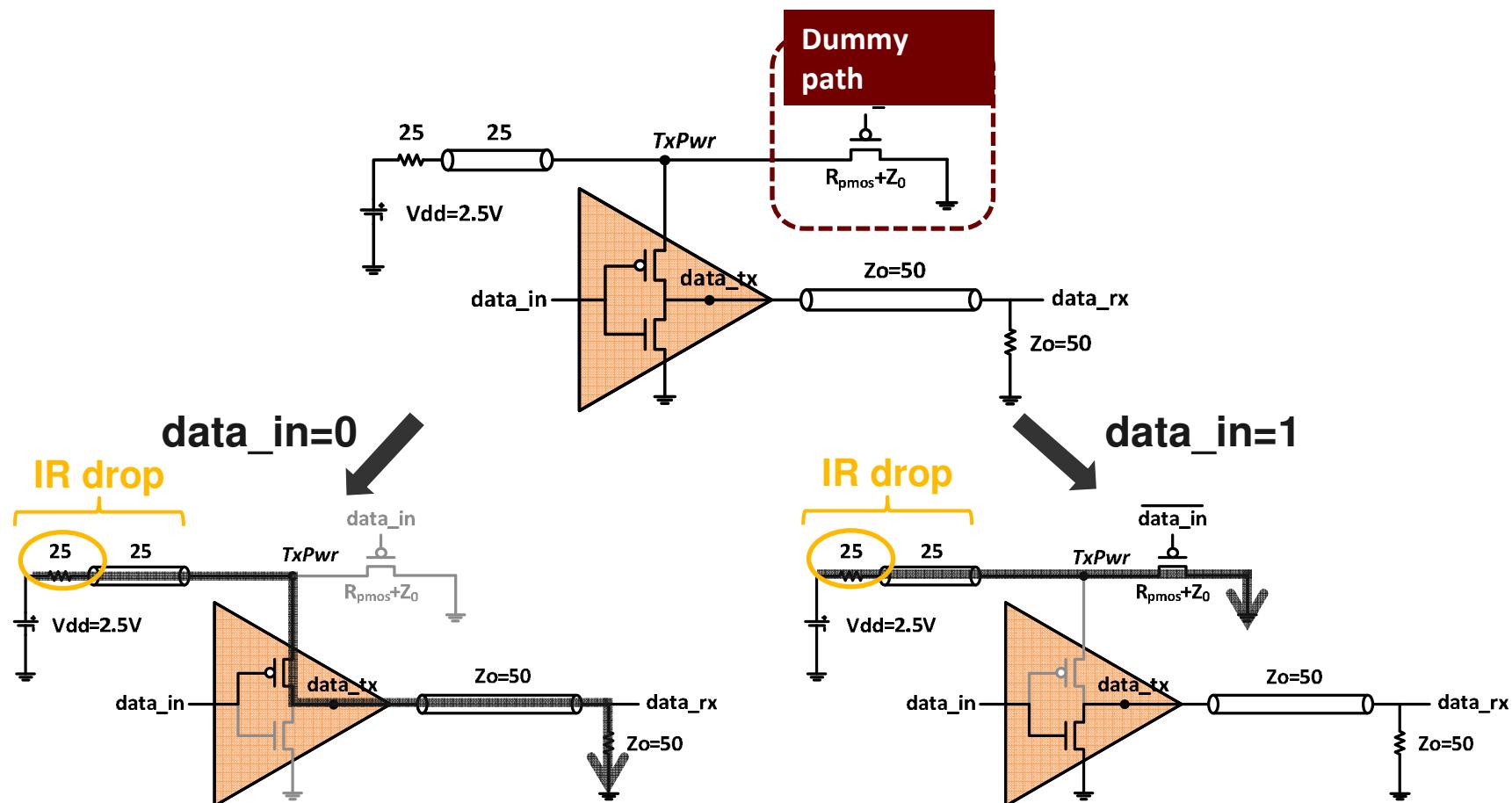


- No Power Planes
- No Return Path Discontinuities
- High Impedance Power Distribution
- Fewer Capacitors

A. E. Engin and M. Swaminathan, "Power Transmission Lines: A New Interconnect Design to Eliminate Simultaneous Switching Noise," in Proc. ECTC, pp. 1139-1143, 2008

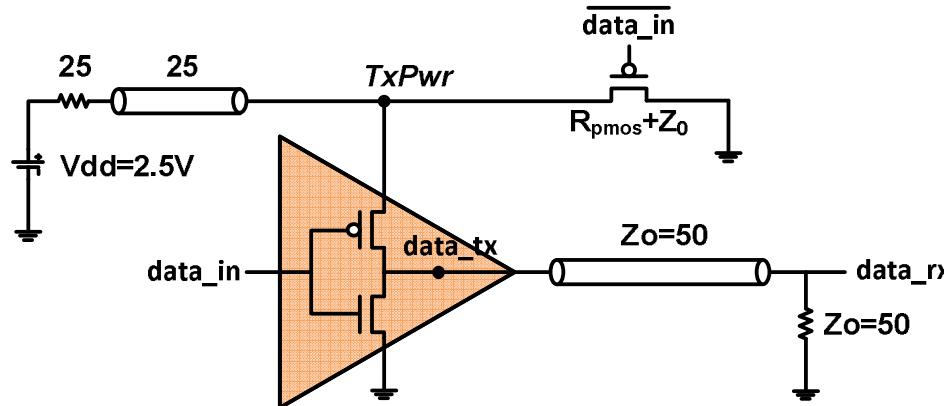
# Can we Eliminate Power Supply Noise as well ?

## Constant Current Power Transmission Line (CCPTL)

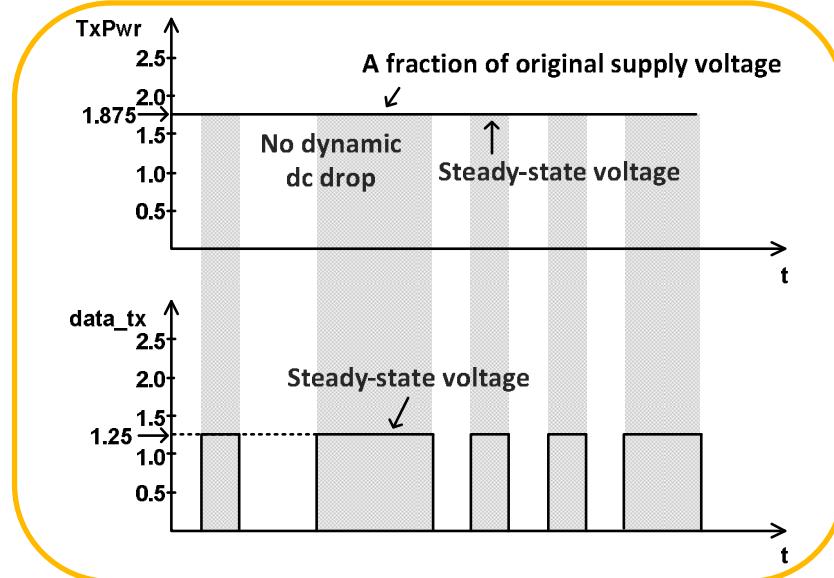


S. Huh, M. Swaminathan, and D. Keezer, "Constant Current Power Transmission Line based Power Delivery Network for Single-Ended Signaling," IEEE Transactions on Electromagnetic Compatibility, 2011

# Does CCPTL Work ? – Atleast Theoretically



Constant current through PTL



Constant IR drop over PTL

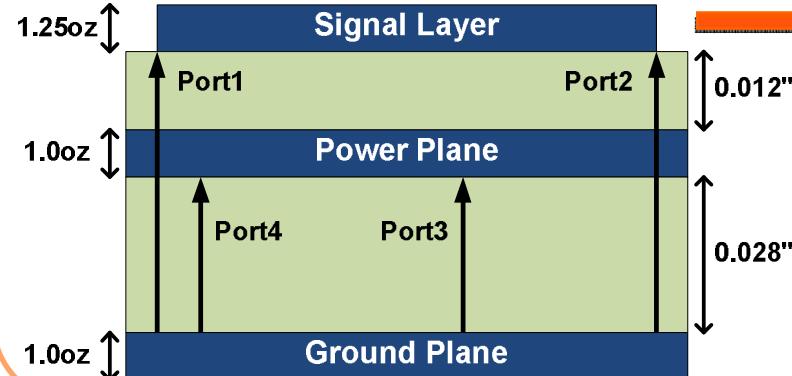
Continuously charged PTL

Constant voltage at TxPwr node

No mismatch effect

# Does CCPTL Work only in theory ? A Simple Test Vehicle to Illustrate the Concept

Power-plane-based test vehicle



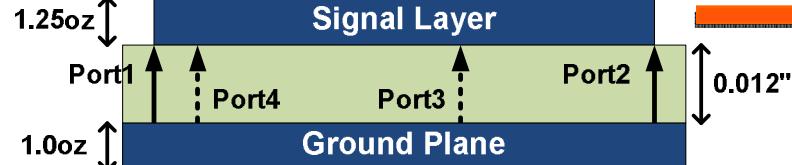
Via to ground plane

Via to power plane

2.6"-long

Dummy path

PTL-based test vehicle



Via to ground plane

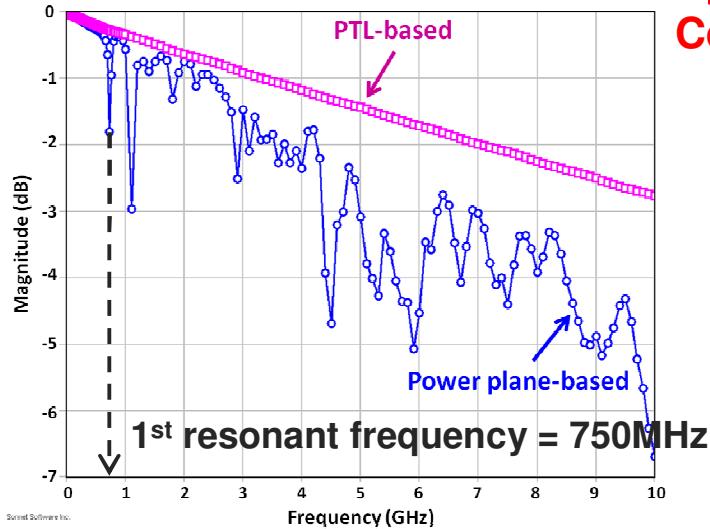
Power transmission line

2.6"-long

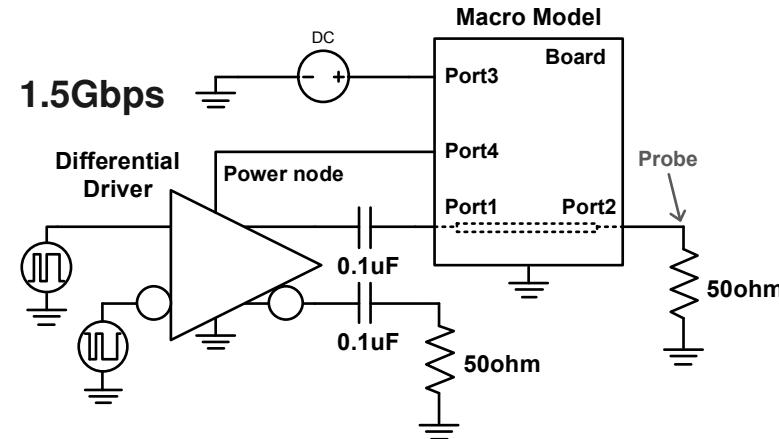
Dummy path

# Modeling and Simulation

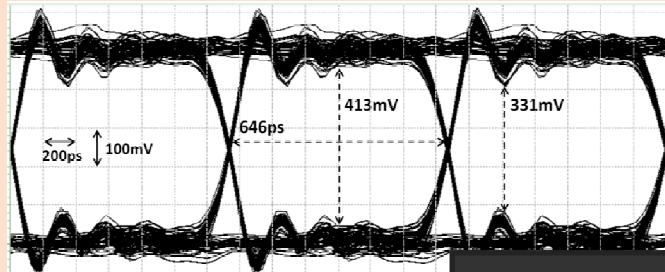
## Modeling in frequency domain



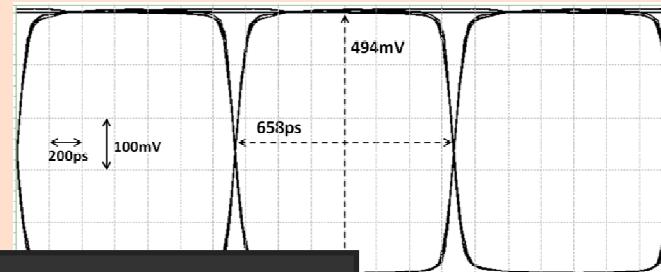
Converted to Macromodel



## Power-plane-based TV



## PTL-based TV

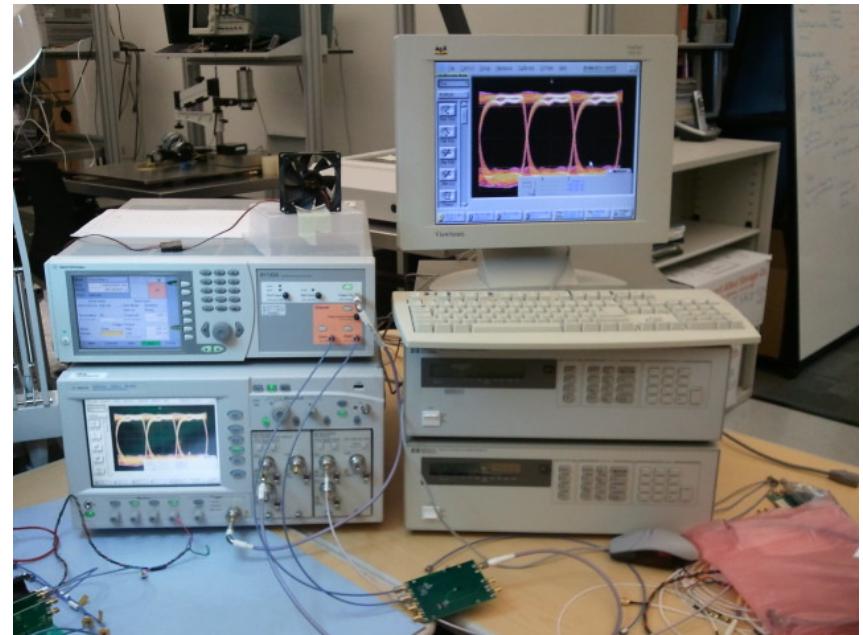
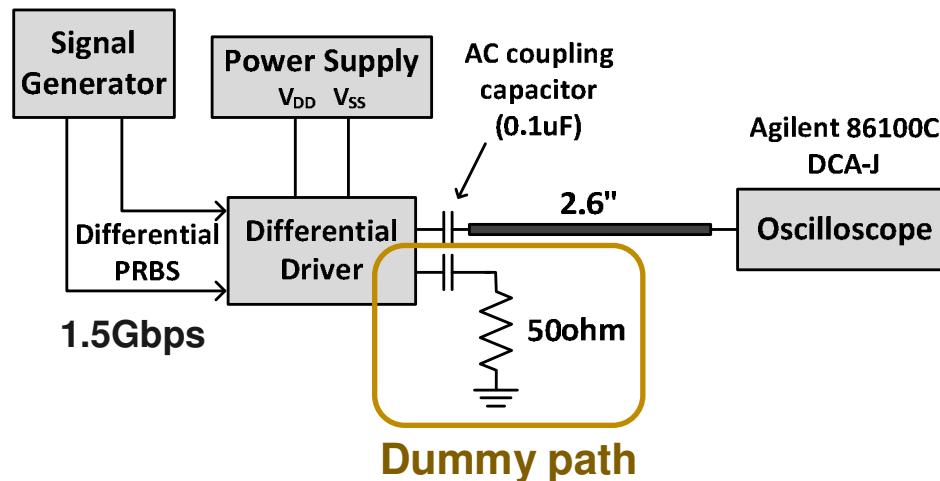


Eye height improves by 19.6%  
Jitter improves by 58%

# Measurement Setup

## Measurement setup

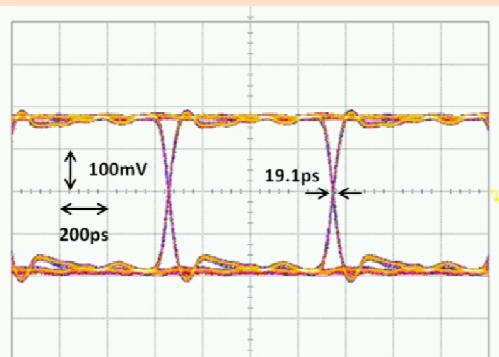
Agilent 81133A



- Dummy path is implemented outside the off-the-shelf chip.
- AC coupling capacitor is used
  - to suppress the DC current flow.
  - to provide bias for the oscilloscope.
- Supply voltage of 3.47V was used for the PTL-based TV, while 2.5V was used for the plane-based TV.

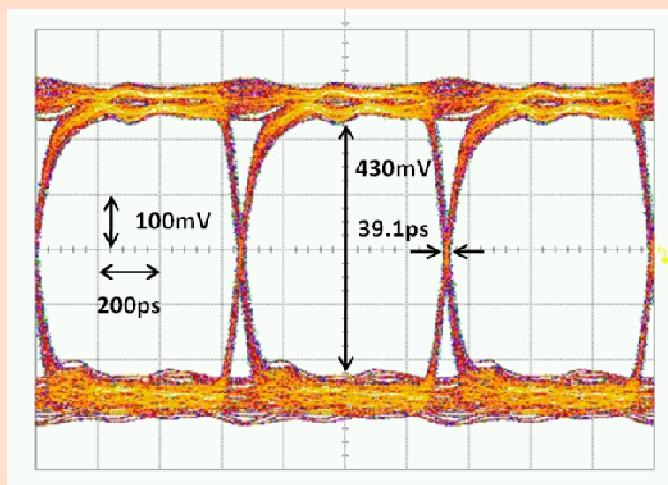
# Measurement Results

Signal generator output

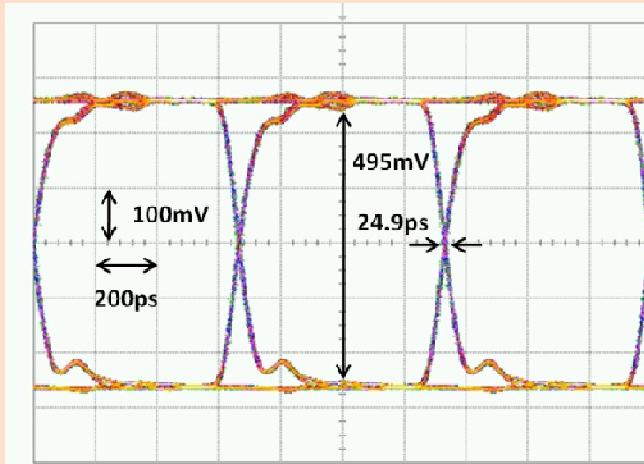


	Eye height	P-P jitter
Power plane	430mV	39.1ps
CCPTL	495mV	24.9ps
Improvement	15.1%	36.3%

Plane-based TV



CCPTL-based TV



# What about Power ?

## Static power consumption

PDN type	Eye height	4 bit					Expectation of Power	Power penalty
		HHHH	HHHL	HHLL	HLLL	LLLL		
Power Plane	$V_{DD}/2$	4	3	2	1	0	2	-
CCPTL	$V_{DD}/2$	4	4	4	4	4	4	100%
PBPTL	$V_{DD}/2$	3	3	3	3	3	3	50%
Probability		0.0625	0.25	0.375	0.25	0.0625		

\*Assumption: Four bits provide 16 data patterns, each of which has an equal probability.

When one output buffer draws current from the power supply, power of 1 is consumed.

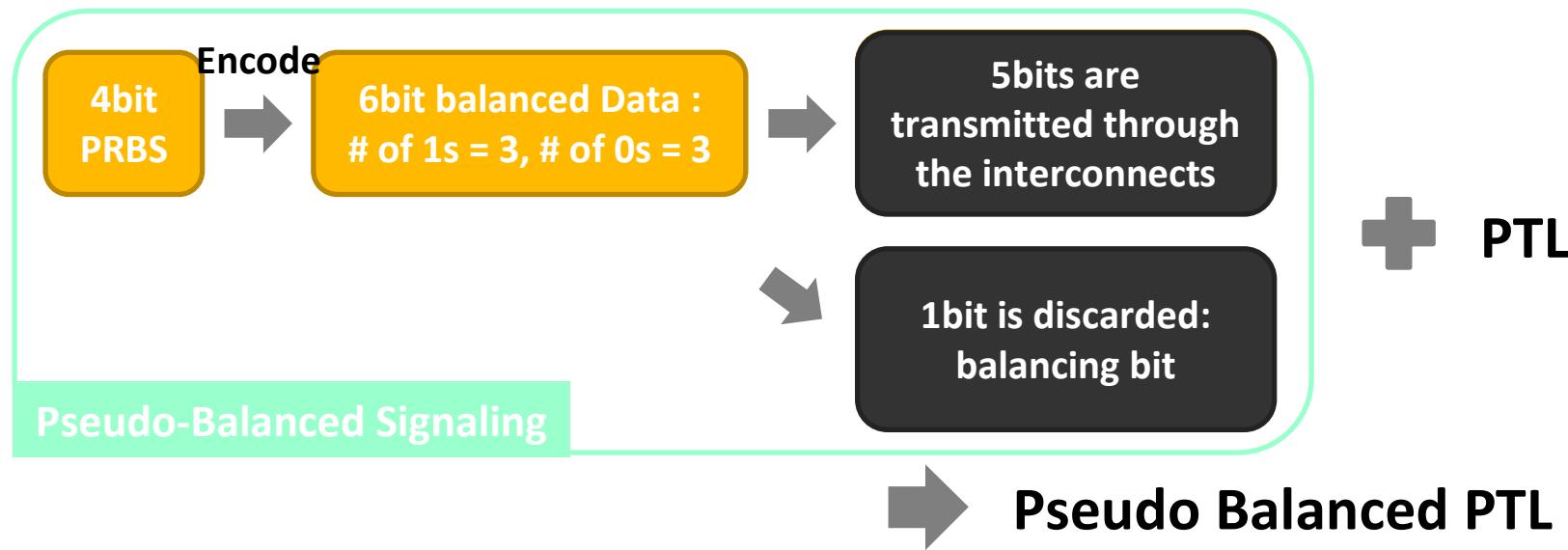
For the PBPTL scheme, 4b/6b encoder is used to generate the balanced data with three 1's and three 0's.

The same amount of dynamic power is consumed regardless of the PDN type.

N	Plane	CCPTL	PBPTL	M
1 bit	$P_1$	$2 \cdot P_1$	-	2 bit
2 bit	$P_2$	$2 \cdot P_2$	$2 \cdot P_2$	4 bit
4 bit	$P_4$	$2 \cdot P_4$	$1.5 \cdot P_4$	6 bit
5 bit	$P_5$	$2 \cdot P_5$	$1.4 \cdot P_5$	7 bit

- The power consumption doubles when using the CCPTL regardless of the bit number.
- The overhead decreases with the increase of bit number when using the PBPTL scheme.

# Pseudo Balanced Power Transmission Line (PBPTL)



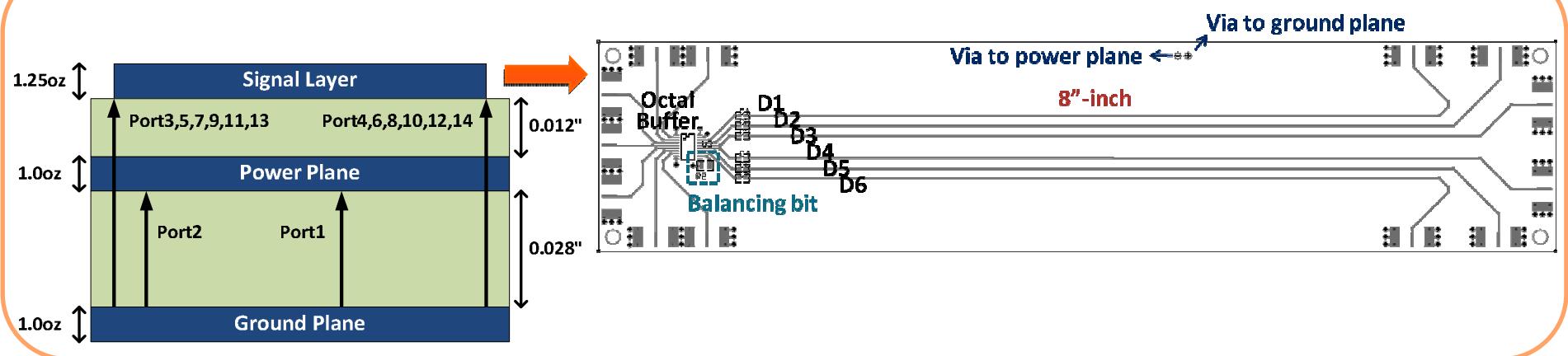
- Expected Advantages
  - The coupling between the PDN and signal network is removed.
  - The current through the PTL is constant at all times.
    - The dynamic dc drop is removed.
    - The PTL is kept fully charged.

S. Huh, M. Swaminathan, D. Keezer; "Pseudo-Balanced Signaling Using Power Transmission Line for Parallel Links," in Proc. IEEE EMC, 2011

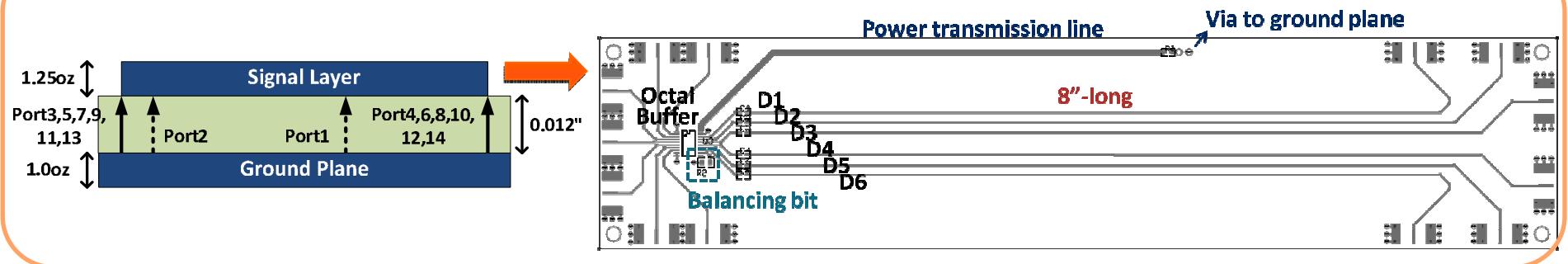
S. Huh, M. Swaminathan, D. Keezer; "Design of Power Delivery Networks using Power Transmission Line for Multiple I/Os using Pseudo-Balanced Signaling," in Proc. IEEE EPEPES, 2011.

# PBPTL Test Vehicle

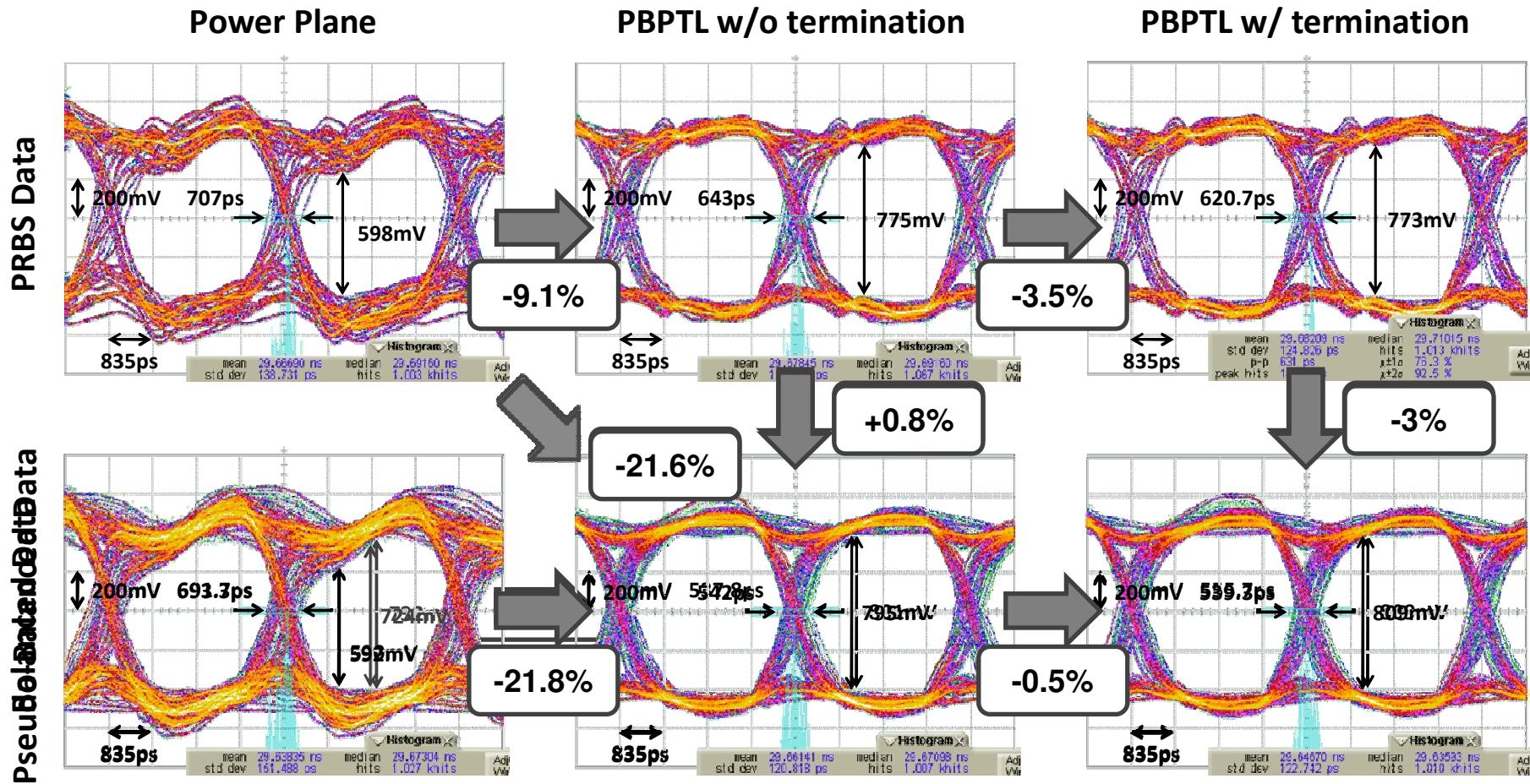
## Power-plane-based test vehicle



## PTL-based test vehicle

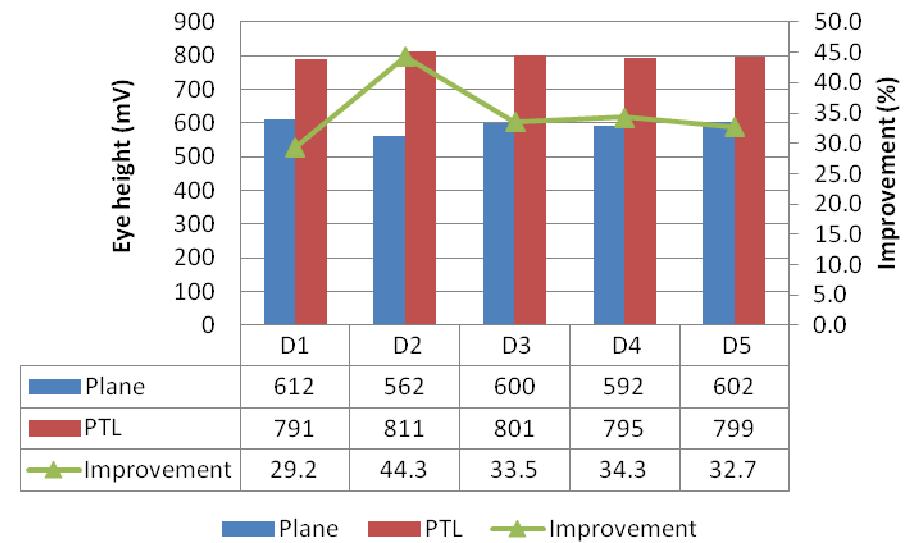
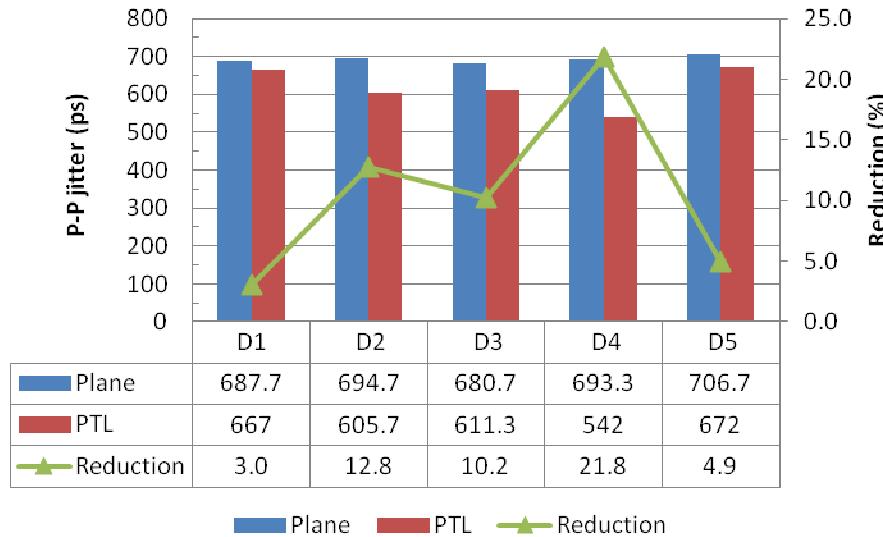


# Measured Eye Diagrams



S. Huh and M. Swaminathan, "Are Power Planes Necessary for High Speed Signaling", Designcon, CA, Jan. 29 – Feb. 2, 2012

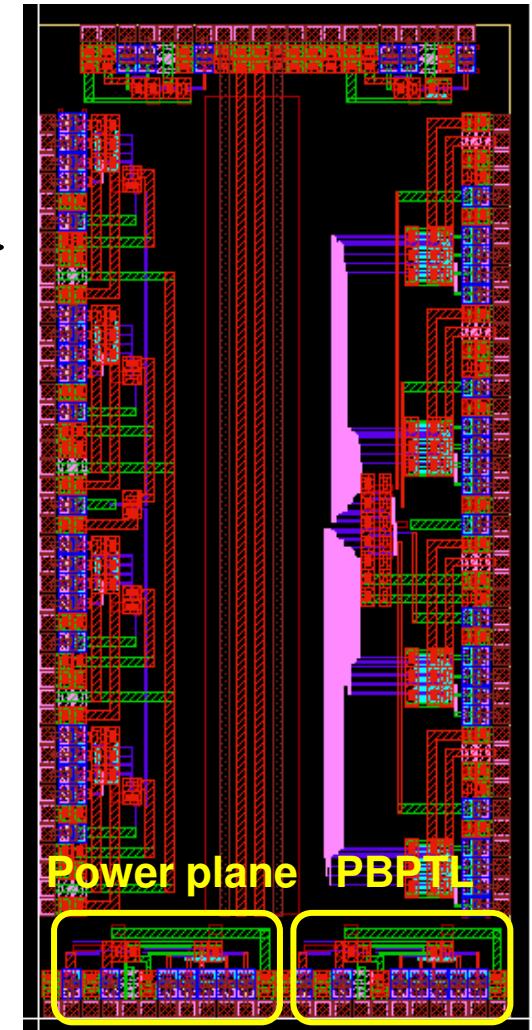
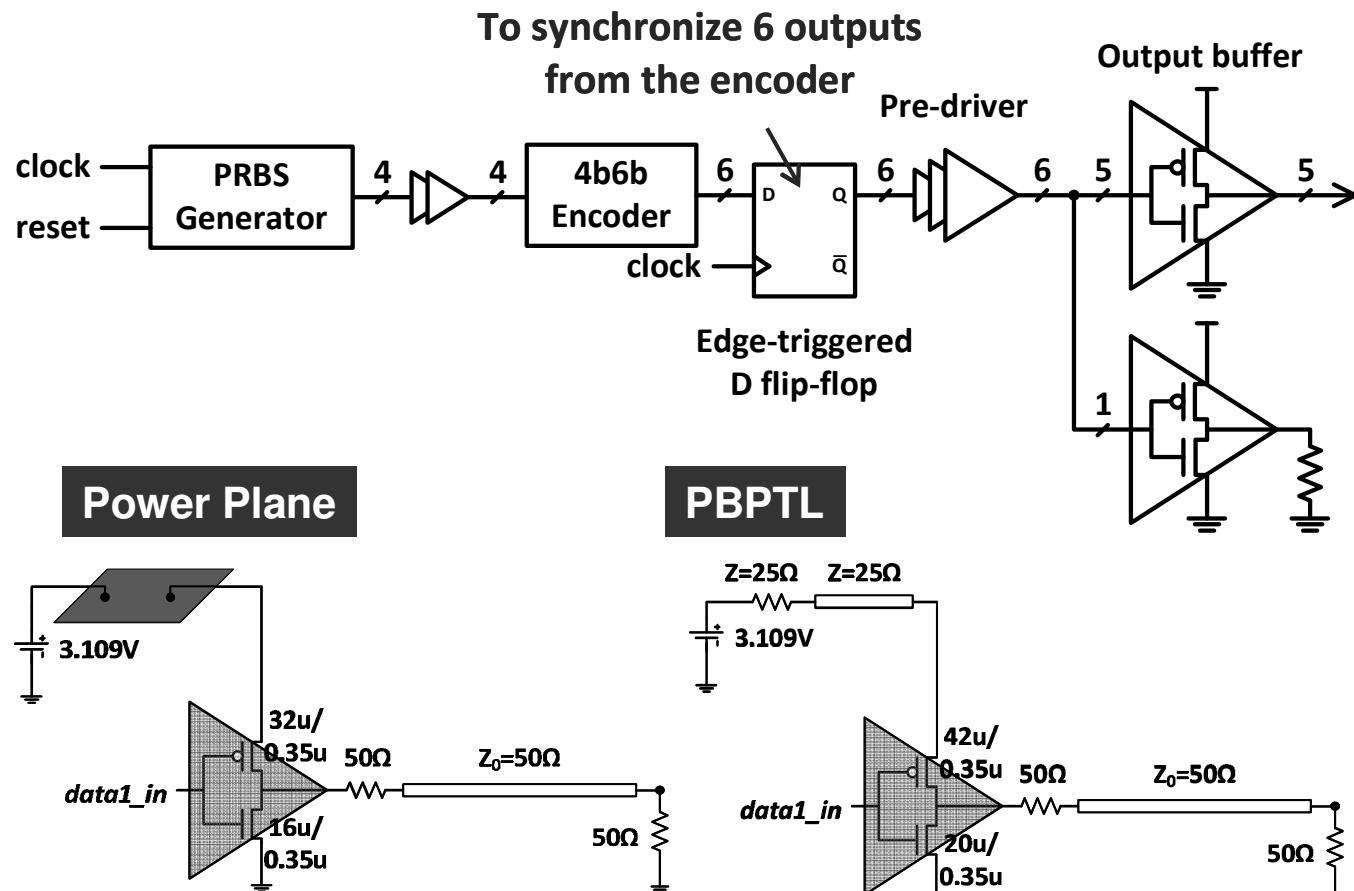
# Measurement Summary



- Based on measurements, using the PBPTL scheme
  - Improves the eye height by 34.8% on average.
  - Reduces p-p jitter by 10.5% on average.

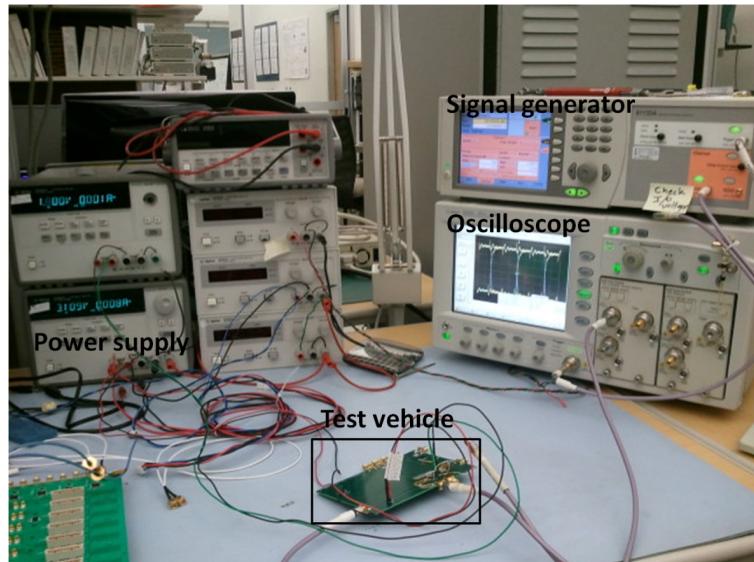
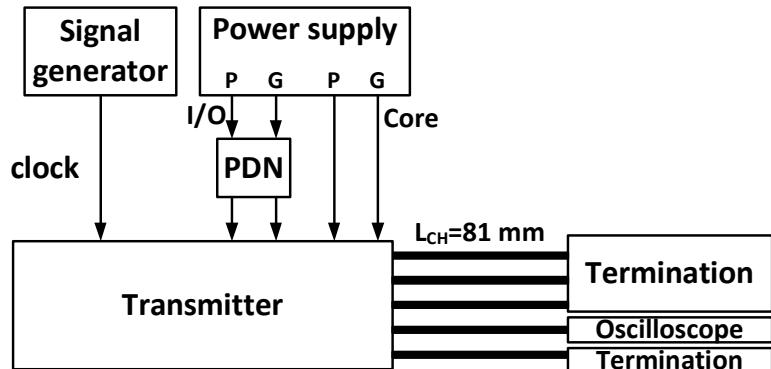
S. Huh and M. Swaminathan, "Are Power Planes Necessary for High Speed Signaling", Designcon, CA, Jan. 29 – Feb. 2, 2012

# PBPTL Implementation Using CMOS 0.18um Process



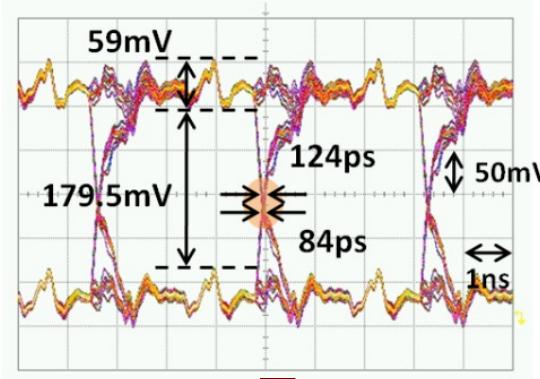
S. Huh and M. Swaminathan, "Are Power Planes Necessary for High Speed Signaling", Designcon, CA, Jan. 29 – Feb. 2, 2012

# Measurement Results

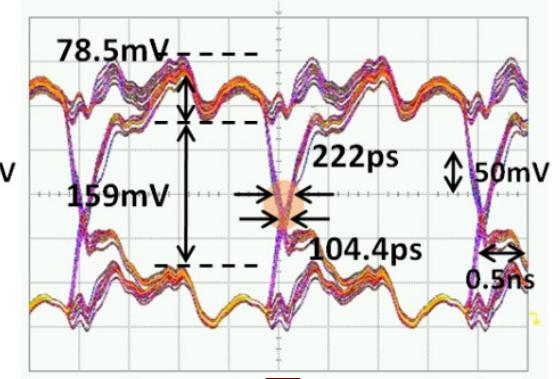


Power Plane  
PBPTL

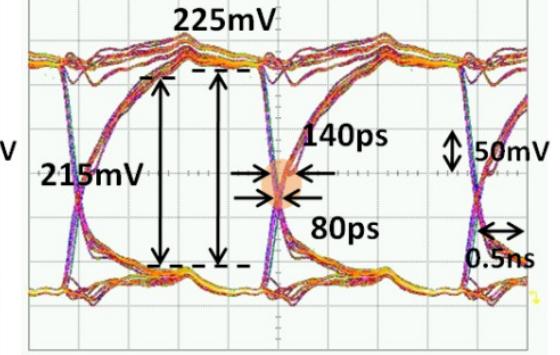
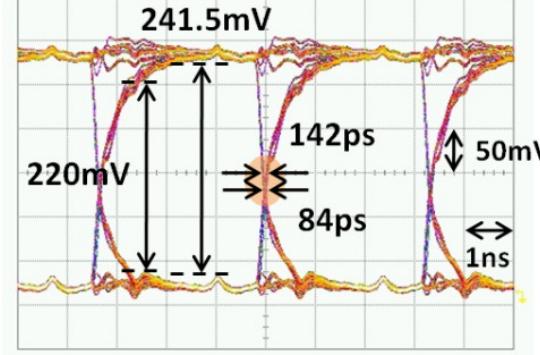
200 Mbps



500 Mbps



Power Plane  
PBPTL



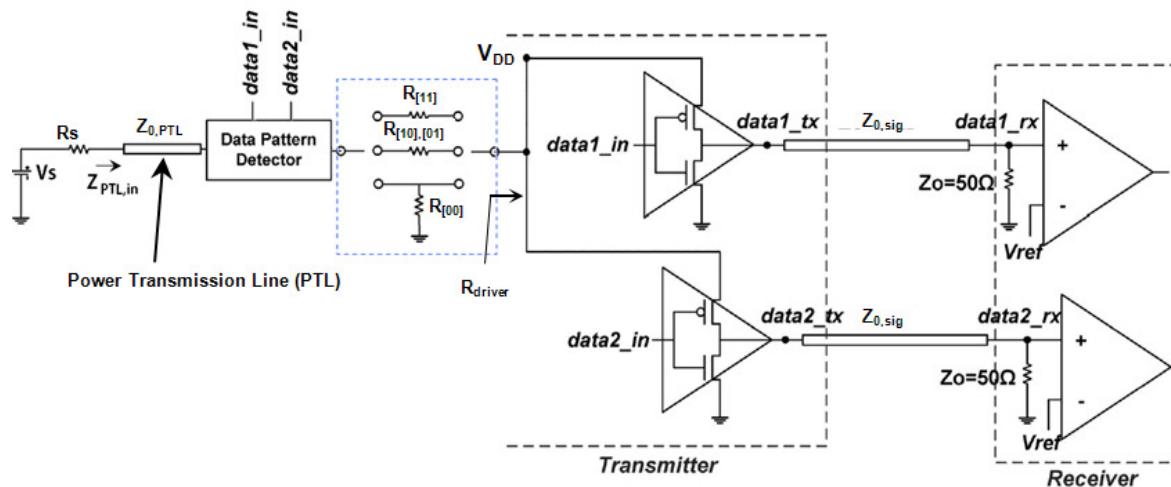
Eye height improvement 35%

Eye height improvement 35%

Jitter improvement 23%

# Constant Voltage Power Transmission Line (CVPTL)

- Depending on the input data, a data pattern detector is used to select a resistor path in the PDN to keep the impedance looking into the input of the PTL ( $Z_{PTL,in}$ ) constant.
- Dynamic resistor path compensates for varying current to keep  $V_{DD}$  constant regardless of data.



Calculate resistor values:

$$R_{driver}[k] = \frac{R_{on} + R_L}{k}$$

$$R_{path}[k] = \frac{1}{V_{dd}} (V_s \cdot R_{driver}[k] - V_{dd} (R_{driver}[k] + R_{sw} + R_s))$$

for  $k = 0, 1, \dots, N-1$

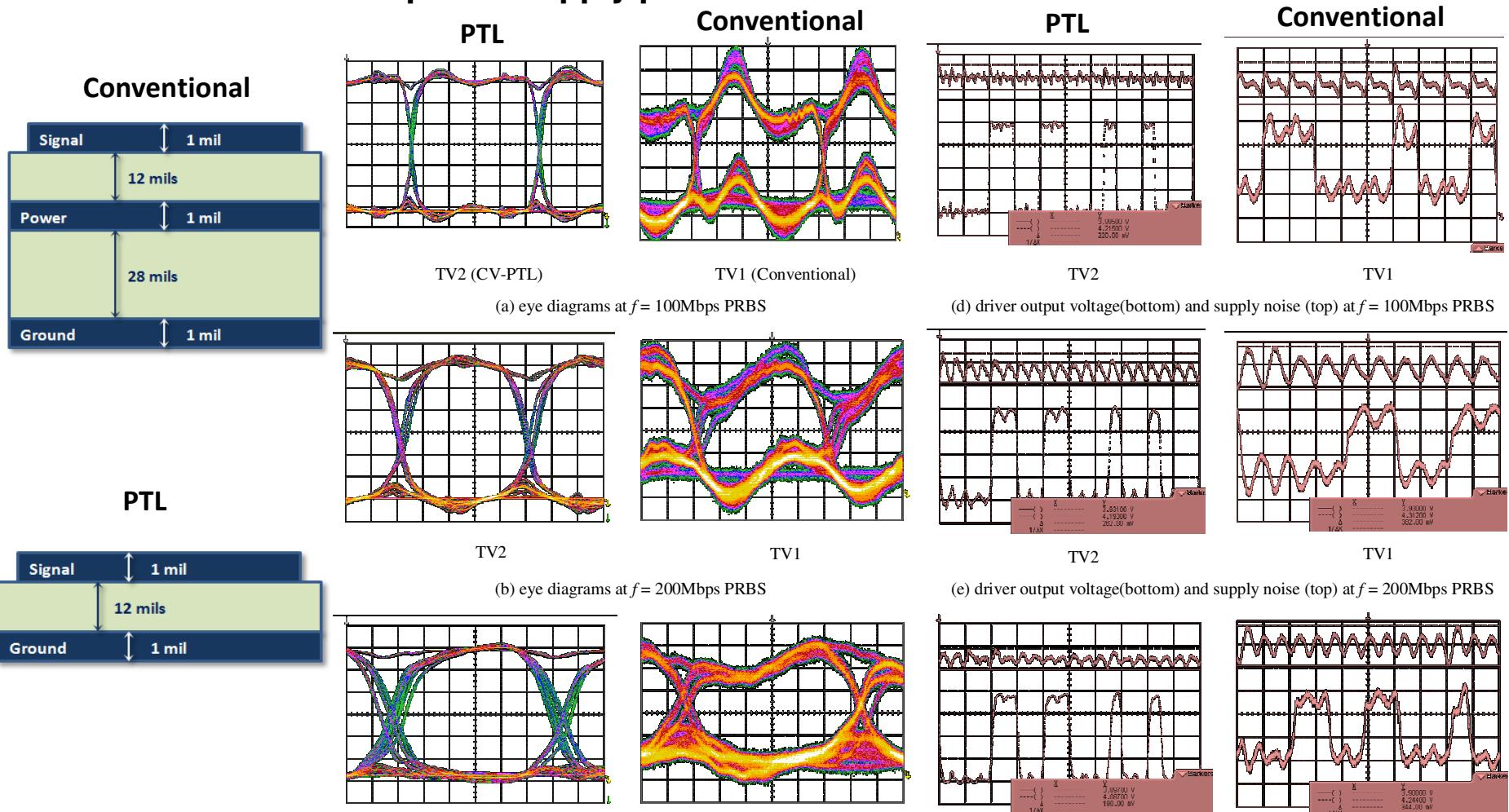
$$R_{path}[N] = \frac{1}{V_{dd} - V_s} (-V_{dd} \cdot (R_s + R_{sw}))$$

[1] Telikepalli, S.; Swaminathan, M.; Keezer, D.; "Minimizing Simultaneous Switching Noise at Reduced Power with Constant Voltage Power Transmission Lines for High-Speed Signaling," International Symposium on Quality Electronic Design (ISQED), 2013

[2] Huh, S.; Chung, D.; Swaminathan, M.; "Near zero SSN power delivery networks using Constant Voltage Power Transmission Lines," Electrical Design of Advanced Packaging & Systems Symposium, 2009. (EDAPS 2009). IEEE , vol., no., pp.1-4, 2-4 Dec. 2009

# Test Vehicle (CVPTL)

- Resistor path is implemented by placing extra drivers in the power supply path.
- Therefore, enabling these extra drivers effectively serves to add a series resistance onto the power supply path.

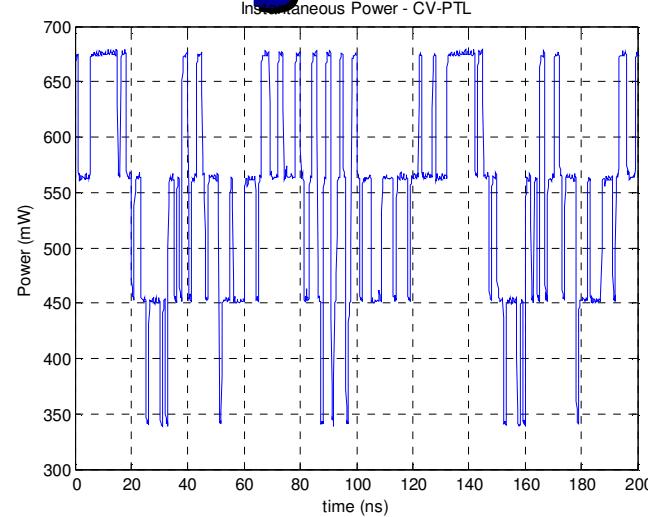


# Power and Energy Savings - CVPTL

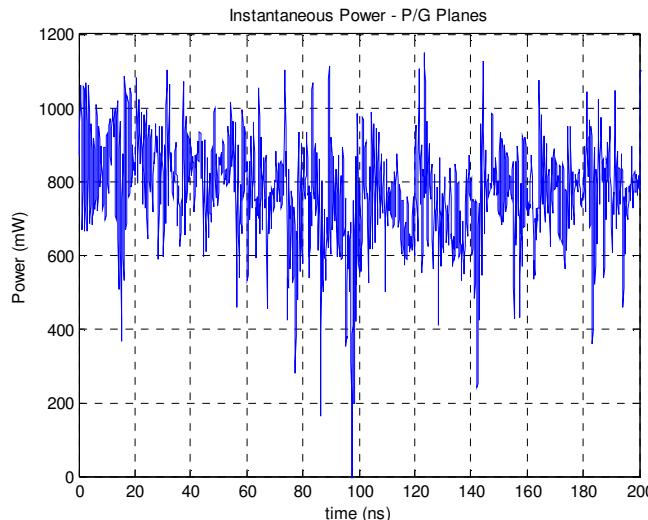
Conventional					CV-PTL						
A	B	C	D	SUM	A	B	C	D	E	F	SUM
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0	0	0	1
0	0	1	1	2	0	0	1	1	0	0	2
0	1	0	0	1	0	1	0	0	0	0	1
0	1	0	1	2	0	1	0	1	0	0	2
0	1	1	0	2	0	1	1	0	0	0	2
0	1	1	1	3	1	0	0	0	1	0	2
1	0	0	0	1	1	0	0	0	0	0	1
1	0	0	1	2	1	0	0	1	0	0	2
1	0	1	0	2	1	0	1	0	0	0	2
1	0	1	1	3	0	1	0	0	1	0	2
1	1	0	0	2	1	1	0	0	0	0	2
1	1	0	1	3	0	0	1	0	1	0	2
1	1	1	0	3	0	0	0	1	1	0	2
1	1	1	1	4	0	0	0	0	1	0	1
Average				2	Average				1.625		

Truth table for signaling schemes

Table III. Power Comparison			
Scheme	Total Energy	Energy/bi t	%Δ of CVPTL
CV-PTL	0.099μJ	8.29nJ	—
Conventional	0.110μJ	9.20nJ	+11.0%



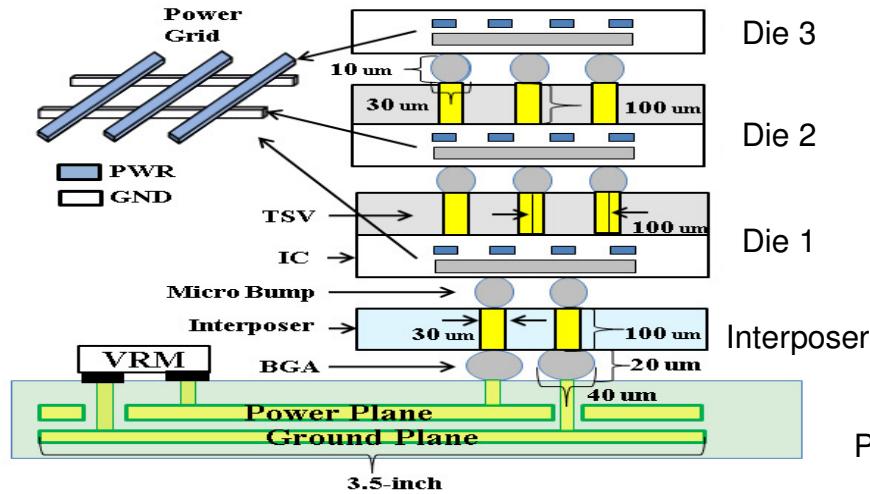
Instantaneous power consumed by the CV-PTL 3D stack (in mW) with 256-bit long PRBS signal at 1 Gbps



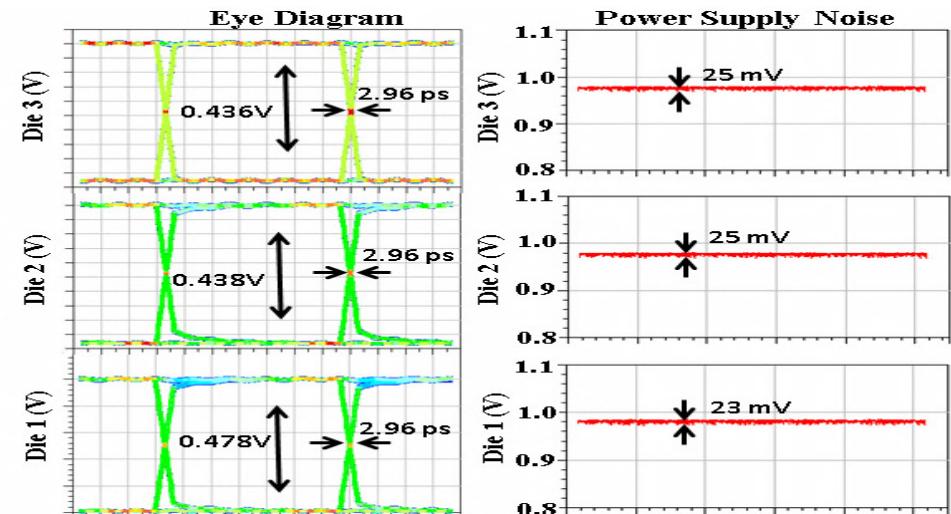
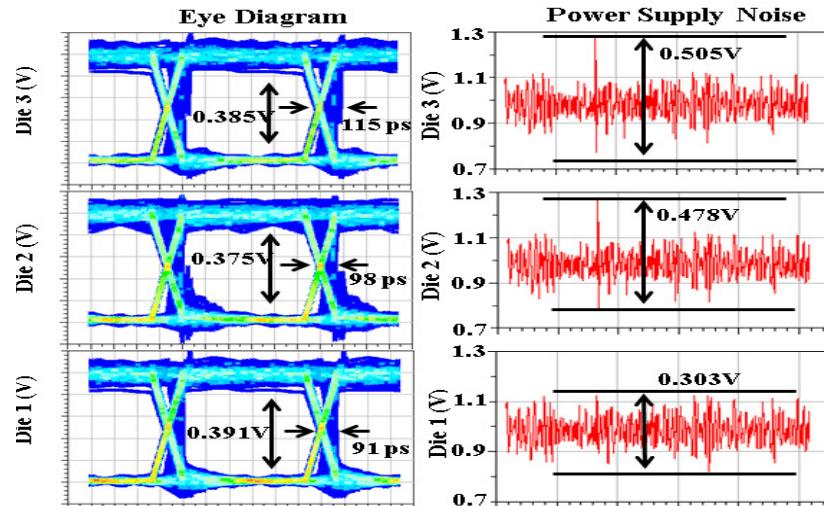
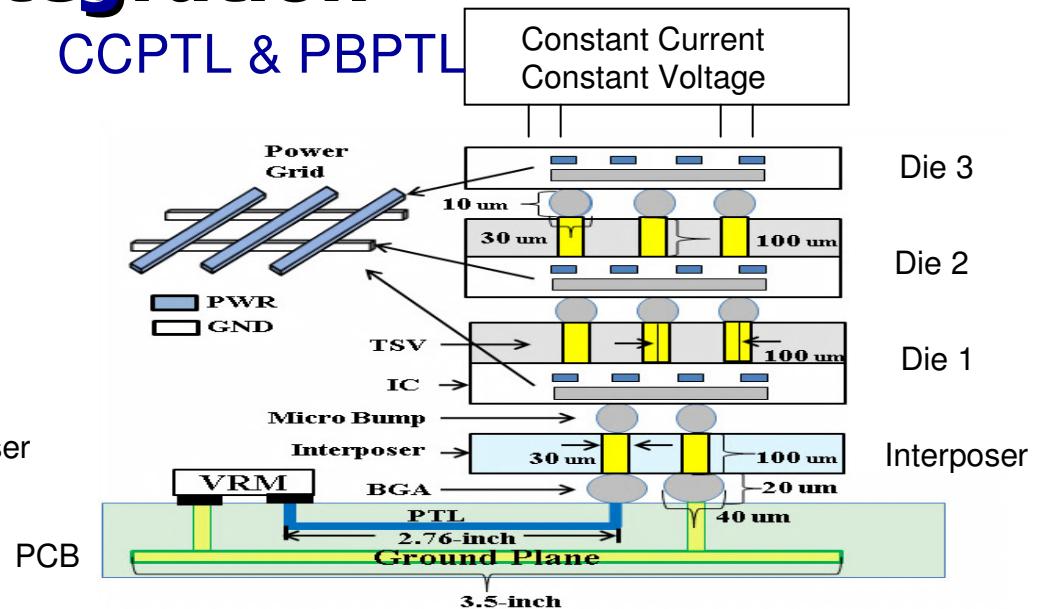
Instantaneous power consumed by the conventional PDN circuit with 256-bit long PRBS signal at 1 Gbps

# 3D Integration

Conventional



CCPTL & PBPTL



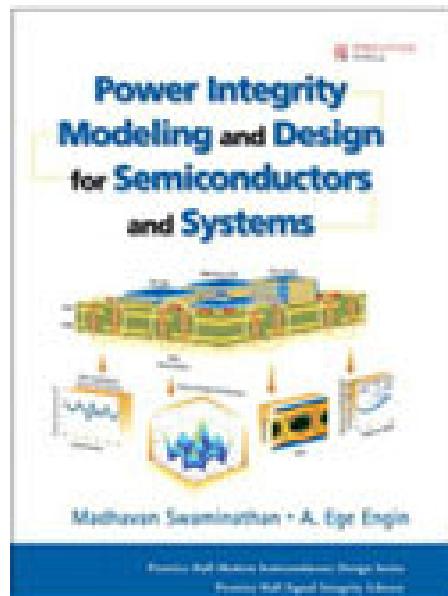
Ref: D. Zhang, M. Swaminathan and S. Huh, "New Power Delivery Scheme for 3D ICs to Minimize Simultaneous Switching Noise for High Speed I/Os", IEEE Electrical Performance of Electronic Packaging and Systems, 2012

# Summary and Conclusions

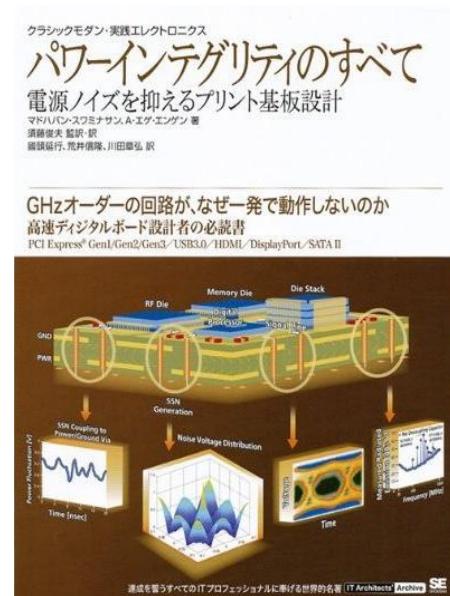
- Power Distribution continues to be a challenging area
- Concept of Power Distribution Target Impedance started in mid 1990s
- Since then, the Target Impedance has been decreasing every generation
- Boards today have more capacitors than ICs – this is a major problem
- With High Speed Signaling, Power and Ground Planes induce Return Path Discontinuities (RPD)
- RPDs create reduced eye height and increased jitter due to cavity resonances
- A possible solution to this problem is the Constant Current, Pseudo-balanced and Constant Voltage Power Transmission Line
- Theory and Measurements indicate ~35% improvement in eye height and Jitter compared to the use of power planes
- Remember: PTL is a High Impedance Power Distribution Network (not Low Impedance) , reduces capacitors (not presented) & eases the entire design procedure

# References

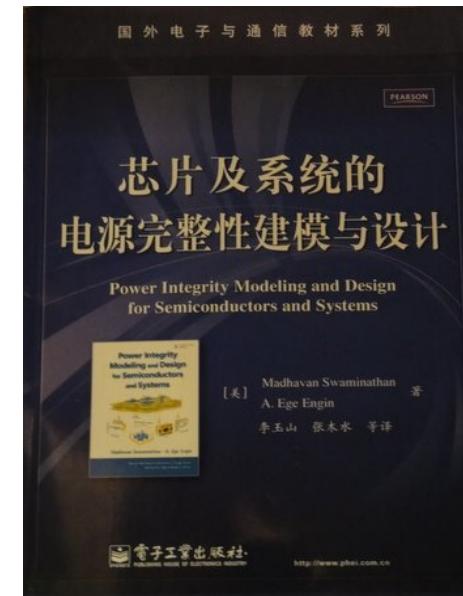
- [1] M. Swaminathan and E. Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", ISBN: 0\_13\_615206\_6, Prentice Hall, November 2007
- [2] Madhavan Swaminathan, Daehyun Chung, Stefano Grivet-Talocia, Krishna Bharath, Vishal Laddha, and Jianyong Xie, "Designing and Modeling for Power Integrity", Invited Paper, IEEE Transactions on Electromagnetic Compatibility, pp. 288 – 310, Vol. 52, No. 2, May 2010
- [3] S. Huh and M. Swaminathan, "Are Power Planes Necessary for High Speed Signaling?", Designcon, CA, 2012 (available for download at [epsilonlab.ece.gatech.edu](http://epsilonlab.ece.gatech.edu) )



English



Japanese



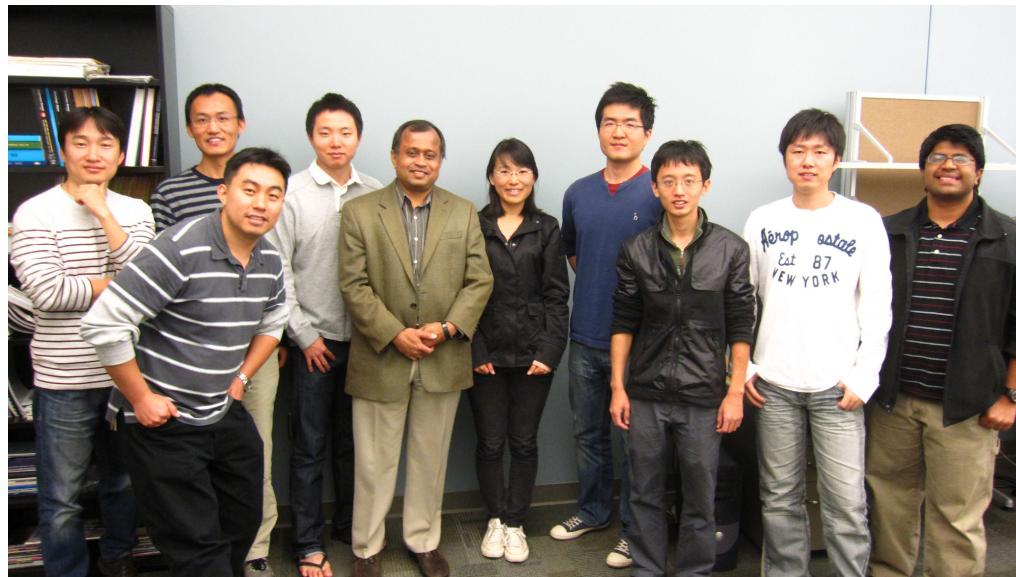
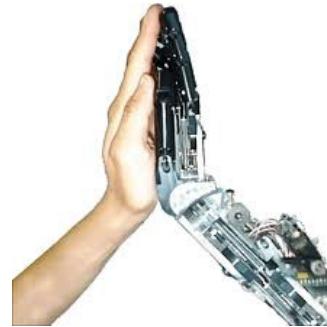
Chinese

# Upcoming Book on 3D Design and Modeling for 3D ICs and Interposers



- Focus on Design, Modeling and Tools for 3D
- Authors: M. Swaminathan and K. J. Han
- Chapters
  - System Integration Concepts
  - Modeling of Cylindrical Interconnections
  - Modeling of Through Silicon Vias
  - Electrical Performance & Signal Integrity
  - Power Distribution and Return Path Discontinuities
  - Thermal Effects
- Publication Date: 2013
- Published by World Scientific Publishers

# Thank you



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Mar 2013

