# A0

Tuesday, April 7, 2020 12:44 PM

Instructions:
1. Gather the MDS and TRM for the MSP432 from Texas Instruments. (While links are provided for each of these documents in Lab Manual Resources section, it would be worthwhile trying to find these documents directly from Texas Instruments to learn how to find datasheets in the future)
2. Review the datasheets to get an idea of their organization and what data they each contain. Note that using a PDF reader that can show bookmarks or table of contents can make navigating these documents easier.

Answer the questions below.
Questions
1. Create a memory map for Code and Peripheral address spaces of the MSP432P401R.

The device supports a 4GB address space that is divided into eight 512MB zones (see Figure 6-1).

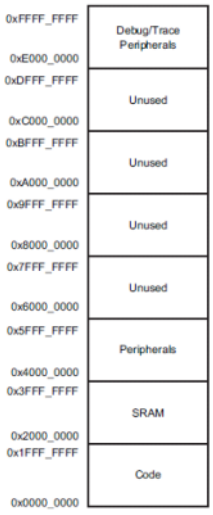


**Figure 6-1. Device Memory Zones**

This is the complete set of address spaces that are divided into eight zones. Each of these zones contain 512 MB and so the code address spaces and peripheral address spaces are provided below:

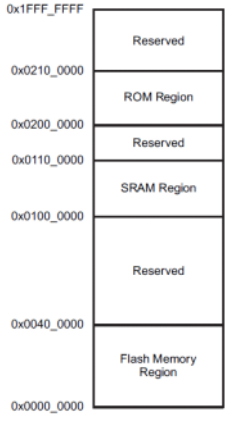


**Figure 6-2. Code Zone Memory Map**

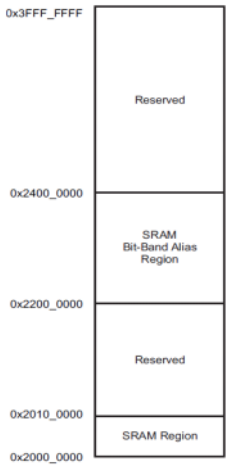


**Figure 6-3. SRAM Zone Memory Map**

2. How many internal oscillators does the MSP432 have?

Five internal oscillators: DCO,VLO,REFO,MODOSC,SYSOSC **TRM (pg 379)**

The clock system module supports low system cost and low power consumption. The clock module can be configured to operate without any external components, with up to two external crystals, or with resonators, or with an external resistor under full software control.

The clock system module includes the following clock resources:

- LFXTCLK: Low-frequency oscillator (LFXT) that can be used either with low-frequency 32768-Hz watch crystals, standard crystals, resonators, or external clock sources in the 32-kHz or below range. When in bypass mode, LFXTCLK can be driven with an external square wave signal in the 32-kHz or below range.
- HFXTCLK: High-frequency oscillator (HFXT) that can be used with standard crystals or resonators in the 1-MHz to 48-MHz range. When in bypass mode, HFXTCLK can be driven with an external square wave signal.

External Oscillators (Crystals)

- DCOCLK: Internal digitally controlled oscillator (DCO) with programmable frequencies and 3-MHz frequency by default
- VLOCLK: Internal very-low-power low-frequency oscillator (VLO) with 9.4-kHz typical frequency
- REFOCLK : Internal, low-power low-frequency oscillator (REFO) with selectable 32.768-kHz or 128-kHz typical frequencies
- MODCLK: Internal low-power oscillator with 25-MHz typical frequency
- SYSOSC: Internal oscillator with 5-MHz typical frequency

Internal Oscillators

3. How many timers does the MSP432P401R have? What size are the timers?
There are 7 timers. 4 of these timers are 16-bit timers, while the other 3 timers each have 32-bits (includes the watchdog timer)
The proper names for these three timers are watchdog timer (32-bit up counter that is not accessible by software but through the select of the WDTCTL), timer32 (two independent counters each configurable as 32-bit or 16- bit counter size), and timer_A (four 16-bit timers able to do multiple captures).

- Timing and Control
  - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
  - Two 32-Bit Timers, Each With Interrupt Generation Capability

4. What is the maximum sampling rate of the analog to digital converter on the MSP432P401R?

The maximum sampling rate of the analog to digital converter is 1 Msps. (MDS pg 132)

5. What is the equation for determining the digital output of the analog to digital converter when operating in single-ended mode on the MSP432?

The equation for determining the digital output of the analog to digital converter when operating in single-ended mode is

### 22.2.1 14-Bit ADC Core

The ADC core converts an analog input to its 14-bit digital representation. The core uses two programmable voltage levels ($V_{R+}$ and $V_{R-}$) to define the upper and lower limits of the conversion. The digital output ($N_{ADC}$) is full scale (3FFFh) when the input signal is equal to or higher than $V_{R+}$, and zero when the input signal is equal to or lower than $V_{R-}$. The input channel and the reference voltage levels ($V_{R+}$ and $V_{R-}$) are defined in the conversion control memory.

Equation 7 shows the conversion formula for the ADC result $N_{ADC}$ for single-ended mode.

$$N_{ADC} = 16384 \times \frac{V_{in+} - V_{R-}}{V_{R+} - V_{R-}}, 1LSB = \frac{V_{R+} - V_{R-}}{16384}$$

**TRM pg 845**

6. Which register is the primary mechanism for changing power modes on the MSP432?

**The primary register for switching power modes is by using the register PCMCTL0. (TRM pg 436)**

### 8.9 Power Mode Selection

Table 8-3 summarizes the various power modes available, the appropriate PCMCTL0 settings, and the entry mechanism for each of the modes.

**Table 8-3. Power Mode Selection(1)**

| Mode | Description | PCMCTL0 | | SLEEPDEEP | Entry Mechanism |
|---|---|---|---|---|---|
| | | AMR[3:0] | LPMR[3:0] | | |
| AM_LDO_VCORE0 | Active mode<br>Core voltage level 0<br>LDO operation | 0h | X | 0 | Writing of AMR register |
| AM_LDO_VCORE1 | Active mode<br>Core voltage level 1<br>LDO operation | 1h | X | 0 | |
| AM_DCDC_VCORE0 | Active mode<br>Core voltage level 0<br>DC/DC operation | 4h | X | 0 | |
| AM_DCDC_VCORE1 | Active mode<br>Core voltage level 1<br>DC/DC operation | 5h | X | 0 | |
| AM_LF_VCORE0 | Low-frequency active mode<br>Core voltage level 0<br>LDO operation | 8h | X | 0 | |
| AM_LF_VCORE1 | Low-frequency active mode<br>Core voltage level 1<br>LDO operation | 9h | X | 0 | |
| LPM0_LDO_VCORE0<br>LPM0_DCDC_VCORE0<br>LPM0_LF_VCORE0<br>LPM0_LDO_VCORE1<br>LPM0_DCDC_VCORE1<br>LPM0_LF_VCORE1 | LPM0 modes<br>Core voltage level same as respective active mode | Same as the corresponding active mode. Programing AMR is not a prerequisite for the device to enter LPM0. | X | 0 | WFI, WFE, Sleep-on-exit |
| LPM3<br>LPM4 | LPM3, LPM4 modes<br>Core voltage level same as respective active mode | X | 0h | 1 | WFI, WFE, Sleep-on-exit |
| LPM3.5 | LPM3.5 mode<br>Core voltage level 0 | X | Ah | 1 | WFI, WFE, Sleep-on-exit |
| LPM4.5 | LPM4.5 mode<br>Core voltage turned off | X | Ch | 1 | WFI, WFE, Sleep-on-exit |

(1) X = don't care

7. When the temperature goes up, does the general I/O output current from the MSP432 go up or down?

**We can see that the normal drive output current decreases (goes down) as temperature goes up. TRM(pg 61)**

### 5.25.6.1 Typical Characteristics, Normal-Drive I/O Outputs at 3.0 V and 2.2 V

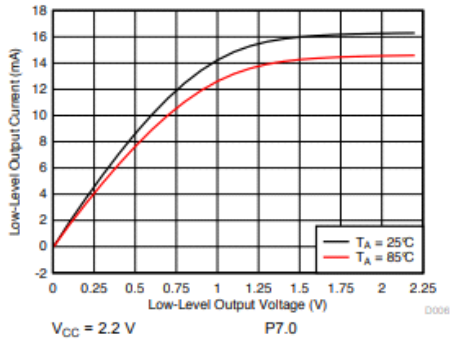


**Figure 5-19. Low-Level Output Voltage vs Low-Level Output Current**

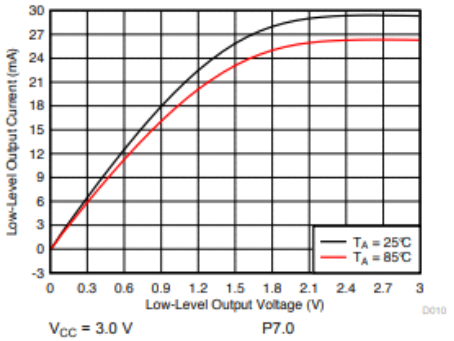


**Figure 5-20. Low-Level Output Voltage vs Low-Level Output Current**

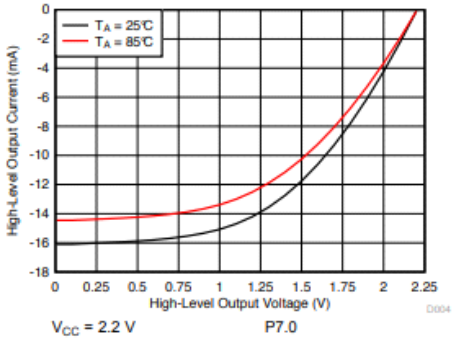


**Figure 5-21. High-Level Output Voltage vs High-Level Output Current**

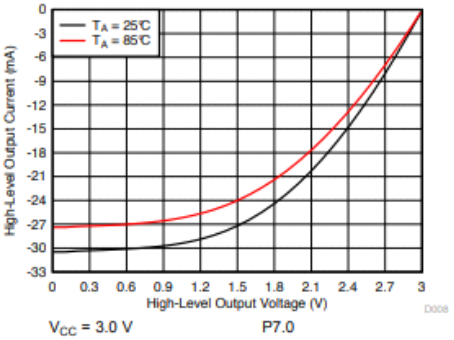


**Figure 5-22. High-Level Output Voltage vs High-Level Output Current**

8. The high drive I/O on the MSP432P401R produces more current by a factor of X. Estimate X according to the datasheet.
From table 5-24 and Table 5-25, we can see that the high drive I/Os can produce current about 5X more than the low drive I/Os. Below we can compare the Voh and the Vol and they turn out to be at 5X difference from Low Drive to High Drive I/Os. (MDS pg 59-60)

**Table 5-24. Digital Outputs, Normal I/Os**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage (see Figure 5-21 and Figure 5-22) | $I_{(OHmax)}$ = –1 mA(1) | 2.2 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA(1) | 3.0 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage (see Figure 5-19 and Figure 5-20) | $I_{(OLmax)}$ = 1 mA(1) | 2.2 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA(1) | 3.0 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

**Table 5-25. Digital Outputs, High-Drive I/Os**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage (see Figure 5-25 and Figure 5-26) | $I_{(OHmax)}$ = –5 mA(1) | 2.2 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –15 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –10 mA(1) | 3.0 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –20 mA(2) | | $V_{CC}$ – 0.50 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage (see Figure 5-23 and Figure 5-24) | $I_{(OLmax)}$ = 5 mA(1) | 2.2 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 15 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 10 mA(1) | 3.0 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 20 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.50 | |