Instructions:

1. Gather the MDS and TRM for the MSP432 from Texas Instruments. (While links are provided for each of these documents in Lab Manual Resources section, it would be worthwhile trying to find these documents directly from Texas Instruments to learn how to find datasheets in the future)

2. Review the datasheets to get an idea of their organization and what data they each contain. Note that using a PDF reader that can show bookmarks or table of contents can make navigating these documents easier.

**Answer the questions below.**

**Questions**

**1. Create a memory map for Code and Peripheral address spaces of the MSP432P401R.**

Machine generated alternative text:
The device supports a 4GB address space that is divided into eight 512MB zones (see Figure 6-1). 
P e." cherals 
oxDFFF_FFFF 
oxcooo 0000 
OXBF FF _FF FF 
OX7F FF _FF FF 
OXSF FF _FF FF 
OX3F FF _FF FF 
OXI F FF _FF FF 
Figure 6-1. Device Memory Zones 

This is the complete set of address spaces that are divided into eight zones. Each of these zones contain 512 MB and so the code address spaces and peripheral address spaces are provided below:

Machine generated alternative text:
OXIFFF FFFF 
Reserved 
ox0210 0000 
ROM Region 
ox0200 0000 
Reserved 
ox0110 0000 
SRAM Region 
ox0100 0000 
Reserved 
ox0040 0000 
Flash Memory 
Region 
Oxoooo 0000 
Figure 6-2. Code Zone Memory Map 

Machine generated alternative text:
Ox3FFF FFFF 
Reserved 
ox2400 0000 
SRAM 
Bit-Band Alias 
Region 
ox2200 0000 
Reserved 
ox2010 0000 
SRAM Region 
ox2000 0000 
Figure 6-3. SRAM Zone Memory Map 

**2. How many internal oscillators does the MSP432 have?**

Five internal oscillators: DCO,VLO,REFO,MODOSC,SYSOSC **TRM (pg 379)**

Machine generated alternative text:
The clock system module supports low system cost and low power consumption. The clock module can 
be configured to operate without any external components, with up to two external crystals, or with 
resonators, or with an external resistor under full software control. 
The clock system module includes the following clock resources: 
LFXTCLK: Low-frequency oscillator (LFXT) that can be used either with low-frequency 32768-Hz watch 
crystals, standard crystals, resonators, or external clock sources in the 32-kHz or below range. When 
in bypass mode, LFXTCLK can be driven with an external square wave signal in the 32-kHz or below 
range. 
HFXTCLK: High-frequency oscillator (HFXT) that can be used with standard crystals or resonators in 
the I-MHz to 48-MHz range. When in bypass mode, HFXTCLK can be driven with an extemal square 
wave signal. 
DCOCLK: Intemal digitally controlled oscillator (DCO) with programmable frequencies and 3-MHz 
frequency by default 
VLOCLK: Intemal very-low-power low-frequency oscillator (VLO) with 9.4-kHz typical frequency 
REFOCLK : Internal, low-power low-frequency oscillator (REFO) with selectable 32.768-kHz or 128- 
kHz typical frequencies 
MODCLK: Internal low-power oscillator with 25-MHz typical frequency 
SYSOSC: Intemal oscillator with 5-MHz typical frequency 

**3. How many timers does the MSP432P401R have? What size are the timers?**

There are 8 timers. 4 of these timers are 16-bit timers, while there are an additional 3 timers that each have 32-bits (includes the watchdog timer), and there is also another timer (SysTick) that is 24-bits.

The proper names for these three timers are watchdog timer (32-bit up counter that is not accessible by software but through the select of the WDTCTL), timer32 (two independent counters each configurable as 32-bit or 16- bit counter size), and timer\_A (four 16-bit timers able to do multiple captures). There is also SysTick Timer that provides a simple 24-bit clear-on write counter.

Machine generated alternative text:
• Timing and Control 
Up to Four 16-Bit Timers, Each With up to Five 
Capture, Compare, PWM Capability 
Two 32-Bit Timers, Each With Interrupt 
Generation Capability 

MDS(pg 1)

Machine generated alternative text:
6.2.4 SysTick 
The Cortex-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit, clear-on- 
write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in 
several different ways, and it is typically deployed either for operating System related purposes or as a 
general-purpose alarm mechanism. 

MDS(pg 90)

**4. What is the maximum sampling rate of the analog to digital converter on the MSP432P401R?**

The maximum sampling rate of the analog to digital converter is 1 Msps. (MDS pg 132)

**5. What is the equation for determining the digital output of the analog to digital converter when operating in single-ended mode on the MSP432?**

The equation for determining the digital output of the analog to digital converter when operating in single-ended mode is

Machine generated alternative text:
22.2.1 14-Bit ADC Core 
The ADC core converts an analog input to its 14-bit digital representation. The core uses two 
programmable voltage levels (VR+ and VR_) to define the upper and lower limits of the conversion. The 
digital output (NAOC) is full scale (3FFFh) when the input signal is equal to or higher than 'JR* , and zero 
when the input signal is equal to or lower than VFR. The input channel and the reference voltage levels 
(VR* and VR_) are defined in the conversion control memory. 
Equation 7 shows the conversion formula for the ADC result NADC for single-ended mode. 
. ILSB- 
16384 

 TRM (pg 845)

**6. Which register is the primary mechanism for changing power modes on the MSP432?**

The primary register for switching power modes is by using the register PCMCTL0. (TRM pg 436)

Machine generated alternative text:
8.9 
Power Mode Selection 
Table 8-3 summarizes the various power modes available, the appropriate PCMCTLO settings, and the 
entry mechanism for each of the modes. 
Table 8-3. Power Mode Selection(') 
PCMCTLO 
Mode 
LPMO LDO VCOREO 
LPMO DCDC VCOREO 
LPMO LF VCOREO 
LPM3 
LPM4 
LPM3.5 
LPM4.5 
X = don't care 
Description 
Active mode 
Core voltage level O 
LDO operation 
Active mode 
Core voltage level 1 
LDO operation 
Active mode 
Core voltage level O 
DC/DC operation 
Active mode 
Core voltage level 1 
DC/DC operation 
Low-frequency active mode 
Core voltage level O 
LDO operation 
Low-frequency active mode 
Core voltage level 1 
LDO operation 
LPMO modes 
Core voltage level same as 
respective active mode 
LPM3, LPM4 modes 
Core voltage level same as 
respective active mode 
LPM3.5 mode 
Core voltage level O 
LPM4.5 mode 
Core voltage tumed off 
Oh 
lh 
4h 
5h 
9h 
Same as the 
corresponding 
active mode. 
Programing 
AMR is not a 
prerequisite 
for the device 
to enter 
LPMO. 
x 
x 
x 
x 
x 
x 
x 
x 
x 
x 
Oh 
Ch 
SLEEPDEEP 
o 
Entry Mechanism 
Writing of AMR register 
WFI, WFE, Sleep-on-exit 
WFI, WFE, Sleep-on-exit 
WFI, WFE, Sleep-on-exit 
WFI, WFE, Sleep-on-exit 
(1) 

**7. When the temperature goes up, does the general I/O output current from the MSP432 go up or down?**

We can see that the normal drive output current decreases (goes down) as temperature goes up. TRM(pg 61)

Machine generated alternative text:
5.25.6.1 
d 10 
Typical Characteristics, Normal-Drive VO Outputs at 3.0 V and 2.2 V 
T. 2SC 
24 
2.7 3 
0 025 os 075 
1 as 1.75 2 225 
Outpu (V) 
Vcc = 22 v 
Fig Lre 5-19. Low-Lovel VS 
Low-Level Output 
0 0.3 0.6 
Vcc = v 
og 1.2 IS 2.1 
Vcaage 
Figure 5-20. Low-Lev el 
VS 
Low-Level O utp ut 
0 0.25 OS 1 1.75 
Vcc = 22 v 
Fig vs 
2.25 
-27 
0 03 0.6 og 1.8 2.1 2.4 
ouW 
Vcc = v 
27 
Figure VoRage VS 

**8. The high drive I/O on the MSP432P401R produces more current by a factor of X. Estimate X according to the datasheet.**

From table 5-24 and Table 5-25, we can see that the high drive I/Os can produce current about 5X more than the low drive I/Os. Below we can compare the Voh and the Vol and they turn out to be at 5X difference from Low Drive to High Drive I/Os. (MDS pg 59-60)

Machine generated alternative text:
Table 5-24. Digital Outputs, Normal VOS 
Over ranges Of supply voltage and operating free-air temperature (unless Otherwise noted) 
- 0.25 
vcc - 060 
cc - 0.25 
vcc - 060 
vss + 025 
vss + 060 
vss + 025 
vss + 060 
PARAMETER 
-level (see 
Figure 5-21 and Figure 5-22) 
Loa—level O utput voltage (see 
5-1 g and Figure 5-20) 
TEST 
—1 mAV1' 
= —3 mA(2' 
mA(lJ 
- mA(1) 
- 3 mA12) 
Vcc 
2.2 v 
v 
3.0 v 
2.2 v 
3.0 v 
MAX 
Vcc 
Vcc 
Vcc 
UNIT 
vss 
vss 
vss 
vss 

Machine generated alternative text:
Table 5-25. Digital Outputs, High-Drive 1/0s 
Over recommended ranges Of supply voltage and Operating free-air temperature (unless Otherwise noted) 
vcc - 0.25 
vcc - 060 
vcc - 0.25 
cc - 0.50 
vss + 025 
vss + 060 
vss + 025 
vss + 050 
PARAMETER 
(see 
Figure 5-25 and Figure 5-26) 
Loa—level output voltage (see 
Figure 5-23 and Figure 5-24) 
TEST CONDITIONS 
—15 mA'2' 
—10 
= —20 
= 15mA12' 
= 10 mm') 
- 20 
Vcc 
2.2 v 
3.0 v 
v 
2.2 v 
3.0 v 
MAX 
Vcc 
Vcc 
Vcc 
UNIT 
vss 
vss 
vss 
vss 