optimization based on 'Flexible 5G New Radio LDPC Encoder Optimized for High Hardware Usage Efficiency'
https://www.mdpi.com/2079-9292/10/9/1106

LDPC encoder without optimization

LDPC encoding is to calculate parity bits w (38.212 5.3.2)such as

$$H\begin{bmatrix} c \\ w \end{bmatrix} = [H1\ H2]\begin{bmatrix} c \\ w \end{bmatrix} = H1 \cdot c + H2 \cdot w = 0$$

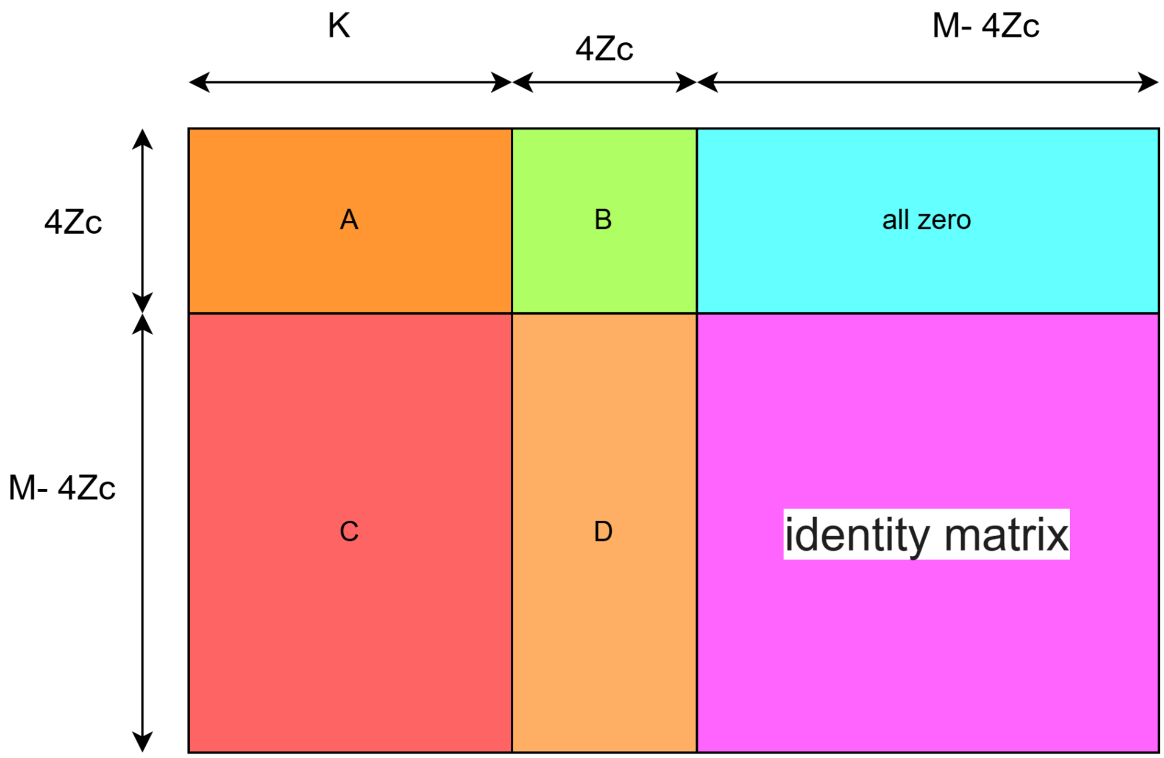
$$\Longrightarrow w = -H2^{-1} H1 \cdot c$$

H1 is 46Zc X 22Zc for LDPC base graph 1 and 42Zc X 10Zc for LDPC base graph 2
H2 is 46Zc X 46Zc for LDPC base graph 1 and 42Zc X 42Zc for LDPC base graph 2
The matrix inverse takes a very long time. The optimization method is as below.

The structure of H matrix

Zc: lifting sizes in 38.212 Table 5.3.2-1
K = 22Zc for LDPC base graph 1 and K =10Zc for LDPC base graph 2; in 38.212 5.2.2
N = 66Zc for LDPC base graph 1 and N =50Zc for LDPC base graph 2;in 38.212 5.3.2
M = N + 2Zc - K: 46Zc for LDPC base graph 1 and 42Zc for LDPC base graph 2

Below is H matrix format



$$H\begin{bmatrix} c \\ w \end{bmatrix} = \begin{bmatrix} A & B & zero \\ C & D & I \end{bmatrix}\begin{bmatrix} c \\ pc \\ ps \end{bmatrix} = 0$$

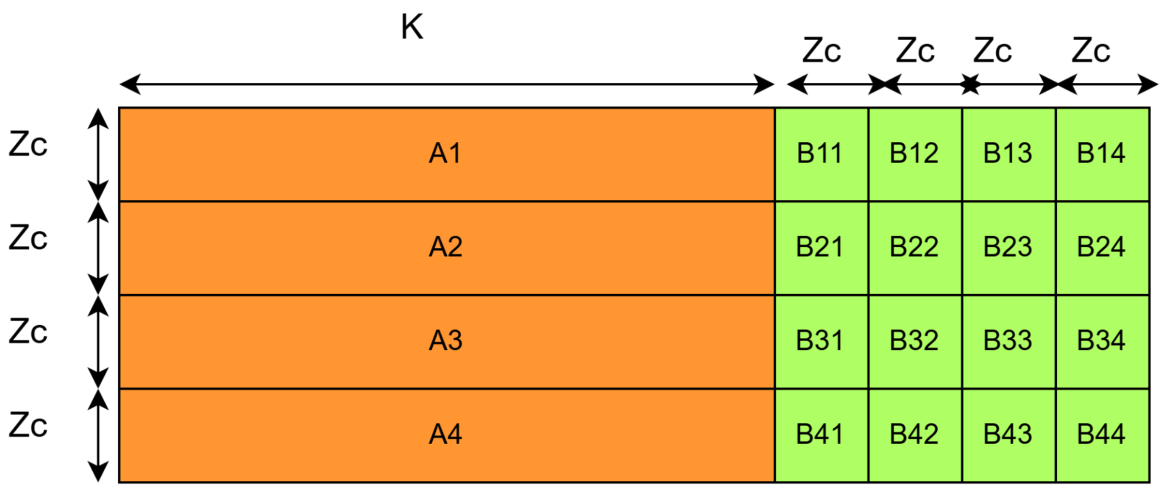
w vector is divided into pc and pa, where

pc represents a 4Zc length vector of so-called core parity bits

pa represents a M - 4Zc length vector of so-called additional parity bits

pc calculation

Rewrite matrix A and B in this way,



Divide pc into 4 Zc length vectors :

$$pc = \begin{bmatrix} pc1 \\ pc2 \\ pc3 \\ pc4 \end{bmatrix}$$

From

$$H \begin{bmatrix} c \\ w \end{bmatrix} = \begin{bmatrix} A & B & zero \\ C & D & I \end{bmatrix} \begin{bmatrix} c \\ pc \\ ps \end{bmatrix} = 0$$

Get

$$\begin{bmatrix} A & B \end{bmatrix} \begin{bmatrix} c \\ pc \end{bmatrix} =$$

$$\begin{bmatrix} A1 & B11 & B12 & B13 & B14 \\ A2 & B21 & B22 & B23 & B24 \\ A3 & B31 & B32 & B33 & B34 \\ A4 & B41 & B42 & B43 & B44 \end{bmatrix} \cdot \begin{bmatrix} c \\ pc1 \\ pc2 \\ pc3 \\ pc4 \end{bmatrix} = 0$$

Get

$$\begin{bmatrix} A1 \\ A2 \\ A3 \\ A4 \end{bmatrix} \cdot c + \begin{bmatrix} B11 & B12 & B13 & B14 \\ B21 & B22 & B23 & B24 \\ B31 & B32 & B33 & B34 \\ B41 & B4 & B43 & B44 \end{bmatrix} \cdot \begin{bmatrix} pc1 \\ pc2 \\ pc3 \\ pc4 \end{bmatrix} =$$

$$\begin{bmatrix} L1 \\ L2 \\ L3 \\ L4 \end{bmatrix} + \begin{bmatrix} B11pc1 + B12pc2 + B13pc3 + B14pc4 \\ B21pc1 + B22pc2 + B23pc3 + B24pc4 \\ B31pc1 + B32pc2 + B33pc3 + B34pc4 \\ B41pc1 + B42pc2 + B43pc3 + B44pc4 \end{bmatrix} = 0$$

For modulo 2 operation, we get :

$$\begin{bmatrix} L1 \\ L2 \\ L3 \\ L4 \end{bmatrix} = \begin{bmatrix} B11pc1 + B12pc2 + B13pc3 + B14pc4 \\ B21pc1 + B22pc2 + B23pc3 + B24pc4 \\ B31pc1 + B32pc2 + B33pc3 + B34pc4 \\ B41pc1 + B42pc2 + B43pc3 + B44pc4 \end{bmatrix}$$

B matrix format for BG1 and BG2 are as below

$$B_{BG1} = \begin{bmatrix} I^{(1)} & I & 0 & 0 \\ I & I & I & 0 \\ 0 & 0 & I & I \\ I^{(1)} & 0 & 0 & I \end{bmatrix}; \quad B_{BG2} = \begin{bmatrix} I & I & 0 & 0 \\ 0 & I & I & 0 \\ I^{(1)} & 0 & I & I \\ I & 0 & 0 & I \end{bmatrix}.$$

Based on B matrix structrure, when adding four lines together on right side, there would be 3pc1,2pc2,2pc3, 2pc4,

For modulo 2 operation, we have

$$2pc1 = 2pc2 = 2pc3 = 2pc4 = 0$$

Now get:

$$L1 + L2 + L3 + L4 = pc1$$

Calculate pc2,pc3,pc4 for BG1,

B11=B12=B21=B22=B23=B33=B34=B41=B44 = I, all other sub-matrixs = 0

$$L1 = pc1 + pc2 \Longrightarrow pc2 = L1 - pc1 = L1 + pc1$$
$$L4 = pc1 + pc4 \Longrightarrow pc4 = L4 - pc1 = L4 + pc1$$
$$L3 = pc3 + pc4 \Longrightarrow pc3 = L3 - pc4 = L3 + pc4$$

Calculate pc2,pc3,pc4 for BG2,

B11=B12=B22=B23=B31=B33=B34=B41=B44=I ,all other sub-matrixs = 0

$$L1 = pc1 + pc2 \Longrightarrow pc2 = L1 - pc1 = L1 + pc1$$
$$L4 = pc1 + pc4 \Longrightarrow pc4 = L4 - pc1 = L4 + pc1$$
$$L2 = pc2 + pc3 \Longrightarrow pc3 = L2 - pc2 = L2 + pc2$$

pa additional parity bits calculation

From

$$H \begin{bmatrix} c \\ w \end{bmatrix} = \begin{bmatrix} A & B & zero \\ C & D & I \end{bmatrix} \begin{bmatrix} c \\ pc \\ ps \end{bmatrix} = 0$$

get:

$$C \cdot c + D \cdot pc + ps = 0 \Longrightarrow ps = C \cdot c + D \cdot pc$$