Assignment 6

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1 Memory Scheduling Mechanism

Row being accessed	Arrival time	Open-page	Close-page
X	10ns	$10 + 40 = 50$	$10 + 40 = 50$
X	70ns	$70 + 20 = 90$	$70 + 20 + 20 = 110$
Y	90ns	$90 + 20 \times 3 = 150$	$110 + 20 \times 4 = 190$
X	100ns	$150 + 20 \times 3 = 210$	$110 + 20 = 130$
Y	180ns	$210 + 20 \times 3 = 270$	$190 + 20 = 210$

2 Memory System Design

For the pros, since the data bus is shrinked , the data we can transfer more each time to increase the parallelism. Also, the energy consumption is reduced each time. For the cons, we may need more time to fetch a line. This will also results in limited bandwidth.

3 Virtually Indexed Physically Tagged Cache

Since the page size is 4KB, we know that the offset bit is 12. We know that it is VIPT cache, so the sum of offset bit and index bit should be the same as the page offset. So we know that, based on that the L1 is 8-way set associative, the maximum capacity would be $8 \times 4KB = 32KB$.

4 DRAM Control

1. t_{CL}
2. $t_{RP} + t_{RCD} + t_{CL}$

5 DRAM Control Tasks Request Scheduling

For the actions:

1. ACT, RD

2. PRE, ACT, RD
3. ACT, RD
4. RD

For the time:

1. t_{RAS}, t_{CAS}
2. $t_{PRE}, t_{RAS}, t_{CAS}$
3. t_{RAS}, t_{CAS}
4. t_{CAS}