Homework4

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1 Cache Hierarchy

1. For L1, $t_1 = 2000 \times 0.5 \times 1$
2. For L2, $t_2 = 2000 \times 0.5 \times 0.55 \times (1 + 3 + 18)$
3. For L3, $t_3 = 2000 \times 0.5 \times 0.45 \times 0.75 \times (1 + 3 + 25 + 85)$
4. For Memory, $t_4 = 2000 \times 0.5 \times 0.45 \times 0.25 \times (1 + 3 + 25 + 440)$

So the total is

$$total = t_1 + t_2 + t_3 + t_4 \approx 104338 cycles$$

2 Performance Metric

$5 + 20\% \times 150 = 35 cycles$.

3 Cache Addressing

Since main memory is 8GB, there are 33 bits.

1. For L1, 16B block means offset is 4 bits. Since there are 32 KB blocks, index bit is 11. The tag bits is $33 - 11 - 4 = 18$bits.
   For L2,, 64B block means offset is 6 bits. Then there are 2^{12} blocks so the index bit is 12. Finally, the tag bit is $33 - 12 - 6 = 15$.
2. For L1, the array size is 32kb. The tag array size is $18 \times 2^{11} = 36864 bits = 4.5 kb$.
   For L2, the array size is 1MB. So the tag array size is $4 \times 15 \times 2^{12} = 245760 bits = 30 kb$.

4 Cache Replacement Policies

1.

P1	Ideal	LRU	MRU
C	M	M	M
A	M	M	M
B	M	M	M
D	M	M	M
B	H	H	H
F	M	M	M
C	H	M	H
E	M	M	M
A	M	M	M
D	H	M	H
B	H	M	H
F	M	M	M
A	H	H	H
B	H	H	H
C	M	M	M
E	H	M	H
B	H	H	M
A	M	M	H
F	H	H	H
D	M	M	M

For Ideal, the miss rate is 55%. For LRU, the miss rate is 75%. For the MRU, the miss rate is 55%.

2.

P2	Ideal	LRU	MRU
D	M	M	M
F	M	M	M
C	M	M	M
B	M	M	M
A	M	M	M
A	H	H	H
F	H	H	H
C	H	M	H
D	H	H	H
D	H	H	H
A	H	H	H
B	M	M	M
A	H	H	M
B	H	H	M
C	M	M	H
E	M	M	M
B	H	H	H
A	M	M	M
B	H	H	M
D	H	H	M

The miss rate of ideal is 45%. The miss rate for LRU is 50%. The miss rate for MRU is 60%.