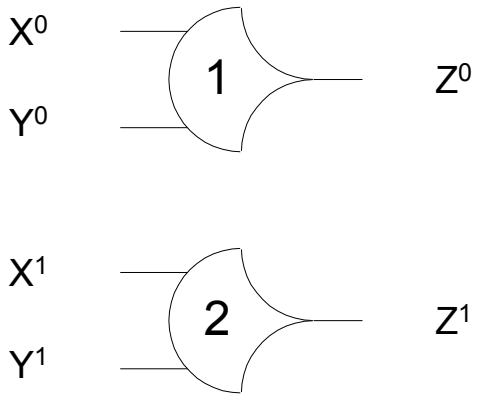
Input-Completeness

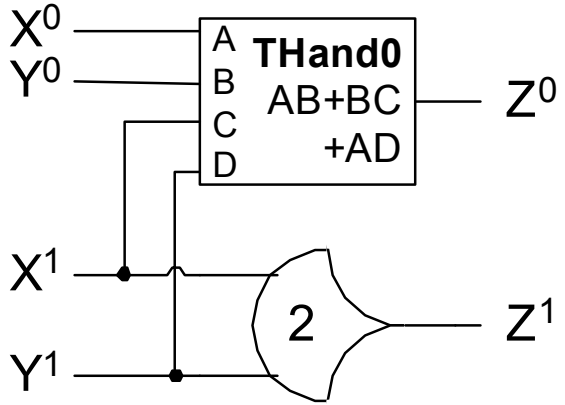
- circuit outputs transition from NULL to DATA only after *all* inputs transition from NULL to DATA, and
- circuit outputs transition from DATA to NULL only after *all* inputs transition from DATA to NULL

Input-Incomplete NCL AND Function



Z = DATA0 when X = DATA0 and Y = NULL, or
when Y = DATA0 and X = NULL

Input-Complete NCL AND Function

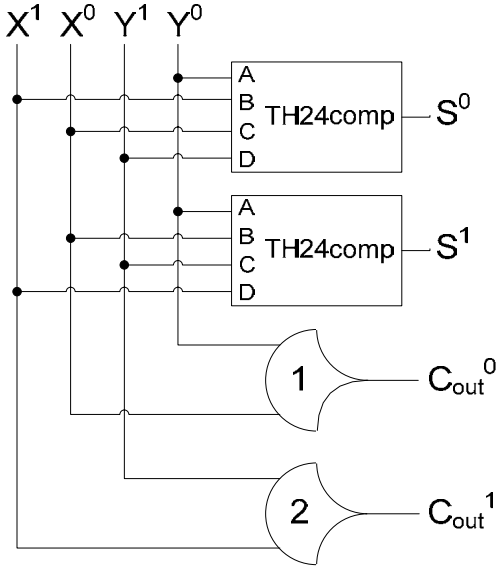


Z = DATA only when both X and Y are DATA

Relaxed Input-Completeness

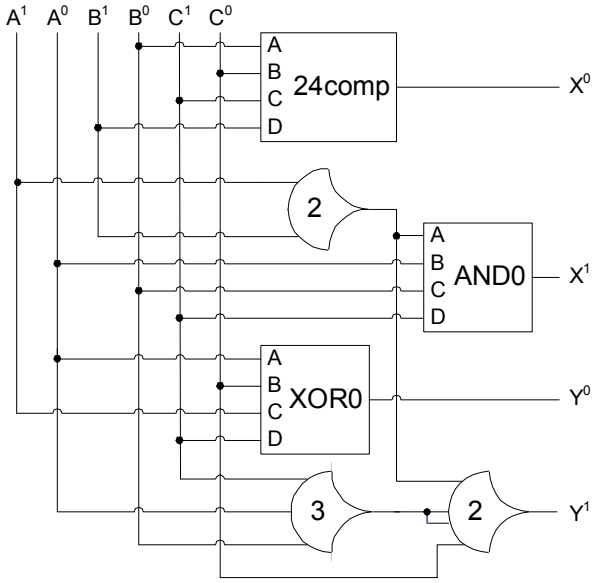
- for circuits with multiple outputs, some outputs can transition to DATA/NULL before all inputs transition to DATA/NULL, as long as all outputs cannot transition to DATA/NULL before all inputs transition to DATA/NULL

Input-Complete NCL Half-Adder



- *S* is input-complete wrt both *X* and *Y*
- C_{out} is not input-complete wrt either input

Input-Complete NCL Circuit

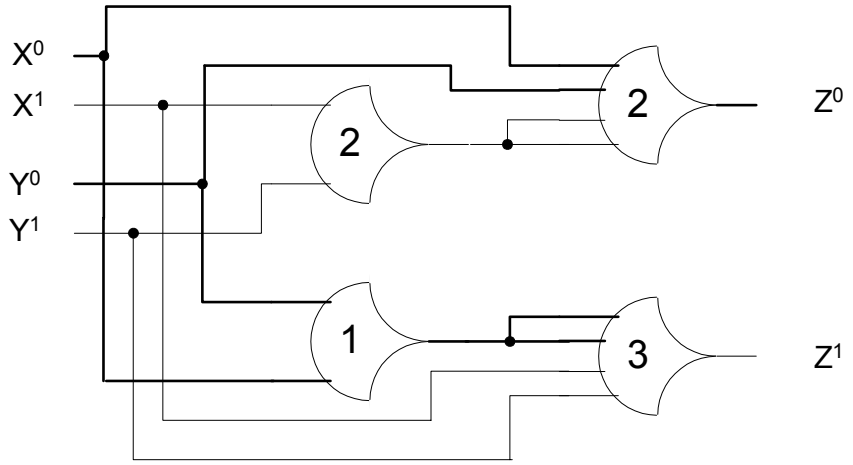


- $X^0 = B^0C^1 + C^0B^1$; $X^1 = A^0B^0 + A^1B^1C^1$
- $Y^0 = A^0C^0 + A^1C^1$; $Y^1 = A^1B^1C^0 + C^1B^0A^0$
- *X* is input-complete wrt *B*
- *Y* is input-complete wrt *A* and *C*

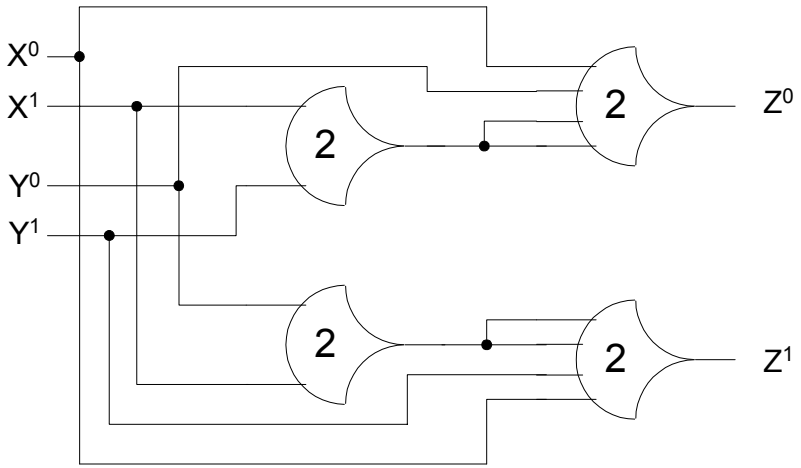
Observability

- All gate transitions must be observable at the output
  - any gate that is asserted must cause at least one output to be asserted

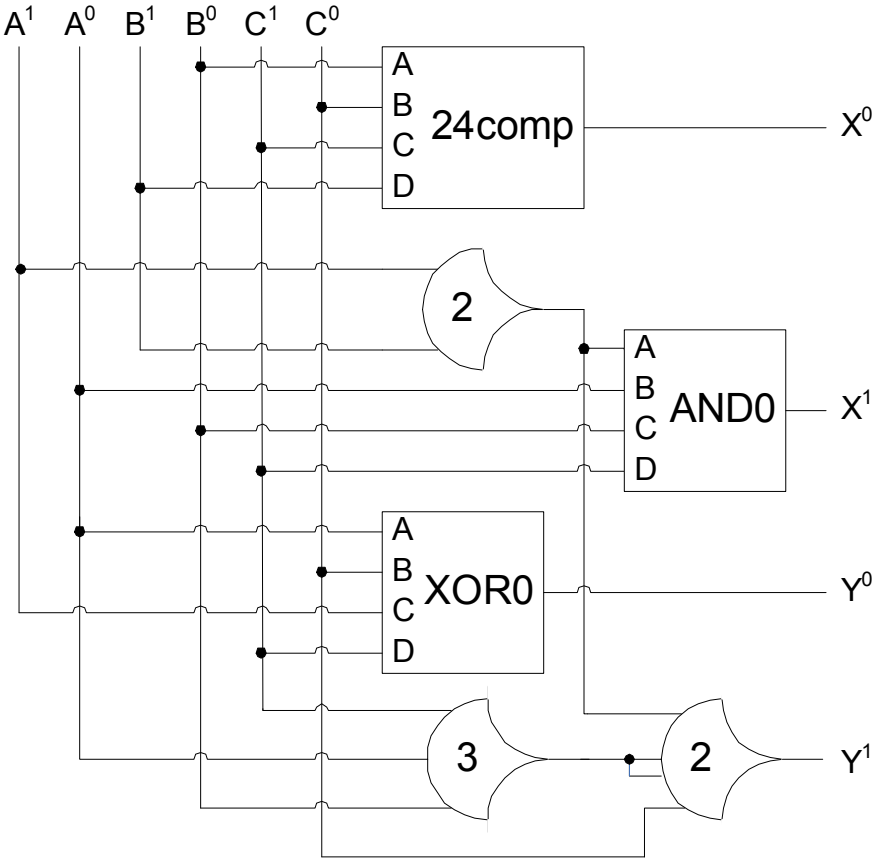
Unobservable NCL XOR Function



Observable NCL XOR Function



Observable NCL Circuit



- $X^0 = B^0C^1 + C^0B^1$; $X^1 = A^0B^0 + (A^1B^1)C^1$
- $Y^0 = A^0C^0 + A^1C^1$; $Y^1 = (A^1B^1)C^0 + C^1B^0A^0$
- TH33 gate is observable since Y^1 will always be asserted whenever the TH33 gate is asserted
- TH22 gate is observable because either X^1 or Y^1 will always be asserted whenever the TH22 gate is asserted