Invited Tutorial

Practical Applications of Asynchronous Pipeline Circuits

J. Brian Johnson, Micron Technology, Inc.

Abstract

Asynchronous circuit designs have shown great promise for overcoming synchronous timing overhead and power requirements of functionally equivalent, continuously-clocked circuit designs. In some instances, such as memory data path applications, speed independent, asynchronous pipelines are used to provide low-latency, high-throughput logic paths. Asynchronous pipelines use local handshaking to avoid the problems of clock skew, switching noise and switching power generated by global clock distributions found in synchronous circuit designs. Asynchronous pipelines that exhibit the property of *speed independence* provide functional tolerance to low supply voltage, and are modular in application, given proper adherence to interface protocol. The advantages of asynchronous circuits, relative to synchronous circuits, are not without cost. Asynchronous circuits can pose difficulties with testing, interfacing to synchronous environments, and a general lack of well-established, industry standard design and verification tools, which often forces asynchronous designs to be realized using full-custom design methodologies. This tutorial will present recent developments in the literature related to asynchronous pipeline protocols and circuits. Unique circuit constructs and applications will be presented with emphasis on interfacing asynchronous circuits to synchronous environments, controlling dynamic logic paths, and applications that call for the flexibility of varying forward path, inter-stage cycle times within an asynchronous logic pipeline.

Speaker's Biography

Brian Johnson earned a B.A. in English from Whitman College, Walla Walla, WA in 1988 and a B.S.E.E. from the University of Idaho, Moscow, ID in 1999. Following that, he completed his M.S.E.E. at the University of Idaho, Moscow, ID in 2004.

He has held various positions with Micron Technology, Inc. beginning in 1990, and is currently a Distinguished Member of the Technical Staff. He is a co-author of "DRAM Circuit Design: Fundamental and High-Speed Topics", IEEE Press, 2007, and has co-authored other papers published in IEEE journals. His current research interests include asynchronous circuit design and design of methods for timing and control circuits for computer memory sub-systems.

Mr. Johnson holds numerous patents related to DRAM design and CMOS circuit design.