CMOS Implementation Comparison of NCL Gates

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***Abstract*— Various CMOS implementations of asynchronous NULL Convention Logic (NCL) gates have been compared in terms of area, speed, energy, power, supply voltage, and noise. Additionally, a new approach to design semi-static NCL gates has been introduced. Each gate type is used to realize a delay-insensitive 4×4 NCL multiplier and the simulation results are compared. It is shown that different realizations excel in different design parameters. This paper aims to provide NCL designers with the tradeoffs of using various NCL gate types.**

I. INTRODUCTION

New advancements in CMOS IC fabrication technology allow for chips with extremely tiny feature sizes, resulting in much smaller ICs with much higher clock rates. Although higher clock rates make synchronous logic designs faster, they also increase power consumption and cause many clock distribution issues. Asynchronous clockless logic design paradigms have recently been considered as a solution for these ever-increasing clock issues. NULL Convention Logic (NCL) [1] is one of the promising delay-insensitive asynchronous logic design paradigms [2]. NCL circuits are comprised of 27 state-holding threshold gates, which constitute the set of all functions of 4 or fewer variables. Each gate is denoted as TH*mn*W*w1w2w3* where *m* is the gate threshold, *n* is the number of inputs, and *w1, w2,* and *w3* are the input weights (if greater than 1). For example, a TH23 gate asserts its output when at least two out of three inputs are asserted. NCL gates are designed with hysteresis, such that once asserted, the output remains asserted until all inputs are deasserted. When *m* equals *n* the NCL gate is equivalent to an n-input C-element [3].

Several CMOS implementation schemes have been introduced for NCL gates, including dynamic, static, semi-static [4], and differential [5]. The dynamic implementation is not delay-insensitive; hence, it is not discussed here. The static and semi-static implementations of C-elements have been extensively discussed in [6]. The differential implementation of NCL gates has been recently introduced and discussed in [5]. In this paper we compare static, semi-static, and differential implementations at the circuit level by using them to realize a delay-insensitive NCL 4×4 multiplier. Additionally, we have introduced a new semi-static design approach that achieves much better performance compared to the existing semi-static designs. Section II explains the various NCL gate CMOS implementations, while Section III introduces the new semi-static design approach. Simulation results for various 4×4 NCL multiplier implementations are presented in Section IV, and finally, Section V draws conclusions based on the comparisons.

II. PREVIOUS WORK

A. Static Implementation of NCL Gates

Synchronous gates are usually comprised of one pull-up and one pull-down network for set and reset functions, which are complements of each other. However, since NCL gates must have hysteresis to ensure delay-insensitivity, an additional pull-up and pull-down network are required to keep the output value unchanged while neither the set nor reset functions are true, since set and reset are not complements of each other in NCL gates. These extra networks are called *Hold0* and *Hold1*. The structure of static NCL gates is shown in Fig. 1(a). A static TH23 gate based on this structure is shown in Fig. 1(b). The number of transistors in Fig. 1(b) can be reduced by sharing transistors between each pair of pull-up or pull-down networks. Also, note that $Hold0 = \overline{Set}$ and $Hold1 = \overline{Reset}$.

B. Semi-Static Implementation of NCL Gates

In the semi-static implementation, as shown in Fig. 2(a), the *Hold0* and *Hold1* networks are replaced with a weak

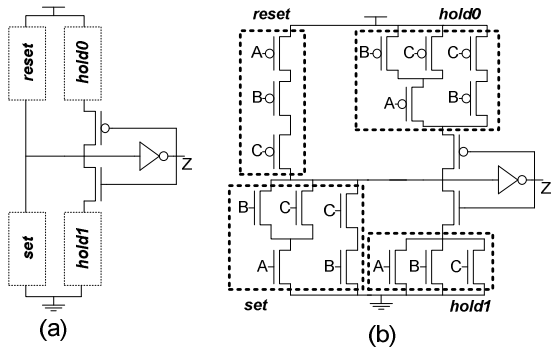

Figure 1. (a) Structure of static NCL gates (b) a static TH23 gate

feedback inverter to keep the charge on the internal node (denoted by $\bar{z}$ in Fig. 2(a)) when neither set nor reset functions are true. The weak inverter size must be selected carefully. If the feedback inverter is not weak enough, the pull-up network will not be able to provide enough contention current to overpower the feedback inverter and reset the output. On the other hand, a very weak feedback inverter will not be able to sink/source enough current to resist noise on the internal node or to make up for charge loss at the internal node in case of charge sharing with the pull-down network. The charge sharing problem can be alleviated by carefully arranging the transistors in the pull-down network [4], but the weak inverter should still be strong enough to resist noise on the internal node and to restore charge on it in case of charge sharing.

To make the feedback inverter weak, usually a smaller channel width is used for its NMOS but if in spite of having the minimum width the inverter is not weak enough, the channel length of the NMOS is increased. The correct sizing requires exhaustive simulations and most of the time involves sizing the pull-up network as well to make it strong enough to overpower the feedback inverter. This will be further discussed in Section III where various methods of weakening the feedback inverter are introduced.

C. Differential Implementation of NCL Gates

Differential implementation of NCL gates (DNCL), recently introduced in [5], is based on removing the pull-up network in the semi-static implementation and replacing it with another pull-down network at the output, as shown in Fig. 2(b). The differential design is most similar to Differential Cascode Voltage-Switch Logic (DCVSL) with cross-coupled PMOS transistors replaced with cross-coupled inverters. The main advantage of DNCL gates over semi-static ones is that they do not require sizing. In other words, all the transistors in the DNCL gates can be minimum-sized. This is because the transistors used for the *Reset* function are now all NMOS transistors, which normally have higher mobility compared to PMOS transistors so they overpower the PMOS transistors of the cross-coupled inverters even when they are minimum-sized. Removing the sizing constraint not only results in smaller gates but also increases the ability of DNCL gates to operate under low-voltage conditions. Note that DNCL gates need both main inputs and their inverted form for correct operation; however, this does not require extra logic because each DNCL gate offers both the main output (z) and its inverted form ($\bar{z}$).

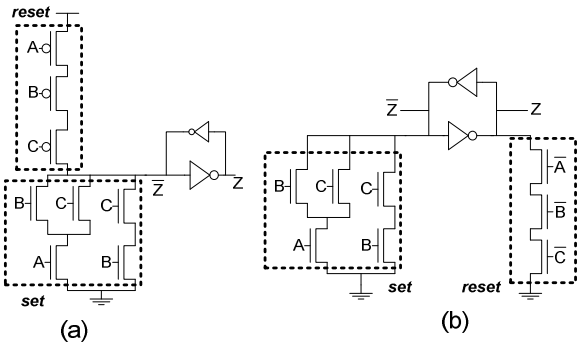

Figure 2. (a) Semi-static and (b) DNCL implementations of TH23 gate

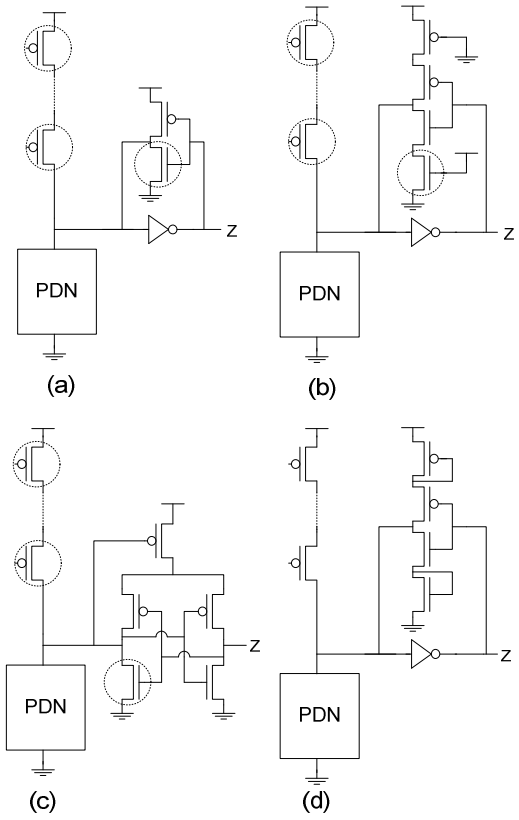

Figure 3. Different weakening methods for feedback inverter (a) standard method (b) resistive method (c) supply feedback method (d) proposed diode-connected method

III. Designing Semi-static NCL Gates

As discussed before, sizing the feedback inverter is essential for semi-static gates to function correctly. Usually decreasing the channel width of the NMOS transistor, or increasing its length in case of having minimum width, does not suffice and one also needs to strengthen the pull-up network by sizing the PMOS transistors. The standard method of weakening the feedback inverter is shown in Fig. 3(a). The transistors that usually need to be sized are shown inside dashed circles in this figure. Resizing these transistors not only increases the area of semi-static gates but also deteriorates their performance.

Another method to weaken the feedback inverter is to add a pair of NMOS and PMOS transistors in series with the transistors of the feedback inverter [7] as shown in Fig. 3(b). The added transistors limit current and hence weaken the feedback inverter. This method, called resistive method hereafter, still requires sizing of the transistors as shown with the dashed circles but the sizing requirement will be milder. A very recent method of weakening the feedback inverter for semi-static C-elements has been proposed in [8]. This method is based on the Supply Feedback concept which is used for designing robust, low-leakage static RAM bitcells. We have applied this method to NCL gates as shown in Fig. 3(c). This method still requires careful sizing for correct operation of NCL gates. Finally, we propose using two minimum-sized diode-connected transistors to weaken the feedback inverter as shown in Fig. 3(d). The two minimum-sized diode-connected

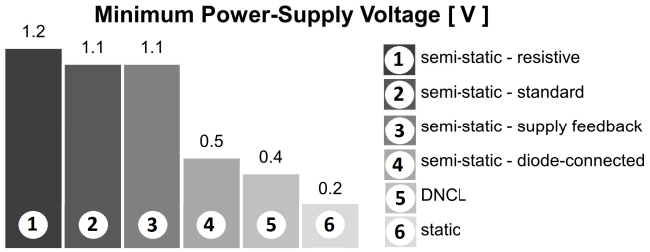

Figure 4. Minimum power-supply voltage

TABLE I. DELAY, ENERGY, AND POWER AT 1.2V

Gate Type	*Power (µw)*	*Delay per Operation (ns)*	*Energy per Operation (pJ)*
static	431	3.8	1.63
DNCL	675	4.5	3.07
semi-static (standard)	655	6	3.95
semi-static (resistive)	538	5.2	2.82
semi-static (supply feedback)	470	6.8	3.18
semi-static (diode connected)	459	2.9	1.35

transistors act as current limiters thus weakening the enclosed inverter. This method of weakening not only allows all minimum-sized transistors to be used, but also dramatically enhances performance of semi-static gates, as shown in the next section.

IV. SIMULATION RESULTS

In order to make a comparison between different implementations of NCL gates, a delay-insensitive 4×4 NCL multiplier was designed and exhaustively simulated at the transistor-level using each type of gate. All simulations are performed using the 1.2V IBM CMRF8SF 130nm CMOS process. To make a fair comparison, all the gates utilize minimum-sized transistors except for the first three types of semi-static gates (standard, resistive, and supply feedback) that require sizing for correct operation. These semi-static gates are only sized to the point where they are functional under the supply voltage of 1.2V. We compare several design parameters including minimum supply voltage, average energy per operation, average delay per operation, average power, area, and noise susceptibility.

A. Minimum Power-Supply Voltage

The minimum supply voltage under which the NCL multiplier can function correctly is shown in Fig. 4 for each gate type. The static multiplier can operate with a supply voltage as low as 0.2V. The multipliers utilizing the first three types of semi-static gates have the highest minimum supply voltage due to the relative transistor sizing requirement for the PUN and the feedback inverter.

B. Average Energy per Operation

Figure 5(a) shows the average energy per operation for different realizations versus different supply voltages. The multiplier realized with the diode-connected semi-static gates consumes the least energy per operation. On the other hand, the standard semi-static realization has the worst energy per operation. The energy per operation for each realization decreases as the supply voltage decreases. Under the supply voltage of 1.2V, the average energy per operation for different realizations is listed in Table I. Based on this table, the multipliers that utilize the static or diode-connected semi-static gates consume less energy than the other realizations.

C. Average Delay per Operation

The average delay per operation for different realizations under the supply voltage of 1.2V is listed in Table I. Based on this table, the diode-connected semi-static and the supply feedback semi-static are the fastest and the slowest realizations, respectively. The average delay per operation versus different supply voltages is shown in Fig. 5(b). This shows an exponential increase in the delay as the supply voltage decreases. Also, the DNCL realization is the fastest realization for supply voltages lower than 0.6V.

D. Average Power

Average power consumption for different realizations versus supply voltage is shown in Fig. 5(c), where power consumption decreases as supply voltage decreases. Based on simulation results, the static and DNCL realizations are the least and most power consuming, respectively. Under the supply voltage of 1.2V, the average power consumption for

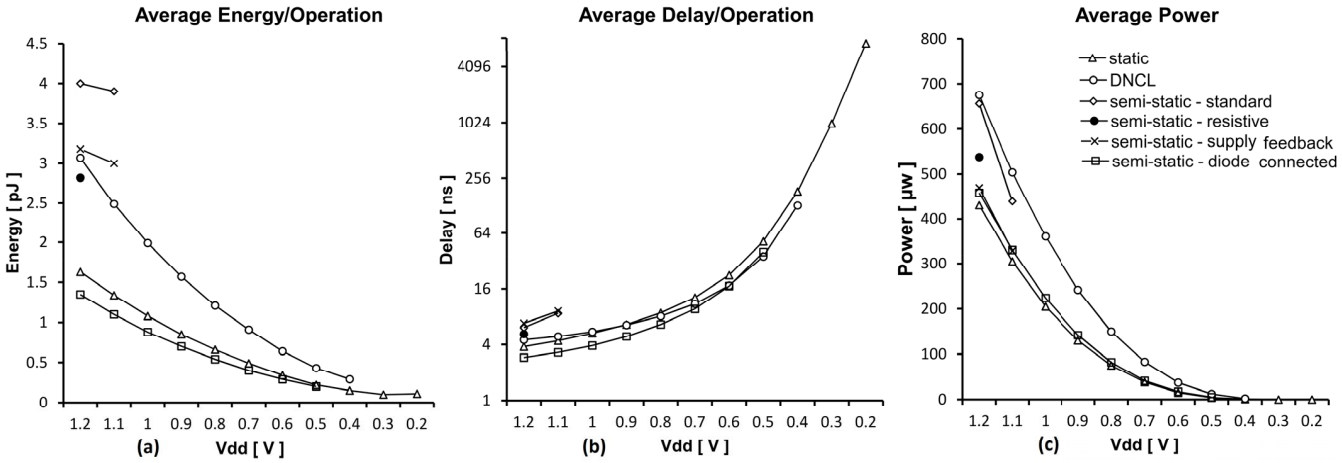

Figure 5. (a) Average energy per operation (b) Average delay per operation (c) Average power for different realizations

different realizations is listed in Table I.

E. Area

The total area for different realizations is shown in Fig. 6. Total area is calculated by adding up the area of transistors used in each realization. As it is shown, DNCL and the standard semi-static realizations have the smallest and largest area, respectively. This could be predicted by considering the fact that DNCL gates use the least number of transistors and they are all minimum-sized. The diode-connected semi-static gates also use all minimum-sized transistors but they require two additional transistors compared to DNCL gates to weaken the feedback inverter, thus they consume slightly more area (15%). The static realization was expected to utilize more area since the static gates have extra pull-up and pull-down networks to maintain hysteresis. The other semi-static realizations were also expected to require more area due to the transistor sizing requirement.

F. Noise Susceptibility

The last parameter measured is noise susceptibility, motivated by the fact that in semi-static gates the feedback inverter should not be too weak such that it can resist the noise currents on the internal node. To test robustness to noise a typical gate (TH22) was selected and simulated for noise susceptibility. The testbench is comprised of a TH22 gate and a noise current source connected to its internal node. The magnitude of the noise current is then swept to the point where the gate output switches. Simulation results show that the minimum current value for which the output switches for different gate types are as follows: static 10.8µA, standard semi-static 19.3µA, diode-connected semi-static 1.7µA, DNCL 19.3µA, resistive semi-static 10.7µA, and supply feedback semi-static 6.2µA. Based on simulation results the standard semi-static and DNCL are the most noise robust implementations. Assuming the noise susceptibility of these two implementations is 1x, the noise susceptibility for the rest of the implementations is shown in Fig. 7.

V. Discussion & Conclusion

According to the simulation results, NCL circuits that utilize different implementations of NCL gates can excel in different design parameters. The static realization of NCL circuits can utilize very low supply voltages. Under these supply voltages, NCL circuits can be very low-energy/power but at the same time be much slower. Therefore, static realizations could be used in applications where low voltage/energy/power are desired but speed and area are not very critical. The DNCL realization utilizes less area and can operate under low-voltage conditions with higher speed but consumes more energy and power.

The only advantage of the standard semi-static realization is its noise susceptibility, which is the same as DNCL; hence even when noise is an issue, DNCL would be preferred. The supply feedback and resistive semi-static realizations have very close features to the standard semi-static except for lower power/energy consumption. The performance of the first three types of semi-static realizations is highly dependent on the

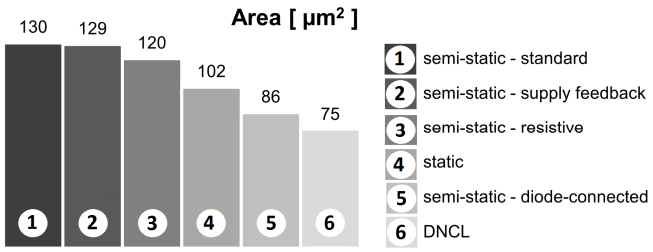

Figure 6. Area for different realizations

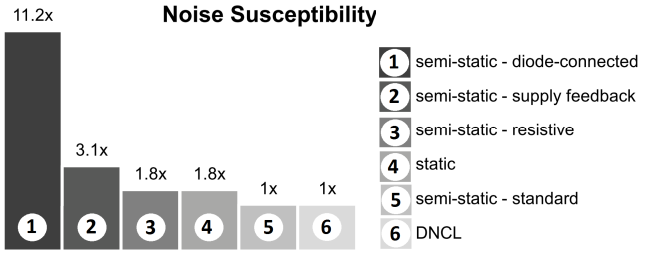

Figure 7. Noise susceptibility for different realizations

sizing of the gates. In this paper, for the sake of a fair comparison, these semi-static gates were only sized to the point where they function correctly, but, one can achieve better performance by increasing their sizing. Finally, the proposed diode-connected semi-static realization, although relatively weak in terms of noise susceptibility, seems to offer an excellent tradeoff between the other design parameters; it requires the second least area, over DNCL, utilizes only slightly more power than the least power consuming static design, can operate under moderately low supply voltage conditions, and is the fastest realization under nominal supply voltage, while consuming the least amount of energy.

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