Asynchronous Circuit Design using New High Speed NCL Gates

Minsu Choi[1], Byung-Ho Kang[2], Yong-Bin Kim[3], Kyung Ki Kim[2]

[1] Department Electrical & Computer Engineering, Missouri University of Science & Technology
Rolla, MO, USA
[2]Department of Electronic Engineering, Daegu University
Gyeongsan, South Korea
[3]Department of Electrical and Computer Engineering, Northeastern University
Boston, MA, USA
choim@mst.edu, kissme0905@live.daegu.ac.kr, ybk@ece.neu.edu, kkkim@daegu.ac.kr (corresponding)

Abstract

The delay-insensitive Null Convention Logic (NCL) as one of innovative asynchronous logic design methodologies has many advantages of inherent robustness, power consumption, and easy design reuses. However, transistor-level topologies of conventional NCL gates have weakness of logic speed, area overhead or wire complexity. Therefore, this paper proposes a new NCL gates designed at transistor level for high-speed, low area overhead. A 4x4 multiplier using the proposed NCL gates has been compared to the multiplier using conventional NCL gates in terms of delay, area and energy consumption.

Keywords-component; asynchronous circuit;null convention logic, NCL, delay insensitive model, multiplier

Null Convention Logic

In the reliable ultra-low power design, asynchronous circuits have recently been re-considered as a solution for scaling issues [1]. Null Convention Logic (NCL) is one of the promising delay-insensitive asynchronous circuit design methodologies [2]-[5]. NCL circuits utilize threshold gates with hysteresis to maintain delay insensitivity. NCL uses delay-insensitive codes for data communication, alternating between set and reset phases. NCL uses threshold gates with hysteresis for its composable logic elements. One type of threshold gate is the *THmn* gate as shown in Fig. 1(a), where $1 \leq m \leq n$. A TH_{mn} gate means that at least *m* of the *n* inputs has to be asserted before the output will become asserted. Threshold gate inputs and outputs can be in of two states, DATA or NULL [1].

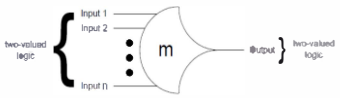

Fig. 1 THmn gate symbol

A threshold gate starting with its output in a NULL state will remain in the NULL state until the specified numbers of inputs are placed in the DATA state. Once the gate reaches the DATA state, it remains in this state until all of the inputs return to the NULL state. A dual-rail signal, *D*, consists of two wires, *D*0 and *D*1, which may assume any value from the set DATA0, DATA1, NULL. The *DATA*0 state (*D*0 = 1, *D*1 = 0) corresponds to logic zero, the DATA1 state (*D*0 = 0, *D*1 = 1) corresponds to logic one, and the NULL state (*D*0 = 0, *D*1 = 0) corresponds to the empty set meaning that the value of D is not yet available. The two rails are mutually exclusive, so that both rails can never be asserted simultaneously; this state is defined as an illegal state.

New Transistor-Level NCL Gates

Several CMOS implementation schemes have been proposed for NCL gates such as dynamic, static, semi-static, and differential [3]-[5]. The dynamic implementation can be used in real-time computing applications where a minimum data rate is guaranteed so the state information can be kept on an isolated node without requiring a feedback mechanism, but this is not delay-insensitive. The static and semi-static implementations utilize feedback to maintain state information and therefore do not require a minimum input data rate [4]. The differential implementation of NCL gates has been recently introduced and discussed in [3]. The differential design is most similar to Boolean Differential Cascode Voltage-Switch Logic (DCVSL) gates, where both the output and its complement are available. NCL threshold gates are state-holding and designed to have hysteresis. As depicted in Fig. 2 (a), each static NCL gate is comprised of 4 transistor networks: *set*, *reset*, *hold1*, and *hold0*. The *set* function determines the gate's functionality as one of the 27 NCL gates. The output then remains asserted through the *hold1* function until all inputs are deasserted. The CMOS implementation of the static, semi-static, and differential TH23 is shown in Fig. 2 (a), (b), and (c), respectively. The differential implementations of NCL gates offer different advantages for design of NCL circuits. However, the differential design has weakness of wire complexity and logic delay. Static gates tend to be faster with lower voltage operation capability, while semi-static gates are more energy efficient, and differential gates are more area efficient. A comprehensive comparison of the different gate styles can be found in [4]. However, each NCL gates of the static implementation has many stack number of transistors as well as a large number of transistors, which leads large gate delay. In case of semi-static, fewer transistors are required, but the speed is slower due to the weak inverter feedback. In this paper, a new CMOS topology has been proposed for implementing gates required by NCL design at the standard-cell level as shown in Fig. 2 (d). The proposed TH23 topology is revised from the semi-static NCL gate. The semi-static NCL gate is the best transistor-level topology compared to other topology only if area overhead and wire

complexity are considered. However, the main problem of the semi-static topology is the slow logic speed due to the weak inverter feedback and the number of PMOS serial stacks as shown in Fig. 2 (b). The proposed topology doesn't have any PMOS stack like the differential one, while a pseudo-NMOS logic block for a reset function is added, and a feedback memory is formed by a inverter and a NOR gate. The pseudo-NMOS logic has the advantage of speed at the cost of static power dissipation. However, the power can be saved enough to use the pseudo-type logic in a real system if the enable signal (EN) is properly controlled. In Fig. 2 (d), MP3 is turned off by EN signal generated by the NCL completion block as shown in Fig. 3, where a request-for-null (rfn) signal is asserted to the NCL completion block. That is, EN is changed from logic '0' to '1' right before NULL signals are asserted to the NCL circuits. The feedback inverter is needed to hold an output logic value, and the NAND gate is deployed to compensate for speed reduction due to the weak inverter feedback: the output switching time is reduced compared to the semi-static one because the output of the NAND gate is determined by Reset and Set block at the same time.

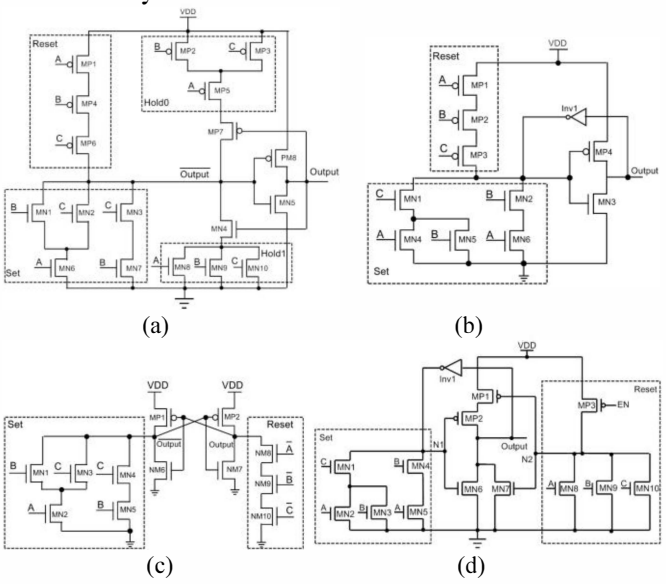

Fig. 2 CMOS implementation of (a) Static TH23, (b) Semi-static TH23, (c) Differential TH23 (d) Proposed TH23.

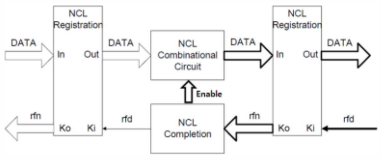

Fig. 3 Enable signal control using Completion signal.

Experimental Results

The proposed circuits have been designed and evaluated using a 0.11um MOSFET technology (VDD=1.2V). The topology has been compared to the classic static, semi-static, and differential topologies in terms of delay, area, and energy consumption using a 4x4 multiplier in Fig. 4 (a). As shown in Table 1, the simulation results show that the new topology offers faster operation and smaller area, with an increase in power. Although the power dissipation increases much more than other topologies due to the pseudo-NMOS structure, it is much smaller than other ones only if EN signal is turned off. Therefore, the average power dissipation is not much higher than expected. In case of the area overhead, the proposed NCL topology has the smallest area compared to other ones as expected because the Reset block in Fig. 2 (d) takes a very small area. Figure 4 (b) shows the layout of a 4x4 multiplier using the proposed NCL topology.

TABLE I
THE COMPARISON OF THE EXPERIMENTAL RESULTS WITH OTHER NCL GATES.

NCL topology	Power(W)	Delay(sec)	Area Overhead (normalized by Proposed NCL)
Static	1.39E-04	7.13E-10	1.50
Semi-static	1.75E-04	2.93E-09	1.25
Differential	2.32E-04	2.40E-09	1.28
Proposed (EN=ON)	4.38E-03	4.39E-10	1
Proposed (EN=OFF)	1.55E-06		

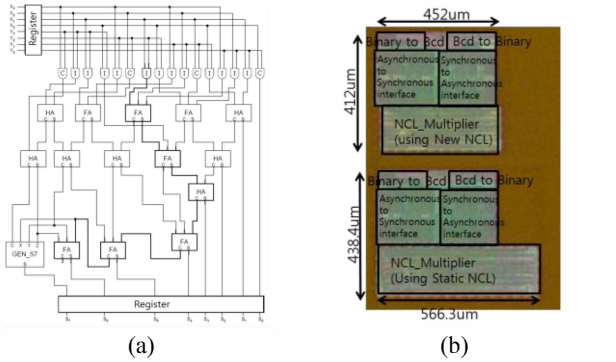

Fig. 4. (a) Block diagram of a 4x4 multiplier, (b) The layout of a 4x4 multiplier using the proposed NCL topology.

Conclusion

This paper proposes a new NCL topology for high-speed, low area overhead, and low wire complexity. The proposed topology is compared to the conventional static, semi-static, and differential topologies in terms of delay, area, and energy consumption using a 4x4 multiplier. As future work, we will improve the proposed NCL topology to reduce the static power consumption.

Acknowledgment

This work was supported by IC Design Education Center (IDEC).

References

[1] Scott C. Smith, Jia Di, "Designing Asynchronous Circuits using NULL Convention Logic (NCL)," Morgan & Claypool Publishers, 2009.

[2] F. A. Parsan, W. K. Al-Assadi, S. C. Smith, "Gate Mapping Automation for Asynchronous NULL Convention Logic Circuits," IEEE Trans. on VLSI Systems, Vol. 22, Issue 1, pp.99-112, Jan. 2014.

[3] S. Yancey and S. C. Smith, "A Differential Design for C-elements and NCL Gates," IEEE Int. Midwest Sym. on Circuits ans Systems (MWSCAS), pp.632-635, Aug. 2010.

[4] F. A. Parsan and S. C. Smith, "CMOS Implementation Comparison of NCL Gates," IEEE/IFIP Int. Conf. on VLSI and System-on_Chip (VLSI-SoC), pp.41-45, Oct. 2012.

[5] F. A. Parsan and S. C. Smith, "CMOS Implementation of Static Threshold Gates with Hysteresis: A New Approach," IEEE Int. Midwest Sym. on Circuits ans Systems, pp.394-397, Aug. 2012.