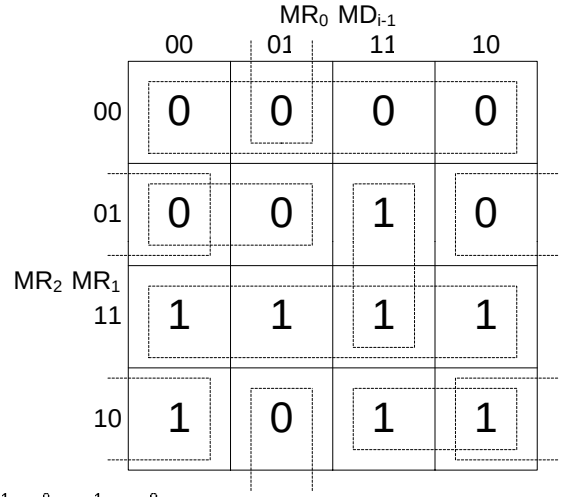
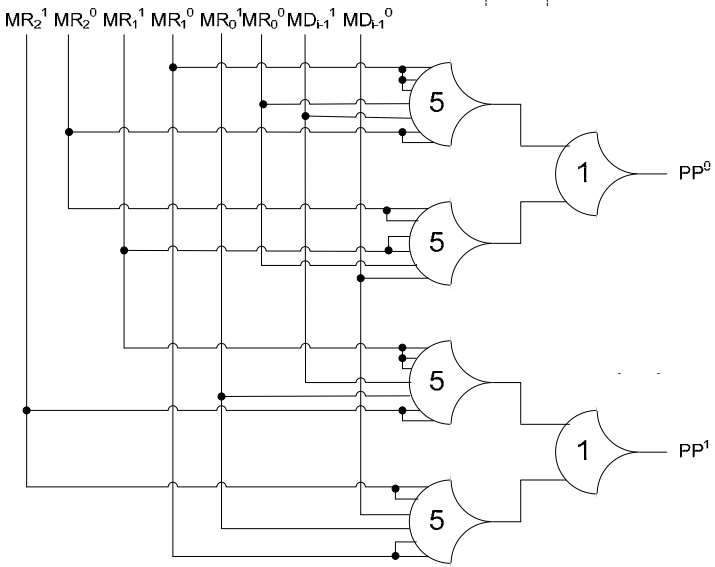
Dual-Rail Combinational Circuit Design

- *0s* refer to a signal's *rail*^{0} and *1s* refer to a signal's *rail*^{1}
- Add missing terms to ensure input-completeness
- Partition output equations into groups of four or fewer variables
  - largest number of product terms per group
  - smallest number of groups
  - map each group to one of the 27 NCL gates
- Booth2 PP generation component
  - input-complete with respect to input, MR_1
  - $PP^1 = MR_2^1MR_1^1 + MR_1^1MR_0^1MD_{i-1}^1 + MR_2^1MR_1^0MR_0^1 + MR_2^1MR_1^0MD_{i-1}^0$
  - $PP^0 = MR_2^0MR_1^0 + MR_1^0MR_0^0MD_{i-1}^1 + MR_2^0MR_1^1MR_0^0 + MR_2^0MR_1^1MD_{i-1}^0$





Optimized Logic Functions

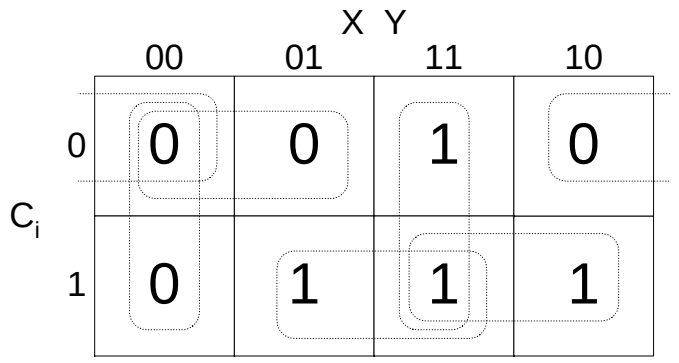
- AND: $Z^0 = X^0Y^0 + X^0Y^1 + X^1Y^0 \rightarrow$ THand0
  $Z^1 = X^1 Y^1 \rightarrow$ TH22

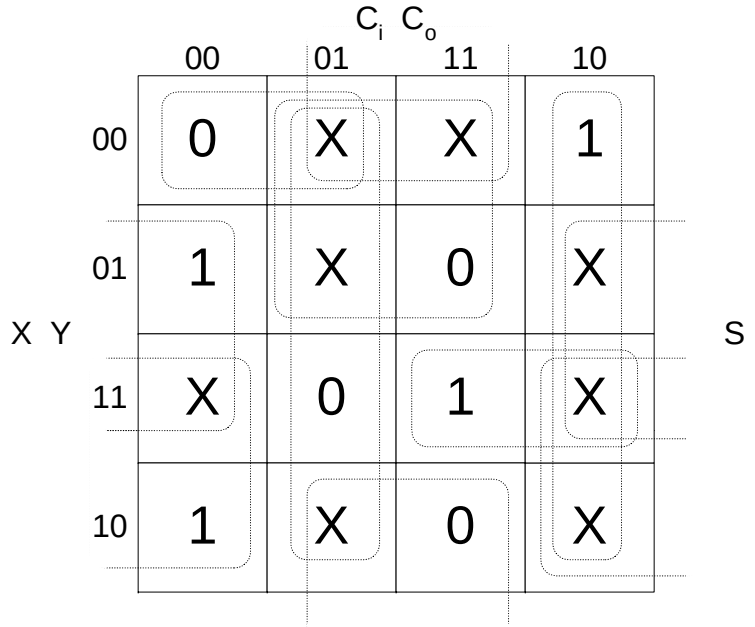
- OR: $Z^0 = X^0Y^0 \rightarrow$ TH22
  $Z^1 = X^1Y^1 + X^0Y^1 + X^1Y^0 \rightarrow$ THand0

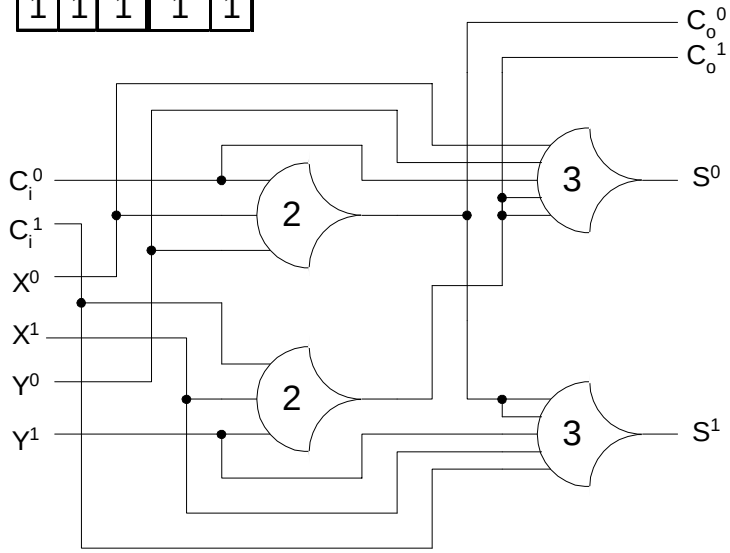
- XOR: $Z^0 = X^0Y^0 + X^1Y^1 \rightarrow$ THxor0
  $= X^0Y^0 + X^1Y^1 + X^0X^1 + Y^0Y^1 \rightarrow$ TH24comp
  $Z^1 = X^1Y^0 + X^0Y^1 \rightarrow$ THxor0
  $= X^1Y^0 + X^0Y^1 + X^0X^1 + Y^0Y^1 \rightarrow$ TH24comp

Optimal NCL Full Adder

X	Y	Ci	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1







$$C_o^0 = X^0Y^0 + C_i^0X^0 + C_i^0Y^0 \rightarrow TH23$$

$$C_o^1 = X^1Y^1 + C_i^1X^1 + C_i^1Y^1 \rightarrow TH23$$

$$S^0 = C_o^1X^0 + C_o^1Y^0 + C_o^1C_i^0 + X^0Y^0C_i^0 \rightarrow TH34W2$$

$$S^1 = C_o^0X^1 + C_o^0Y^1 + C_o^0C_i^1 + X^1Y^1C_i^1 \rightarrow TH34W2$$

- inherently input-complete
- check by expanding *S* in terms of *X*, *Y*, and C_i