NCL Low Power Design

As the transistor feature size continues scaling down into deep submicron (DSM) region, power consumption has long been a top design consideration. Since the supply voltage (V_{DD}) and threshold voltage (V_{TH}) are considerably reduced with transistor size, leakage power has been growing exponentially and has become the dominant power figure in DSM devices.

Among all leakage control and minimization techniques, Multi-Threshold CMOS (MTCMOS) has been widely adopted. MTCMOS incorporates transistors with two or more different threshold voltages in a circuit. Low threshold transistors offer fast speed but cost high leakage. In contrast, high threshold transistors suffer from reduced speed, but leak less current when turned off. MTCMOS combines these two types of transistors by utilizing low threshold voltage transistors for circuit switching to preserve performance and high threshold voltage transistors to gate the supply power when the circuit is idle (in sleep mode) in order to suppress the subthreshold leakage, as shown in Figure 1.

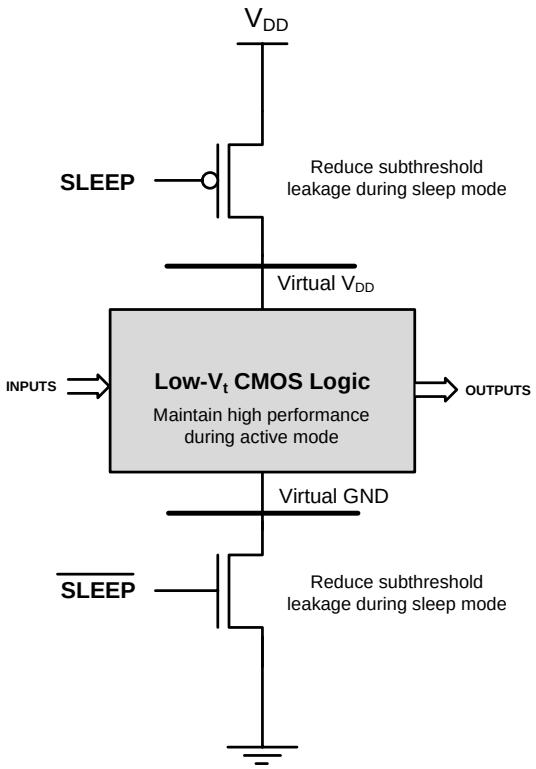

Figure 1: General MTCMOS Circuit Architecture

In general, three serious drawbacks hinder the widespread use of MTCMOS in synchronous circuits: 1) the generation of *Sleep* signals is timing critical, often requiring complex logic circuits; 2) synchronous circuits lose data when the power transistors are turned off; and 3) proper sizing of the sleep transistors is a very difficult task, which is critical for correct circuit operation. However, all these drawbacks can be eliminated by utilizing NCL in conjunction with the MTCMOS technique: 1) as shown in Figure 2, the combinational logic block in between two NCL registers goes to NULL, which is equivalent to sleep mode (i.e., all gate outputs become 0), when requested by the *Ko* signal from the subsequent register. Therefore, *Ko* signals naturally serve as inverted *Sleep* signals to their respective combinational logic blocks, without any additional hardware: if *Ko* is *request-for-NULL*, the circuit is in sleep mode; otherwise it is in active mode; 2) when a combinational logic block is in sleep mode, which is equivalent to a NULL cycle, its DATA output has already been latched by the following NCL register, indicated by the *Ko* signal becoming *request-for-NULL*. Therefore, no data will be lost during sleep mode; 3) the TCMOS method is incorporated into each NCL threshold gate, instead of the whole combinational logic block, which eases sizing the sleep transistors. Since NCL threshold gates are usually larger and more powerful than Boolean gates, the area overhead is reduced.

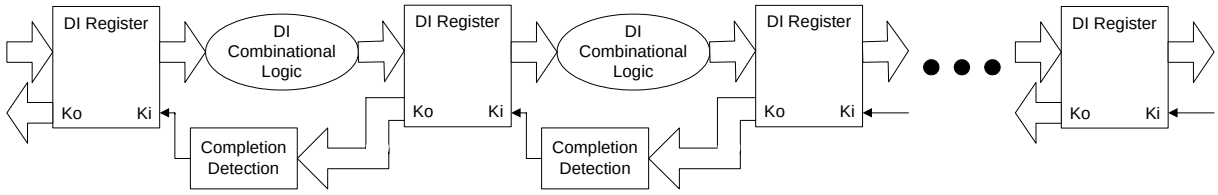

Figure 2: NCL System Architecture: input wavefronts are controlled by local handshaking signals and Completion Detection instead of by a global clock signal.

MTCMOS Threshold Gates

To incorporate MTCMOS in threshold gates, of the four functional blocks in each threshold gate, shown in Figure 3 (Go-to-NULL, Hold-NULL, Go-to-DATA, and Hold-DATA), the Go-to-NULL block can be removed because all threshold gates will be forced to enter sleep mode after each DATA state, which has the same effect as undergoing a NULL state, i.e., the output becomes logic zero; and the Hold-DATA block can also be removed because right after a DATA state, all threshold gates will enter sleep mode simultaneously, such that the NULL wavefront no longer propagates through the combinational logic. Hence, hysteresis is no longer needed. The resulting circuit is shown in Figure 4.

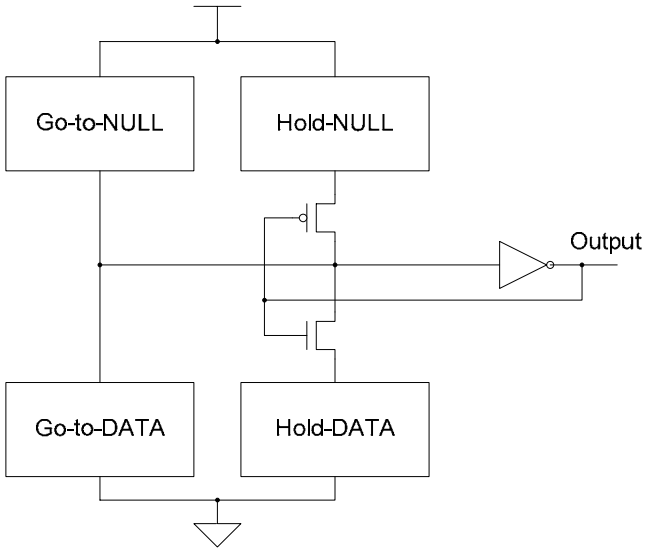

Figure 3: General Circuit Structure of NCL Threshold Gates

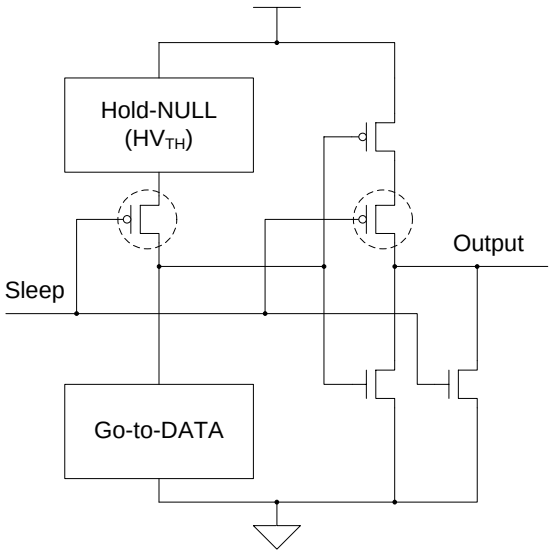

Figure 4: General Circuit Structure of MTCMOS NCL Threshold Gates (circled transistors are high-V_{TH})

In Figure 4, when *Sleep* signal is logic 0, the gate is in active mode. The Go-to-DATA block determines the output value. The circuit speed loss is insignificant since the Go-to-DATA block and the output inverter consist of low-V_{TH} transistors; when *Sleep* signal is logic 1, the gate goes to sleep mode. The low-V_{TH} NMOS sleep transistor at the output pulls the output low quickly, while the high-V_{TH} PMOS sleep transistors gate the leakage. The high-V_{TH} Hold-NULL block also helps with leakage reduction, while its slow speed will not affect the circuit behavior since the quick pull-down at the output overcomes the slow turn-on time of the Hold-NULL block. As an example, the original and MTCMOS TH23 gates are shown in Figure 5. In fact, multiple MTCMOS threshold gate designs can be achieved by evaluating the tradeoffs among active energy, leakage power, and speed.

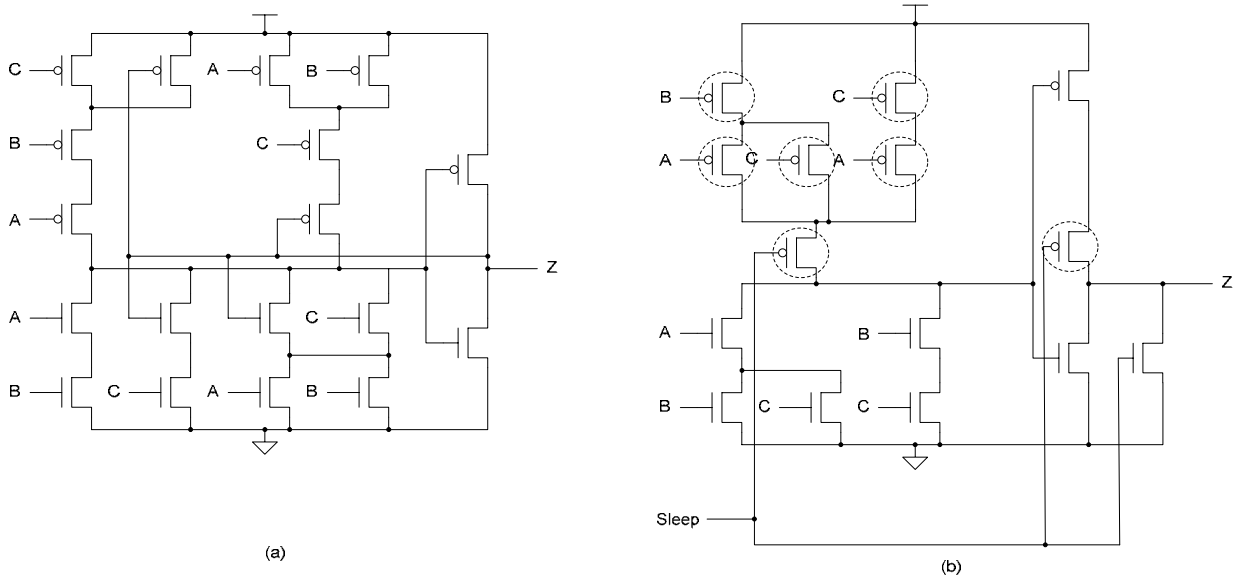

Figure 5: Static TH23 Gate (a) original version (b) MTCMOS version (circled transistors are high-V_t)

MTCMOS NCL Circuit Architecture

For the MTCMOS NCL circuit architecture, the standard NCL pipeline architecture, shown in Figure 2, needs to be slightly modified by utilizing the Early Completion technique, shown in Figure 6, in order to maintain delay-insensitivity. Otherwise, if the output of stage$_i$'s regular NCL completion component was used to sleep stage$_i$'s

combinational logic, all circuitry would become logic 0 whenever the completion component requested NULL, without first waiting for the circuit inputs to become NULL, as required for delay-insensitive signaling. Early Completion utilizes the inputs of register$_{i-1}$ along with the K_i request to register$_{i-1}$ to generate the request signal to register$_{i-2}$. Now this request signal to register$_{i-2}$ can be used to sleep the combinational circuitry in stage$_i$ without compromising delay-insensitivity, since stage$_i$ will only be put to sleep when both its inputs are NULL and it is requesting NULL.

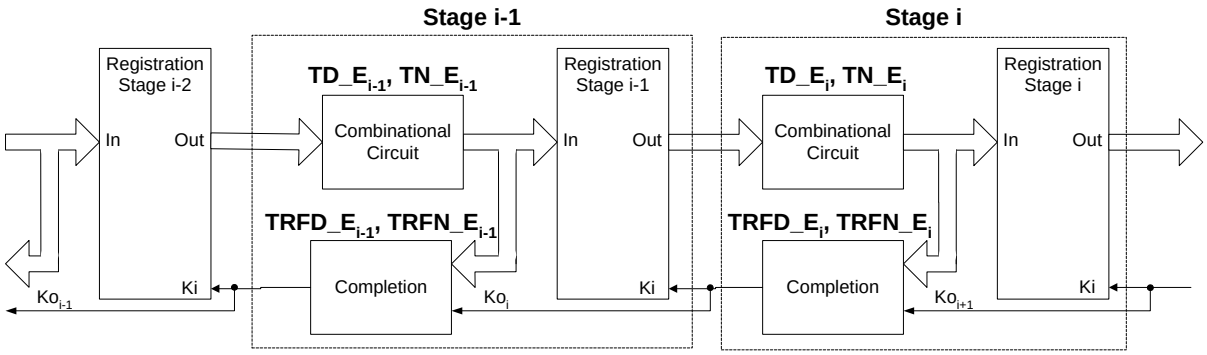

Figure 6: NCL Pipeline Utilizing Early Completion