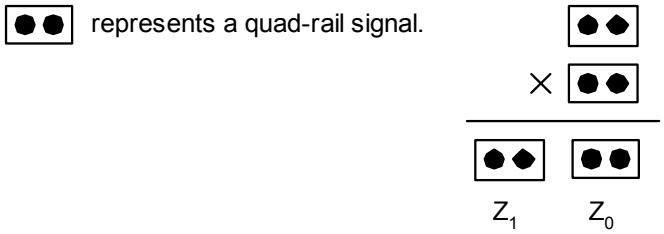
Quad-Rail Combinational Circuit Design

- *0s, 1s, 2s, 3s* refer to a signal's $rail^0$, $rail^1$, $rail^2$, $rail^3$, respectively
- Add missing terms to ensure input-completeness
- Partition output equations into groups of four or fewer variables
  - largest number of product terms per group
  - smallest number of groups
  - map each group to one of the 27 NCL gates
- Only 4-coverings can be utilized to eliminate a quad-rail signal from the corresponding product term
- Input order does not need to be rearranged like required for Boolean and dual-rail K-maps

Quad-rail PP Generation Component



Example: A = 2; B = 3 → Z1 = 1; Z0 = 2

PPH

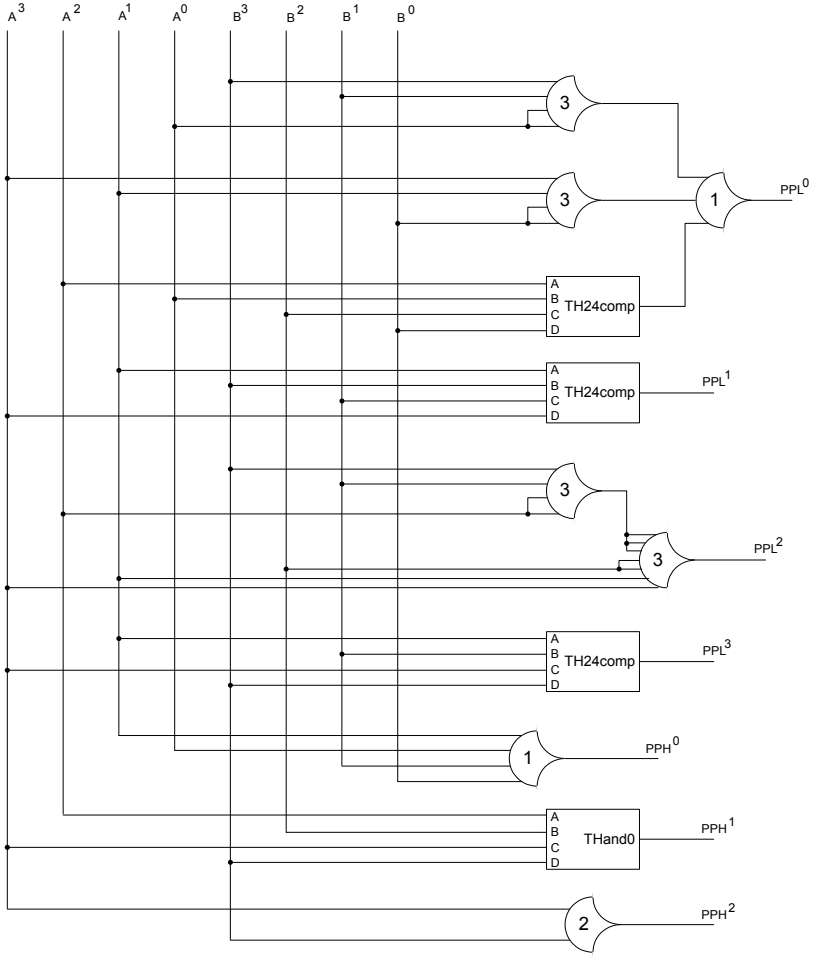
A \ B	0	1	2	3
0	0	0	0	0
1	0	0	0	0
2	0	0	1	1
3	0	0	1	2

PPL

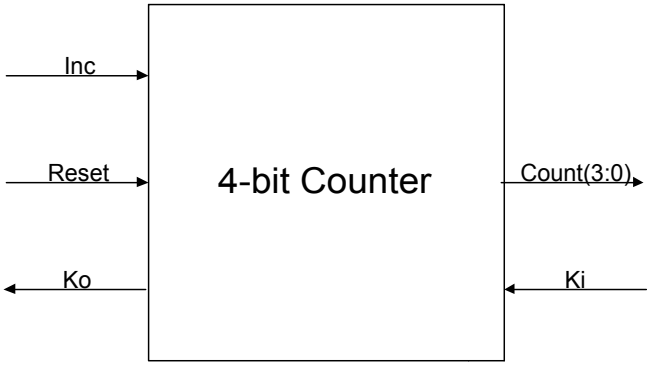
A \ B	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	0	2
3	0	3	2	1

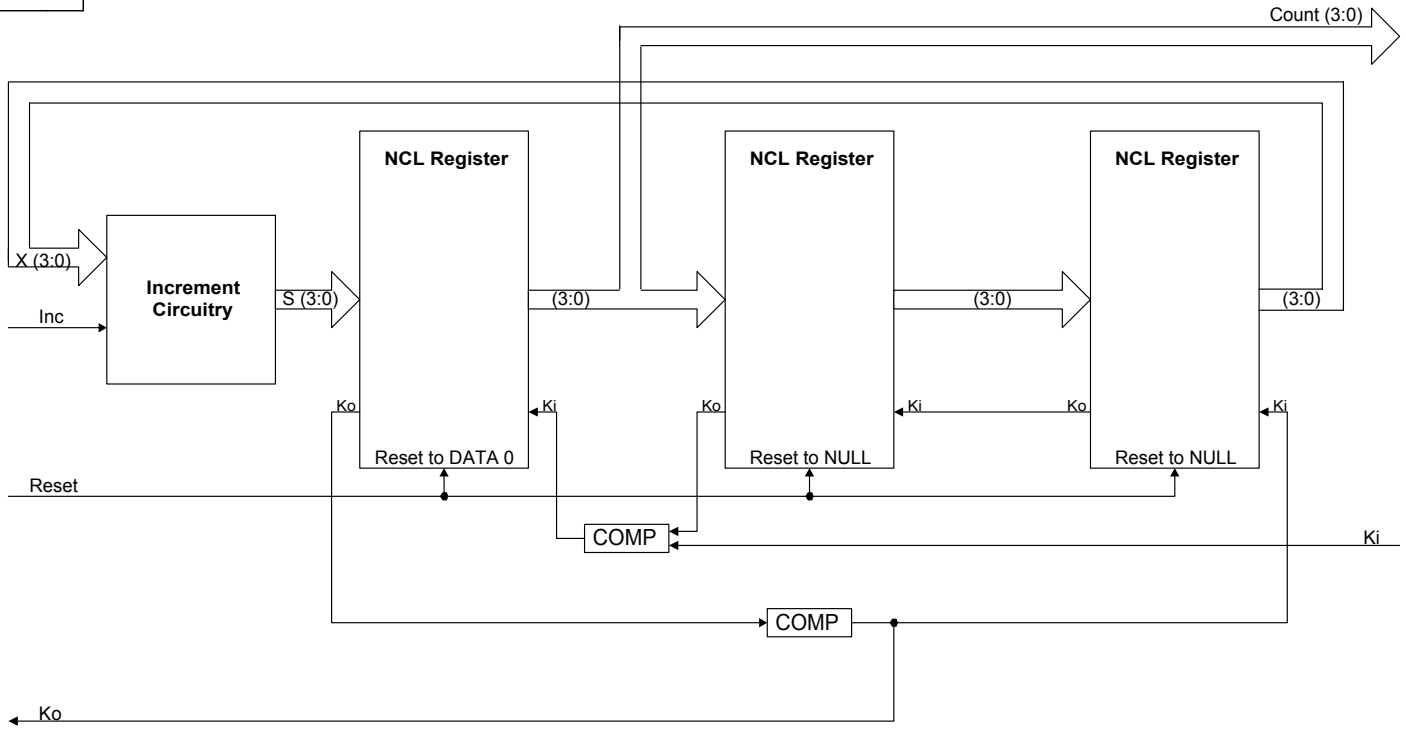
Optimized Quad-Rail PP Generation Component

- $PPL^0 = A^0 + B^0 + A^2B^2 = A^0\bullet(B^0 + B^1 + B^2 + B^3) + B^0\bullet(A^0 + A^1 + A^2 + A^3) + A^2B^2$
  $= A^0B^3 + A^0B^1 + A^3B^0 + A^1B^0 + A^2B^2 + A^2B^0 + A^0B^2 + A^0B^0$
- $PPL^1 = A^1B^1 + A^3B^3 = A^1B1 + A^3B^3 + A^1A^3 + B^1B^3$
- $PPL^2 = A^2B^1 + A^2B^3 + A^1B^2 + A^3B^2$
- $PPL^3 = A^1B^3 + A^3B^1 = A^1B^3 + A^3B^1 + A^1A^3 + B^1B^3$
- $PPH^0 = A^0 + A^1 + B^0 + B^1$
- $PPH^1 = A^2B^2 + A^2B^3 + A^3B^2$
- $PPH^2 = A^3B^3$



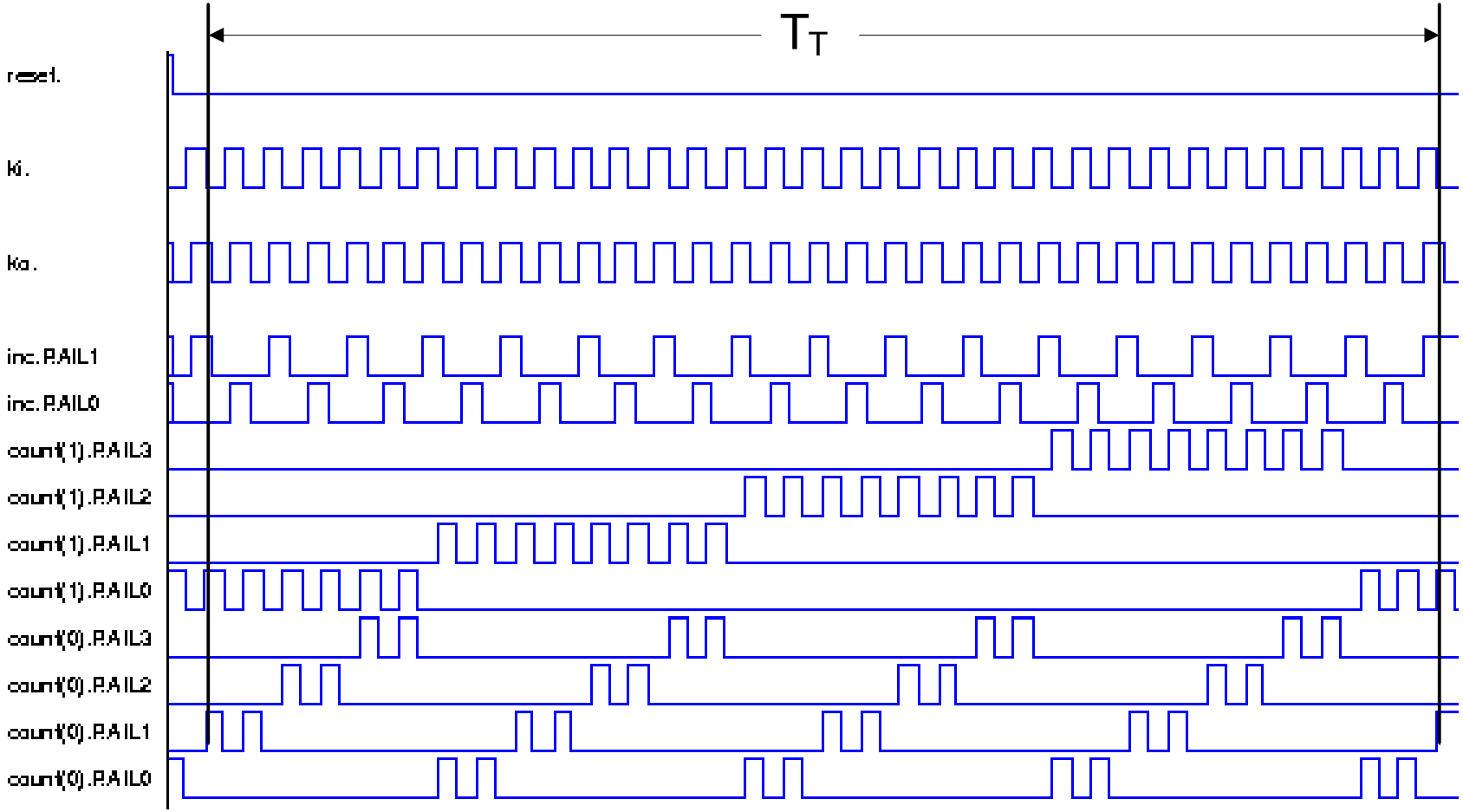
Counter Overview



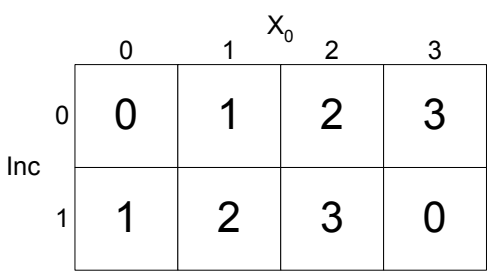


Quad-Rail Counter Waveforms

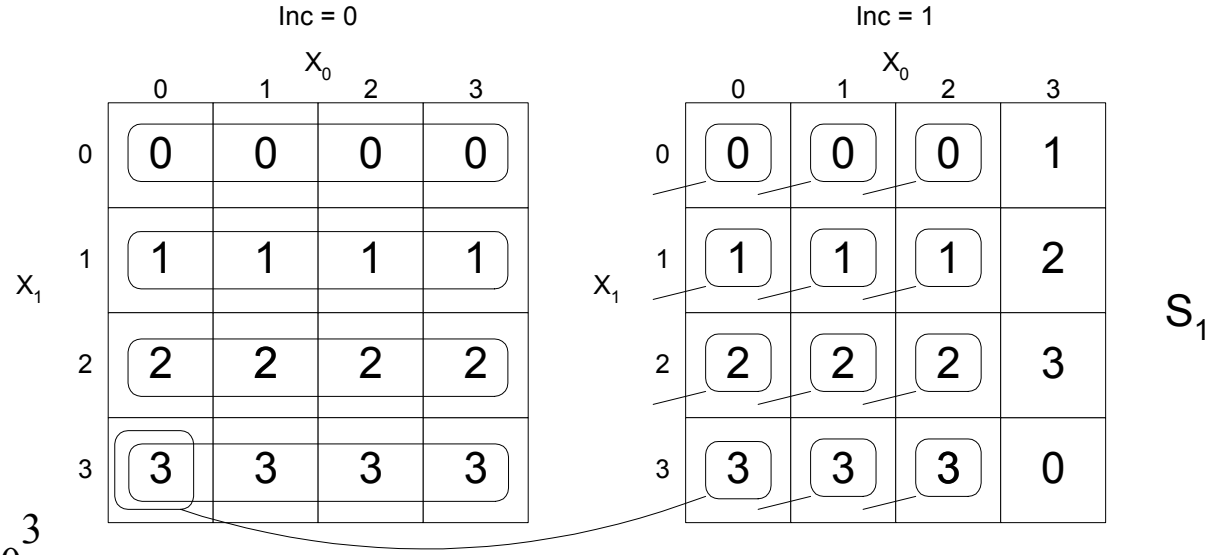
- There are 32 possible combinations of the 5 circuit inputs (i.e. $2^5 = 32$)
- Average DATA-to-DATA cycle time: $T_{DD} = T_T / 32$



Quad-Rail Increment Circuitry K-Maps



S_0



S_1

- $S_0^0 = Inc^0X_0^0 + Inc^1X_0^3$
- $S_0^1 = Inc^0X_0^1 + Inc^1X_0^0$
- $S_0^2 = Inc^0X_0^2 + Inc^1X_0^1$
- $S_0^3 = Inc^0X_0^3 + Inc^1X_0^2$
- $S_1^0 = Inc^0X_1^0 + X_0^0X_1^0 + X_0^1X_1^0 + X_0^2X_1^0 + Inc^1X_0^3X_1^3$
- $S_1^1 = Inc^0X_1^1 + X_0^0X_1^1 + X_0^1X_1^1 + X_0^2X_1^1 + Inc^1X_0^3X_1^0$
- $S_1^2 = Inc^0X_1^2 + X_0^0X_1^2 + X_0^1X_1^2 + X_0^2X_1^2 + Inc^1X_0^3X_1^1$
- $S_1^3 = Inc^0X_1^3 + X_0^0X_1^3 + X_0^1X_1^3 + X_0^2X_1^3 + Inc^1X_0^3X_1^2$

Optimized Quad-Rail Increment Circuitry

$$S_1^0 = X_1^0 \bullet (Inc^0 + X_0^0 + X_0^1 + X_0^2) + X_1^3 \bullet (Inc^1 X_0^3) + (Inc^0 + X_0^0 + X_0^1 + X_0^2) \bullet (Inc_1 X_0^3) + X_1^0 X_1^3$$

$$S_1^1 = X_1^1 \bullet (Inc^0 + X_0^0 + X_0^1 + X_0^2) + X_1^0 \bullet (Inc^1 X_0^3) + (Inc^0 + X_0^0 + X_0^1 + X_0^2) \bullet (Inc_1 X_0^3) + X_1^0 X_1^1$$

$$S_1^2 = X_1^2 \bullet (Inc^0 + X_0^0 + X_0^1 + X_0^2) + X_1^1 \bullet (Inc^1 X_0^3) + (Inc^0 + X_0^0 + X_0^1 + X_0^2) \bullet (Inc_1 X_0^3) + X_1^1 X_1^2$$

$$S_1^3 = X_1^3 \bullet (Inc^0 + X_0^0 + X_0^1 + X_0^2) + X_1^2 \bullet (Inc^1 X_0^3) + (Inc^0 + X_0^0 + X_0^1 + X_0^2) \bullet (Inc_1 X_0^3) + X_1^2 X_1^3$$

$$S_0^0 = Inc^0 X_0^0 + Inc^1 X_0^3 + Inc^0 Inc^1 + X_0^0 X_0^3$$

$$S_0^1 = Inc^0 X_0^1 + Inc^1 X_0^0 + Inc^0 Inc^1 + X_0^0 X_0^1$$

$$S_0^2 = Inc^0 X_0^2 + Inc^1 X_0^1 + Inc^0 Inc^1 + X_0^1 X_0^2$$

$$S_0^3 = Inc^0 X_0^3 + Inc^1 X_0^2 + Inc^0 Inc^1 + X_0^2 X_0^3$$