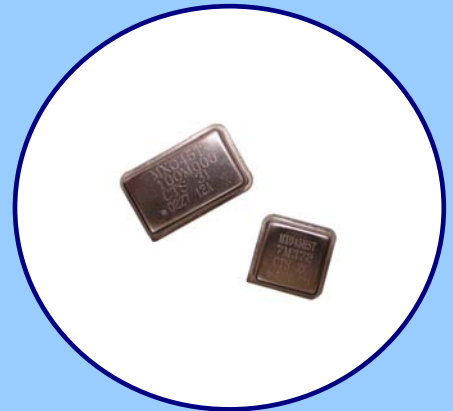# MXO45 & MXO45HS
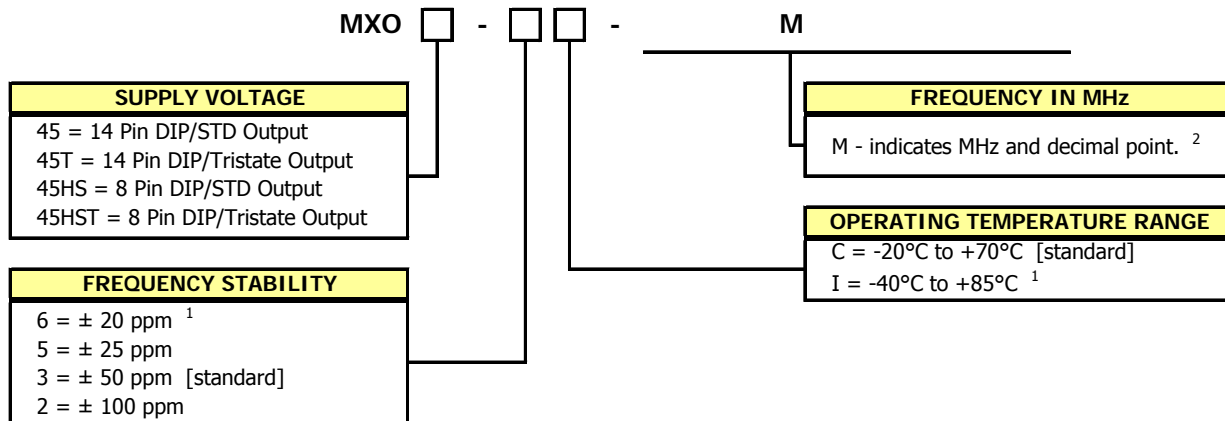## HCMOS/TTL Clock Oscillator

FEATURES
- **Standard 14 Pin or 8 Pin DIP Packages**
- **HCMOS/TTL Compatible Output**
- **Fundamental and 3rd Overtone Crystal Designs**
- Frequency Range 1 – 200 MHz
- Frequency Stability ±50 ppm Standard
- Operating Voltage +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Plastic Tray Packaging
- RoHS/Green Compliant (6/6)

APPLICATIONS
Applications for MXO45 and MXO45HS include microprocessors/DSP/FPGA, networking equipment, broadband access, storage area networks, computers and peripherals, test and measurement, Ethernet/Gigabit Ethernet.

ORDERING INFORMATION

MXO☐ - ☐☐ - ___ M

SUPPLY VOLTAGE
45 = 14 Pin DIP/STD Output
45T = 14 Pin DIP/Tristate Output
45HS = 8 Pin DIP/STD Output
45HST = 8 Pin DIP/Tristate Output

FREQUENCY STABILITY
6 = ± 20 ppm [1]
5 = ± 25 ppm
3 = ± 50 ppm [standard]
2 = ± 100 ppm

FREQUENCY IN MHz
M - indicates MHz and decimal point. [2]

OPERATING TEMPERATURE RANGE
C = -20°C to +70°C [standard]
I = -40°C to +85°C [1]

1] 6I Stability/Temperature combination is not available. Check availability for 6C combination.

2] Frequency is recorded with only leading significant digits before the 'M' and 4 - 6 significant digits after the 'M' (including zeros).
[Ex. XMXXXXXX (3M579545), XXMXXXXX (14M31818), XXXMXXXX (125M0000)]

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]
Product is packaged in plastic trays. Typical packaging format is as follows:

- 50 pcs./Plastic Tray.
  Tray size is approximately 180 x 136 x 18mm [LxWxH].

- 2 Trays per Anti-Static Bag [100 pcs.] or 10 Trays per Anti-Static Bag [500 pcs.].
  Bag height for 10 Trays is approximately 175mm.

- 1 anti-static bag per cardboard carton.

- Master-pack multiple cardboard cartons in a larger carton.
  8 cardboard cartons [10 trays per carton] is approximately 460 x 380 x 400mm [LxWxH].

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	+7.0	V
Storage Temperature	T_{STG}	-	-40	-	+100	°C
Frequency Range	f_O	-	1.0	-	200	MHz
Frequency Stability	$\Delta f/f_O$	See Note 1 and Ordering Information	-	-	20,25,50 or 100	± ppm
Aging	Δf	First year	-	3	5	± ppm
Operating Temperature Commercial Industrial	T_A	-	-20 -40	+25	+70 +85	°C
Supply Voltage	V_{CC}	±10%	4.5	5.0	5.5	V
Supply Current	I_{CC}	Frequency Range Tested load condition noted for typical values. 1.0MHz to 20MHz $\quad C_L$=50pF 20.001MHz to 40MHz $\quad C_L$=30pF 40.001MHz to 80MHz $\quad C_L$=30pF 80.001MHz to 125MHz $\quad C_L$=15pF 125.001MHz to 200MHz $\quad C_L$=15pF	- - - - -	10 20 30 40 55	26 40 60 70 80	mA
Output Load						
CMOS TTL	C_L	1.0MHz to 50MHz 50.001MHz to 80MHz 80.001MHz to 200MHz 1.0MHz to 200MHz	- - - -	- - - -	50 30 15 10	pF TTL
Output Voltage Levels Logic '1' Level Logic '0' Level	V_{OH} V_{OL}	CMOS Load 10 TTL LOAD CMOS TTL Load	90%V_{CC} 2.4 - -	- - -	- 10%V_{CC} 0.4	V
Output Current Logic '1' Level Logic '0' Level	I_{OH} I_{OL}	V_{OH} = 3.9V $\quad V_{CC}$ = 4.5V V_{OL} = 0.4V $\quad V_{CC}$ = 4.5V	- -	- -	-16 16	mA
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 10% - 90% Levels Tested load condition noted for typical values. 1.0MHz to 20MHz $\quad C_L$=50pF 20.001MHz to 80MHz $\quad C_L$=30pF 80.001MHz to 125MHz $\quad C_L$=15pF 125.001MHz to 200MHz $\quad C_L$=15pF	- - - -	8 5 2.5 -	10 8 5 2	ns
Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
Enable Function Enable Input Voltage Disable Input Voltage Enable Time Standby Current	 V_{IH} V_{IL} T_{PLZ} I_{ST}	Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled Pin 1 Logic '1' Pin 1 Logic '0', Output Disabled	2.0 - - -	- - - -	- 0.8 200 10	V ns µA
Period Jitter, Pk-Pk Period Jitter, RMS Phase Jitter, RMS	- - -	- - Bandwidth 12kHz - 20MHz	- - -	- - -	50 5 1	ps

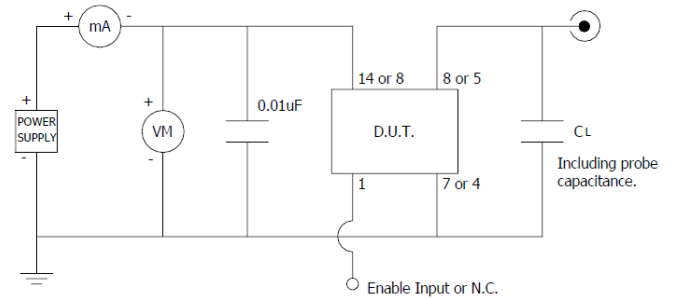*Left vertical label: ELECTRICAL PARAMETERS*

Notes:
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

ELECTRICAL CHARACTERISTICS

LVCMOS OUTPUT WAVEFORM

DUTY CYCLE = t/T x 100 (%)
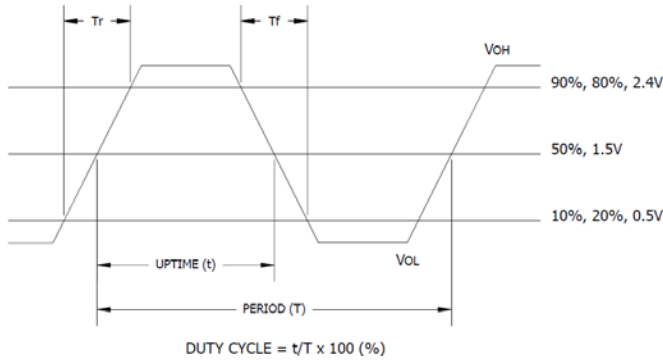
TEST CIRCUIT, CMOS LOAD

ENABLE TRUTH TABLE

PIN 1	PIN 5 or PIN 8
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input or No Connect
7 or 4	GND	Circuit & Package Ground
8 or 5	Output	RF Output
14 or 8	V_{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING
DIP-14
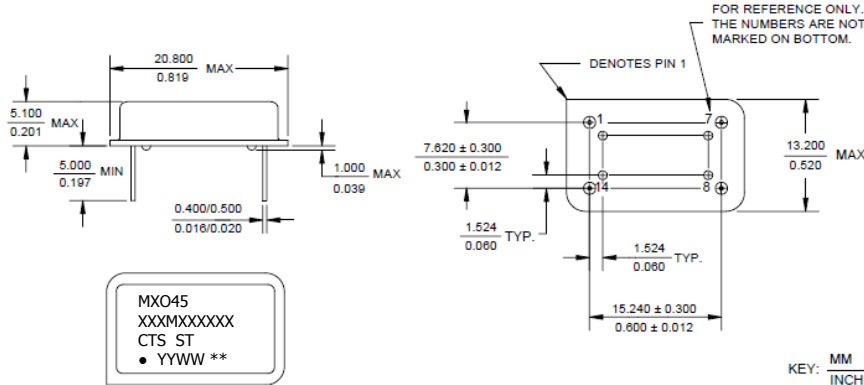
DIP-8

MARKING INFORMATION

1. Model Name:
   DIP-14 – MXO45 or MXO45T.
   DIP-8 – MXO45HS or MXO45HST.
2. XXXMXXXXXX – Frequency is marked with only leading significant digits before the 'M' and 4 – 6 digits after the 'M' (including zeros).
   Ex. XMXXXXXX [3M579545]
        XXMXXXXX [14M31818]
        XXXMXXXX [125M0000]
3. ST – Frequency stability/temperature code. [Refer to Ordering Information.]
4. YYWW – Date code, YY – year, WW – week.
5. ** – Manufacturing Site Code.

NOTES

1. Lead finish [e1], SnAgCu.
2. Reflow conditions per JEDEC J-STD-020, 260°C maximum.
3. Moisture Sensitivity Level 1, per JEDEC J-STD-020.