

# MCF5208 Reference Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5208 Reference Manual*, order number MCF5208RM. For convenience, the addenda items are grouped by revision. Please check our website at <http://www.freescale.com/coldfire> for the latest updates.

The current version available of the *MCF5208 Reference Manual* is Revision 0.1.

## 1 Errata for Revision 0.1

**Table 1. MCF5208RM Rev 0.1 Errata**

Location	Description
Section 1.3.16/Page 1-10	The DRAMSEL bit settings should be swapped. DRAMSEL = 0 for DDR mode, and DRAMSEL = 1 for SDR mode.
Table 2-1/Page 2-2	BE/BWE[3:0] for 144 LQFP should be "20, 48, 18, 50" instead of "18, 20, 48, 50"
Table 2-1/Page 2-5	Pin 33 for 144 LQFP package should be EVDD instead of SD_VDD.

Table 1. MCF5208RM Rev 0.1 Errata (continued)

Location	Description
Section 6.2.1/Page 6-2	<p>Add the following two notes:</p> <p><b>Note:</b> By default the RAMBAR is invalid, but the back door is enabled. In this state, any core accesses to the SRAM will be routed through the backdoor. Therefore the SRAM is accessible by the core, but it will not have a single-cycle access time. In order to insure that the core will have single-cycle access to the SRAM, the RAMBAR[V] bit should be set.</p> <p><b>Note:</b> Any access within the memory range allocated for the on-chip SRAM (0x8000_0000-0x8FFF_FFFF) will "hit" in the SRAM even if the address is beyond the defined size for the SRAM. This creates a ghosting effect for the on-chip SRAM memory. For example, writes to addresses 0x8000_0000 and 0x8000_8000 will actually modify the exact same memory location. System software should ensure that SRAM address pointers do not exceed the size of the SRAM in order to prevent unwanted overwriting of SRAM.</p>
Figure 6-1/Page 6-2	Change the reset value for the RAMBAR[BDE] bit from 0 to 1.
Chapter 9	Remove instances of D8 being used for reset configuration within chapter.
Section 9.2.2/Page 9-2	<p>Add the following note to the end of the section:</p> <p>"It is recommended that the logic levels for reset configuration on D[9,7:1] be actively driven when RCON is used. The rest of the data bus should either be allowed to float or be pulled high."</p>
Table 9-2/Page 9-2	Change reset value of RCON entry to 0x0201.
Figure 9-2/Page 9-3	Change last sentence in note to read "Default reset value ( $\overline{\text{RCON}}$ is not asserted) is 0x0201." instead of "Default reset value ( $\overline{\text{RCON}}$ is not asserted) is 0x0001."
Table 9-6/Page 9-6	Change default configuration entry for "Chip Select Configuration" row from "RCON9 = 0" to "RCON9 = 1".
Table 11-1/Page 11-2	Change Master Privilege Register entry's mnemonic from "MPR1" to "MPR".
Section 24.4.1.1/Page 24-17	Change first bullet from "An external clock signal on the DTnIN pin. When divided by the 16-bit divider, DTnIN provides an asynchronous clock, which can be further divided by a 1 or 16 prescaler." to "An external clock signal on the DTnIN pin. When not divided, DTnIN provides a synchronous clock; when divided by 16, it is asynchronous."
Figure 24-19/Page 24-17	Remove 16-bit divider blocks from both timer inputs, as it is not available when using an external clock source.
Section 24.4.1.2.2/Page 24-18	Change equation to: Baudrate = $f_{\text{ext}}/(16 \text{ or } 1)$ , since the 16-bit divider is not available when using an external clock source.

## 2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
0	<p>Initial release.</p> <ul style="list-style-type: none"> <li>Added pin 33 and <math>\overline{\text{BE/BWE}}</math> errata for 144 LQFP package.</li> <li>Added DRAMSEL errata.</li> </ul>	08/2005
0.1	<ul style="list-style-type: none"> <li>Added three UART external clock source 16-bit divider errata.</li> </ul>	08/2005

**Table 2. Revision History Table (continued)**

Rev. Number	Substantive Changes	Date of Release
0.2	<ul style="list-style-type: none"><li>• Added boot device table errata in CCM chapter.</li><li>• Added chip select configuration RCON9 reset value errata.</li></ul>	09/2005
0.3	<ul style="list-style-type: none"><li>• Rescinded errata for Table 9-6 “Boot Device” settings. The reference manual is correct.</li><li>• Added RAMBAR notes errata.</li><li>• Added RAMBAR[BDE] bit reset value errata.</li><li>• Added MPR1-&gt;MPR errata.</li><li>• Added D8 errata in Chapter 9</li><li>• Added RCON reset value in memory map errata.</li><li>• Added note in Section 9.2.2.</li></ul>	12/2005

## How to Reach Us:

### Home Page:

[www.freescale.com](http://www.freescale.com)

### E-mail:

[support@freescale.com](mailto:support@freescale.com)

### USA/Europe or Locations Not Listed:

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### Japan:

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064, Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2005. All rights reserved.

MCF5208RMAD  
Rev. 0.3  
12/2005