Product Change Notice

PCN 001

NetBurner Part Numbers: MOD5441X-100IR, MOD5441X-200IR
Implementation Date: July 19, 2013
Revision Number: 1.7

Description: J2 connector pin-out change to expose USB signals

Hardware Effectively:

The USB D+ and D- signals were not routed to the J2 50-pin header. To provide access to the USB signals, the third I2C port signals on J2-17 and J2-18 have been replaced with the USB D- (J2-17) and D+ (J2-18) signals. Selection of USB Host versus USB On the Go can be accomplished with resistor selection on the module. The default mode will be USB On the Go.

USB operation also requires an exact 60MHz clock. This can be provided 2 ways:

1. The USB_CLKIN input is shared with IRQ6 on pin J2-47, which will can be attached to a 60MHz oscillator.
2. The processor core can be slowed from 250MHz to 150MHz, which enables the processor PLL to divide evenly into 60MHz.

Signal Selection with Zero Ohm Resistors, Revision 1.9 and Later:

Revision 1.9 and later assemblies include 3 pairs of zero ohm resistors to select between USB Hose, USB Device and the earlier revision I2C2 signals.

J2.17 and J2.18 pin options. The net label for J2.17 is USB_N, and J2.18 is USB_P.

1. Default, USB Device, MOD54415-100IR, MOD54415-200IR
   J2.17 = USBO_N (A14)
   J2.18 = USBO_P (B14)
   Do not install: R37, R38, R80, R81
   Install: R35, R36

2. USB Host, MOD54415-100IR-USBH
   J2.17 = USBH_N (A15)
   J2.18 = USBH_P (B15)
   Do not install: R35, R36, R80, R81
   Install: R37, R38

3. I2C2, MOD54415-100IR-I2C2 (Compatible with PCB revision 1.6 configuration)

J2.17 = SSIO_RXD/I2C2_SDA (C12)
J2.18 = SSIO_TXD/I2C2SCL (C13)
Do not install: R35, R36, R37, R38
Install: R80, R81

Software Effectively:

Any application using the third I2C port will need to be modified to use a different I2C port.

PCN 002

NetBurner Part Numbers: MOD5441X-100IR, MOD5441X-200IR
Implementation Date: August 7, 2013
Revision Number: 1.8

Description:
Byte write steering signals *BE2 J1.9, and *BE3 J1.10 are incorrect when the external data bus is configured for 16-bits and 8-bit writes are attempted. Pin J1.9 has been changed from *BE2 to *BE1, and pin J1.10 has been changed from *BE3 to *BE0.

Note: On all other Freescale ColdFire platforms the correct byte steering signals for a 16 bit bus are *BE2 and *BE3. The MCF54415 processor is the first design with the signals reversed.

Description from the Freescale manual: *FB_BWE[3..0]: Byte Write Enable Signals

20.2.3 Byte Enables/Byte Write Enables (FB_BE/BWE[3:0])
When driven low, the byte enable (FB_BE/BWE[3:0]) outputs indicate data is to be latched or driven ontoa byte of the data bus. FB_BE/BWEn signals are asserted only to the memory bytes used during write accesses. A configuration option is provided to assert these signals on reads and writes (byte enable)or writes only (byte-write enable).

The FB_BE/BWEn signals are asserted during accesses to on-chip peripherals but not to on-chip SRAM or cache. For external SRAM or flash devices, the FB_BE/BWEn outputs must be connected to individual byte strobe signals.

Hardware Effectively:

Revision 1.8 or later modules are required for any designs using a 16-bit external bus that need to perform upper or low 8-bit writes.

Software Effectively:

None.

If you have any questions please contact our sales team at 858-558-0293.

Sincerely,

NetBurner Customer Service