MCF5208 Reference Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5208 Reference Manual*, order number MCF5208RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates.

The current version available of the *MCF5208 Reference Manual* is Revision 0.1.

1 Errata for Revision 0.1

Table 1. MCF5208RM Rev 0.1 Errata

Location	Description
Section 1.3.16/Page 1-10	The DRAMSEL bit settings should be swapped. DRAMSEL = 0 for DDR mode, and DRAMSEL = 1 for SDR mode.
Table 2-1/Page 2-2	$\overline{\text{BE}}$/$\overline{\text{BWE}}$[3:0] for 144 LQFP should be “20, 48, 18, 50“ instead of “18, 20, 48, 50”
Table 2-1/Page 2-5	Pin 33 for 144 LQFP package should be EVDD instead of SD_VDD.

Table 1. MCF5208RM Rev 0.1 Errata (continued)

Location	Description
Section 6.2.1/Page 6-2	Add the following two notes: **Note:** By default the RAMBAR is invalid, but the back door is enabled. In this state, any core accesses to the SRAM will be routed through the backdoor. Therefore the SRAM is accessible by the core, but it will not have a single-cycle access time. In order to insure that the core will have single-cycle access to the SRAM, the RAMBAR[V] bit should be set. **Note:** Any access within the memory range allocated for the on-chip SRAM (0x8000_0000-0x8FFF_FFFF) will "hit" in the SRAM even if the address is beyond the defined size for the SRAM. This creates a ghosting effect for the on-chip SRAM memory. For example, writes to addresses 0x8000_0000 and 0x8000_8000 will actually modify the exact same memory location. System software should ensure that SRAM address pointers do not exceed the size of the SRAM in order to prevent unwanted overwriting of SRAM.
Figure 6-1/Page 6-2	Change the reset value for the RAMBAR[BDE] bit from 0 to 1.
Chapter 9	Remove instances of D8 being used for reset configuration within chapter.
Section 9.2.2/Page 9-2	Add the following note to the end of the section: "It is recommended that the logic levels for reset configuration on D[9,7:1] be actively driven when RCON is used. The rest of the data bus should either be allowed to float or be pulled high."
Table 9-2/Page 9-2	Change reset value of RCON entry to 0x0201.
Figure 9-2/Page 9-3	Change last sentence in note to read "Default reset value ($\overline{\text{RCON}}$ is not asserted) is 0x0201." instead of "Default reset value ($\overline{\text{RCON}}$ is not asserted) is 0x0001."
Table 9-6/Page 9-6	Change default configuration entry for "Chip Select Configuration" row from "RCON9 = 0" to "RCON9 = 1".
Table 11-1/Page 11-2	Change Master Privilege Register entry's mnemonic from "MPR1" to "MPR".
Section 24.4.1.1/Page 24-17	Change first bullet from "An external clock signal on the DT*n*IN pin. When divided by the 16-bit divider, DT*n*IN provides an asynchronous clock, which can be further divided by a 1 or 16 prescaler." to "An external clock signal on the DT*n*IN pin. When not divided, DT*n*IN provides a synchronous clock; when divided by 16, it is asynchronous."
Figure 24-19/Page 24-17	Remove 16-bit divider blocks from both timer inputs, as it is not available when using an external clock source.
Section 24.4.1.2.2/Page 24-18	Change equation to: Baudrate = f_{extc}/(16 or 1), since the 16-bit divider is not available when using an external clock source.

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
0	Initial release. • Added pin 33 and $\overline{\text{BE/BWE}}$ errata for 144 LQFP package. • Added DRAMSEL errata.	08/2005
0.1	• Added three UART external clock source 16-bit divider errata.	08/2005

Table 2. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
0.2	• Added boot device table errata in CCM chapter. • Added chip select configuration RCON9 reset value errata.	09/2005
0.3	• Rescinded errata for Table 9-6 “Boot Device” settings. The reference manual is correct. • Added RAMBAR notes errata. • Added RAMBAR[BDE] bit reset value errata. • Added MPR1->MPR errata. • Added D8 errata in Chapter 9 • Added RCON reset value in memory map errata. • Added note in Section 9.2.2.	12/2005

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