Circuit Design for a Radiation Tolerant 2.4 GHz Synthesizer Based on COTS Components

Steffen Mueller[1], Andreas Och[1], Salvatore Danzeca[2], Rubén García Alía[2], Markus Brugger[2], Robert Weigel[1], and Alexander Koelpin[3]

[1]Friedrich-Alexander University of Erlangen-Nuremberg, Institute for Electronics Engineering, Cauerstr. 9, 91058 Erlangen, Germany, Email: ste.mueller@fau.de
[2]European Organization for Nuclear Research (CERN), CH-1211, Geneve 23, Switzerland
[3]Brandenburg University of Technology Cottbus-Senftenberg, Chair for Electronics and Sensor Systems, Siemens-Halske-Ring 14, 03046 Cottbus, Germany

***Abstract*— This paper presents a radiation tolerant integer-N phase-locked loop synthesizer based on commercial off-the-shelf components. The circuit features a tuning range from 2.24 GHz to 2.45 GHz and a phase noise of -82 dBc/Hz at 1 kHz offset. System level irradiation testing is conducted using high energy mixed-field radiation. First tests show excellent long-term stability of the circuit with no significant degradation up to an 1 MeV equivalent fluence of 8E+11 cmˆ-2.**

***Index Terms*— COTS, phase-locked loop, radiation effects, synthesizer, SEE, TID.**

I. Motivation

The deployment of commercial wireless technologies to the space radiation environment is a recent trend in the context of the Internet of Space (IoS) and for ”new space” applications [1], [2]. Typical scenarios address intra-satellite or intra-spacecraft communication and sensing. Besides that, research on radiation tolerant wireless links is also relevant for other radiation environments such as high energy physics, high altitude flights, fission or fusion reactors, and medical applications.

Frequency synthesis is a fundamental operation of wireless transceivers required during up- and down-conversion of radio frequency (RF) signals. The concept of phase-locked loop (PLL) is commonly used to derive a RF output signal from a precise local reference input [3]. According to Fig. 1, PLL represents a feedback control system comprising several elementary sub-circuits, namely phase detector (PD), loop filter (LF), voltage controlled oscillator (VCO), and frequency divider (DIV). Each of these sub-circuits is subject to radiation-induced degradation in terms of total ionizing dose (TID), displacement damage (DD), or single event effects (SEEs). These effects alter the signal fidelity at the PLL’s output through various failure signatures, e. g. frequency deviation, signal distortion, increased closed-loop noise, decreased output power, loss of lock, or temporarily stop of oscillation [4].

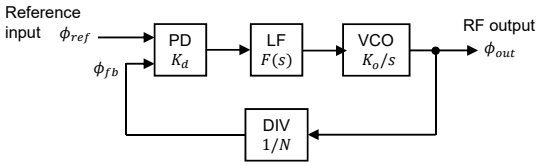

Fig. 1. Basic architecture and system level model of a integer-N phase-locked loop.

In the past, the majority of investigations stressed concepts for radiation hardening of application specific integrated circuit (ASIC) PLLs [4]–[8]. But less emphasis has been given to PLLs using commercial off-the-shelf (COTS) component technology. We present a design approach for a radiation tolerant 2.4 GHz PLL-based synthesizer using state-of-the-art COTS only.

II. Circuit Design

A. PLL Integration Levels

COTS PLLs are available at different integration levels. Fully integrated PLLs contain all building blocks (usually except LF) on a single integrated circuit (IC). These ICs feature superior performance but users barely have any flexibility to optimize these circuits regarding radiation tolerant design aspects. Few adaptions can be made through programming of internal control logic, but this portions of ICs are fairly susceptible to SEEs. Partially integrated PLLs refer to ICs that integrate at least two building blocks (typically PD together with DIV), thereby users have the possibility to choose from alternatives if a specific IC shows high susceptibility to radiation. Discrete ICs provide only one functionality on a dedicated chip. The user is responsible for both appropriate PLL design and circuit integration. Although the overall performance of discrete designs is inferior compared to fully integrated counterparts, the former approach are preferred as they

TABLE I
COMPARISON OF PLL INTEGRATION LEVELS.

Criterion	Fully integrated	Partially integrated	Discrete components
Signal fidelity	high	high	low
Functional performance	high	medium	low
Implementation effort	low	medium	high
Design flexibility	low	medium	high
Component diversity	high	medium	medium
Power consumption	low	medium	high
Testability	low	medium	high
Costs	low	medium	high

provide more degrees of freedom with respect to radiation tolerant circuit design and testing. Table I summarizes the pros and cons of different PLL integration levels with respect to radiation tolerant design perspective.

B. Circuit Architecture

A simple integer-N architecture is favored as it features the lowest complexity regarding the total number of active components which are likely to degrade. The RF output f_{out} is an integer multiple N of the reference input f_{ref} according to

$$f_{\mathrm{out}} = N \cdot f_{\mathrm{ref}}. \tag{1}$$

Choosing $f_{\mathrm{ref}} = 20\,\mathrm{MHz}$ and $N = 120$ yields an output of $f_{\mathrm{out}} = 2.4\,\mathrm{GHz}$ and a minimum tuning grid of 20 MHz. Fig. 2 shows the schematic of the PLL circuit design, where the resulting printed circuit board (PCB) is depicted in Fig. 3. For the sake of testability (see Section III) the reference signal is externally supplied instead of being sourced from a local oscillator (LO). Furthermore, the reference is passed through an on-board low-pass (LP) filter with a cut-off frequency of 83 MHz in order to suppress spurious signals at the PLL's input which could be unintentionally introduced by the test bed setup. For the final design the LO can be conveniently integrated on-board where the LP will be discarded then. A phase-frequency detector (PFD) with voltage output is preferred over charge pump (CP) type, since the latter are known to be considerably prone to SEEs when an energetic particle strikes a capacitive node of the CP [9]. In addition, voltage output PFDs provide an inherently larger pull-in range which is valuable to mitigate SEE induced offsets between f_{ref} and f_{fb}. The PFD's error signal outputs (UP, DN) are integrated using a PI-type loop filter in order to provide the DC tuning voltage for the VCO. Thanks to the active filter implementation using an operational amplifier (OPA), the tuning voltage can be individually adjusted to the tuning range of the VCO. The VCO is selected to have a small tuning gain K_o while covering the desired frequency range of 2.24 to 2.45 GHz. The smaller K_o the less the probability of frequency modulation of the VCO's output by a single event transient (SET) that

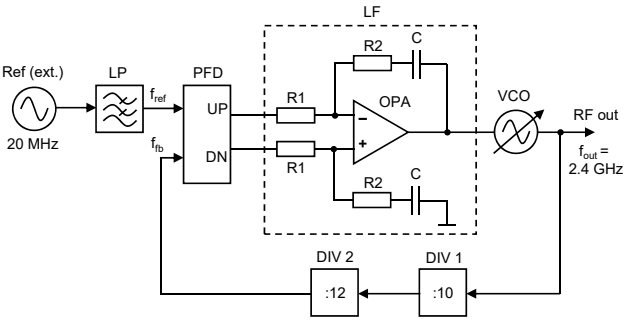

Fig. 2. Circuit architecture of the PLL.

Fig. 3. PCB of the synthesizer circuit (52 mm × 52 mm).

might occur at the OPA's output. Optional passive RC low-pass filtering could be applied subsequent to the OPA to mitigate SETs while filtering the inherent noise which is introduced by the OPA. However, the RC filter would add another pole to the system and even a parasitic pole could arise from the interaction with the input capacitance of the VCO, where both poles affect the loop stability. Since the OPA is low-noise type additional filtering was found to be not necessary. As no adequate frequency divider with a divider ratio of $N = 120$ could be identified, two identical lower order dividers were put in sequence within the feedback path. The overall divider ration calculates to $N = N_{\mathrm{DIV1}} \cdot N_{\mathrm{DIV2}}$. The divider ratio can be user-defined using static configuration pins at the corresponding ICs. Thanks to the discrete design approach, the overall circuit gets rid of any additional control logic that might be subject to single event upsets (SEUs). All aforementioned ICs were selected to feature gallium arsenide (GaAs) process technology, since GaAs devices are known to have superior TID and DD tolerance, while being immune to single event latchup (SEL) [10].

C. System Level Model and Noise Performance

The circuit architecture in Fig. 2 is directly related to the basic system level model given in Fig. 1. The PLL is mainly characterized by its closed-loop transfer function $H(s) = \phi_{\mathrm{out}}/\phi_{\mathrm{ref}}$ and the corresponding error transfer function $E(s) = \phi_{\mathrm{out}}/\phi_{\mathrm{fb}}$. Assuming the PLL is in linear

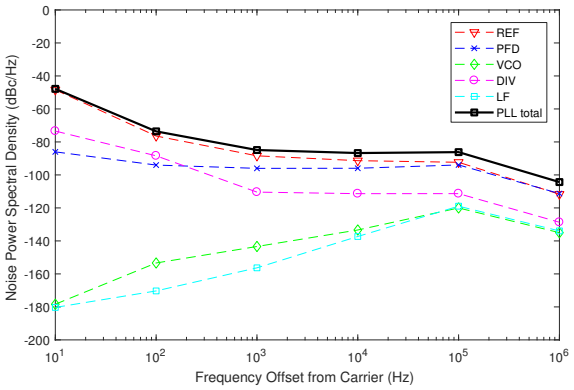

Fig. 4. Noise contribution by circuit component.

operation (locked state), $H(s)$ and $E(s)$ are given by

$$H(s) = \frac{K_d K_o F(s)/N}{s + K_d K_o F(s)/N} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2)$$

$$E(s) = 1 - H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3)$$

with

$$\zeta = \frac{\omega_n R_2 C}{2}, \qquad \omega_n = \sqrt{\frac{K_d K_o}{N R_1 C}} \quad (4)$$

$$\text{and} \quad F(s) = \frac{sR_2C + 1}{sR_1C}, \quad (5)$$

where ζ denotes the damping factor, ω_n the natural frequency, K_d the phase detector gain, K_o the VCO gain, and $F(s)$ the transfer function of the loop-filter [3]. $H(s)$ has low-pass characteristic for in-band noise which is dominated by the noise of the reference signal. $E(s)$ has high-pass characteristic that shapes the noise contribution of the VCO. Considering noise shaping of both $H(s)$ and $E(s)$, the optimum loop bandwidth for this circuit is located at about 100 kHz, since at this frequency PLL in-band noise and VCO noise are intersecting. A drawback of integer-N architecture is that the closed-loop gain amplifies in-band noise dependent on the divider ratio by the magnitude of $20 \log N$ that equals 41.6 dB for $N = 120$. Hence a trade-off is made between noise performance and frequency tuning step size. Fig. 4 depicts the noise contribution for all circuit components including the noise of the entire PLL circuit. It is clearly observable that the overall PLL noise performance for this experiment is limited by the noise contribution of the reference signal.

III. Experimental Results

A. Test Bed Setup

Radiation testing was conducted in a mixed-field radiation environment at CHARM facility at the European Organization for Nuclear Research (CERN). For a detailed facility description the reader is referred to [11]. Three synthesizer DUTs were irradiated at room temperature

TABLE II
HEH spectra content and hardness energies.

Cfg.	Composition				Hardness Energy (GeV)		
	n	p	$\pi^{\pm}$	k	H50	H10	H1
1	49.94	20.11	28.54	1.17	0.21	0.85	1.73
2	58.82	17.24	22.68	1.11	0.19	0.78	1.67

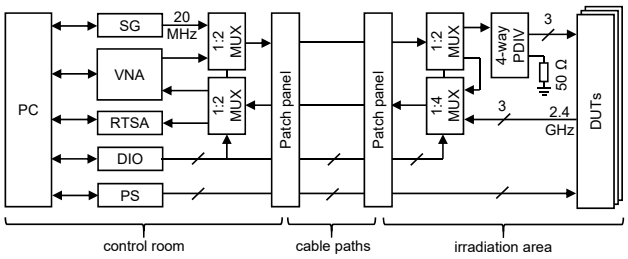

Fig. 5. Test bed setup used for irradiation at CHARM facility.

using two different configurations of high energy hadron (HEH) spectra according to Table II. All DUTs were equally fabricated ensuring same date and lot codes. The experiment was stopped after a total runtime of 147 h, corresponding to an 1 MeV equivalent fluence of $8 \cdot 10^{11}\,\mathrm{cm}^{-2}$ and an accumulated dose of 112 Gy. Instrumentation was performed according to the setup given in Fig. 5, which is a variant of our concept presented in [12]. This setup allows fully automated in-situ instrumentation of multiple DUTs.

B. Radiation Results

Fig. 6 shows the change of output frequency relative to the initial value at the start of the experiment. The standard deviation of the output frequency is about 6.3 Hz, where temporal drift is highly correlated between DUTs. It was verified that drift is not related to radiation. Instead the PLL followed the drift of the common 20 MHz input reference which was externally supplied by a signal generator (SG). The SG was subject to ambient temperature change in the control room. Nevertheless, the output frequency change is effectively small and well below measurement uncertainty.

Fig. 7 shows the change of output power relative to the initial value at the start of experiment. Again, the drift is highly correlated between DUTs. The two notches in the

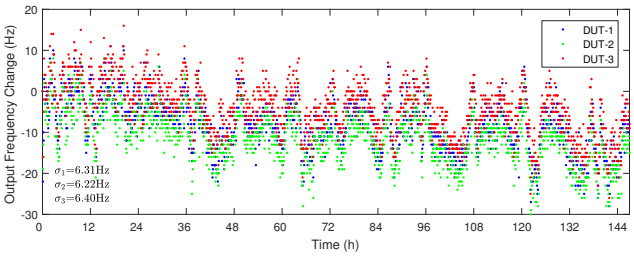

Fig. 6. Change of output frequency relative to its initial value.

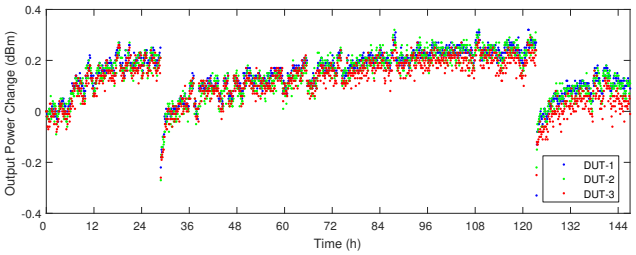

Fig. 7. Change of output power relative to its initial value.

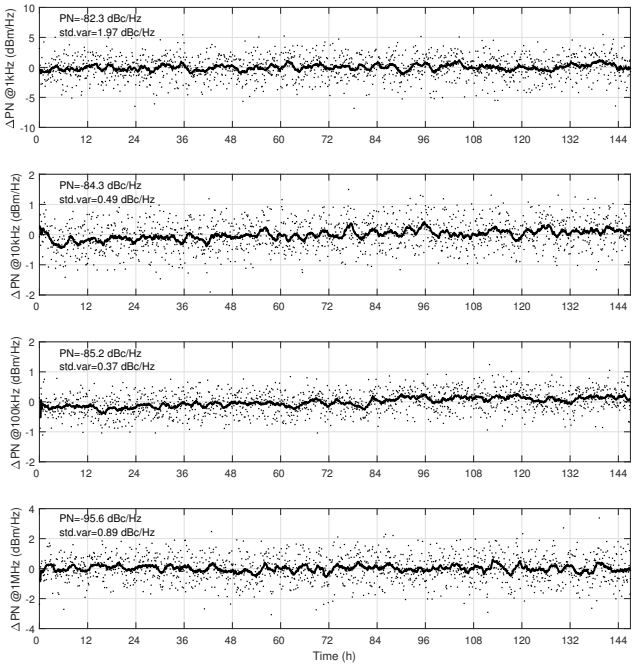

Fig. 8. Phase noise change of DUT-1 at different frequency offsets from carrier.

curve are expected to be an systematic error induced by the reference source. The output change is effectively small and well below measurement uncertainty.

Fig. 8 shows the change of phase noise at different offset from the carrier frequency for DUT-1. No significant increase of phase noise can be observed. The standard deviation of about 2 dBc/Hz at 1 kHz offset is considerably low. Taken all together, the circuit did not show any significant degradation of relevant circuit parameters. In addition, real-time spectrum analysis (RTSA) featuring event based frequency mask triggering (FMT) on the absolute location of the RF carrier was applied. It could be proofed that the PLL did not experience any detectable unlock state during the entire experiment runtime which could be attributed to SEE.

IV. Conclusion

Discrete COTS appear to be a reasonable approach for circuit level radiation hardening of a 2.4 GHz synthesizer. First test results using mixed-field irradiation did not show significant degradation of circuit parameters. Additional radiation tests are about to be prepared in order to derive the circuits upper radiation performance. The concept presented is in principal not limited to 2.4 GHz synthesizers.

References

[1] S. Xie, Xiong, Lee, G. X., K.-S. Low, and E. Gunawan, "Wireless sensor network for satellite applications: A survey and case study," *Unmanned Systems*, vol. 2, no. 3, pp. 261–277, 2014.

[2] H. J. Beestermöller, J. Sebald, M.-C. Sinnreich, H.-J. Borchers, M. Schneider, H. Luttmann, and V. Schmid, "Wireless-sensor networks in space technology demonstration on ISS," *12. Dresdner Sensor-Symposium*, pp. 99–102, 2015.

[3] P. V. Brennan, *Phase-Locked Loops: Principles and Practice*, 1st ed. McGraw-Hill, 1996.

[4] H. H. Chung, W. Chen, B. Bakkaloglu, H. J. Barnaby, B. Vermeire, and S. Kiaei, "Analysis of single events effects on monolithic PLL frequency synthesizers," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3539–3543, 2006.

[5] G. Lyons, W. G, T. Mellissinos, and J. Cable, "A high performance rad hard 2-3 GHz integer N CMOS phase lock loop," *IEEE Radiation Effects Data Workshop*, pp. 46–52, 1999.

[6] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, B. L. Bhuva, and W. T. Holman, "Towards SET mitigation in RF digital PLLs: From error characterization to radiation hardening considerations," *IEEE Transactions on Nuclear Science*, vol. 53, no. 4, pp. 2047–2053, 2006.

[7] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, R. A. Reed, D. McMorrow, J. S. Melinger, and P. Jenkins, "A single-event-hardened phase-locked loop fabricated in 130 nm CMOS," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2012–2020, 2007.

[8] Z. Chen, M. Lin, D. Ding, Y. Zheng, Z. Sang, and S. Zou, "Analysis of single-event effects in a radiation-hardened low-jitter PLL under heavy ion and pulsed laser irradiation," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 106–112, 2017.

[9] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, A. F. Witulski, and Y. Boulghassoul, "A hardened-by-design technique for rf digital phase-locked loops," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3432–3438, 2006.

[10] C. Claeys and E. Simoen, *Radiation Effects in Advanced Semiconductor Materials and Devices*. Springer, 2002.

[11] J. Mekki, M. Brugger, R. G. Alía, A. Thornton, Dos Santos Mota, N. C., and S. Danzeca, "CHARM: A mixed field facility at CERN for radiation tests in ground, atmospheric, space and accelerator representative environments," *IEEE Transactions on Nuclear Science*, vol. 63, no. 4, pp. 2106–2114, 2016.

[12] S. Mueller, S. Danzeca, R. G. Alía, M. Brugger, R. Weigel, and A. Koelpin, "Advanced in-situ instrumentation of RF circuits for mixed-field irradiation testing purpose," *European Conference on Radiation and its Effects on Components and Systems (RADECS)*, 2017 (to be published).