CubeSat Subsystem Interface Definition

CSID (Proposal)

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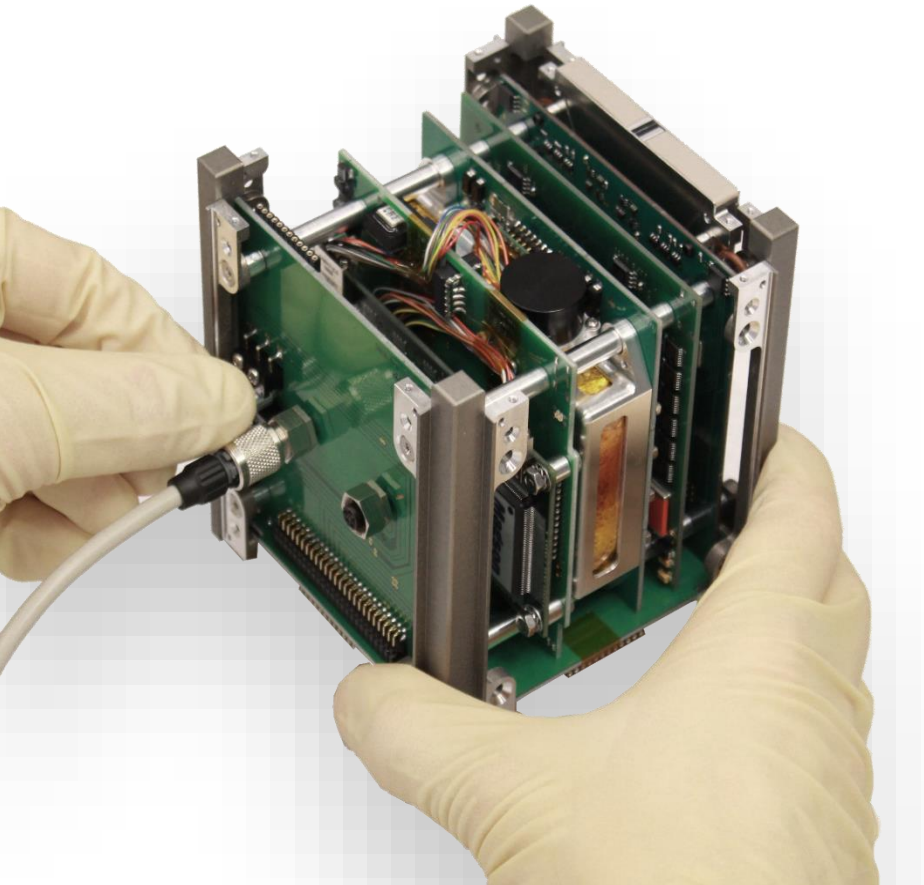

Change Log

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01.06.2015	0.3	SB	
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2 Introduction

The success of the CubeSats was based on standardization of geometric dimensions, allowing joint use of launcher adaptors. An important next step in order to be able to exchange boards at subsystem level would be a specification and standardization of the electrical interfaces, which is addressed in this contribution. There have been attempts in this direction, nevertheless the sometimes used PC104-approach was designed for completely different applications and is not very suitable and efficient for the CubeSat context. With the goal to promote a generic satellite platform related standardized electrical interfaces were realized at the UWE-3 mission, which accumulates in-flight experiences since November 2013. In order to be expanded to a suitable CubeSat standard related interface definitions are summarized in this contribution. The design has been optimized with respect to mass, size and energy efficiency while trying to maintain a modular and flexible architecture. Thus, the proposed bus supports robust and rapid development, integration and testing of the satellite as well as simple maintenance, extension and replacement of subsystems in any configuration during flat-sat development or flight model integration.

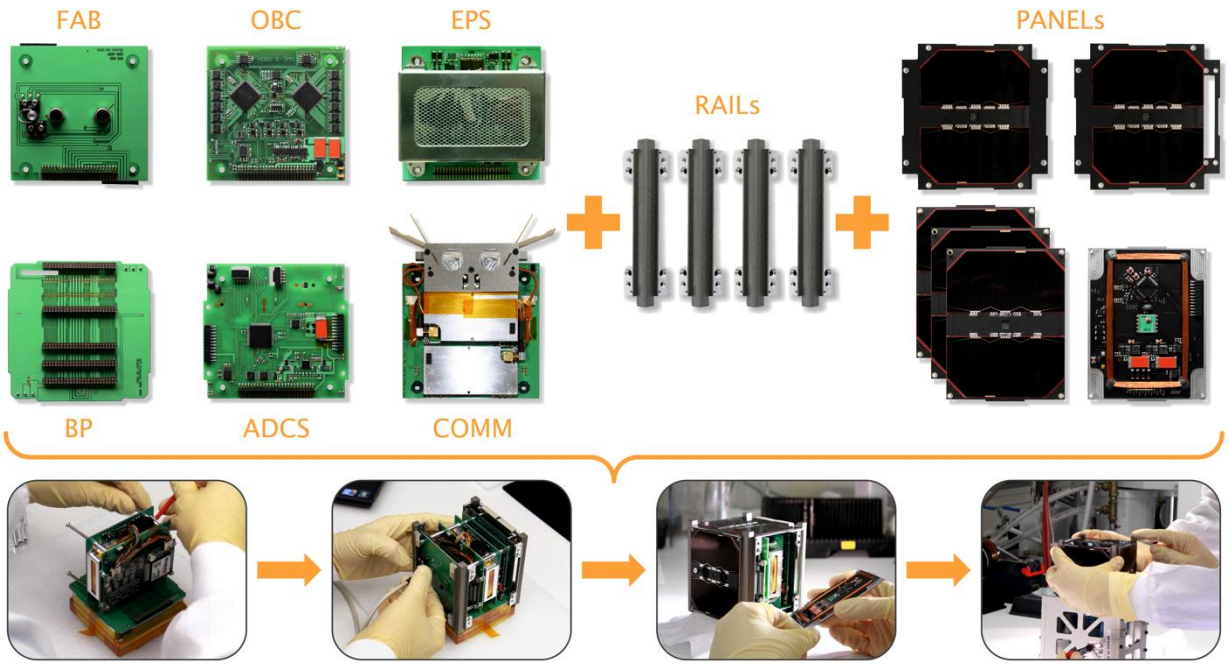

Figure 2.1: Overview of the modular UWE-3 pico-satellite bus
being optimized for rapid integration and testing.

3 Mechanical Interface Definition

A standardized backplane (BP+FAB) implements the entire harnessing. Subsystem boards and satellite side panels can be plugged to the backplanes subsystem bus interface and panel bus interface, whereas the panel bus represents a subset of the subsystem bus. The resulting electrical structure is fully functional, independent of any further structural component.

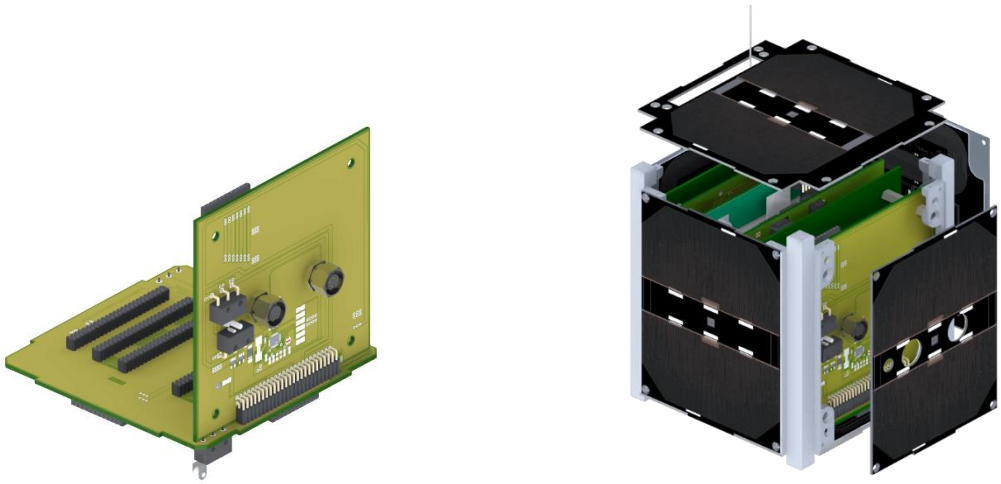

Figure 3.1: UWE-3 Backplane Concept for Subsystem Interconnection. FAB and BP (left), partially connected side panels (right).

The backplane implements a redundant set of deployment switches (kill switches) according to CDS[1] 2.3.2 while the front access board implements a backplane extension to provide umbilical line connectors (CDS 2.3.3) and redundant remove-before-flight switches (CDS 2.3.4). The umbilical line is divided in an analog interface for test activation and battery maintenance and a digital interface for software flashing, test and in-system debugging of the onboard computer.

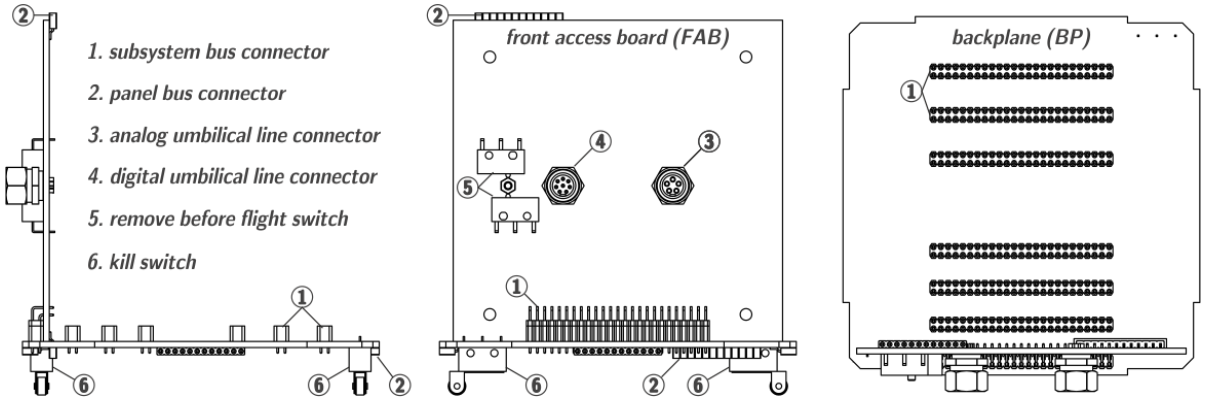

Figure 3.2: UWE-3 Backplane and Front Access Board with interfaces and deployment switches.

[1] CubeSat Design Specification, The CubeSat Design Program, Rev. 12, Cal Poly SLO

The mechanical layout of the backplane is typically adapted to the specific satellite configuration in order to allow desired spatial distribution and especially very compact placement of the subsystems inside the satellite. The electrical bus definition combines the power bus and the data bus and is described in chapter 0.

3.1 Dimensions

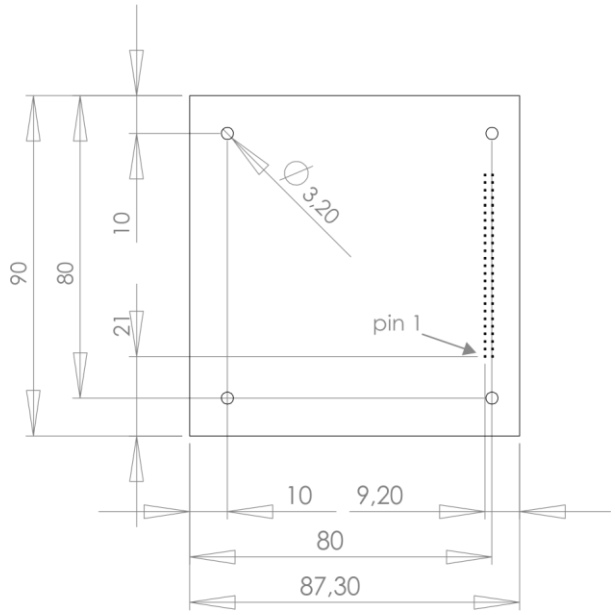

Figure 3.3: Subsystem layout and connector alignment [mm].

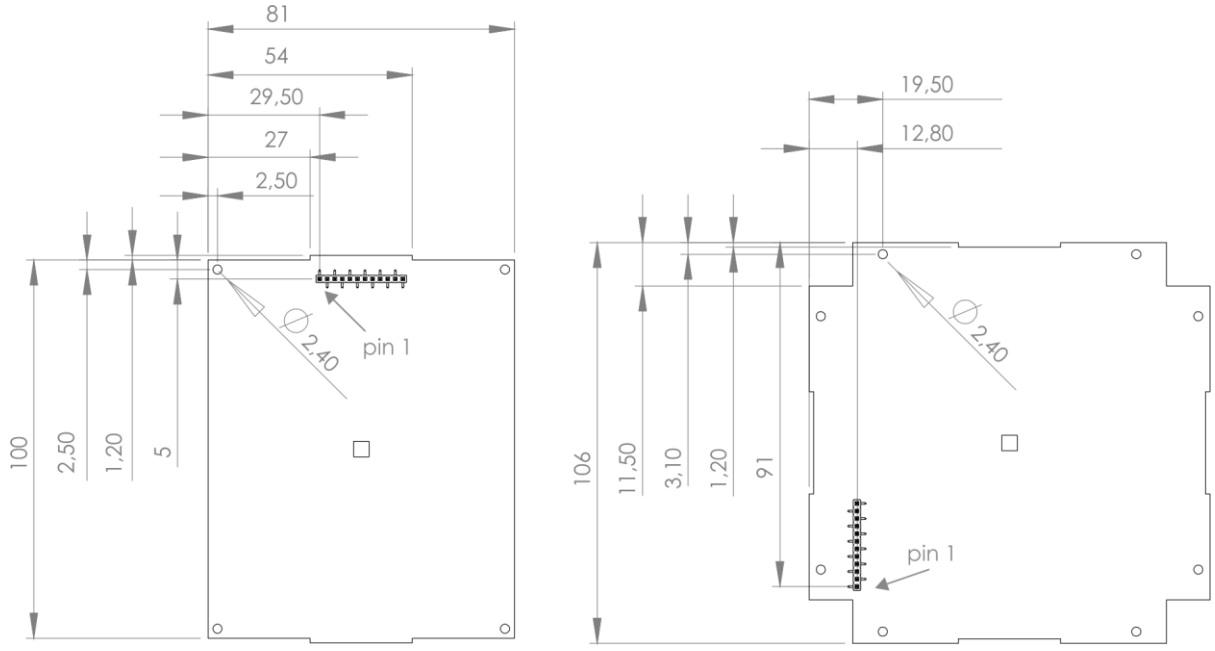

Figure 0.1: Panel layout and connector alignment [mm].

4 Electrical Interface Definition

The electrical interface is distributed in the standardized power bus and the data bus.

4.1 Power Bus

The UWE-3 electrical power system (EPS) foresees complete redundant power paths for generation, storage, and conversion. The EPS bases on a peak power tracking architecture with unregulated battery bus implemented in a distributed manner. The power generation block of the EPS is located on the satellite side panels which are connected to the panel bus in order to supply the unregulated battery bus. The power storage block is located on a dedicated subsystem attached to the subsystem bus. A master low side switch allows for global deactivation of all electrical components in order to comply with CDS 2.3.1, 2.3.2, 2.3.2.1, and 2.3.4.2.

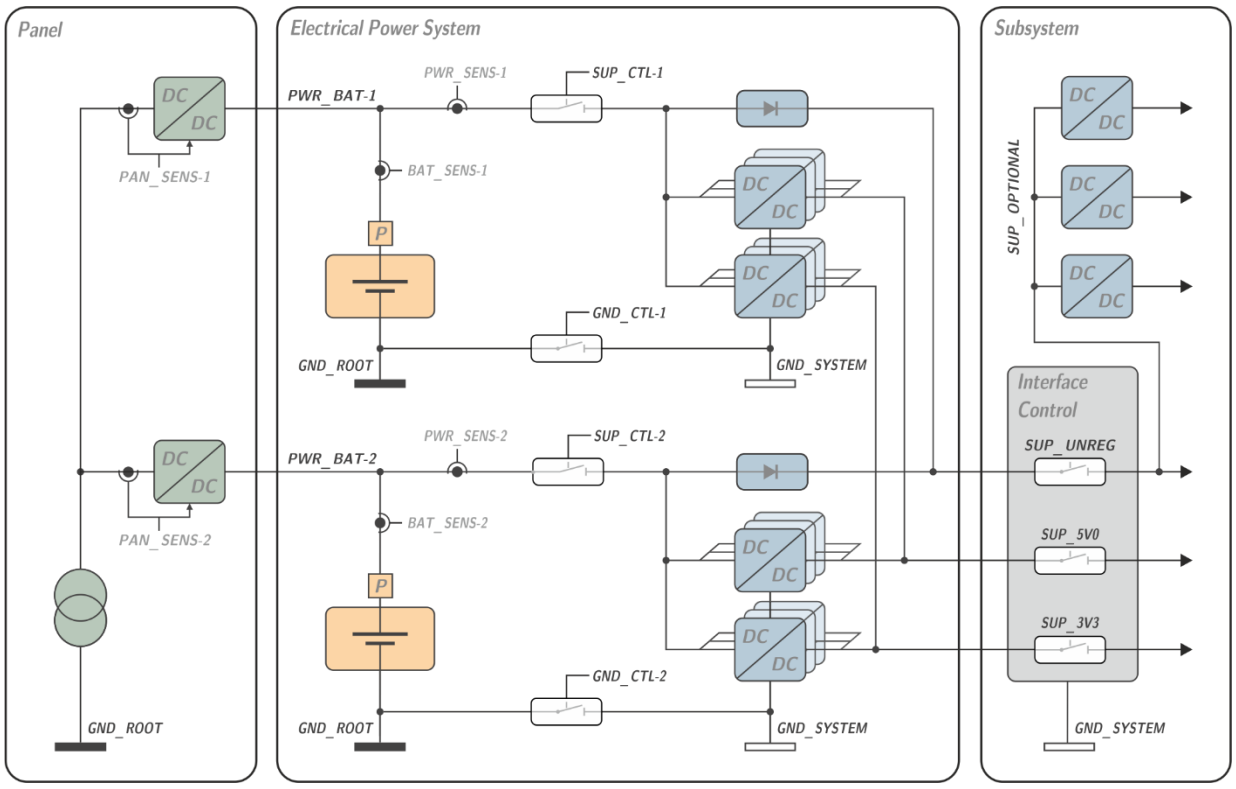

Figure 4.1: UWE-3 Distributed Electrical Power Concept.

Besides the unregulated battery bus also 3.3 V and 5 V power lines are available to the subsystems to be able to supply most common types of electrical components. The power buses are distributed to the subsystems via shared power lines on the backplane, while individual power switches with monitoring and protection circuits are directly located on the individual subsystem modules. This topology reduces the number of power lines required on the backplane and ensures that the power distribution capabilities scale with the number of subsystems, being always optimized to their individual requirements.

A standardized interface circuit, the so-called subsystem interface controller (SIC) is implemented on each subsystem of the satellite. Please contact UNISEC-Europe Office to obtain an electrical reference design.

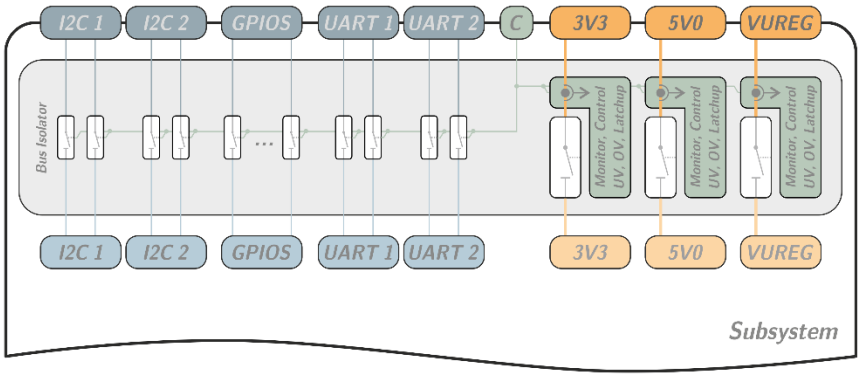

Figure 4.2: UWE-3 Subsystem Interface Control Circuit.

In order to ensure that a subsystem can be completely powered down while other subsystems connected to the backplane are still operating on shared data lines, the subsystem interface controller foresees electrical isolators for each relevant data signal used on a subsystem. Robust analogue switches with over-voltage and power-off protection guarantee that all data lines are high impedance when no power is supplied to the subsystem. Thus, it is ensured that no parasitic current paths, e.g. via standard CMOS ESD protection diodes, prevent the circuit from properly powering down or even cause permanent damage to the device.

4.1.1 Signal Description

System Ground and Global Deactivation Low-Side Switch	
GND_ROOT	Ground potential of power generating or storing devices. To be disconnected from GND_SYSTEM for storage and launch to comply with CDS 2.3.1, 2.3.2, 2.3.2.1, and 2.3.4.2. Subsystems must use GND_SYSTEM.
GND_SYSTEM	Global ground potential to be used by subsystems. Signal is floating during storage and launch.
GND_CTL-1	Redundant digital signals to control redundant ground bridge switches connecting GND_ROOT with GND_SYSTEM for testing and after satellite deployment. Signals driven by *Remove Before Flight Pin* and *Kill Switch* circitury accroding to CDS 2.3.2 and 2.3.4.
GND_CTL-2	

Power Path Source	
PWR_BAT-1	Direct access to redundant unregulated power buses for battery maintenance via umbilical line. Can be directly supplied by distributed peak power tracker on side panels.
PWR_BAT-2	
PWR_SC_X	Optional: Input for 3 central independent peak power tracking units. To be supplied by the solar panels.
PWR_SC_Y	
PWR_SC_Z	

Power Supply Buses	
SUP_3V3	3.3V common regulated bus combining both redundant power paths.
SUP_5V0	5.0V common regulated bus combining both redundant power paths.
SUP_UNREG	Common unregulated bus combining both redundant power paths.
SUP_BACKUP	Common unregulated bus (backup) combining both redundant power paths. Bus bypasses master switches of redundant power paths and is not affected during intentional power cycles initiated by asserting SUP_CTL-1 and SUP_CTL-1 simultaneously.
SUP_CTL-1	Redundant watchdog supervised digital control signals for individual deactivation of redundant power paths for maintenance or power cycles. Periodic signal change deactivates corresponding paths contributing to SUP_3V3, SUP_5V0, and SUP_UNREG. Simultaneous assertion initiates power cycle. For power path switch over simultaneous path activation has to be assured during transition. To be controlled by the OBC.
SUP_CTL-2	

4.2 Data Bus

UWE-3 data bus provides various signal lines for general subsystem control and communication such as redundant bidirectional communication buses, a subsystem programming interface, global reset and time synchronization. Crucial subsystems such as radio communication and electrical power have dedicated control and communication lines. Further dedicated signal lines allow OBC programming, in-system-debugging, test and checkout after integration via the satellites umbilical line.

4.2.1 Signal Description

General Subsystem Control	
BUS_I2C-1 (SDA)	Redundant I^2C interfaces for bidirectional data exchange among subsystems or direct access to remote I^2C devices (i.e. power monitors, temperature sensors). Subsystems might use the buses in multi-master mode for reception (subsystem is slave as default) and transmission (subsystem becomes master when required).
BUS_I2C-1 (SCL)	
BUS_I2C-2 (SDA)	
BUS_I2C-2 (SCL)	
BUS_JTAG (TDI)	Shared JTAG interface for subsystem software update via OBC. At maximum one JTAG device can be connected to the bus interface at a time. Per default the interface has to be disconnected by the standard subsystem interface control circuit.
BUS_JTAG (TDO)	
BUS_JTAG (TCK)	
BUS_JTAG (TMS)	
CTL_RESET	Global not-reset signal (low-active) driven by the OBC (default high).
CTL_SYNC	Global synchronization signal, driven by the OBC.
GPIO	General Purpose Input/Output Lines: UWE-3 OBC provides general purpose input/output lines with optional analog-digital converters or signal interrupt inputs for specific applications.
GPIO	
GPIO	
GPIO	
GPIO	

Special Subsystem Control: OBC Debug & Test Interface for Umbilical Line	
UML_UART (RXD)	Serial interface of the OBC for test and debug purpose during development, integration, test and checkout. Inactive in flight mode. Available on the digital interface of the umbilical line for checkout tests after integration in launch adapter.
UML_UART (TXD)	
UML_SBW-1 (TCK)	Spy-By-Wire interface for programming and in-system-debugging of the redundant OBC. Available on the digital interface of the umbilical line for software updates after integration in launch adapter.
UML_SBW-1 (TDIO)	
UML_SBW-2 (TCK)	
UML_SBW-2 (TDIO)	

Special Subsystem Control: Communication	
COM_UART-1 (RXD)	Redundant serial interfaces for dedicated one-2-one communication with the redundant radio communication subsystem.
COM_UART-1 (TXD)	
COM_UART-2 (RXD)	
COM_UART-2 (TXD)	
COM_IRQ	Dedicated interrupt request from redundant radio communication subsystem to indicate incoming frame.

4.3 Connector Layout

The following sections define the connector and pin layout of the individual interfaces.

4.3.1 Subsystem Interface Connector

The subsystem interface foresees double row high precision PCB connectors in the standard grid pattern 2.00mm (THT) with 50 pins.

Backplane Connector: female header (e.g. *BLY 2-50, female, Fischer Elektronik)*

Subsystem Module: male header *(e.g. SLY 4 035-50-Z, male, Fischer Elektronik)*

UML_UART (RXD)	1	2	UML_UART (TXD)
UML_SBW-1 (TDIO)	3	4	UML_SBW-1 (TCK)
UML_SBW-2 (TDIO)	5	6	UML_SBW-2 (TCK)
BUS_I2C-1 (SDA)	7	8	BUS_I2C-1 (SCL)
BUS_JTAG (TDI)	9	10	BUS_JTAG (TCK)
BUS_JTAG (TDO)	11	12	BUS_JTAG (TMS)
GND_SYSTEM	13	14	GND_SYSTEM
SUP_5V0	15	16	SUP_5V0
CTL_RESET	17	18	CTL_RESET
COM_UART-1 (RXD)	19	20	BUS_I2C-2 (SDA)
COM_UART-1 (TXD)	21	22	BUS_I2C-2 (SCL)
SUP_UNREG	23	24	SUP_UNREG
SUP_3V3	25	26	SUP_3V3
PWR_BAT-2	27	28	PWR_BAT-2
PWR_BAT-1	29	30	PWR_BAT-1
reserved (PWR_SC_Y)	31	32	reserved (PWR_SC_X)
reserved (PWR_SC_Z)	33	34	CTL_SYNC
GND_ROOT	35	36	GND_ROOT
GND_CTL-1	37	38	GND_CTL-2
SUP_BACKUP	39	40	SUP_BACKUP
SUP_CTL-1	41	42	SUP_CTL-2
General Purpose Input/Output	43	44	COM_IRQ
General Purpose Input/Output	45	46	General Purpose Input/Output
COM_UART-2 (TXD)	47	48	General Purpose Input/Output
COM_UART-2 (RXD)	49	50	General Purpose Input/Output

4.3.2 Panel Interface Connector

The panel bus is in principle a subset of the subsystem bus. The panel interface foresees single row high precision PCB connectors in the standard grid pattern 2.00mm (SMT) with 12 pins.

Backplane Connector: female header (e.g. *BLY 6 SMD/ 12, Fischer Elektronik)*

Panel Connector: male header (e.g. *SLY 7 SMD/ 045/ 12 G, Fischer Elektronik)*

GND_SYSTEM	1
SUP_5V0	2
CTL_RESET	3
BUS_I2C-2 (SDA)	4
BUS_I2C-2 (SCL)	5
SUP_UNREG	6
SUP_3V3	7
PWR_BAT-2	8
PWR_BAT-1	9
reserved (PWR_SC)	10
CTL_SYNC	11
GND_ROOT	12

4.3.3 Umbilical Line Connector

GND_SYSTEM	1
GND_CTL-1	2
GND_ROOT	3
PWR_BAT-1	4
PWR_BAT-2	5

GND_SYSTEM	1
UML_UART (RXD)	2
UML_UART (TXD)	3
UML_SBW-1 (TDIO)	4
UML_SBW-1 (TCK)	5
UML_SBW-2 (TDIO)	6
UML_SBW-2 (TCK)	7

5 Conclusions

This document outlines an efficient electrical interface standard for CubeSats (including data and power lines), exhibiting the potential for increased exchange at subsystem board level within the CubeSat community.

6 Contact

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