Hailan Zhang Shanbhag

Email: <u>hailan.shanbhag@epfl.ch</u> Website: <u>hailanshanbhag.github.io</u>

Address: BC 118 Chem. Alan Turing 1015 Ecublens, VD

Area of Interest: Wireless sensing and communications, environmentalism

Education

École polytechnique fédérale de Lausanne

January 2023 – *present*

Ph.D., Computer and Communication Sciences

Advisor: Haitham Hassanieh

University of Illinois at Urbana-Champaign

August 2021 – December 2022

Master of Science, Electrical and Computer Engineering

GPA: 4.0./4.0

Advisor: Haitham Hassanieh

University of Illinois at Urbana-Champaign

August 2017 - May 2021

GPA: 3.8./4.0

Bachelor of Science, Computer Engineering

Skills

Languages: Python, MATLAB, C/C++, Verilog/SystemVerilog, x86 Software/Frameworks: Eagle, KiCad, mmWave Studio, CUDA

Spoken Languages: English, Mandarin Chinese

Research Experience

Graduate Research Assistant

August 2021 – December 2022

EPFL/UIUC, Prof. Haitham Hassanieh

Contactless Material Sensing with mmWave

• Created a system with Texas Instruments 77 GHz mmWave radar boards and applying machine learning techniques to accurately classify materials and objects.

Interference Mitigation

Validating and running simulations for various radar interference mitigation techniques.

Senior Research Project & Thesis

August 2020 - May 2021

UIUC, Prof. Haitham Hassanieh

- Calibrated four 60 GHz Qualcomm phased array antennas to construct a 12x12 MIMO array for both a transmitter and receiver (hardware acquired from the M-Cube project of UCSD).
- Measured beam patterns of the transmitter and receiver radios and prepared the hardware for future applications.

Undergraduate Research Assistant

May 2018 – May 2019

UIUC, Prof. Viktor Gruev

- Designed and fabricated a PCB for a Hamamatsu CMOS area image sensor realizing lownoise multi-spectral imaging for image-guided surgery and underwater polarization imaging.
- Began programming XEM7310 OpalKelly FPGA in Verilog to communicate with and process LVDS pixel data received from the image sensor.
- Communicated to the FPGA using OpalKelly's FrontPanel C++ API to interface through a PC.

Honors & Awards

Promise of Excellence Fellowship TI Women STEM Stars Scholarship $August\ 2021-May\ 2022$

August 2017 - May 2021

Relevant Coursework

Random Processes, Signal Processing, Digital Communications, Wireless and Communication Networks, Machine Learning

Internships & Activities

Silicon Verification Intern

June 2019 – August 2019

Sunnyvale, CA, Microsoft

- Enhanced a UVM based verification IP by providing support for OCP VIPs.
- Created a translation layer from the AXI protocol to the OCP protocol, which was integrated into an inhouse verification IP.
- Integrated part of the translation layer via fully synthesizable code to reuse an inhouse AXI slave.