Lab4

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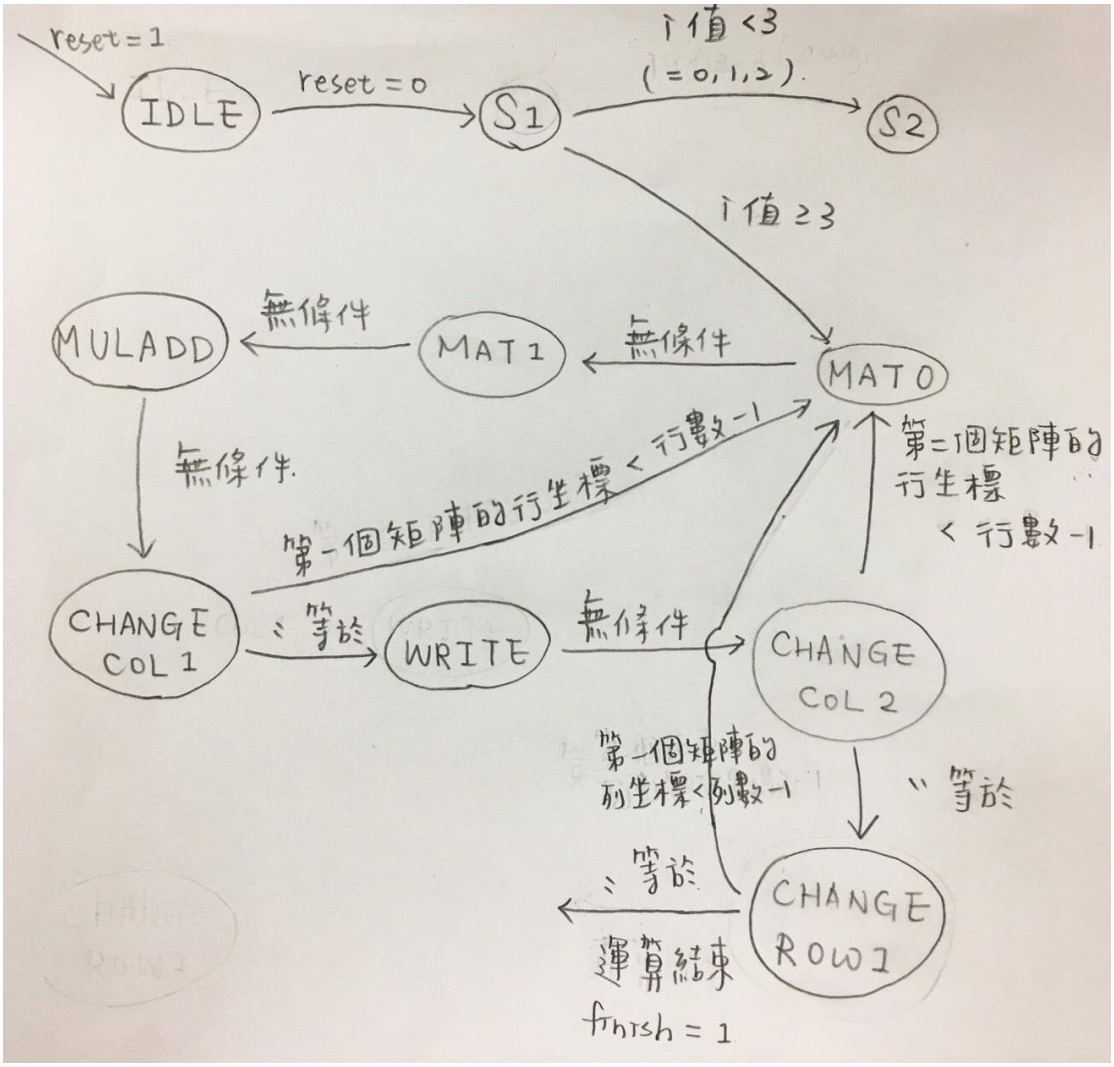
- State Trasition Graph



IDLE: reset=1 時，回到的初始 state。

S1: 將 read、write 都設為 1，i 分別等於 0、1、2，經由 read_data 讀取矩陣的行數列數。

S2: 讓 i=i+1。

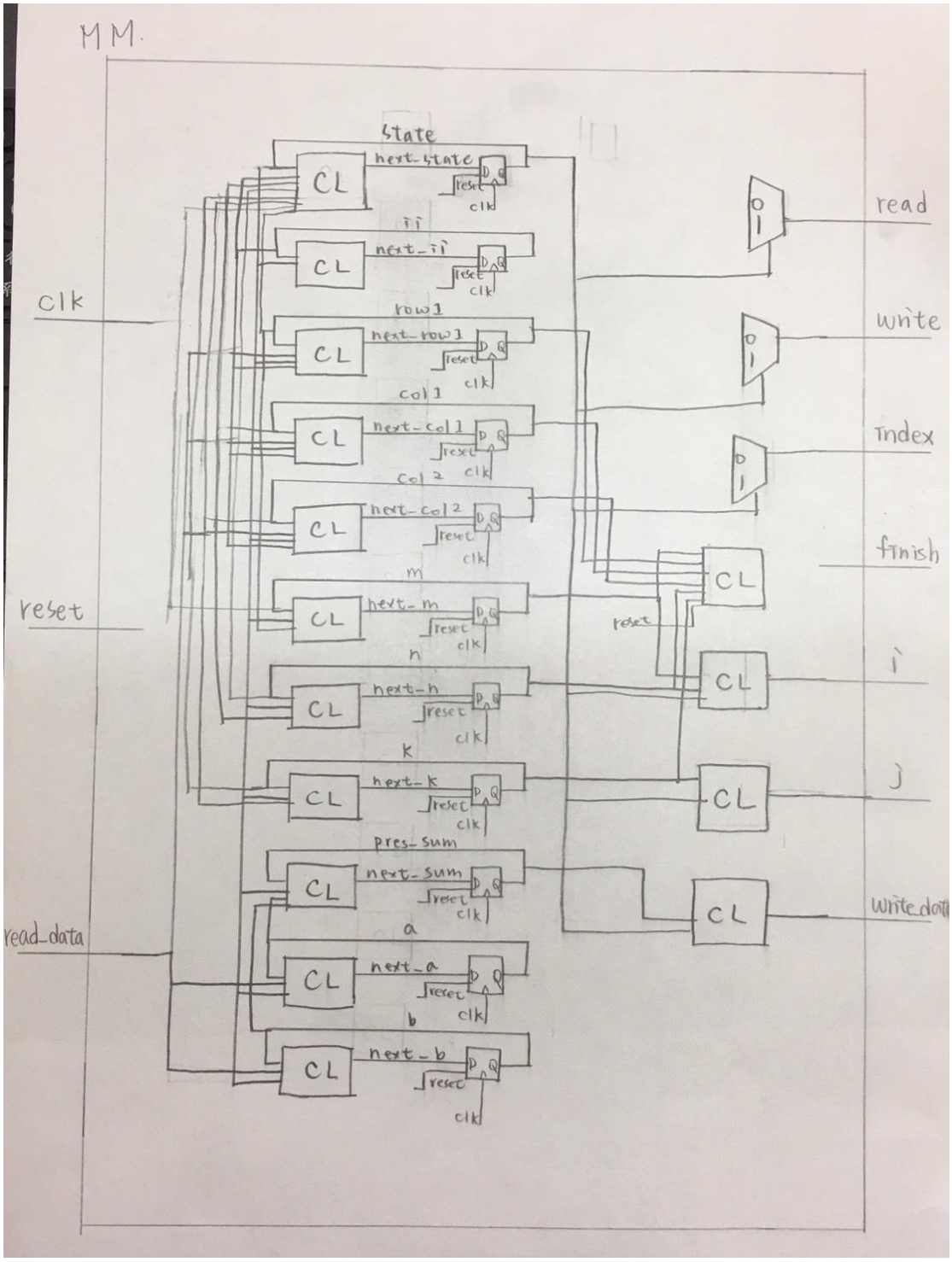
MAT0: 將 read 設為 1，write 設為 0，index 設為 0，經由 read_data 讀取第一個矩陣的資料（從第一筆開始讀）。

MAT1: 將 read 設為 1，write 設為 0，index 設為 1，經由 read_data 讀取第二個矩陣的資料（從第一筆開始讀）。

MULADD: 把兩個矩陣的兩筆資料相乘，並累加。
CHANGECOL1: 將第一個矩陣的行座標加一，直到等於行數就歸零。
WRITE: 將 read 設為 0，write 設為 1，算出一列乘以一行的數值，設定 write_data 的數值，將資料寫入。
CHANGECOL2: 將第二個矩陣的行座標加一，直到等於行數就歸零。
CHANGEROW1: 將第一個矩陣的列座標加一，直到等於列數就結束運算。

- Block Diagram

（clk 跟 reset 太多了，所以用標註的）



- ncverilog 模擬結果

```
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Recompiling... reason: file './MM.v' is newer than expected.
        expected: Mon May 14 23:12:37 2018
        actual:   Mon May 14 23:48:18 2018
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: .................... Done
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                2       2
                Registers:             42      42
                Scalar wires:           6       -
                Vectored wires:         4       -
                Always blocks:          5       5
                Initial blocks:         3       3
                Cont. assignments:      1       7
                Pseudo assignments:     1       1
        Writing initial simulation snapshot: worklib.test:v
Loading snapshot worklib.test:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'MM.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
      2       3       3       4
      2       3       3       4
##########################
Row:          0 Column:          0 is correct.
##########################
##########################
Row:          0 Column:          1 is correct.
##########################
##########################
Row:          0 Column:          2 is correct.
##########################
##########################
Row:          0 Column:          3 is correct.
##########################
##########################
Row:          1 Column:          0 is correct.
##########################
##########################
Row:          1 Column:          1 is correct.
##########################
##########################
Row:          1 Column:          2 is correct.
##########################
##########################
Row:          1 Column:          3 is correct.
##########################
##################
#Congratulation!!!#
##################
Simulation complete via $finish(1) at time 9880 NS + 3
./MM_tb.v:118           $finish;
```

```
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: MM_syn.v
        module worklib.MM_DW01_inc_0:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_inc_1:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_inc_2:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_inc_3:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_cmp6_0:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_dec_0:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_dec_1:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_dec_2:v
                errors: 0, warnings: 0
        module worklib.MM_DW_mult_tc_0:v
                errors: 0, warnings: 0
        module worklib.MM_DW01_add_0:v
                errors: 0, warnings: 0
        module worklib.MM:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
                Caching library 'worklib' ....... Done
  ADDHXL U1_1_18 ( .A(A[18]), .B(carry[18]), .CO(carry[19]), .S(SUM[18]) );
                 |
ncelab: *E,CUVMUR (./MM_syn.v,14|15): instance 'test.mmmmm@MM<module>.add_120@MM_DW01_inc_0<module>.U1_1_18' of design unit 'ADDHXL' is u
nresolved in 'worklib.MM_DW01_inc_0:v'.
  ADDHXL U1_1_17 ( .A(A[17]), .B(carry[17]), .CO(carry[18]), .S(SUM[17]) );
                 |
ncelab: *E,CUVMUR (./MM_syn.v,15|15): instance 'test.mmmmm@MM<module>.add_120@MM_DW01_inc_0<module>.U1_1_17' of design unit 'ADDHXL' is u
nresolved in 'worklib.MM_DW01_inc_0:v'.
  ADDHXL U1_1_16 ( .A(A[16]), .B(carry[16]), .CO(carry[17]), .S(SUM[16]) );
                 |
ncelab: *E,CUVMUR (./MM_syn.v,16|15): instance 'test.mmmmm@MM<module>.add_120@MM_DW01_inc_0<module>.U1_1_16' of design unit 'ADDHXL' is u
```

這次的 lab，我在如何換行換列的部分想了很久，雖然覺得自己用了有點多 state 和 Sequential Circuits，所以導致跑得有點慢，但因為打太久所以沒時間修改了，悲慘。