Lab3

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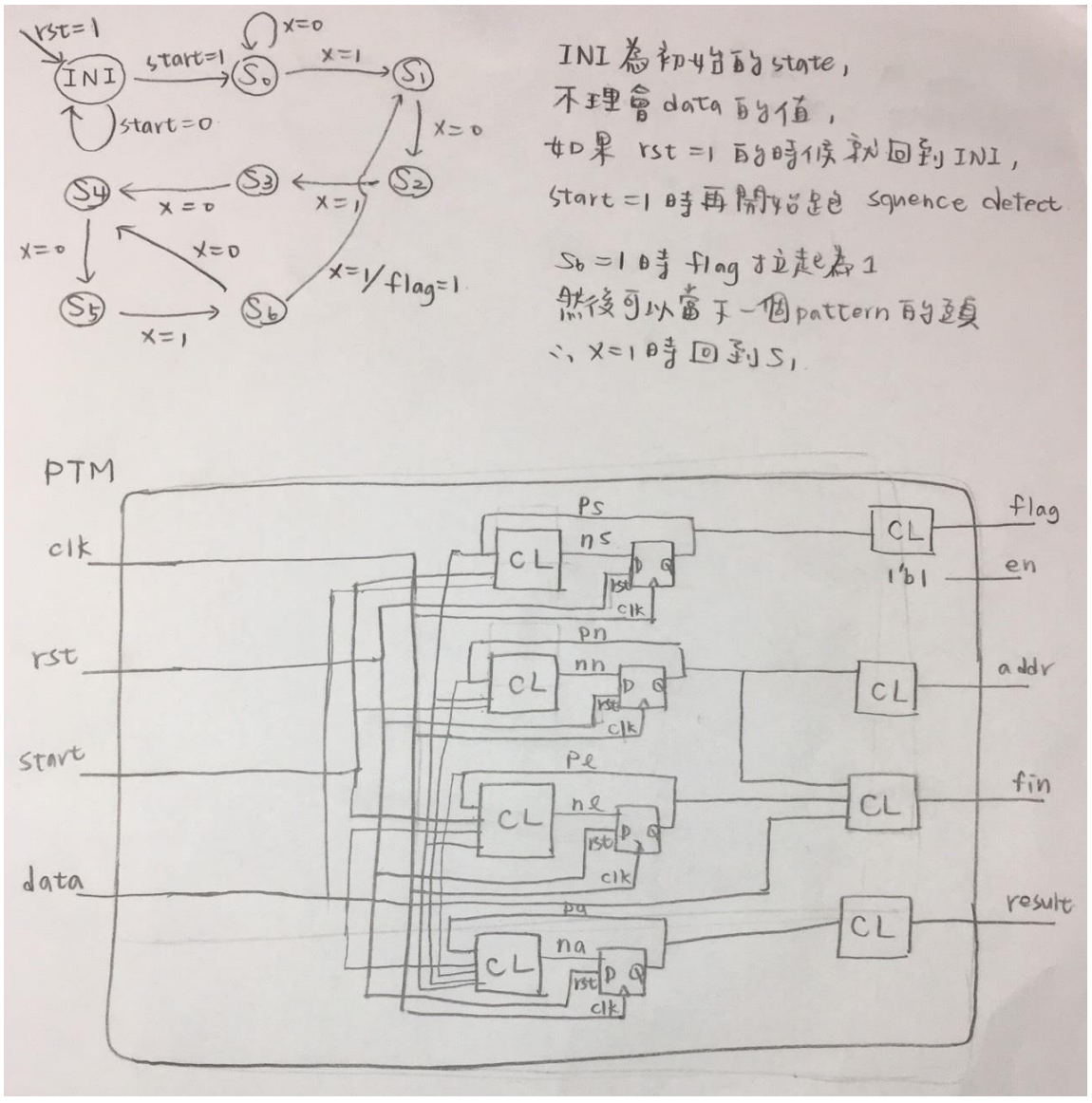
State Transition Graph & Block Diagram



ncverilog 模擬結果

```
Recompiling... reason: file './PTM.v' is newer than expected.
        expected: Sun Apr 22 02:43:29 2018
        actual:   Sun Apr 22 02:53:15 2018
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: ..................... Done
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                2       2
                Registers:             17      17
                Scalar wires:           6       -
                Vectored wires:         3       -
                Always blocks:          3       3
                Initial blocks:         3       3
                Cont. assignments:      3       5
                Pseudo assignments:     2       2
        Writing initial simulation snapshot: worklib.PTM_tb:v
Loading snapshot worklib.PTM_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'PTM.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

GET ! addr =   18 , your_flag = 1 , ans_flag = 1
GET ! addr =   32 , your_flag = 1 , ans_flag = 1
GET ! addr =   45 , your_flag = 1 , ans_flag = 1
GET ! addr =   58 , your_flag = 1 , ans_flag = 1
GET ! addr =   70 , your_flag = 1 , ans_flag = 1
GET ! addr =   86 , your_flag = 1 , ans_flag = 1
GET ! addr =  120 , your_flag = 1 , ans_flag = 1
GET ! addr =  159 , your_flag = 1 , ans_flag = 1
GET ! addr =  199 , your_flag = 1 , ans_flag = 1

Result =    9 , Answer =    9
!!!!! ACCEPTED !!!!!
```

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          |
ncelab: *E,CUVMUR (./PTM_syn.v,207|13): instance 'PTM_tb.ptm@PTM<module>.U349' of design unit 'XNOR2X1' is unresolved in 'worklib.PTM:v'.
  AOI2BB2X1 U350 ( .B0(n282), .B1(n283), .A0N(n282), .A1N(n274), .Y(n284) );
                |
ncelab: *E,CUVMUR (./PTM_syn.v,208|15): instance 'PTM_tb.ptm@PTM<module>.U350' of design unit 'AOI2BB2X1' is unresolved in 'worklib.PTM:v
'.
  OAI222XL U351 ( .A0(n292), .A1(n285), .B0(n276), .B1(n284), .C0(n283), .C1(
          |
ncelab: *E,CUVMUR (./PTM_syn.v,209|14): instance 'PTM_tb.ptm@PTM<module>.U351' of design unit 'OAI222XL' is unresolved in 'worklib.PTM:v'
.
  XNOR2X1 U352 ( .A(N10), .B(state[0]), .Y(n286) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,211|13): instance 'PTM_tb.ptm@PTM<module>.U352' of design unit 'XNOR2X1' is unresolved in 'worklib.PTM:v'.
  NOR2X1 U353 ( .A(state[3]), .B(n286), .Y(n288) );
        |
ncelab: *E,CUVMUR (./PTM_syn.v,212|12): instance 'PTM_tb.ptm@PTM<module>.U353' of design unit 'NOR2X1' is unresolved in 'worklib.PTM:v'.
  NAND4X1 U354 ( .A(state[0]), .B(state[1]), .C(n274), .D(n292), .Y(n287) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,213|13): instance 'PTM_tb.ptm@PTM<module>.U354' of design unit 'NAND4X1' is unresolved in 'worklib.PTM:v'.
  OAI21XL U355 ( .A0(n275), .A1(n288), .B0(n287), .Y(next_state[2]) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,214|13): instance 'PTM_tb.ptm@PTM<module>.U355' of design unit 'OAI21XL' is unresolved in 'worklib.PTM:v'.
  OA21XL U356 ( .A0(n290), .A1(n289), .B0(state[3]), .Y(next_state[3]) );
        |
ncelab: *E,CUVMUR (./PTM_syn.v,215|12): instance 'PTM_tb.ptm@PTM<module>.U356' of design unit 'OA21XL' is unresolved in 'worklib.PTM:v'.
  INVX1 U357 ( .A(n294), .Y(n295) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,216|11): instance 'PTM_tb.ptm@PTM<module>.U357' of design unit 'INVX1' is unresolved in 'worklib.PTM:v'.
  INVX1 U358 ( .A(n294), .Y(n296) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,217|11): instance 'PTM_tb.ptm@PTM<module>.U358' of design unit 'INVX1' is unresolved in 'worklib.PTM:v'.
  INVX1 U359 ( .A(N96), .Y(n299) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,218|11): instance 'PTM_tb.ptm@PTM<module>.U359' of design unit 'INVX1' is unresolved in 'worklib.PTM:v'.
  INVX1 U360 ( .A(N96), .Y(n300) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,219|11): instance 'PTM_tb.ptm@PTM<module>.U360' of design unit 'INVX1' is unresolved in 'worklib.PTM:v'.
  INVX1 U361 ( .A(N96), .Y(n301) );
          |
ncelab: *E,CUVMUR (./PTM_syn.v,220|11): instance 'PTM_tb.ptm@PTM<module>.U361' of design unit 'INVX1' is unresolved in 'worklib.PTM:v'.
ncverilog: *E,ELBERR: Error during elaboration (status 1), exiting.
```

遇到的問題：

1. 為什麼多設一個 S7，然後 S6 在 X=1 時跳到 S7，再拉起 flag，跑 tb 答案就會是錯的。如果是在 S6 給 if 兩種 X 的情況，跑 tb 就對了？
2. 為什麼 reg flag0 給值 flag，就會產生 latch？這樣會讓電路產生問題嗎？
3. ncverilog syn的時候為什麼會出現那樣的結果？還有最底下的error是怎麼回事？