Lab 07: Digital Photo Frame

(Dec 4, 2018)

Submission deadlines:

Source Code:	18:30, Dec 4, 2018
Report:	23:59, Dec 9, 2018

Objective

- ➢ To be familiar with modeling finite state machines with Verilog.
- ➢ To be familiar with the FPGA design flow.
- ➢ To be familiar with the control of VGA Display and other I/Os on the FPGA demo-board.

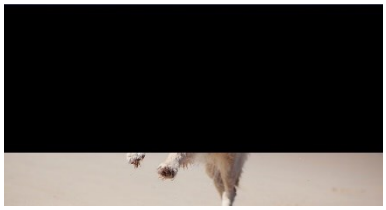
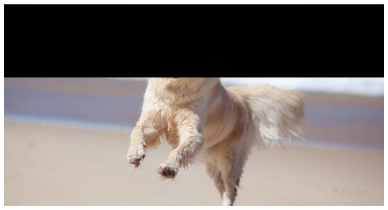
Description

In this lab, you are asked to implement some transition effects of showing pictures on the VGA display, as a digital photo frame. We define 4 transition effects. **You should implement 3 of them to get full credit in this lab**.

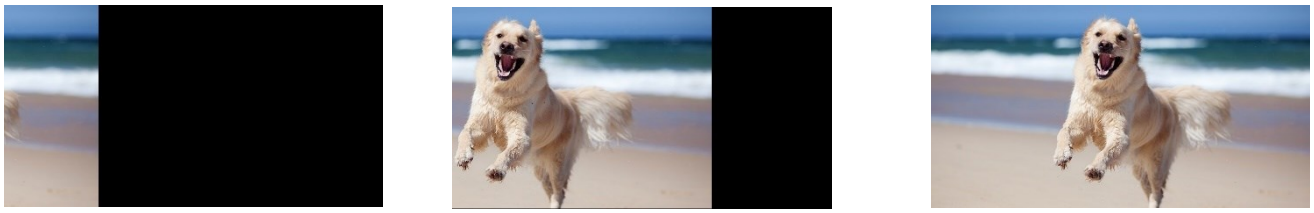
- After the reset, the screen should display nothing (the whole screen is black).

- When a button is pressed, its corresponding transition effect will start to operate. Each transition effect is briefed in the follows:

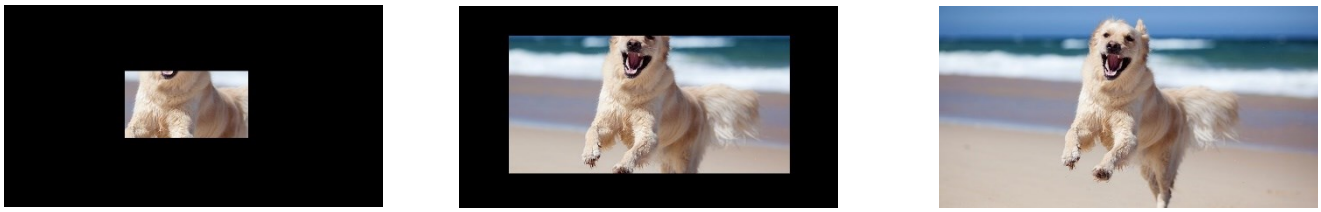
1. **Rising Curtain** (**btnC**): The image will appear from bottom to top, like rising a curtain.

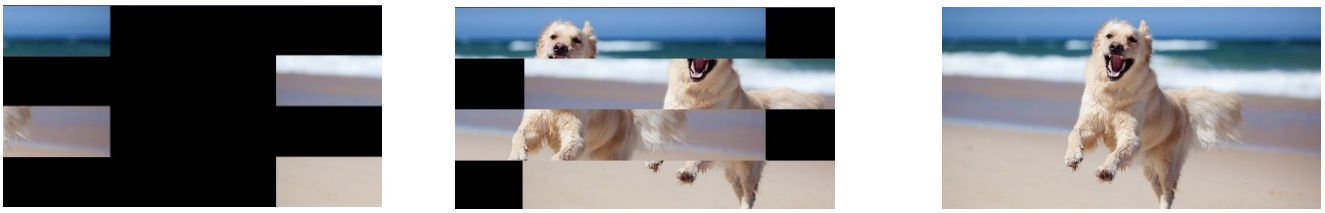

2. **Sliding In** (**btnR**): The image will slide in from left to right.



3. **Box** (**btnL**): There will be a box in the center revealing the image, the box's size will keep increasing (t**he box's aspect ratio is the same as the image**).



4. **Split** (**btnU**): The image splits into 4 horizontal part. Each part of the image will slide in (1st and 3rd are from left to right, 2nd and 4th are from right to left).



- When the transition effect is complete, the screen should keep displaying the image for a specific period (i.e., one clock cycle of the frequency of clk/(2^27)). Then the screen will display nothing (i.e., the whole screen turns black) until any button is pressed again.

Demo video: https://youtu.be/B7Kr6tQn8sE

Note:

1. You should choose the image you like and use PicTrans.exe to generate your own .coe file. **Note: make sure it is an appropriate image**.
2. **You should implement 3 of the transition effects to get full credit in this lab. If you implement all 4 transition effects, you will get extra credit**.
3. The clock frequency used for each transition effect is not restricted. You can use any clock frequency to make the transition look the best.
4. During the transition, pressing any buttons has no effect (except **rst**).

I/O signal specification:

- **rst**: asynchronous active-high reset (connected to **btnD**). When the reset is high, the screen will display nothing (whole screen is black)
- **clk**: clock signal with the frequency of 100MHz (connected to pin **W5**)
- **btnC**: pressed to activate the "**Rising Curtain**" transition effect
- **btnR**: pressed to activate the "**Sliding In**" transition effect
- **btnL**: pressed to activate the "**Box**" transition effect
- **btnU**: pressed to activate the "**Split**" transition effect
- **vgaRed**: 4 bits to represent the intensity of red color (connected to pin **N19, J19, H19, G19**)
- **vgaGreen**: 4 bits to represent the intensity of green color (connected to pin **D17, G17, H17, J17**)
- **vgaBlue**: 4 bits to represent the intensity of blue color (connected to pin **J18, K18, L18, N18**)
- **hsync**: the horizontal synchronization signal of the VGA display (connected to pin **P19**)
- **vsync**: the vertical synchronization signal of the VGA display (connected to pin **R19**)

You can use the following template for your design.

```
module lab07( input clk,
              input rst,
              input btnC, btnL, btnR, btnU,
              output [3:0] vgaRed,
              output [3:0] vgaGreen,
              output [3:0] vgaBlue,
              output hsync,
              output vsync);

    //add your design here
    //…
endmodule
```

Attention:

1. You should hand in only lab07.v. If you have several modules for your design, put them in lab07.v together.
2. You should also hand in your report as lab07_report_StudentID.pdf (i.e., lab07_report_106062001.pdf).
3. You should be able to answer questions of this lab from TA during the demo.
4. You need to generate bitstream before demo.