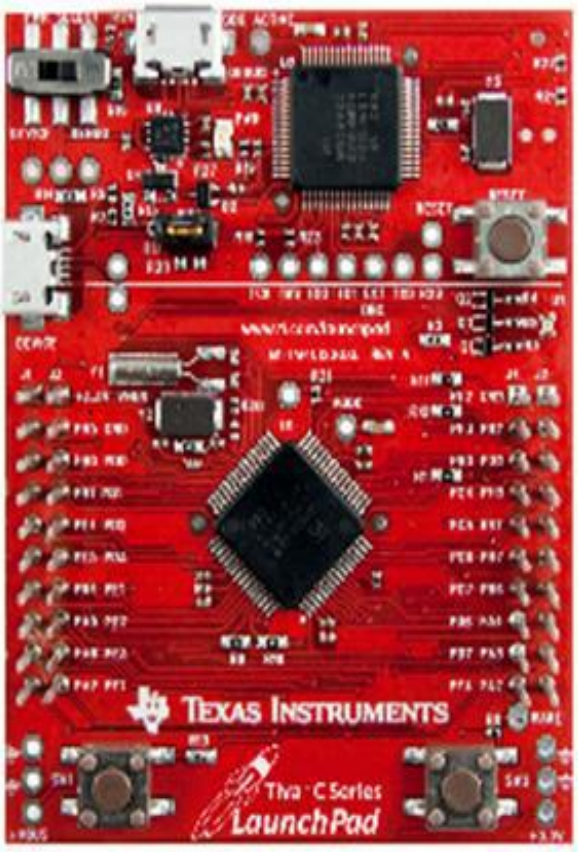
TIVA MICROCONTROLLER and IT'S ARCHITECTURE

Architectural Overview

Texas Instrument's Tiva™ C Series microcontrollers provide designers a high-performance ARM Cortex™-M-based architecture with a broad set of integration capabilities and a strong ecosystem of software and development tools. Targeting performance and flexibility, the Tiva™ C Series architecture offers an 80 MHz Cortex-M with FPU, a variety of integrated memories and multiple programmable GPIO.

Tiva™ C Series devices offer consumers compelling cost-effective solutions by integrating application-specific peripherals and providing a comprehensive library of software tools which minimize board costs and design-cycle time. Offering quicker time-to-market and cost savings, the Tiva™ C Series microcontrollers are the leading choice in high-performance 32-bit applications.

- ARM® Cortex™-M4F 64-pin 80MHz TM4C123GH6PM
- On-board USB ICDI (In-Circuit Debug Interface)
- Micro AB USB port
- Device/ICDI power switch
- BoosterPack XL pinout also supports legacy BoosterPack pinout
- 2 user pushbuttons (SW2 is connected to the WAKE pin)
- Reset button
- 3 user LEDs (1 tri-color device)
- Current measurement test points
- 16MHz Main Oscillator crystal
- 32kHz Real Time Clock crystal
- 3.3V regulator
- Support for multiple IDEs:



Tiva™ C Series Overview

The Tiva™ C Series ARM Cortex-M4 microcontrollers provide top performance and advanced integration. The product family is positioned for cost-conscious applications requiring significant control processing and connectivity capabilities such as:

- Low power, hand-held smart devices
- Gaming equipment
- Home and commercial site monitoring and control
- Motion control
- Medical instrumentation
- Test and measurement equipment
- Factory automation
- Fire and security
- Smart Energy/Smart Grid solutions
- Intelligent lighting control
- Transportation

TM4C123GH6PM Microcontroller Architecture and Features

1. ARM Cortex-M4F Processor Core

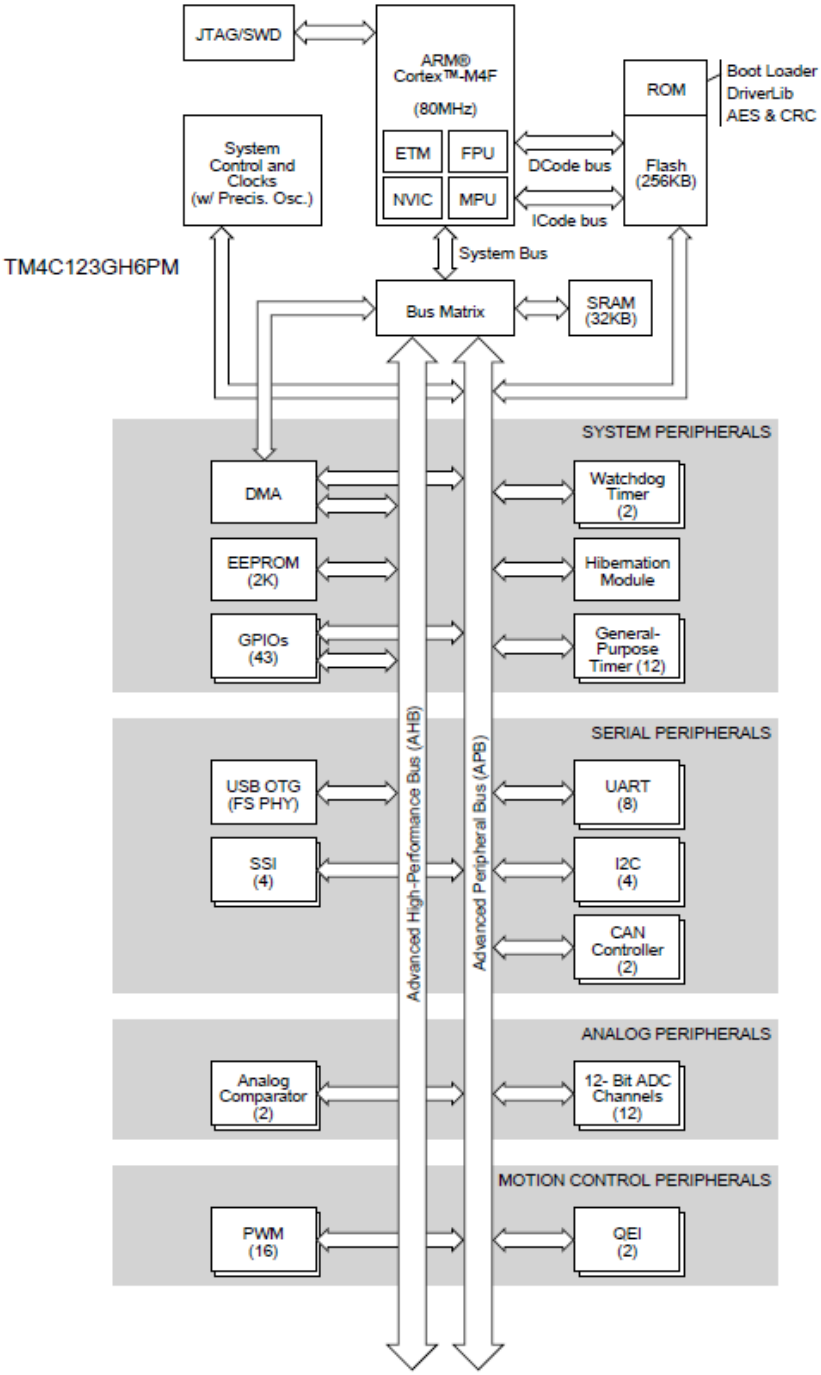
All members of the Tiva™ C Series, including the TM4C123GH6PM microcontroller, are designed around an ARM Cortex-M processor core. The ARM Cortex-M processor provides the core for a high-performance, low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- 32-bit ARM Cortex-M4F architecture optimized for small-footprint embedded applications
- 80-MHz operation;

2. System Timer (SysTick)

ARM Cortex-M4F includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- A high-speed alarm timer using the system clock
- A simple counter used to measure time to completion and time used



3. Nested Vectored Interrupt Controller (NVIC)

The TM4C123GH6PM controller includes the ARM Nested Vectored Interrupt Controller (NVIC). The NVIC and Cortex-M4F prioritize and handle all exceptions in Handler Mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the Interrupt Service Routine (ISR). The interrupt vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, meaning that back-to-back interrupts can be performed without the overhead of state saving and restoration.

Software can set eight priority levels on 7 exceptions (system handlers) and 78 interrupts.

- Deterministic, fast interrupt processing: always 12 cycles, or just 6 cycles with tail-chaining
- External non-maskable interrupt signal (NMI) available for immediate execution of NMI handler for safety critical applications

4. System Control Block

The SCB provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

5. Memory Protection Unit (MPU)

The MPU supports the standard ARM7 Protected Memory System Architecture (PMSA) model. The MPU provides full support for protection regions, overlapping protection regions, access permissions, and exporting memory attributes to the system.

6. Floating-Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

- 32-bit instructions for single-precision (C float) data-processing operations
- Combined multiply and accumulate instructions for increased precision (Fused MAC)
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
- 32 dedicated 32-bit single-precision registers, also addressable as 16 double-word registers

7. On-Chip Memory

The TM4C123GH6PM microcontroller is integrated with the following set of on-chip memory and features:

- 32 KB single-cycle SRAM
- 256 KB Flash memory
- 2KB EEPROM
- Internal ROM loaded with TivaWare™ for C Series software:

– TivaWare™ Peripheral Driver Library
– TivaWare Boot Loader
– Advanced Encryption Standard (AES) cryptography tables
– Cyclic Redundancy Check (CRC) error detection functionality

8. SRAM

The TM4C123GH6PM microcontroller provides 32 KB of single-cycle on-chip SRAM. The internal SRAM of the device is located at offset 0x2000.0000 of the device memory map. Because read-modify-write (RMW) operations are very time consuming, ARM has introduced *bit-banding* technology in the Cortex-M4F processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation.
Data can be transferred to and from SRAM by the following masters:

- µDMA
- USB

9. Flash Memory

The TM4C123GH6PM microcontroller provides 256 KB of single-cycle on-chip Flash memory. The Flash memory is organized as a set of 1-KB blocks that can be individually erased. Erasing a block causes the entire contents of the block to be reset to all 1s. These blocks are paired into a set of 2-KB blocks that can be individually protected. The blocks can be marked as read-only or execute-only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed, and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or by a debugger.

10. ROM

The TM4C123GH6PM ROM is pre-programmed with the following software and programs:

- TivaWare Peripheral Driver Library
- TivaWare Boot Loader
- Advanced Encryption Standard (AES) cryptography tables
- Cyclic Redundancy Check (CRC) error-detection functionality

The TivaWare Peripheral Driver Library is a royalty-free software library for controlling on-chip peripherals with a boot-loader capability. The library performs both peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. In addition, the library is designed to take full advantage of the stellar interrupt performance of the ARM Cortex-M4F core.
For applications that require in-field programmability, the royalty-free TivaWare Boot Loader can act as an application loader and support in-field firmware updates.

The Advanced Encryption Standard (AES) is a publicly defined encryption standard used by the U.S. Government. AES is a strong encryption method with reasonable performance and size. In addition, it is fast in both hardware and software, is fairly easy to implement, and requires little memory.

CRC (Cyclic Redundancy Check) is a technique to validate a span of data has the same contents as when previously checked. This technique can be used to validate correct receipt of messages (nothing lost or modified in transit), to validate data after decompression, to validate that Flash memory contents have not been changed, and for other cases where the data needs to be validated. A CRC is preferred over a simple checksum (for example, XOR all bits) because it catches changes more readily.

11. EEPROM

The TM4C123GH6PM microcontroller includes an EEPROM with the following features:

- 2Kbytes of memory accessible as 512 32-bit words
- 32 blocks of 16 words (64 bytes) each

12. Serial Communications Peripherals

The TM4C123GH6PM controller supports both asynchronous and synchronous serial communications with:

- Two CAN 2.0 A/B controllers
- USB 2.0 OTG/Host/Device
- Eight UARTs with IrDA, 9-bit and ISO 7816 support.
- Four I2C modules with four transmission speeds including high-speed mode
- Four Synchronous Serial Interface modules (SSI)

The following sections provide more detail on each of these communications functions.

13. Controller Area Network (CAN)

Controller Area Network (CAN) is a multicast shared serial-bus standard for connecting electronic control units (ECUs). CAN was specifically designed to be robust in electromagnetically noisy environments. Originally created for automotive purposes, it is now used in many embedded control applications (for example, industrial or medical). Bit rates up to 1 Mbps are possible at network lengths below 40 meters.

A transmitter sends a message to all CAN nodes (broadcasting). Each node decides on the basis of the identifier received whether it should process the message. The identifier also determines the priority that the message enjoys in competition for bus access. Each CAN message can transmit from 0 to 8 bytes of user information.

14. Universal Serial Bus (USB)

Universal Serial Bus (USB) is a serial bus standard designed to allow peripherals to be connected and disconnected using a standardized interface without rebooting the system.

The TM4C123GH6PM microcontroller supports three configurations in USB 2.0 full and low speed:

USB Device, USB Host, and USB On-The-Go (negotiated on-the-go as host or device when connected to other USB-enabled systems).

15. UART

A Universal Asynchronous Receiver/Transmitter (UART) is an integrated circuit used for RS-232C serial communications, containing a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

The TM4C123GH6PM microcontroller includes eight fully programmable 16C550-type UARTs. Although the functionality is similar to a 16C550 UART, this UART design is not register compatible. The UART can generate individually masked interrupts from the Rx, Tx, modem flow control, and error conditions. The module generates a single combined interrupt when any of the interrupts are asserted and are unmasked.

16. I2C

The Inter-Integrated Circuit (I2C) bus provides bi-directional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL). The I2C bus interfaces to external I2C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on.

The I2C bus may also be used for system testing and diagnostic purposes in product development and manufacture.

Each device on the I2C bus can be designated as either a master or a slave. I2C module supports both sending and receiving data as either a master or a slave and can operate simultaneously as both a master and a slave. Both the I2C master and slave can generate interrupts.

17. SSI

Synchronous Serial Interface (SSI) is a four-wire bi-directional communications interface that converts data between parallel and serial. The SSI module performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data transmitted to a peripheral device. The SSI module can be configured as either a master or slave device. As a slave device, the SSI module can also be configured to disable its output, which allows a master device to be coupled with multiple slave devices. The TX and RX paths are buffered with separate internal FIFOs.

The SSI module also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the SSI module's input clock. Bit rates are generated based on the input clock and the maximum bit rate is determined by the connected peripheral.

18. Direct Memory Access

The TM4C123GH6PM microcontroller includes a Direct Memory Access (DMA) controller, known as micro-DMA (μDMA). The μDMA controller provides a way to offload data transfer tasks from the Cortex-M4F processor, allowing for more efficient use of the processor and the available bus bandwidth. The μDMA controller can perform transfers

between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

19. System Control and Clocks

System control determines the overall operation of the device. It provides information about the device, controls power-saving features, controls the clocking of the device and individual peripherals, and handles reset detection and reporting.

- Power control
- Multiple clock sources for microcontroller system clock. The following clock sources are provided to the TM4C123GH6PM microcontroller:
- Flexible reset sources

20. Programmable Timers

Programmable timers can be used to count or time external events that drive the Timer input pins. Each 16/32-bit GPTM block provides two 16-bit timers/counters that can be configured to operate independently as timers or event counters, or configured to operate as one 32-bit timer or one 32-bit Real-Time Clock (RTC). Each 32/64-bit Wide GPTM block provides two 32-bit timers/counters that can be configured to operate independently as timers or event counters, or configured to operate as one 64-bit timer or one 64-bit Real-Time Clock (RTC). Timers can also be used to trigger analog-to-digital (ADC) conversions and DMA transfers.
The General-Purpose Timer Module (GPTM) contains six 16/32-bit GPTM blocks and six 32/64-bit

21. Hibernation Module

The Hibernation module provides logic to switch power off to the main processor and peripherals and to wake on external or time-based events.

22. Watchdog Timers

A watchdog timer is used to regain control when a system has failed due to a software error or to the failure of an external device to respond in the expected way. The TM4C123GH6PM Watchdog Timer can generate an interrupt, a non-maskable interrupt, or a reset when a time-out value is reached.

23. Programmable GPIOs

General-purpose input/output (GPIO) pins offer flexibility for a variety of connections. The TM4C123GH6PM GPIO module is comprised of six physical GPIO blocks, each corresponding to an individual GPIO port. The GPIO module is FiRM-compliant (compliant

to the ARM Foundation IP for Real-Time Microcontrollers specification) and supports 0-43 programmable input/output pins.

24. Advanced Motion Control

The TM4C123GH6PM microcontroller provides motion control functions integrated into the device, including:

■ Two PWM modules, with a total of 16 advanced PWM outputs for motion and energy applications

■ Two fault inputs to promote low-latency shutdown

■ Two Quadrature Encoder Inputs (QEI)

25. PWM

The TM4C123GH6PM microcontroller contains two PWM modules, each with four PWM generator blocks and a control block, for a total of 16 PWM outputs. Pulse width modulation (PWM) is a powerful technique for digitally encoding analog signal levels. High-resolution counters are used to generate a square wave, and the duty cycle of the square wave is modulated to encode an analog signal. Typical applications include switching power supplies and motor control.

Each TM4C123GH6PM PWM module consists of four PWM generator block and a control block. Each PWM generator block contains one timer (16-bit down or up/down counter), two comparators, a PWM signal generator, a dead-band generator, and an interrupt/ADC-trigger selector. Each PWM generator block produces two PWM signals that can either be independent signals or a single pair of complementary signals with dead-band delays inserted.

26. QEI

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, the position, direction of rotation, and speed can be tracked. In addition, a third channel, or index signal, can be used to reset the position counter. The TM4C123GH6PM quadrature encoder with index (QEI) module interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel. The input frequency of the QEI inputs may be as high as 1/4 of the processor frequency (for example, 20 MHz for a 80-MHz system).

27. Analog

The TM4C123GH6PM microcontroller provides analog functions integrated into the device, including:

- Two 12-bit Analog-to-Digital Converters (ADC), with a total of 12 analog input channels and each
- with a sample rate of one million samples/second
- Two analog comparators

- On-chip voltage regulator

28. ADC

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number. The TM4C123GH6PM ADC module features 12-bit conversion resolution and supports 12 input channels plus an internal temperature sensor. Four buffered sample sequencers allow rapid sampling of up to 12 analog input sources without controller intervention.

Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. Each ADC module has a digital comparator function that allows the conversion value to be diverted to a comparison unit that provides eight digital comparators.

29. Analog Comparators

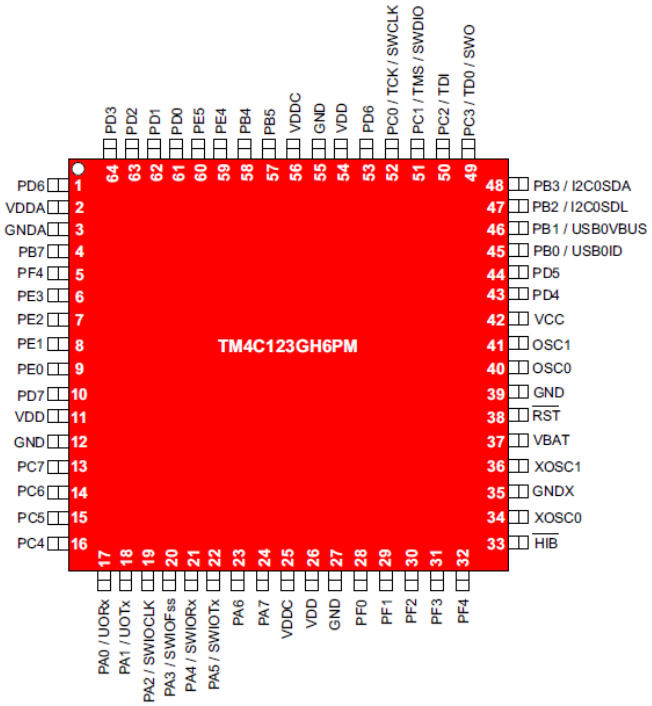
An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result. The TM4C123GH6PM microcontroller provides two independents integrated analog comparators that can be configured to drive an output or generate an interrupt or ADC event.

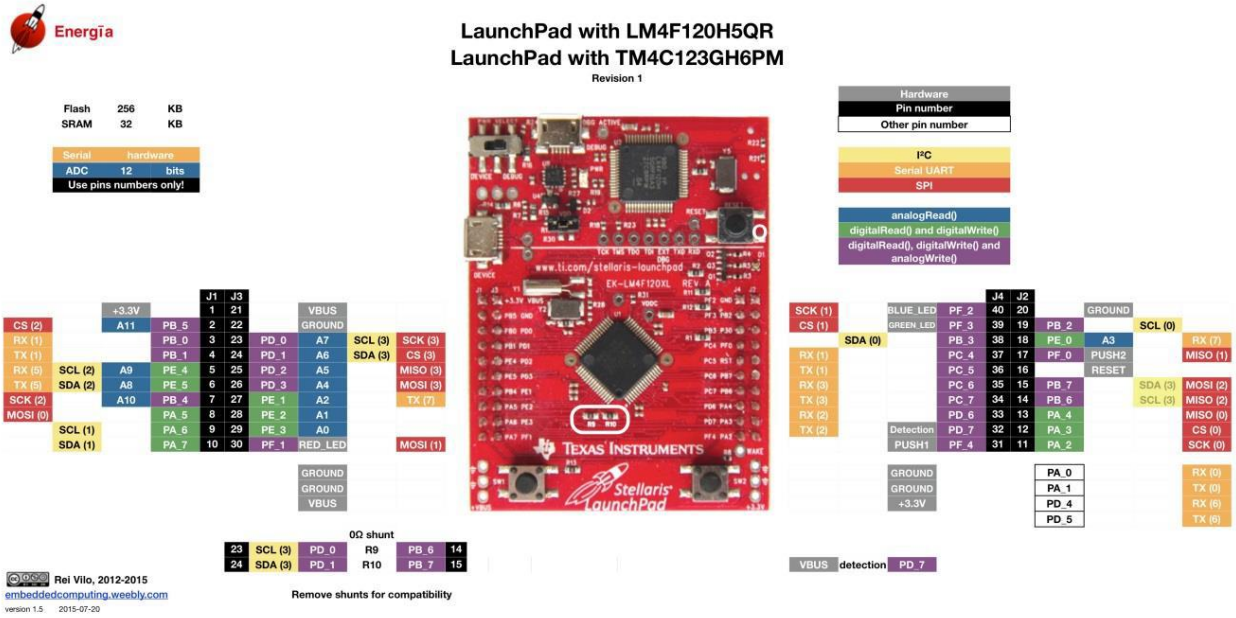
The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board, or it can be used to signal the application via interrupts or triggers to the ADC to cause it to start capturing a sample sequence. The interrupt generation and ADC triggering logic is separate. This means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.

30. JTAG and ARM Serial Wire Debug

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The SWJ-DP interface combines the SWD and JTAG debug ports into one module providing all the normal JTAG debug and test functionality plus real-time access to system memory without halting the core or requiring any target resident code.

PIN DIAGRAM OF TM4C123GH6PM / TM4C123GH6PM Energia Pin map





Pin Number	Pin Name	Pin Type	Buffer Type[a]	Description
1	PB6	I/O	TTL	GPIO port B bit 6.
	M0PWM0	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.
	SSI2Rx	I	TTL	SSI module 2 receive.
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
2	VDDA	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in Table 24-5 on page 1360, regardless of system implementation.
3	GNDA	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
4	PB7	I/O	TTL	GPIO port B bit 7.
	M0PWM1	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
	SSI2Tx	O	TTL	SSI module 2 transmit.
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
5	PF4	I/O	TTL	GPIO port F bit 4.
	IDX0	I	TTL	QEI module 0 index.
	M1FAULT0	I	TTL	Motion Control Module 1 PWM Fault 0.
	T2CCP0	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
6	PE3	I/O	TTL	GPIO port E bit 3.
	AIN0	I	Analog	Analog-to-digital converter input 0.
7	PE2	I/O	TTL	GPIO port E bit 2.
	AIN1	I	Analog	Analog-to-digital converter input 1.
8	PE1	I/O	TTL	GPIO port E bit 1.
	AIN2	I	Analog	Analog-to-digital converter input 2.
	U7Tx	O	TTL	UART module 7 transmit.
9	PE0	I/O	TTL	GPIO port E bit 0.
	AIN3	I	Analog	Analog-to-digital converter input 3.
	U7Rx	I	TTL	UART module 7 receive.

Pin Number	Pin Name	Pin Type	Buffer Type[3]	Description
10	PD7	I/O	TTL	GPIO port D bit 7.
	NMI	I	TTL	Non-maskable interrupt.
	PhB0	I	TTL	QEI module 0 phase B.
	U2Tx	O	TTL	UART module 2 transmit.
	WT5CCP1	I/O	TTL	32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.
11	VDD	-	Power	Positive supply for I/O and some logic.
12	GND	-	Power	Ground reference for logic and I/O pins.
13	PC7	I/O	TTL	GPIO port C bit 7.
	C0-	I	Analog	Analog comparator 0 negative input.
	U3Tx	O	TTL	UART module 3 transmit.
	USB0PFLT	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
	WT1CCP1	I/O	TTL	32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.
14	PC6	I/O	TTL	GPIO port C bit 6.
	C0+	I	Analog	Analog comparator 0 positive input.
	PhB1	I	TTL	QEI module 1 phase B.
	U3Rx	I	TTL	UART module 3 receive.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
	WT1CCP0	I/O	TTL	32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.
15	PC5	I/O	TTL	GPIO port C bit 5.
	C1+	I	Analog	Analog comparator 1 positive input.
	M0PWM7	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.
	PhA1	I	TTL	QEI module 1 phase A.
	U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.
	U1Tx	O	TTL	UART module 1 transmit.
	U4Tx	O	TTL	UART module 4 transmit.
	WT0CCP1	I/O	TTL	32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.
16	PC4	I/O	TTL	GPIO port C bit 4.
	C1-	I	Analog	Analog comparator 1 negative input.
	IDX1	I	TTL	QEI module 1 index.
	M0PWM6	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
	U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.
	U1Rx	I	TTL	UART module 1 receive.
	U4Rx	I	TTL	UART module 4 receive.
	WT0CCP0	I/O	TTL	32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.
17	PA0	I/O	TTL	GPIO port A bit 0.
	CAN1Rx	I	TTL	CAN module 1 receive.
	U0Rx	I	TTL	UART module 0 receive.

Pin Number	Pin Name	Pin Type	Buffer Type[a]	Description
18	PA1	I/O	TTL	GPIO port A bit 1.
	CAN1Tx	O	TTL	CAN module 1 transmit.
	U0Tx	O	TTL	UART module 0 transmit.
19	PA2	I/O	TTL	GPIO port A bit 2.
	SSI0Clk	I/O	TTL	SSI module 0 clock
20	PA3	I/O	TTL	GPIO port A bit 3.
	SSI0Fss	I/O	TTL	SSI module 0 frame signal
21	PA4	I/O	TTL	GPIO port A bit 4.
	SSI0Rx	I	TTL	SSI module 0 receive
22	PA5	I/O	TTL	GPIO port A bit 5.
	SSI0Tx	O	TTL	SSI module 0 transmit
23	PA6	I/O	TTL	GPIO port A bit 6.
	I2C1SCL	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M1PWM2	O	TTL	Motion Control Module 1 PWM 2. This signal is controlled by Module 1 PWM Generator 1.
24	PA7	I/O	TTL	GPIO port A bit 7.
	I2C1SDA	I/O	OD	I^2C module 1 data.
	M1PWM3	O	TTL	Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.
25	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 24-12 on page 1373 .
26	VDD	-	Power	Positive supply for I/O and some logic.
27	GND	-	Power	Ground reference for logic and I/O pins.
28	PF0	I/O	TTL	GPIO port F bit 0.
	C0o	O	TTL	Analog comparator 0 output.
	CAN0Rx	I	TTL	CAN module 0 receive.
	M1PWM4	O	TTL	Motion Control Module 1 PWM 4. This signal is controlled by Module 1 PWM Generator 2.
	NMI	I	TTL	Non-maskable interrupt.
	PhA0	I	TTL	QEI module 0 phase A.
	SSI1Rx	I	TTL	SSI module 1 receive.
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.

Pin Number	Pin Name	Pin Type	Buffer Type[a]	Description
29	PF1	I/O	TTL	GPIO port F bit 1.
	C1o	O	TTL	Analog comparator 1 output.
	M1PWM5	O	TTL	Motion Control Module 1 PWM 5. This signal is controlled by Module 1 PWM Generator 2.
	PhB0	I	TTL	QEI module 0 phase B.
	SSI1Tx	O	TTL	SSI module 1 transmit.
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	TRD1	O	TTL	Trace data 1.
	U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.
30	PF2	I/O	TTL	GPIO port F bit 2.
	M0FAULT0	I	TTL	Motion Control Module 0 PWM Fault 0.
	M1PWM6	O	TTL	Motion Control Module 1 PWM 6. This signal is controlled by Module 1 PWM Generator 3.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	TRD0	O	TTL	Trace data 0.
31	PF3	I/O	TTL	GPIO port F bit 3.
	CAN0Tx	O	TTL	CAN module 0 transmit.
	M1PWM7	O	TTL	Motion Control Module 1 PWM 7. This signal is controlled by Module 1 PWM Generator 3.
	SSI1Fss	I/O	TTL	SSI module 1 frame signal.
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	TRCLK	O	TTL	Trace clock.
32	$\overline{\text{WAKE}}$	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
33	$\overline{\text{HIB}}$	O	TTL	An output that indicates the processor is in Hibernate mode.
34	XOSC0	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 32.768-kHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
35	GNDX	-	Power	GND for the Hibernation oscillator. When using a crystal clock source, this pin should be connected to digital ground along with the crystal load capacitors. When using an external oscillator, this pin should be connected to digital ground.
36	XOSC1	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.
37	VBAT	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
38	$\overline{\text{RST}}$	I	TTL	System reset input.
39	GND	-	Power	Ground reference for logic and I/O pins.
40	OSC0	I	Analog	Main oscillator crystal input or an external clock reference input.
41	OSC1	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
42	VDD	-	Power	Positive supply for I/O and some logic.

Pin Number	Pin Name	Pin Type	Buffer Type[a]	Description
43	PD4	I/O	TTL	GPIO port D bit 4. This pin is not 5-V tolerant.
	U6Rx	I	TTL	UART module 6 receive.
	USB0DM	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
	WT4CCP0	I/O	TTL	32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.
44	PD5	I/O	TTL	GPIO port D bit 5. This pin is not 5-V tolerant.
	U6Tx	O	TTL	UART module 6 transmit.
	USB0DP	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
	WT4CCP1	I/O	TTL	32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.
45	PB0	I/O	TTL	GPIO port B bit 0. This pin is not 5-V tolerant.
	T2CCP0	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
	U1Rx	I	TTL	UART module 1 receive.
	USB0ID	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).
46	PB1	I/O	TTL	GPIO port B bit 1. This pin is not 5-V tolerant.
	T2CCP1	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
	U1Tx	O	TTL	UART module 1 transmit.
	USB0VBUS	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.
47	PB2	I/O	TTL	GPIO port B bit 2.
	I2C0SCL	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
48	PB3	I/O	TTL	GPIO port B bit 3.
	I2C0SDA	I/O	OD	I^2C module 0 data.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
49	PC3	I/O	TTL	GPIO port C bit 3.
	SWO	O	TTL	JTAG TDO and SWO.
	T5CCP1	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
	TDO	O	TTL	JTAG TDO and SWO.
50	PC2	I/O	TTL	GPIO port C bit 2.
	T5CCP0	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	TDI	I	TTL	JTAG TDI.
51	PC1	I/O	TTL	GPIO port C bit 1.
	SWDIO	I/O	TTL	JTAG TMS and SWDIO.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	TMS	I	TTL	JTAG TMS and SWDIO.

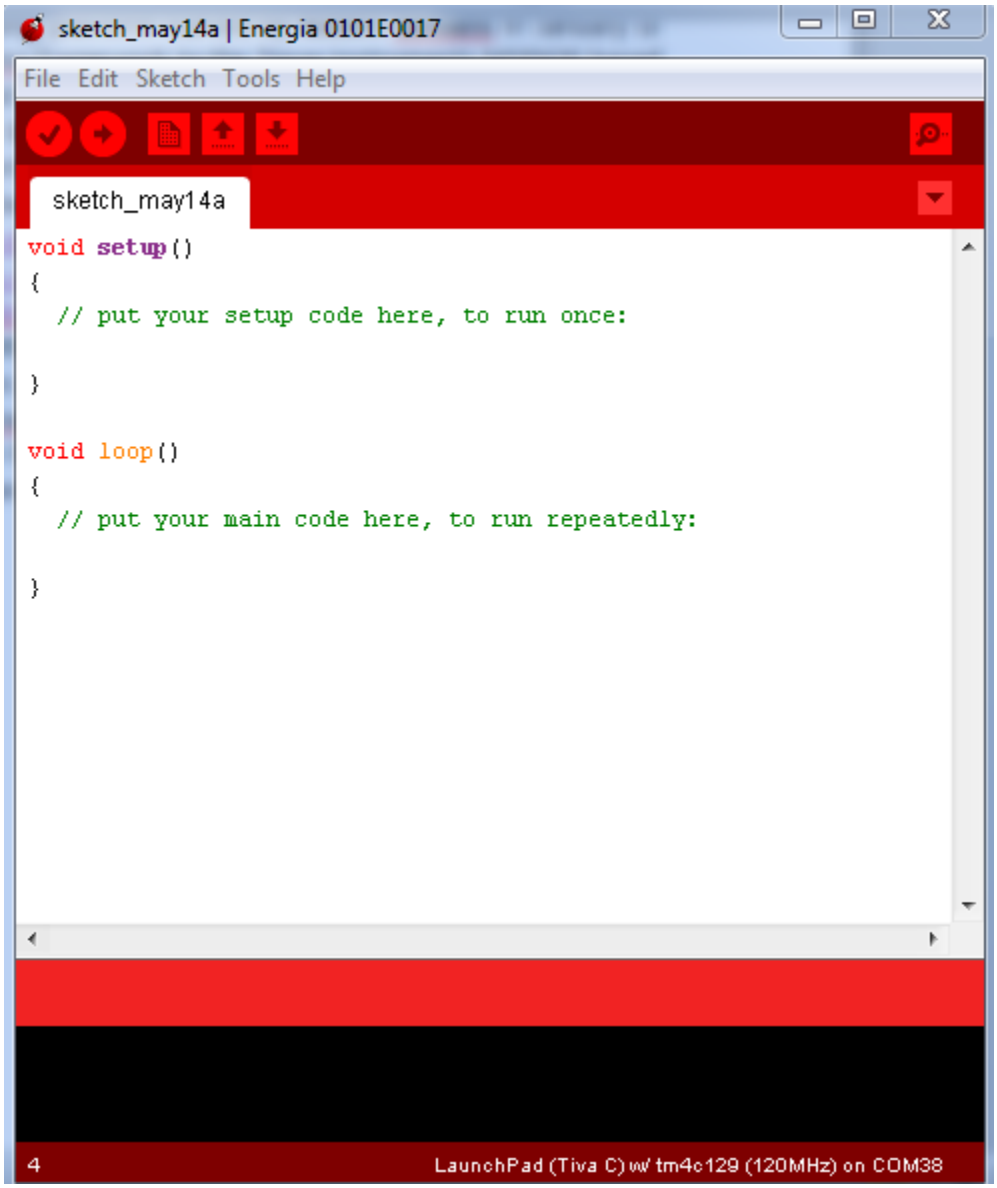
Pin Number	Pin Name	Pin Type	Buffer Type[a]	Description
52	PC0	I/O	TTL	GPIO port C bit 0.
	SWCLK	I	TTL	JTAG/SWD CLK.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	TCK	I	TTL	JTAG/SWD CLK.
53	PD6	I/O	TTL	GPIO port D bit 6.
	M0FAULT0	I	TTL	Motion Control Module 0 PWM Fault 0.
	PhA0	I	TTL	QEI module 0 phase A.
	U2Rx	I	TTL	UART module 2 receive.
	WT5CCP0	I/O	TTL	32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.
54	VDD	-	Power	Positive supply for I/O and some logic.
55	GND	-	Power	Ground reference for logic and I/O pins.
56	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 24-12 on page 1373 .
57	PB5	I/O	TTL	GPIO port B bit 5.
	AIN11	I	Analog	Analog-to-digital converter input 11.
	CAN0Tx	O	TTL	CAN module 0 transmit.
	M0PWM3	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
	SSI2Fss	I/O	TTL	SSI module 2 frame signal.
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
58	PB4	I/O	TTL	GPIO port B bit 4.
	AIN10	I	Analog	Analog-to-digital converter input 10.
	CAN0Rx	I	TTL	CAN module 0 receive.
	M0PWM2	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
	SSI2Clk	I/O	TTL	SSI module 2 clock.
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
59	PE4	I/O	TTL	GPIO port E bit 4.
	AIN9	I	Analog	Analog-to-digital converter input 9.
	CAN0Rx	I	TTL	CAN module 0 receive.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0PWM4	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
	M1PWM2	O	TTL	Motion Control Module 1 PWM 2. This signal is controlled by Module 1 PWM Generator 1.
	U5Rx	I	TTL	UART module 5 receive.

Pin Number	Pin Name	Pin Type	Buffer Type[a]	Description
60	PE5	I/O	TTL	GPIO port E bit 5.
	AIN8	I	Analog	Analog-to-digital converter input 8.
	CAN0Tx	O	TTL	CAN module 0 transmit.
	I2C2SDA	I/O	OD	I^2C module 2 data.
	M0PWM5	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.
	M1PWM3	O	TTL	Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.
	U5Tx	O	TTL	UART module 5 transmit.
61	PD0	I/O	TTL	GPIO port D bit 0.
	AIN7	I	Analog	Analog-to-digital converter input 7.
	I2C3SCL	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0PWM6	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
	M1PWM0	O	TTL	Motion Control Module 1 PWM 0. This signal is controlled by Module 1 PWM Generator 0.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
	SSI3Clk	I/O	TTL	SSI module 3 clock.
	WT2CCP0	I/O	TTL	32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.
62	PD1	I/O	TTL	GPIO port D bit 1.
	AIN6	I	Analog	Analog-to-digital converter input 6.
	I2C3SDA	I/O	OD	I^2C module 3 data.
	M0PWM7	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.
	M1PWM1	O	TTL	Motion Control Module 1 PWM 1. This signal is controlled by Module 1 PWM Generator 0.
	SSI1Fss	I/O	TTL	SSI module 1 frame signal.
	SSI3Fss	I/O	TTL	SSI module 3 frame signal.
	WT2CCP1	I/O	TTL	32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.
63	PD2	I/O	TTL	GPIO port D bit 2.
	AIN5	I	Analog	Analog-to-digital converter input 5.
	M0FAULT0	I	TTL	Motion Control Module 0 PWM Fault 0.
	SSI1Rx	I	TTL	SSI module 1 receive.
	SSI3Rx	I	TTL	SSI module 3 receive.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
	WT3CCP0	I/O	TTL	32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.
64	PD3	I/O	TTL	GPIO port D bit 3.
	AIN4	I	Analog	Analog-to-digital converter input 4.
	IDX0	I	TTL	QEI module 0 index.
	SSI1Tx	O	TTL	SSI module 1 transmit.
	SSI3Tx	O	TTL	SSI module 3 transmit.
	USB0PFLT	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
	WT3CCP1	I/O	TTL	32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

INTRODUCTION TO ENERGIA SOFTWARE

Energia is open-source electronics prototyping platform started by Robert Wessels in January of 2012 with the goal to bring the Wiring and Arduino framework to the Texas Instruments based LaunchPad. The Energia IDE is cross platform and supported on Mac OS, Windows, and Linux. Energia uses the msp-gcc compiler by Peter Bigot and is based on the Wiring and Arduino framework. Energia includes an integrated development environment (IDE) that is based on Processing.



Void Setup()
This is used to initialize the pins of Controller to be used.

Void Loop()
This is used for generating infinite iterations (i.e., repetition) in the program.