1. Description

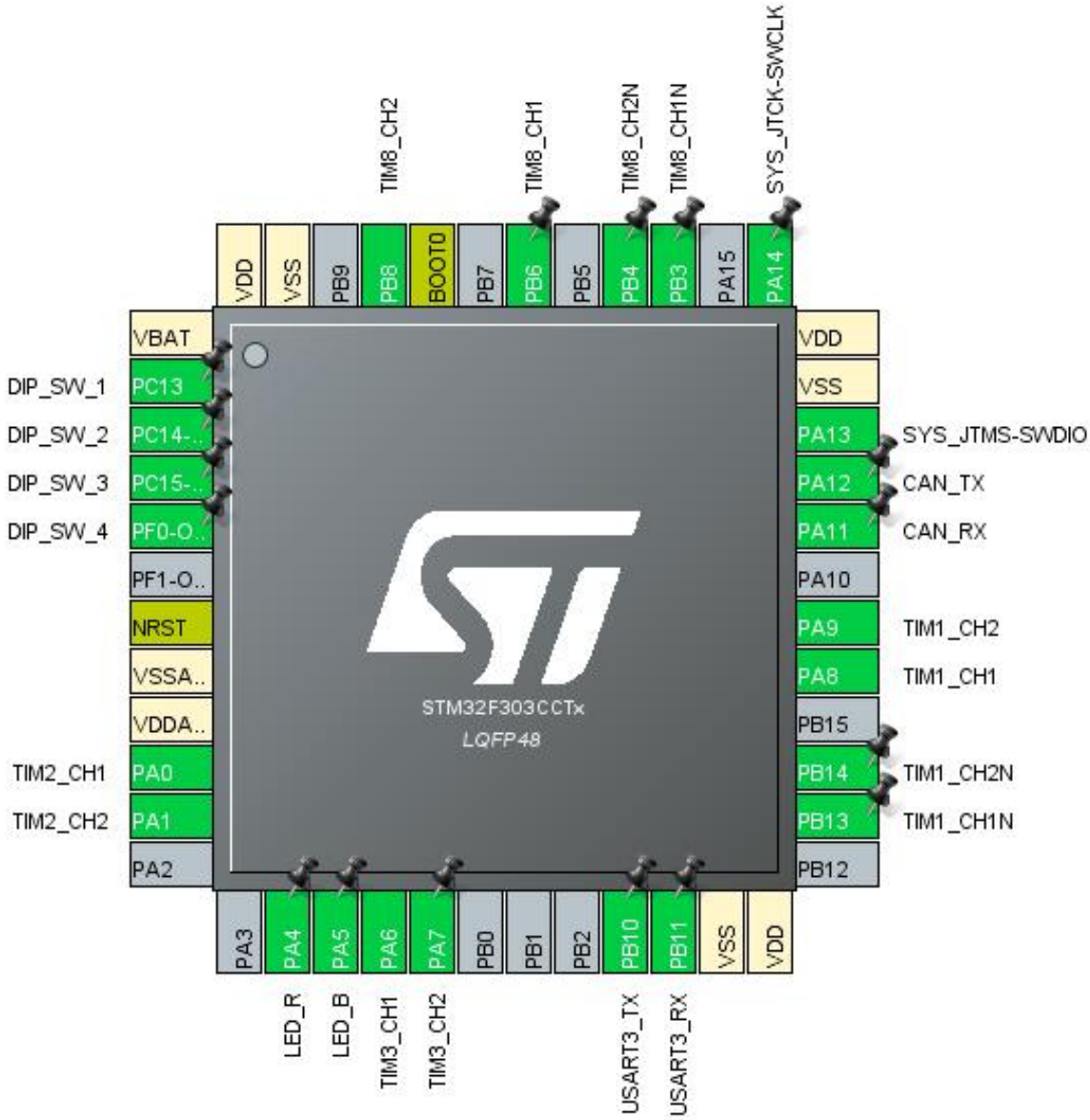
1.1. Project

Project Name	CanmdProject
Board Name	custom
Generated with:	STM32CubeMX 5.2.1
Date	06/13/2019

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303CCTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration

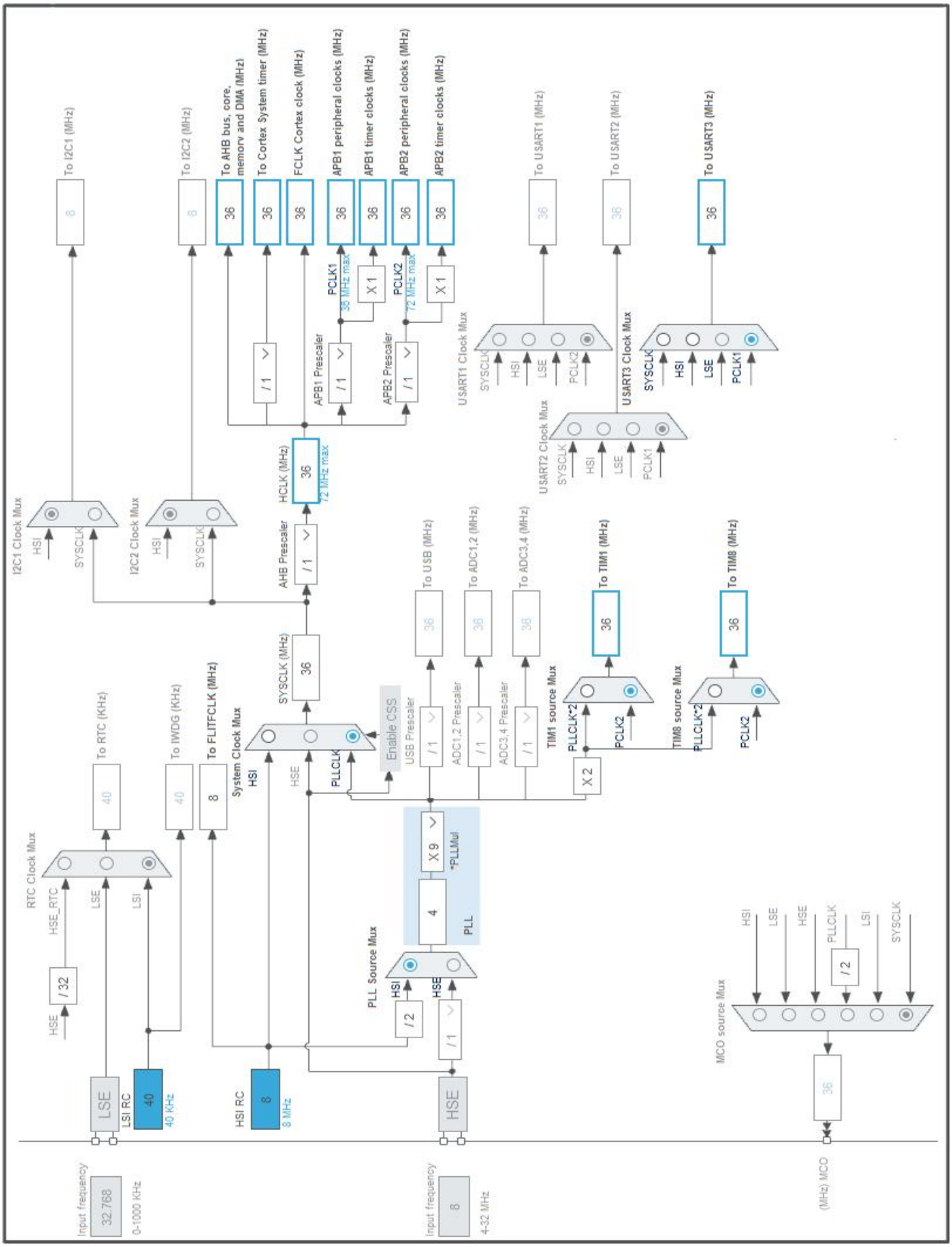


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Input	DIP_SW_1
3	PC14-OSC32_IN *	I/O	GPIO_Input	DIP_SW_2
4	PC15-OSC32_OUT *	I/O	GPIO_Input	DIP_SW_3
5	PF0-OSC_IN *	I/O	GPIO_Input	DIP_SW_4
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	TIM2_CH1	
11	PA1	I/O	TIM2_CH2	
14	PA4 *	I/O	GPIO_Output	LED_R
15	PA5 *	I/O	GPIO_Output	LED_B
16	PA6	I/O	TIM3_CH1	
17	PA7	I/O	TIM3_CH2	
21	PB10	I/O	USART3_TX	
22	PB11	I/O	USART3_RX	
23	VSS	Power		
24	VDD	Power		
26	PB13	I/O	TIM1_CH1N	
27	PB14	I/O	TIM1_CH2N	
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
32	PA11	I/O	CAN_RX	
33	PA12	I/O	CAN_TX	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
39	PB3	I/O	TIM8_CH1N	
40	PB4	I/O	TIM8_CH2N	
42	PB6	I/O	TIM8_CH1	
44	BOOT0	Boot		
45	PB8	I/O	TIM8_CH2	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	CanmdProject
Project Folder	C:\Users\hajime\Documents\SystemWorkbench\CanmdProject
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303CCTx
Datasheet	023353_Rev13

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. CAN

mode: Mode

7.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**6 ***
Time Quantum	**166.66666666666669 ***
Time Quanta in Bit Segment 1	**3 Times ***
Time Quanta in Bit Segment 2	**2 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.2. RCC

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.3. SYS

Debug: Serial Wire
Timebase Source: SysTick

7.4. TIM1

Channel1: PWM Generation CH1 CH1N
Channel2: PWM Generation CH2 CH2N

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**18 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**PWM_PERIOD ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	**18 ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	**PWM_DUTY_ZERO ***
Fast Mode	Disable

CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	**PWM_DUTY_ZERO ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.5. TIM2

Combined Channels: Encoder Mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFF ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.6. TIM3

Combined Channels: Encoder Mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.7. TIM6

mode: Activated

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**319 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. TIM7

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**6399 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. TIM8

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**18 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**PWM_PERIOD ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	**18 ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	**PWM_DUTY_ZERO ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	**PWM_DUTY_ZERO ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN	PA11	CAN_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA12	CAN_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PB13	TIM1_CH1N	Alternate Function Push Pull	No pull up pull down	Low	
	PB14	TIM1_CH2N	Alternate Function Push Pull	No pull up pull down	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull up pull down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull up pull down	Low	
TIM8	PB3	TIM8_CH1N	Alternate Function Push Pull	No pull up pull down	Low	
	PB4	TIM8_CH2N	Alternate Function Push Pull	No pull up pull down	Low	
	PB6	TIM8_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PB8	TIM8_CH2	Alternate Function Push Pull	No pull up pull down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
GPIO	PC13	GPIO_Input	Input mode	**Pull up ***	n/a	DIP_SW_1
	PC14-OSC32_IN	GPIO_Input	Input mode	**Pull up ***	n/a	DIP_SW_2
	PC15-OSC32_OUT	GPIO_Input	Input mode	**Pull up ***	n/a	DIP_SW_3
	PF0-OSC_IN	GPIO_Input	Input mode	**Pull up ***	n/a	DIP_SW_4
	PA4	GPIO_Output	Output Push Pull	No pull up pull down	Low	LED_R
	PA5	GPIO_Output	Output Push Pull	No pull up pull down	Low	LED_B

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USB low priority or CAN_RX0 interrupts	true	7	0
Timer 6 interrupt and DAC underrun interrupts	true	6	0
TIM7 global interrupt	true	1	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority or CAN_TX interrupts	unused		
CAN RX1 interrupt	unused		
CAN SCE interrupt	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
TIM8 break global interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger com interrupt	unused		
TIM8 capture compare interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

9. Software Pack Report