Weekly Report – 21.01.2019

Balanced Conditions

- Single Module
  - Device
  - Capacitor ESL
  - Power Loop Ind.
  - Commutation Ind.
- Parallel Modules
  - Interleaving
  - Switching Frequency
  - Module Connection Ind.
- Series Modules
  - Interleaving
  - Switching Frequency
  - Module Connection Ind.

Unbalanced Conditions

- Single Module
  - Capacitance Unbalance
  - Load Unbalance Among Phases
- Parallel Modules
  - Capacitance Unbalance
  - Load Unbalance Among Modules
    - Power Rating
    - Power Factor
  - Module Connection Ind.
- Series Modules
  - Capacitance Unbalance
  - Load Unbalance Among Modules
    - Power Rating
    - Power Factor

BALANCED CONDITIONS

Single Module

Figure 1: A view of single module

- Power Loop Inductance and device speed determines how much stress is generated on a phase capacitor. (Lp*di/dt)
- For a three phase system, if the commutation inductances don't exist, the stress generated by each phase is distributed equally to all capacitors.
- Commutation inductances are the main reason of the capacitor isolation; in other words, a capacitor cannot share its stress if there is a large inductive connection to other capacitors.
- Capacitor ESL increases the response time of a capacitor; that is, a high ESL capacitor becomes unwilling to overcome the stress. Having that, it may increase the power loop inductance or it behaves reluctantly to generated stress on a phase. This explains why high-frequency by-pass ceramic capacitors are used.

Parallel Modules

Figure 2: Parallel Connection Scheme
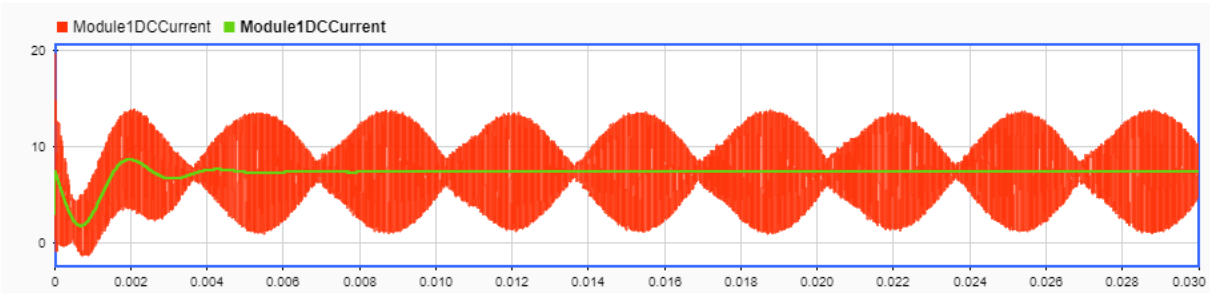
Figure 3: Module Input Current with and without Interlaving
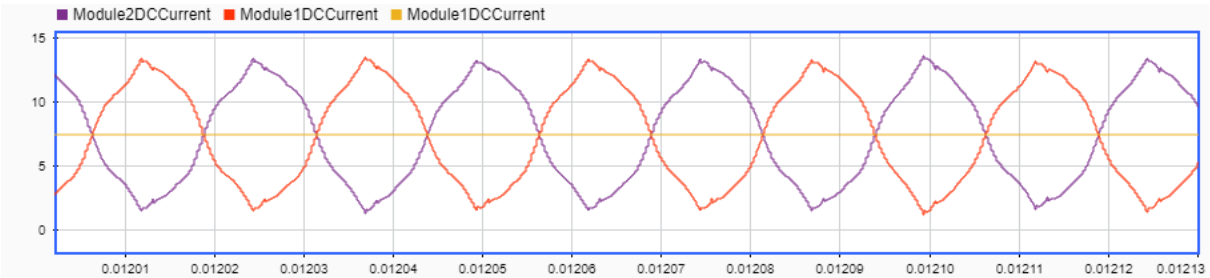
Figure 4: Module 1 and Module 2 Input Currents
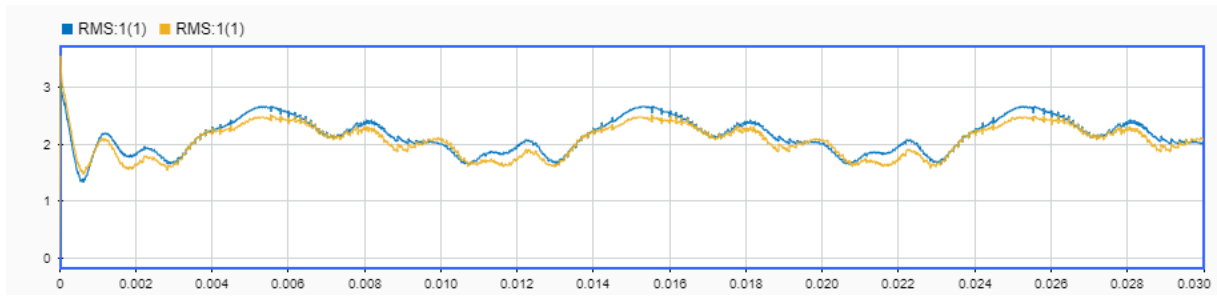
Figure 5: RMS of Capacitor Current without and with interlaving

- Interlaving reduces the stress on a capacitor by cancelling the ripples of two modules.
- Interlaving causes oscillation on module currents. Since we have a DC voltage on input side of a module, the oscillating current means reactive power transfer among the modules.
- Oscillating current might cause EMI problems.
- Note that, interlaving breaks the symmetry between modules; therefore, a stress generated on a module affect other modules.
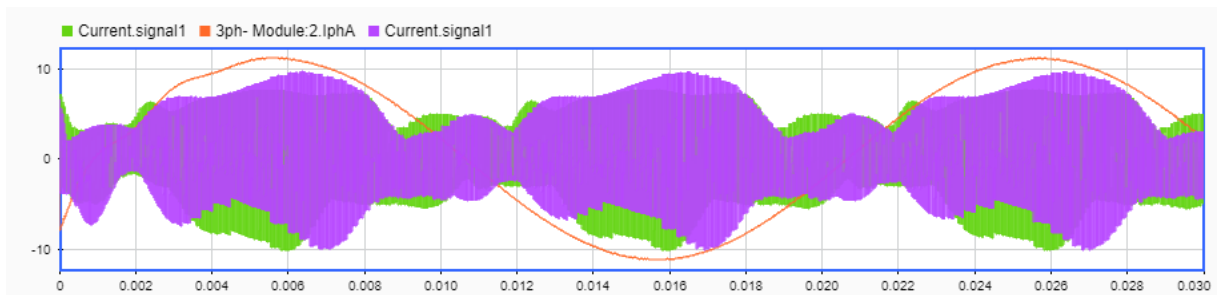
Figure 6: Capacitor Current Waveform for 40kHz (Green) and 80kHz (Purple) switching frequency
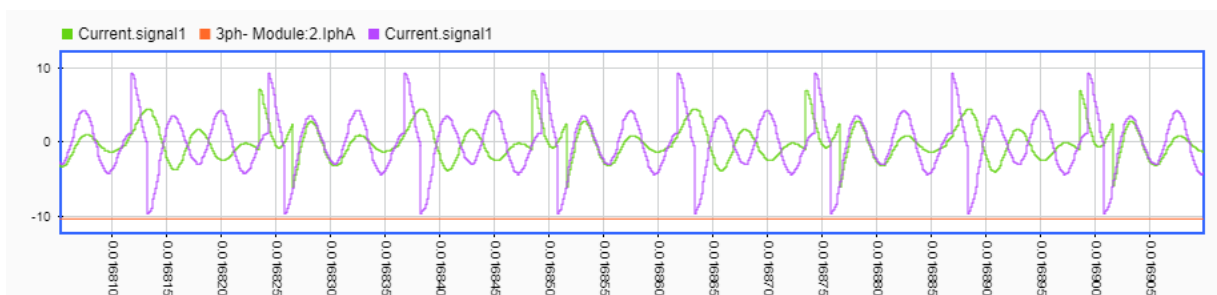
Figure 7: Capacitor Current Waveform (Zoomed)
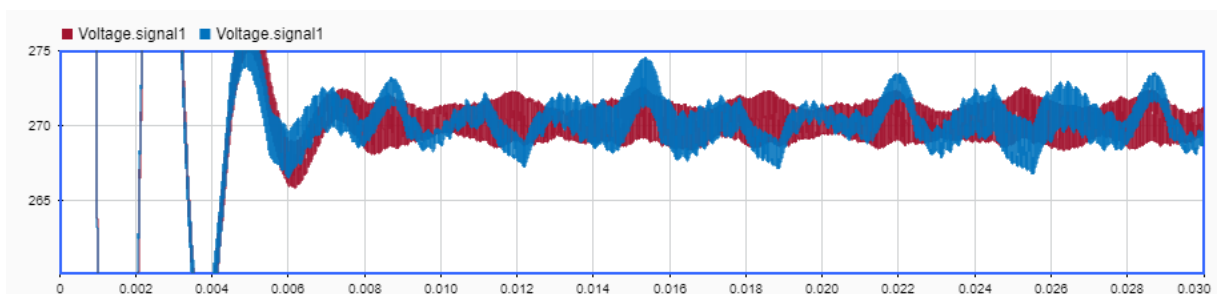
Figure 8: Capacitor Voltage Waveform for 40kHz (Brown) and 80kHz (Blue) switching frequency
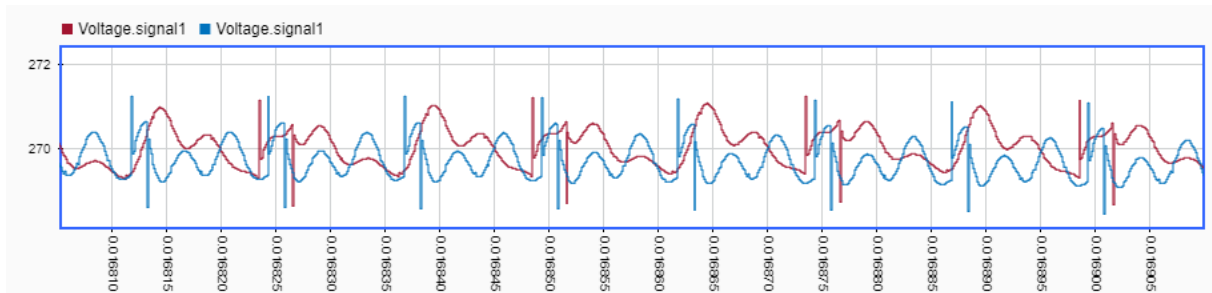
Figure 9: Capacitor Voltage Waveform (Zoomed)

- Effect of switching frequency is more complex than it assumed. Simply increasing switching frequency results in lower stress.
- For an inverter structure including commutation inductances, an oscillation takes time to damp. If two successive step changes are applied and if the settling time is longer than the period, it means the oscillations will be high in amplitude. So, for increased switching frequency we observe larger oscillation for some cases.
- The amount of commuted current is also important, i.e. the step function amplitude. Therefore, for the different levels of load current, oscillations observed with different amplitudes.
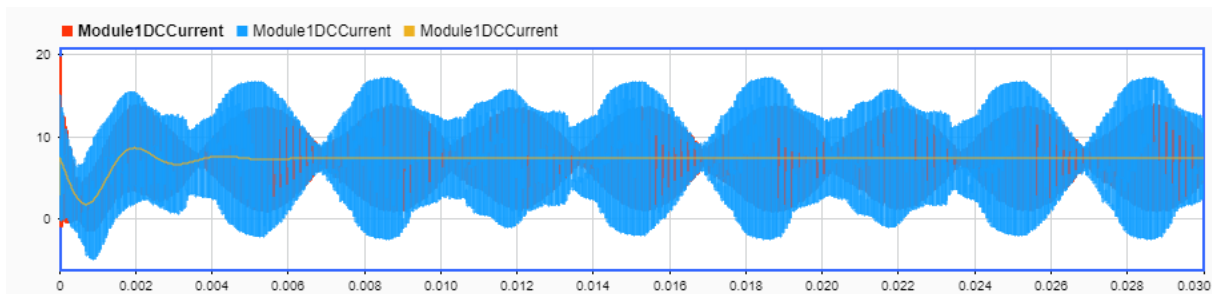
Figure 10: Module Current Waveforms with and without Module Connection Inductances (Orange is with conn. Induct.)
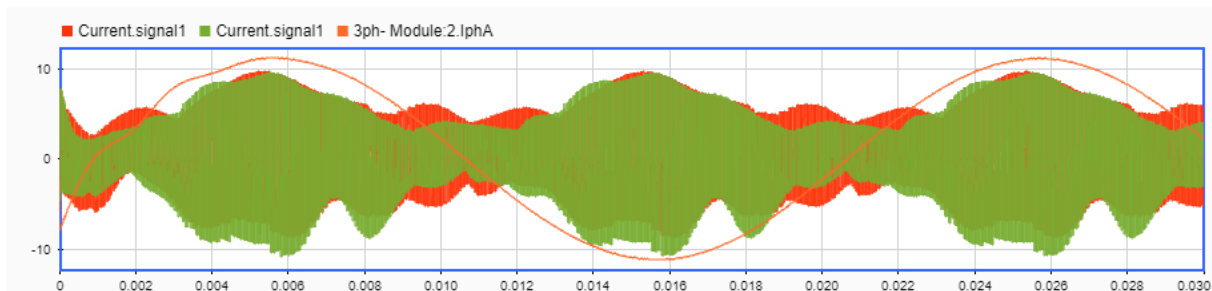

Figure 11: Capacitor Current Waveform with (red) and and without (green) Module Connection Inductances

- For parallel structure, having low module connection inductances acts as if it is a six phase module; that is, six capacitors can share their stress to the extent permitted by commutation inductances.
- Since the commutation inductances are unbalanced, if there is no connection inductance we observe asymmetric module current oscillation because each time the module generates unbalanced response for the unbalanced stress sources in other module. It is the reason for module current waveforms in Figure 10.
- In Figure 11, it is seen that a phase stress increases with connection inductance when the other phase currents are around their peak.
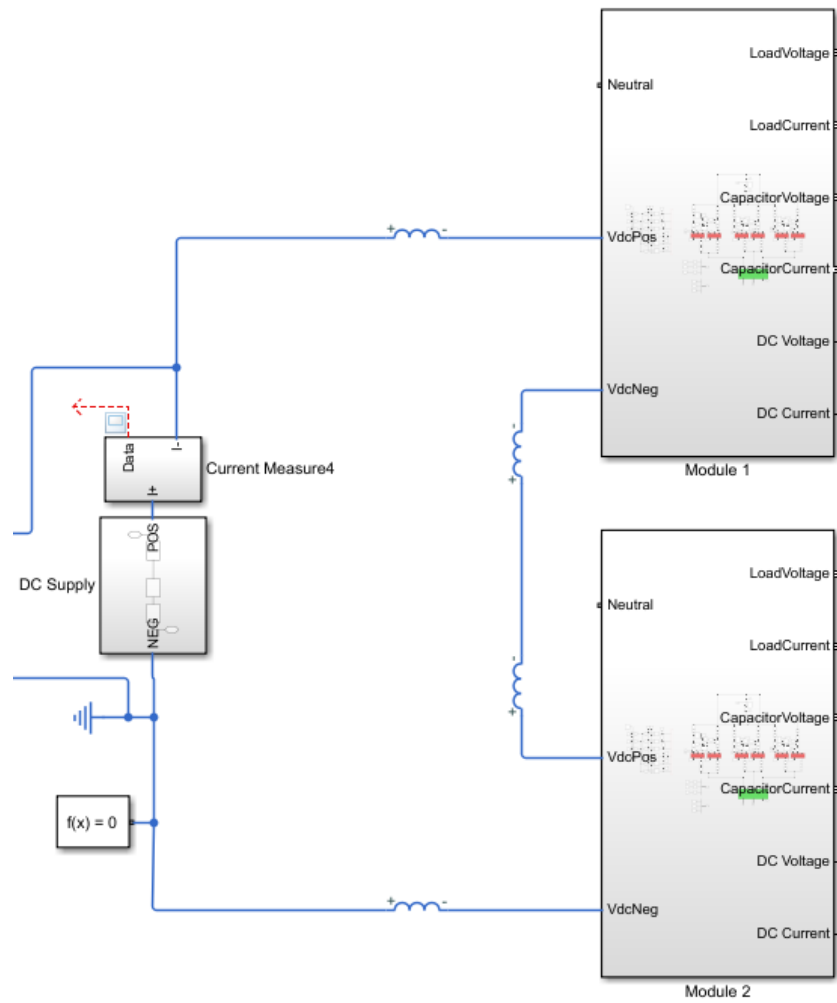
Series Modules
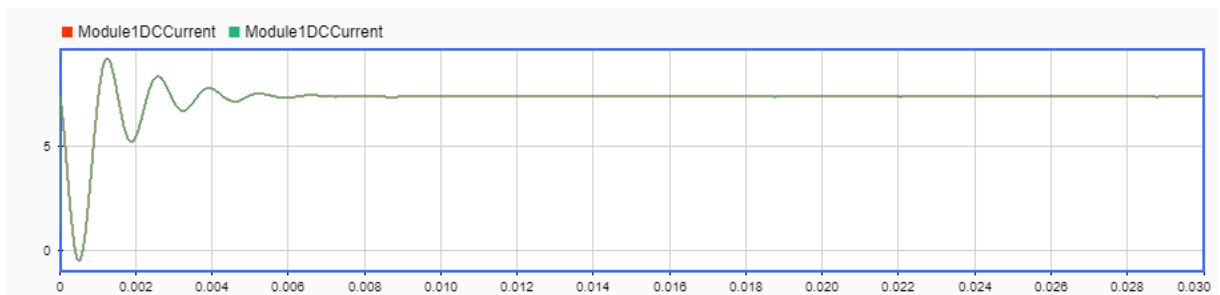

Figure 12: Series Connection Scheme

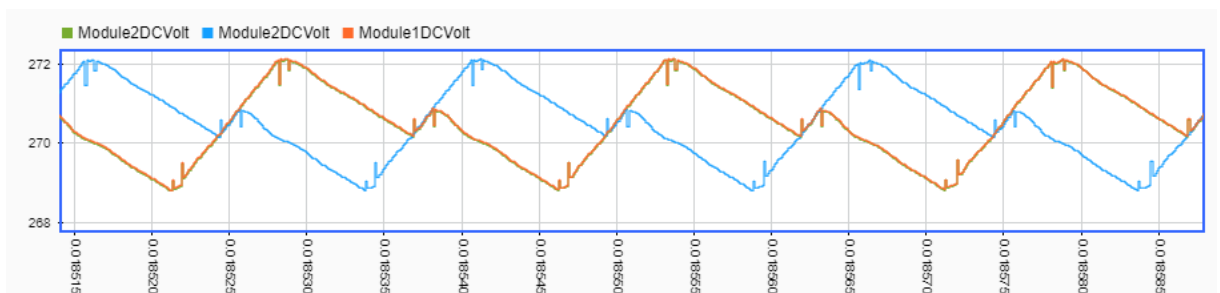*Figure 13: Module Currents with and without interlaving*

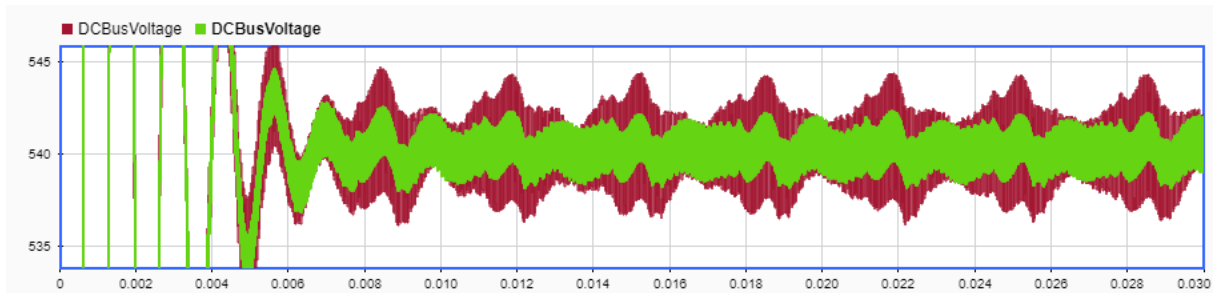*Figure 14: Module DC Voltages with (Blue-Orange) and without (Green) interlaving*

Figure 15: DC Bus Voltage without and with interlaving

- Since modules are connected in series now it is impossible to cancel the current ripples because the same current flows through the both modules.
- Since the module voltage ripple shifts with interlaving, the DC supply ripple reduces.
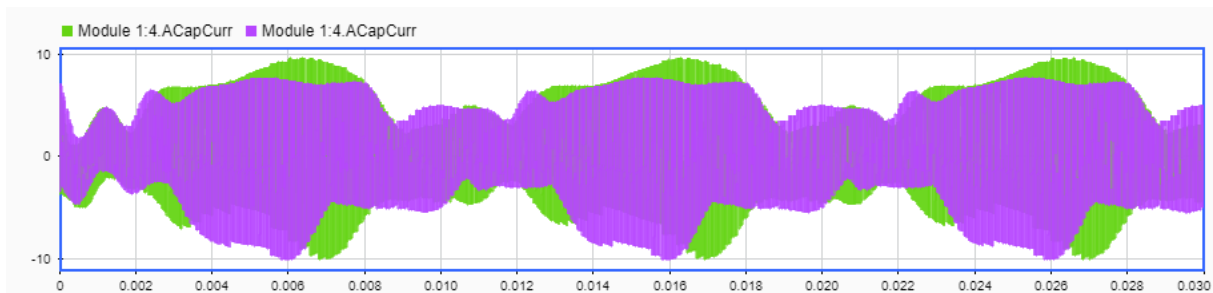- The most important gain of the series connection is reduced voltage stress on the devices.

Figure 16: Capacitor Current Waveform for 80 kHz(green) and 40 kHz(purple) switching frequency

- The same comment with parallel connection is valid for series connection as well.
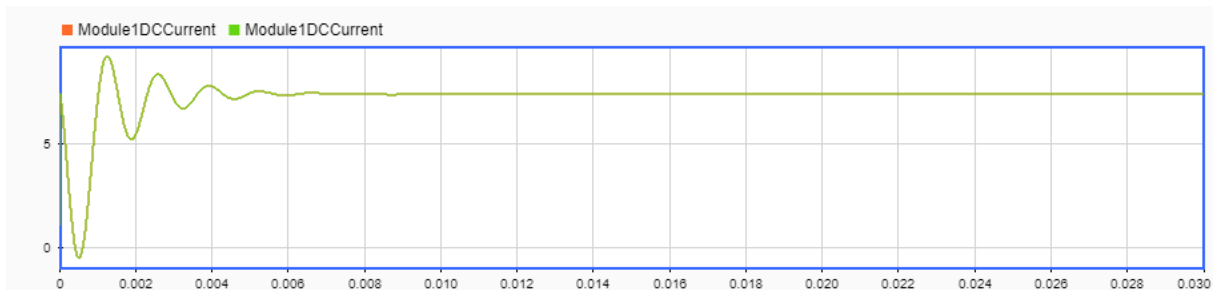

Figure 17: Module current waveform with and without module connection inductances

- For a line carrying DC current, inductor behaves as a short circuit. Therefore, for the series connection, module connection inductances are not effective.
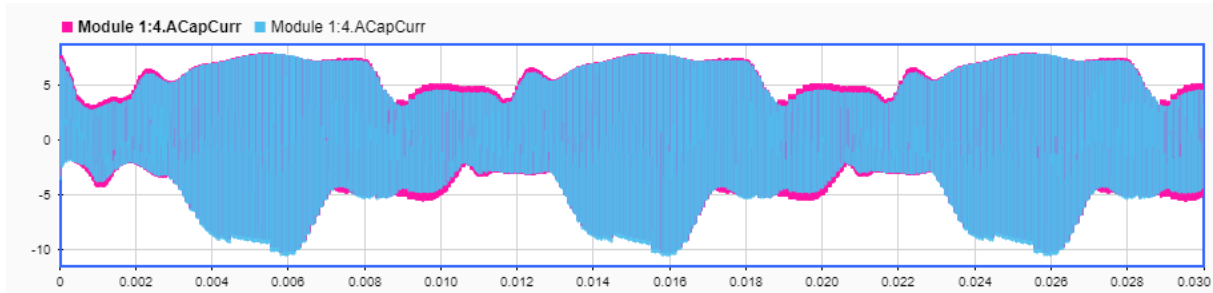
UNBALANCED CONDITIONS

Single Module

Figure 18: Phase A Capacitor Current for 5u, 5u, 5u (Pink) and 4.5u, 5u, 5.5u (Blue) Phase Capacitors
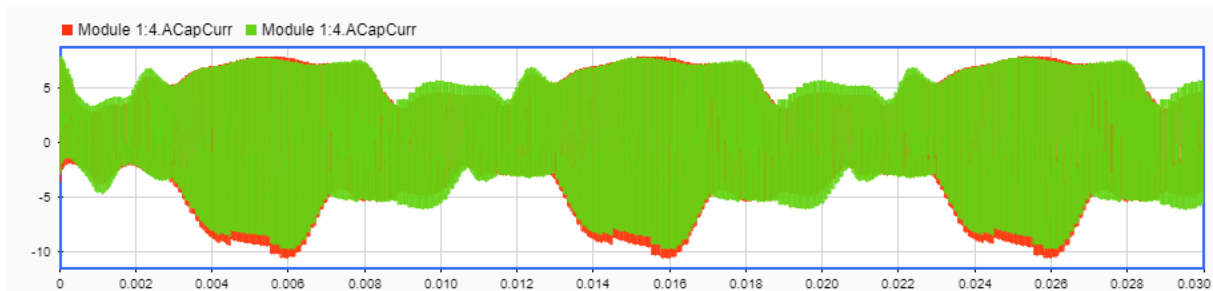

Figure 19: Phase A Capacitor Current for 5.5u, 5u, 4.5u (Pink) and 5.5u, 5u, 4.5u (Green) Phase Capacitors

- It is observed that the tolerance differences of the capacitors have minimal effects on current and voltage ripple. In other words, capacitor's tolerance (%10) is tight enough.
- For a single module, the capacitance differences becomes more significant if there is no commutation inductance.
- For a single module, the capacitor stress increases around the peak value of that phase load current if capacitance is lower. However, the stress reduces around the peak of other phase currents for low capacitances. Besides all these, the stress difference is very small.

Parallel Modules

Table 1: Percent Ripple of Module Voltages

Percent Ripple of Module Voltages	With Interlaving	Without Interleaving
1.5u	2.63	1.93
5u	0.63	1.33
8.5u	0.82	1.37

- The results shown in Table 1 indicates that interlaving enables the stress sharing among modules and so the low capacitance takes the higher stress.
- Results show that effect of interleaving reduces with increasing module connection inductances.

Table 2: Mean of RMS of Capacitor Current

Mean of RMS value of Capacitor Current	With Interleaving	Without Interleaving
1.5u	2	1.82
5u	2.1	2.15
8.5u	3.26	3.33

Table 3: Peak value of RMS of Capacitor Current

Peak value of RMS of Capacitor Current	With Interleaving	Without Interleaving
1.5u	2.7	2.3
5u	2.5	2.66
8.5u	3.8	3.8

- The modules with different capacitors share stress unequally. For module with low capacitances the stress reduces smally whereas the stress increases significantly for the module with high capacitances.

Series Modules

Series Modules