28.02.2019

Date: 28.02.2019

Attendees: Mesut Uğur, Furkan Karakaya

Location: Electrical Machines Laboratory

Target: V1.1 Gate Driver Board

Test type: Double Pulse Test

Aims before the test:

1. To observe the effect of Ron resistance to 9V supply, bottom gate waveform (at false turn-on) and top gate waveform (during miller region) when load is connected to bottom switch.

2. To understand the reason behind the secondary peak occuring during the false turn-on duration

Conditions: Phase-A, 22 Ohm Ron, 2 Ohm Roff.

Steps:

1. For phase A, it is tried to observe the 9V and Vgs voltages of bottom side transistor simultaneously. With LeCroy, three different probes are soldered such that one is connected to Vgs and the other probes are connected to P6V and N3V nodes. It is assumed that the 9V can be followed differentially while the trigger is taken using the Vgs voltage. However, due to layout mismatch between P6V-GND and N3V-GND, the voltage seen differentially is not correct.

2. Then, with isolated oscilloscope (Tektronix), it is tried to measure 9V and Vgs with two different probes. When the Vgs voltage is checked for false turn-on (FTO) period, the result was wrong. Also, the Vgs FTO waveforms is compared for LeCroy and Tektronix and as a conclusion, LeCroy is favored and it is said that isolated oscilloscope is not working fine.

3. Since we decided to continue with LeCroy, we cannot measure 9V and Vgs at the same time and it is not possible to get trigger correctly while measuring 9V. Therefore, only Vgs is followed for different voltage levels without any additional ceramic capacitor soldered to 9V. At that time, only 33uF tantalum capacitor is present.

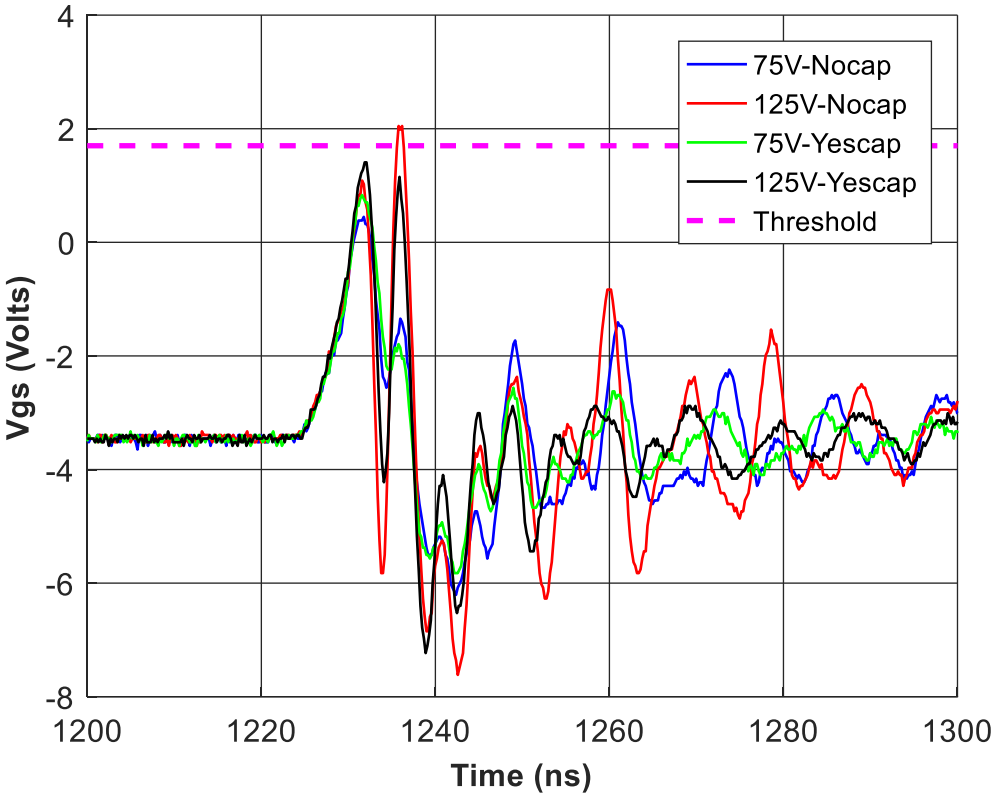
4. A 1uF ceramic capacitor is soldered near the 9V tantalum capacitor so that it can be seen whether ceramic capacitor helps suppressing the Vgs oscillation or not. It is observed that the amplitude of first peak seen in the FTO period is increased but not to a risky value. However, the second peak is suppressed significantly such that it is lower than first peak. Without ceramic capacitor, the second peak was nearly 2.1V for 125V DC wherease it is reduced to 1.4V with this capacitor. Therefore, we decided to increase the DC voltage level and increased up to 200V. The peak values were fine for these voltage levels. The waveforms are shown at the end of this document.

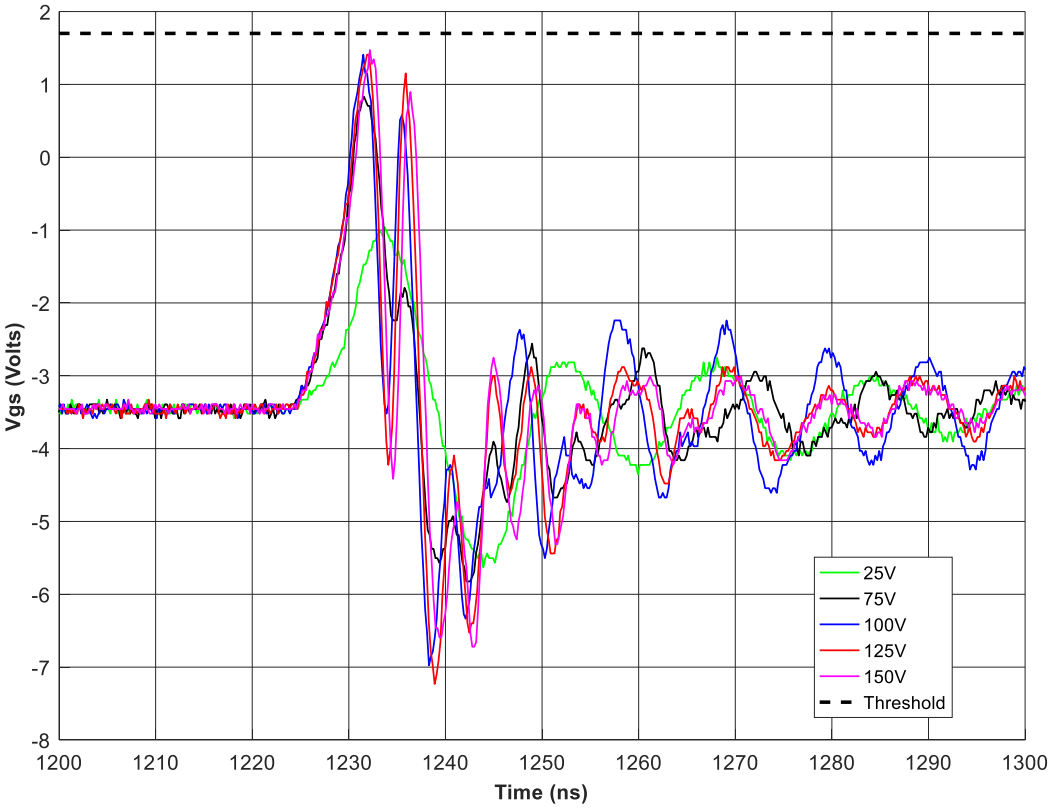
5. Then, to increase the voltage further and to limit the load current we increased the load inductance. When we re-checked the peak values for the same voltage levels, it is observed that the peaks are increased. So, it means the load current also affects the FTO peak values. However, the relation between those values and load current could not be explained. The results suggest that, when the load current increases, the oscillation peak during FTO decreases.

28.02.2019

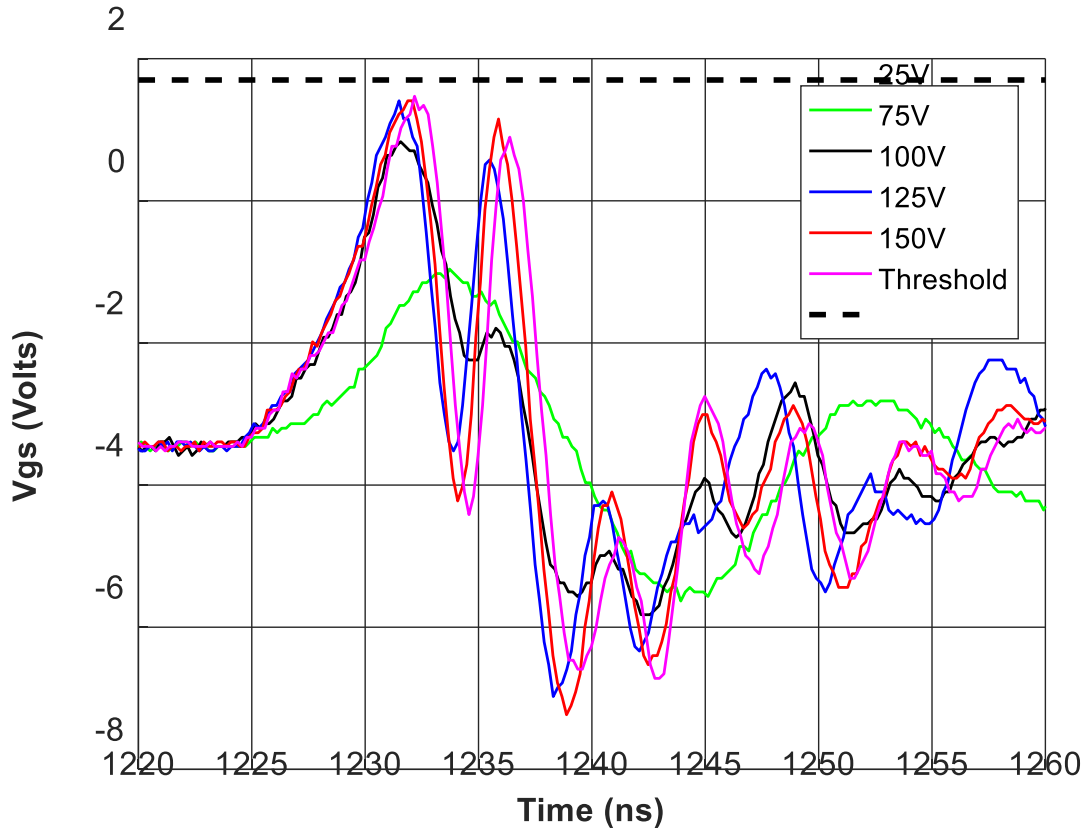
Results:

All the results are for a load inductance value of ___ mH (stage 4 of the load bank). Charging time is 2.5 ms.





28.02.2019



The data for 50V, 175v and 200V are corrupted. They will be fetched from the Lecroy.

What to do next:

1. For a different load inductance (should be at stage 2), the test will be repeated for 22 Ohm Ron. Then, it will be repeated for 10 Ohm Ron and 15 Ohm Ron.

2. The bottom switch gate voltage waveform when load is connected to top switch will be observed during potential FTO duration. The behavior during Miller region will be observed.