Investigation of the Effects of Parasitic Components on Parallel and Series Connected Modular Motor Drives

Abstract: In this paper, the effect of parasitic inductances on power semiconductor device stress, DC link capacitor current ripple and DC link voltage ripple in a motor drive are investigated. A GaN based motor drive inverter module designed for an Integrated Modular Motor Drive (IMMD) application is considered. The actual capacitor current stress in a single module is shown to be much more adverse when the commutation inductances are taken into account. The change in the interleaving scheme is discussed when the connection inductances between inverter modules that are connected in series or parallel are considered. A comparison between series and parallel connection in a modular motor drive is performed with several aspects.

1 Introduction

Integrated modular motor drives (IMMD) gained special interest in recent years to replace the conventional motor drives thanks to their high power density and fault tolerance capability. By the modularization of motor drive, redundancy of the motor drive system can be increased which is especially desired in safety critical applications [1]. Moreover, power semiconductor devices having lower ratings can be utilized such as Gallium Nitride (GaN) Field Effects Transistors (FETs) resulting in higher efficiency and higher power density [2].

There are several IMMD studies which use different types of modularity in terms of DC link connection, such as series connected [2] and parallel connected [1] topologies. In series connected drives, the main motivation is to be able to utilize low voltage GaN devices in a higher DC link voltage. Moreover, it is aimed to reduce the DC link current ripple by using gate signal interleaving between modules [3]. Parallel connection is usually used to distribute the heat dissipation and reduce the size of DC link capacitors via interleaving [4].

Connection of several voltage source inverters (VSI) in a modular fashion brings its own challenges. In addition to the conventional speed and current control strategies, synchronous control of multiple modules is necessary. Potential circulating currents and unbalanced voltages may also occur under abnormal operating conditions. Moreover, the parasitic components due to the physical connections between the modules may result in unbalanced stress on module capacitors.

Careful power loop and DC bus layout design and connection architecture is required in order to

minimize these effects, however too few studies in the literature give special attention to parasitic component effects in modular drive topologies. In [5], two candidate DC bus architectures are proposed and compared in terms of DC bus current oscillations due to layout inductances.

In this paper, the effects of PCB parasitic inductances are investigated in a GaN based 8 kW IMMD where both series and parallel connection is applied. The voltage overshoots on GaN voltages due to power loop inductance are investigated. The actual DC link capacitor current stress and voltage ripples are analyzed considering commutation inductances between phases. Series and parallel connected inverter modules and the effect of connection inductances to their performance are analyzed.

Referanslarmz: [1], [6], [2], [5], [4], [3]

2 Description of the IMMD System

The IMMD system is composed of 4 identical modules which are to be connected in 2-series and 2-parallel fashion on the DC link. A 2 kW 3-phase GaN based motor drive inverter modules printed circuit board (PCB) and a control and power distribution PCB are designed for the system. The specifications are listed in Table 1.

Table 1: IMMD system specifications

Parameter	Value	Parameter	Value
Total output power	8 kW	DC link voltage	540 V
Number of modules	4	Motor speed	600 rpm
Phase induced voltage	80 Vrms	Line current	8.5 A
GaN breakdown voltage	650 V	GaN continuous current	30 A

2.1 GaN based motor drive module

The picture of the GaN based 3-phase inverter module of the IMMD system is shown in Fig. 1 excluding the heat sink. The module consists of half-bridge legs with GaN FETs. Each leg has a 5 μF metal film capacitor, isolated gate driver circuit dedicated to each GaN and a phase current measurement circuit. In order to overcome the challenge of size reduction due to integration, it is aimed to reduce the size of DC link capacitors and heat sink by utilizing GaN FETs at high switching frequency. The DC link capacitor size is determined according to required capacitance which is calculated based on voltage ripple and required current rating [4], by also taking the effect of interleaving into account. The layout design is based on keeping gate loop and power loop

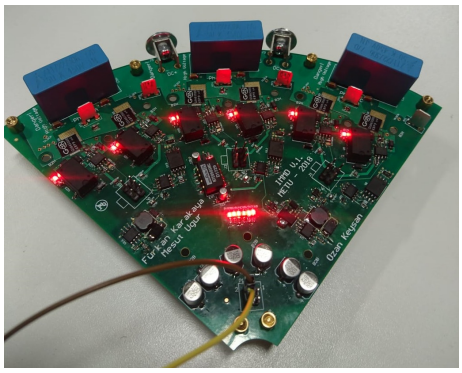
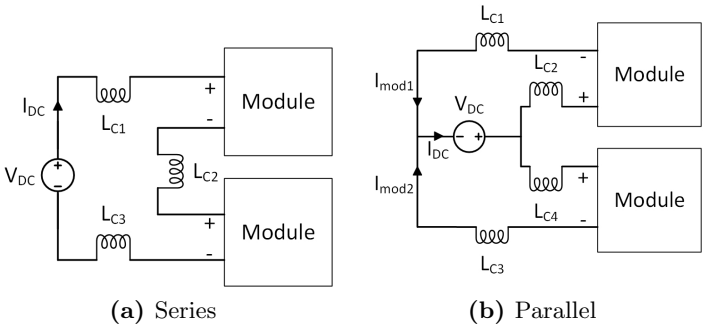


Fig. 1: GaN based 3-phase inverter module



(a) Series **(b)** Parallel

Fig. 2: Series and Parallel Connected Modules Configurations

inductances as well as keeping DC link capacitors as close as possible. Ceramic capacitors are also added to the half-bridge layout to reduce the voltage overshoots.

2.2 Parasitic Inductances

In physical realization of power electronics circuit, the parasitic inductances of the layout is an important consideration especially for the paths carrying switched current. For the inverter circuit given in Fig. 1, the power loop and commutation loop inductances are identified using Ansys Q3D tool and given in Fig. 3. The power loop is a closed path including half-bridge switches, a DC link capacitor and parasitic inductances which connects them each other . Another closed path is the commutation loop which includes two DC link capacitors and the parasitic inductances between the capacitors. The commutation loop is effective between any two phases of the system whenever a current commutes from one phase to another one. In the following sections, these two loops will be discussed in detail.

2.3 Series and Parallel Connection

As shown in Fig. 2, two modules can be connected in series or parallel. The inductances given in Fig. 2a, L_{C1}, L_{C3}, are total equivalent inductors of connectors and module to supply terminal connections. Similarly, L_{C2} represents the total inductance of connectors and module to module connection. In addition, the equivalent inductors are shown in Fig. 2b for parallel connection where L_{C1} & L_{C3}, L_{C2} & L_{C4} represents the total equivalent inductance from module to supply negative and positive terminals, respectively.

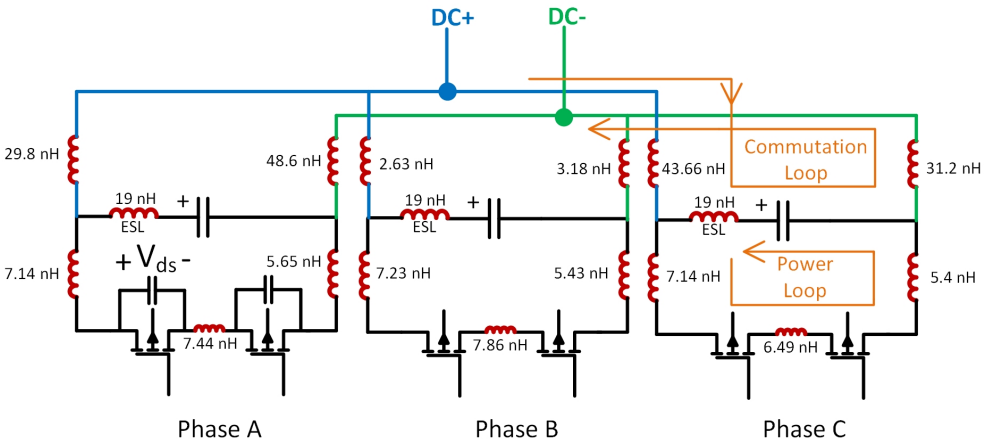


Fig. 3: Parasitic Inductance Map of a Single Module

3 Investigation of a Single Inverter Module

3.1 Effect on Power Device Stress

In physical realization of power electronics circuit, the parasitic inductances of the layout is an important consideration especially for the paths carrying switched current. In Fig. 3, an inductance map is given for the designed three phase inverter system as shown in Fig.1. In an inverter structure, two loops are critical for device and capacitance stresses. As shown in Fig. 3, the power loop includes two switches and the phase capacitor. When the phase current transfers from one of the switch to other switch in a half-bridge, the power loop parasitic inductances cause either a voltage overshoot or undershoot on a switch's drain-source terminals as much voltage as $L_p * di/dt$. Considering the high current rise and fall time capability of GaN HEMTs, i.e. high di/dt, the power loop inductance is very the most important factor for device stress.

3.2 Effect on DC link Capacitor Stress

As seen in Fig. 1, a distributed DC bus architecture is designed on each module where each half-bridge leg has its own capacitor in close proximity. These capacitors are used to supply and sink the current ripple during switching periods. The power loop inductances are not effective on these capacitors' stress assuming ceramic capacitors with small ESL are placed in much closer proximity.

When an ideal inverter is considered with a single DC bus capacitor, it is seen that commutation of all the phases are reflected to this capacitor. When the capacitors are distributed and the parasitic

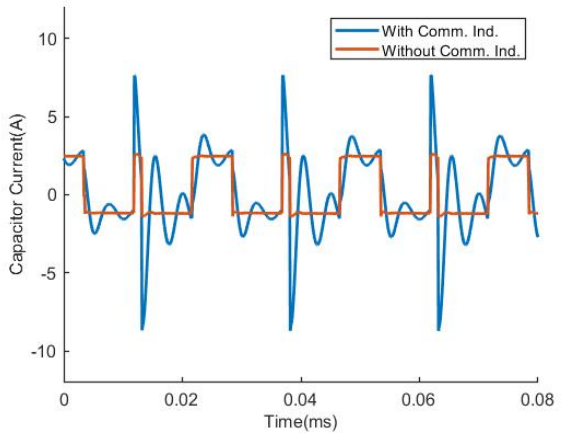


Fig. 4: DC bus capacitor current ripple with and without commutation loop inductances

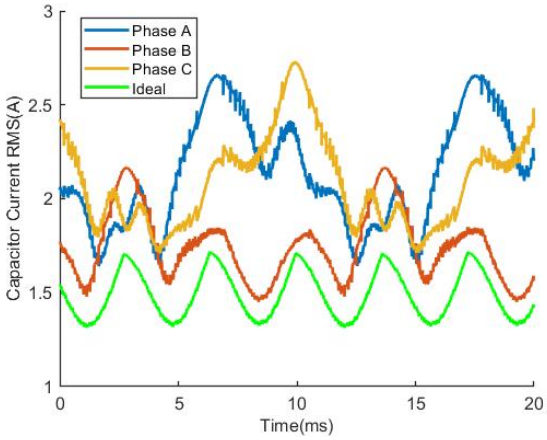


Fig. 5: Waveform of RMS values of capacitor currents with and without commutation inductances

inductances are of considerable amount, the stress of individual capacitors increase on the peak of corresponding phase current due to the longer path which the other capacitors have. This situation is visualised in Fig. 4. This results in higher capacitor RMS currents than analytically calculated and must be taken into account as the selected capacitor temperature may increase too much, eventually shortening its lifetime. On the other hand, this effect is not significantly reflected to the voltage ripple.

Stress sharing olay ve arada doan farkn nemi

Mmknse voltage ripple experimental datas

4 Investigation of Series and Parallel Connection

Modler yapya dair motivasyon (ksaca)

4.1 Series Connection

The fundamental motivation behind series connection of inverter modules is the reduction of module DC bus voltage. It is persistently emphasized in [3], [6] and [2] that the application of interleaving in series connection reduces the size of DC bus capacitors. However, it is not entirely true. The DC bus voltage ripple of each module along with total DC bus are shown in Fig. 6. It has been shown that interleaving only reduces the ripple on total DC bus ripple which has no positive effect on the system since the module voltages always has the ripple. Moreover, the capacitor ripple currents are not affected by interleaving since it is simply impossible to have a different current when modules are connected in series. For this very reason, the connection inductances between

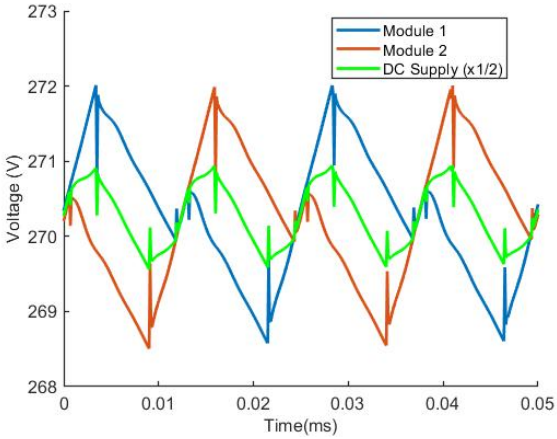


Fig. 6: DC bus voltage ripple in series connected modules

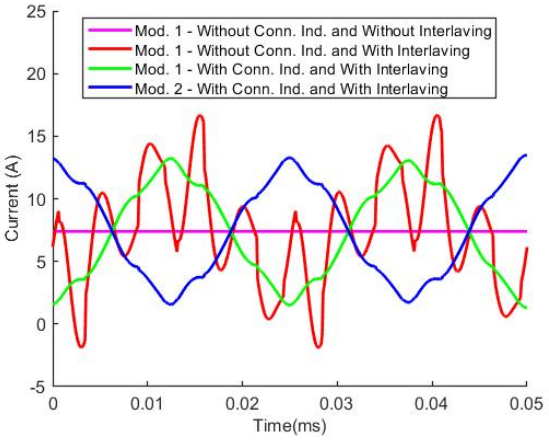


Fig. 7: Current transition occuring due to interleaving in parallel connected modules

modules have no direct effect.

4.2 Parallel Connection

The parallel connection is usually favored to reduce the size of DC bus capacitors with interleaving. However, when gate signals of two modules are phase shifted with proper angle, transition (circulating) currents between modules emerge, as shown in Fig. 7.

The reduction on the capacitor current stress on the DC link capacitor currents when interleaving is applied in parallel connected modules has been shown for different number of modules and phase shift angles [4]. However, this analysis is only valid in ideal case where commutation and connection inductances are ignored. the voltage ripple is also expected to reduce in accordance. However, the results of the model which takes those parasitics into account suggest otherwise such that the application of interleaving may even worsen the situation. The voltage ripple and the current ripple of Dc bus capacitors with interleaving are shown in Fig. 8 and Fig. **??**, respectively. To better visualise the severity of the situation, the RMS of DC bus currents with and without interleaving are obtained for a full cycle of 3-phase currents and shown in Fig. **??** for different phases.

Burada RMS akmlar yorumlanacak (peak nerede oluyor vs.)

Akm geilerinin potansiyel problemleri ???

4.3 Discussions

Serinin potansiyel skntlar

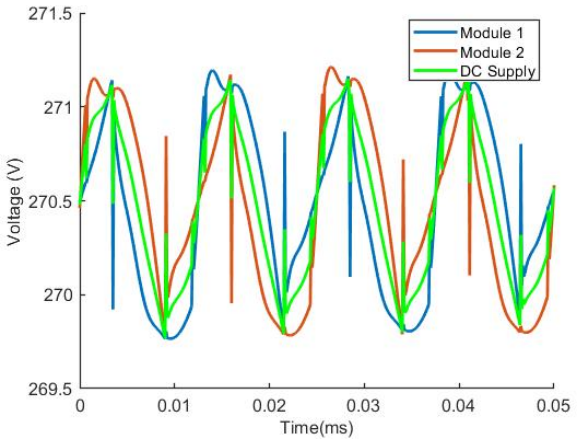


Fig. 8: DC bus voltage ripple in parallel connected modules

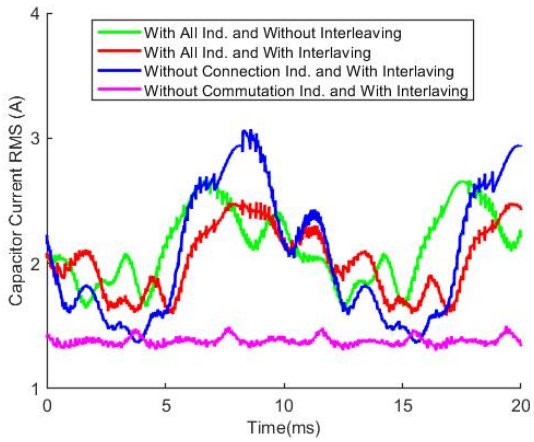


Fig. 9: Variation of DC bus capacitor current RMS in parallel connected modules

Serinin avantajlar ve dezavantajlar

Seride interleaving aslnda efektif olarak etken deil

Paralelde ideal durumdakinin daha bile ktsne gidebilir

Paralelin avantajlar

ok sayda modl olsa ne olurdu (seri)

ok sayda modl olsa ne olurdu (paralel) - interleavin daha bile ktletirebilir- modllerin nasl balandna bal

5 Conclusion

Deductions:

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In the final paper, a complete analytical model will be introduced through which parasitic inductance, number of modules and interleaving effects can be analyzed. The variation of each stress will also be analyzed with varying switching frequency so that the relation between the resonance frequency due to capacitance and inductance combination and switching frequency will be more clear.

The aforementioned IMMD prototype is currently on its integration and testing stage where the dedicated permanent magnet motor and control PCB are also realised. The power distribution architecture is designed such that 4 inverter modules can be connected in all-series, all-parallel or 2-series and 2-parallel fashion.

All the simulation results presented in this manuscript will be validated via experiments and presented in the final paper.

Kapasitr voltajlar iin deney sonucu vercez (akm lemeyiz onu derive etcez?)

Modller aras akm geileri llebilir aslnda (seri /paralelde)

References

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