Date: 03.08.2019

Attendees: Hakan Saraç, Mesut Uğur

Location: Electrical Machines Laboratory

Target: V1.3 Gate Driver Board (#1) and (#2)

Test type: Series Connected Inverter tests with RL load at High Voltage

Data: *....\IMMD data\2019.08.03\series_unbalance_data.mat*

Objectives:

1. To observe and record the DC bus of series connected modules to understand the unbalance and 100 Hz harmonic phenomena.
2. To test the control board power stage at high voltage and different connection configurations.

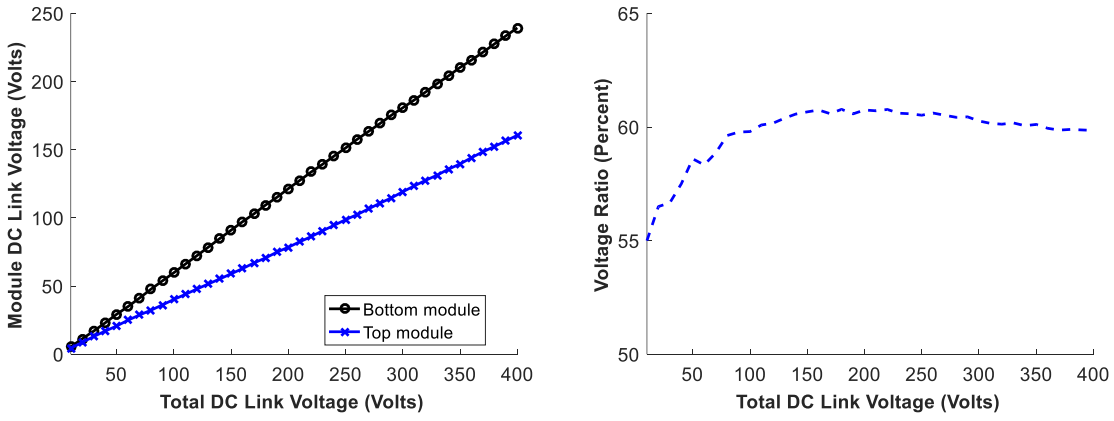
Conditions: 22 Ohm Ron, 2 Ohm Roff. 0-400V VDC. RL Load. 40kHz fsw. 0.9 power factor. Sinusoidal PWM with 0.9 modulation index.

Steps:

1. Series connected inverters are tested at input voltages up to 400 V without interleaving. The DC voltage sharing of modules is recorded.
2. Phase-A currents of both modules and DC bus voltage ripples are recorded with standard current probes and high voltage passive probes.
3. The DC bus voltage ripple waveforms are obtained for large windows (up to 10 seconds) to be able to analyze the time-varying very low frequency harmonics on DC bus voltages.
4. High voltage up to 540 V is applied to the control board DC bus main input. A series connected configuration is performed on the control board power layer and tested at low voltages. Unbalance is observed and analyzed.

Results:

1. The unbalance in the DC bus voltages is lower (55%-45%) at low voltages and it increases up to (60%-40%) and converges around that value, as shown in Fig 1. The calculated unbalance was around 55%-45%. This situation should be analyzed.



(a) *(b)*

Fig. 1. (a) Module DC bus voltages, (b) Ratio of the bottom module DC bus voltage to the total DC bus voltage

2. Ripple waveforms of Top Module, Bottom Module and Total DC bus voltages are shown in Fig. 2 for different input voltages up to 400V.

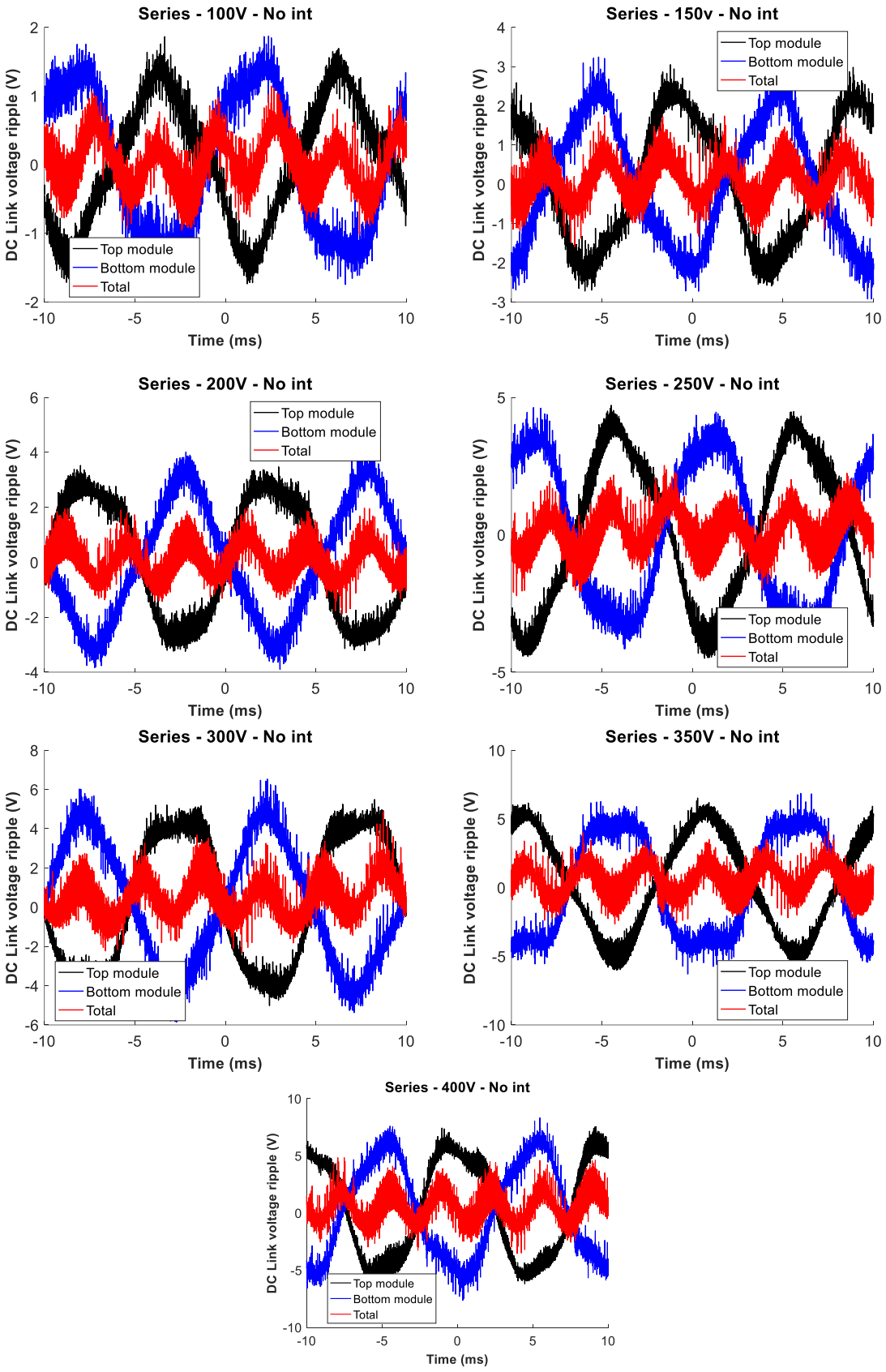


Fig. 2. Ripple waveforms of Top Module, Bottom Module and Total DC bus voltages

Previously, 100 Hz components are observed on module DC bus voltages. However, they were completely out-of-phase, cancelling each other perfectly on the total DC bus voltage. It was suspected that these 100Hz components might be a result of phase unbalance in addition to module unbalance. In this test, additional third harmonic (of 100Hz) component is present in all the voltages. Since its frequency is 300 Hz, the rectifier is considered to be the cause of it. It has also been observed that, the 300 Hz component changes its phase in the order of seconds (can be seen in time) in the module voltages. 10-second-long sets of data are recorded to better understand this, which are covered in Section 4.

3. Phase-A current waveforms of Top Module and Bottom Module are shown in Fig. 3 for different input voltages up to 400V. (*150V ve 200V dataları eksik. Ya almayı unuttuk ya da kayboldu*).

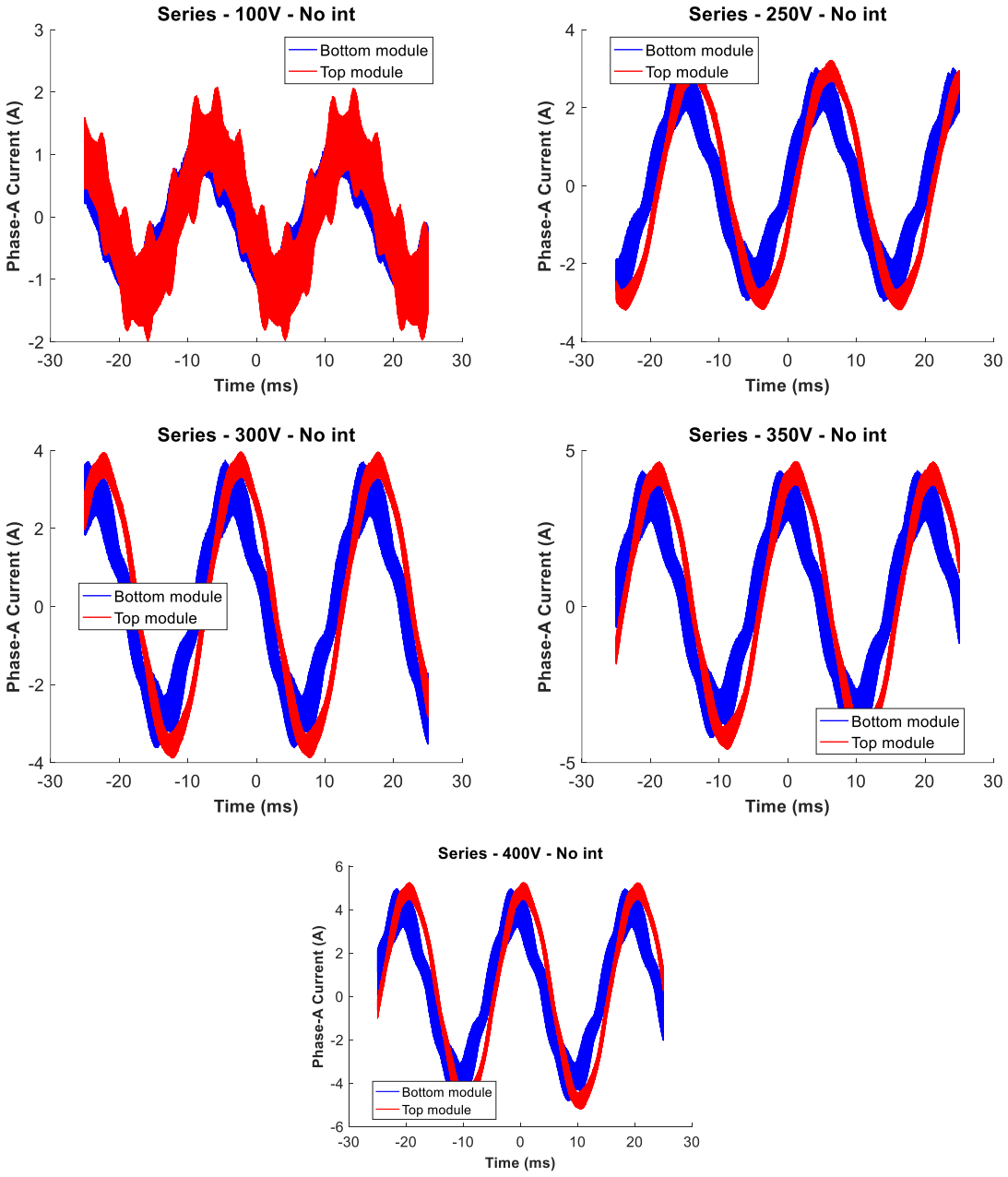


Fig. 3. Phase-A current waveforms of Top Module and Bottom Module

The ripples of phase-A currents are quite different. Magnitude, phase and ripple content of these currents should be studied via simulation.

4. *Buraya 10 saniyelik waveformların FFT analizleri gelecek.*

5. 540V is successfully applied to the control board main DC bus input with no module connections. A 4-series configuration is achieved on the control board power stage and it is tested with low input voltages. Unbalance and some oscillations are observed on the voltages where only capacitors are present (no inverter, no load). A resistive circuit should be applied to each module. The resistor selection should be studied and this topic should be researched from the literature.

Next time:

1. A resistor-based balancing circuit will be applied to the control board.
2. After balancing is achieved on the control board, 4-series, 4-parallel and 2-series/2-parallel connections will be tested.
3. Integration of the control board with a single module will be achieved testing the following:
    a. PWM
    b. Current measurement (to be observed on CCS)
    c. Inverter operation with RL load at 300V and 2 kW.