Investigation of the Effects of Parasitic Components on Parallel and Series Connected Modular Motor Drives

Abstract: In this paper, the effect of parasitic inductances on power semiconductor device stress, DC link capacitor current ripple and DC link voltage ripple in a motor drive are investigated. A GaN based motor drive inverter module designed for an Integrated Modular Motor Drive (IMMD) application is considered. The actual capacitor current stress in a single module is shown to be much more adverse when the commutation inductances are taken into account. The change in the interleaving scheme is discussed when the connection inductances between inverter modules that are connected in series or parallel are considered. A comparison between series and parallel connection in a modular motor drive is performed with several aspects.

1 Introduction

Integrated modular motor drives (IMMD) gained special interest in recent years to replace the conventional motor drives thanks to their high power density and fault tolerance capability. By the modularization of motor drive, redundancy of the motor drive system can be increased which is especially desired in safety critical applications [1]. Moreover, power semiconductor devices having lower ratings can be utilized such as Gallium Nitride (GaN) Field Effects Transistors (FETs) resulting in higher efficiency and higher power density [2].

There are several IMMD studies which use different types of modularity in terms of DC link connection, such as series connected [2] and parallel connected [1] topologies. In series connected drives, the main motivation is to be able to utilize low voltage GaN devices in a higher DC link voltage. Parallel connection is usually used to distribute the heat dissipation and reduce the size of DC link capacitors via interleaving [3].

Connection of several voltage source inverters (VSI) in a modular fashion brings its own challenges. Potential circulating currents and unbalanced voltages may also occur under abnormal operating conditions. Moreover, the parasitic components due to the physical connections between the modules may result in unbalanced stress on module capacitors.

Careful layout and connection architecture design is required in order to minimize these effects, however too few studies in the literature give special attention to parasitic component effects in modular drive topologies. In [4], two candidate DC bus architectures are proposed and compared

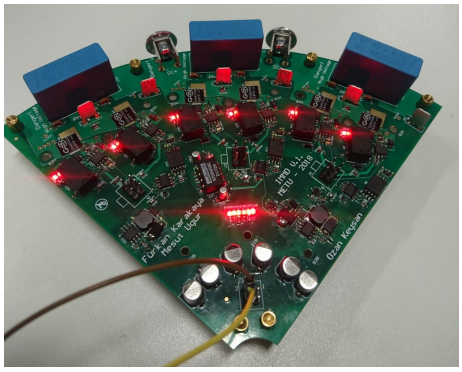


Fig. 1: GaN based 3-phase inverter module

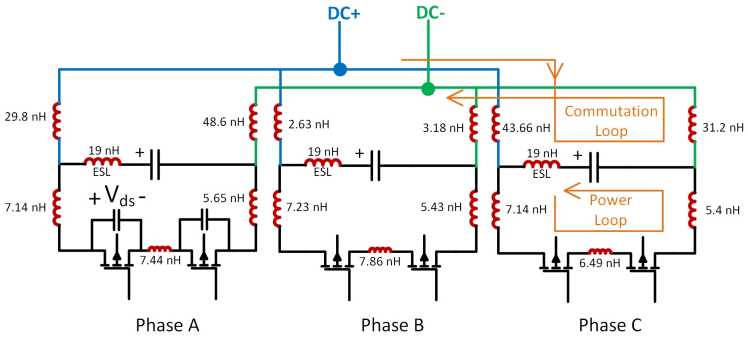


Fig. 2: Parasitic Inductance Map of a Single Module

in terms of DC bus current oscillations due to layout inductances.

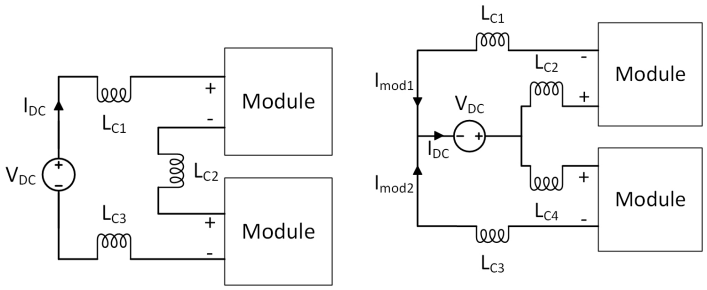
In this paper, the effects of PCB parasitic inductances are investigated in a GaN based IMMD. The overshoots on GaN voltages due to power loop inductance are investigated. The actual DC link capacitor current stress and voltage ripples are analyzed considering commutation inductances between phases. Series and parallel connected inverter modules and the effect of connection inductances to their performance are analyzed.

2 Description of the IMMD System

The IMMD system is composed of 4 identical modules which can be connected in series or parallel on the DC link. A 2 kW 3-phase GaN based motor drive inverter printed circuit board (PCB) and a control PCB are designed for the system. Total system output power is 8 kW and the module DC link voltage is 270 V.

2.1 GaN based motor drive module

The photograph of the 3-phase inverter module of the IMMD system is shown in Fig. 1 excluding the heat sink. The module consists of half-bridge legs with GaN FETs having 650 V and 30 A ratings. Each leg has a 5 μF metal film capacitor, isolated gate driver dedicated to each GaN and a phase current measurement circuit. The DC link capacitor size is determined according to required capacitance which is calculated based on voltage ripple and required current rating [3], by also taking the effect of interleaving into account. It is aimed to minimize the gate loop and power loop inductances keeping DC link film and ceramic capacitors as close as possible.



(a) Series **(b)** Parallel

Fig. 3: Series and Parallel Connected Modules Configurations

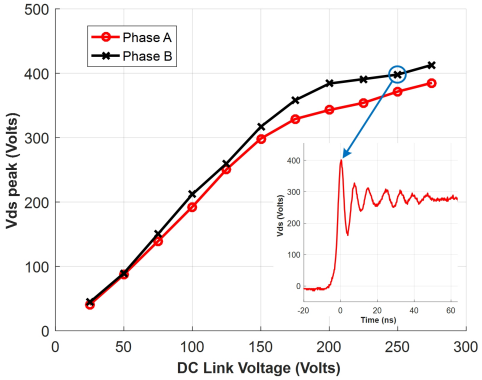


Fig. 4: Experimental voltage overshoot results

2.2 Parasitic Inductances

For the inverter circuit given in Fig. 1, the power loop and commutation loop inductances are identified using ANSYS/Q3D tool and given in Fig. 2. The power loop is effective when a commutation occurs between transistors on a single half-bridge while the commutation loop is effective whenever a current commutes from one phase to another.

2.3 Series and Parallel Connection

As shown in Fig. 3, two modules can be connected in series or parallel. The inductances given in Fig. 3a, L_{C1} & L_{C3}, are total equivalent inductances of connectors and module to supply terminal connections and L_{C2} represents the total inductance of connectors and module to module connection. Similar inductances are also present in parallel connection.

3 Investigation of a Single Inverter Module

3.1 Effect on Power Device Stress

As shown in Fig. 2, the power loop includes two switches and the phase capacitor. When the phase current transfers from one switch to the other, the power loop parasitic inductances cause either a voltage overshoot on the drain-source terminals of a switch as much as $L_p * di/dt$. Considering the high current rise and fall time capability of GaN FETs, i.e. high di/dt, the power loop inductance is the most important factor for device stress. Experimental results of device stress can be seen in Fig. 4 for different DC link voltages. It has been shown that the peak stress on phase-B is higher since its power loop equivalent inductance is slightly larger than phase-A.

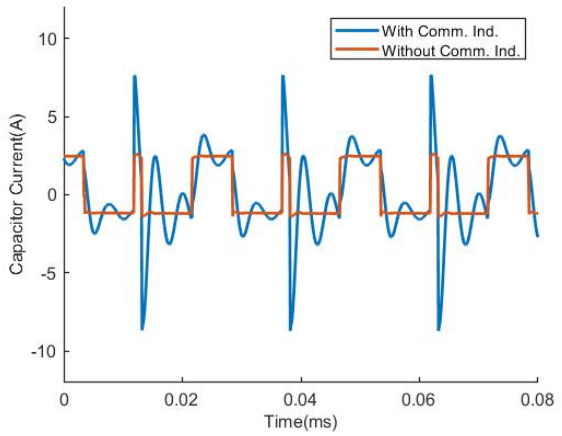


Fig. 5: DC bus capacitor current ripple with and without commutation loop inductances

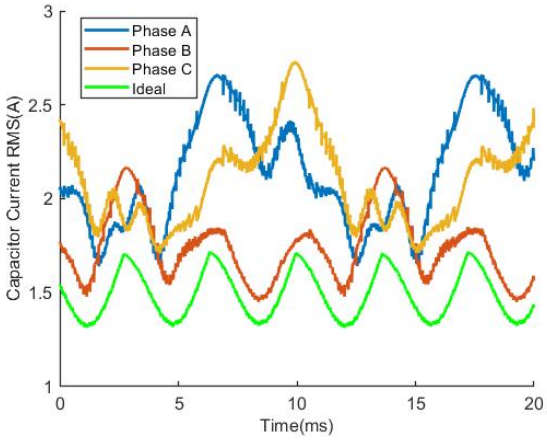


Fig. 6: Variation of RMS values of capacitor currents with and without commutation inductances

3.2 Effect on DC link Capacitor Stress

The DC link capacitors placed on each half-bridge are used to supply and sink the current ripple during switching periods. The power loop inductances are not effective on these capacitors' stress assuming ceramic capacitors are placed in much closer proximity. When the parasitic inductances are of considerable amount on the commutation loop, the stress of individual capacitors increase due to the longer path which the other capacitors have, as shown in Fig. 5. This results in higher capacitor RMS currents than analytically calculated [3] as shown in Fig. 6 and must be taken into account as the selected capacitor temperature may increase too much, eventually shortening its lifetime. On the other hand, this effect is not significantly reflected to the voltage ripple.

4 Investigation of Series and Parallel Connection

4.1 Series Connection

The DC bus voltage ripple of each module along with total DC bus are shown in Fig. 8. It has been shown that interleaving only reduces the ripple on total DC bus which has no positive effect on the modules since the module voltage ripples remain the same. Moreover, the capacitor ripple currents are not affected by interleaving since it is simply impossible to have a different current when modules are connected in series. Therefore, interleaving on series connection does not reduce the size of DC bus capacitors, although it is claimed so in the literature [2].

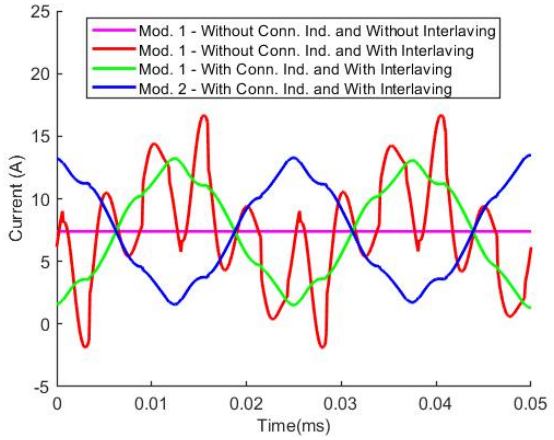


Fig. 7: Current transition occuring due to interleaving in parallel connected modules

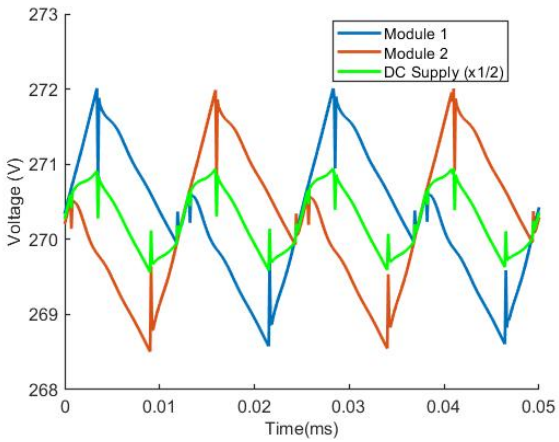


Fig. 8: DC bus voltage ripple in series connected modules

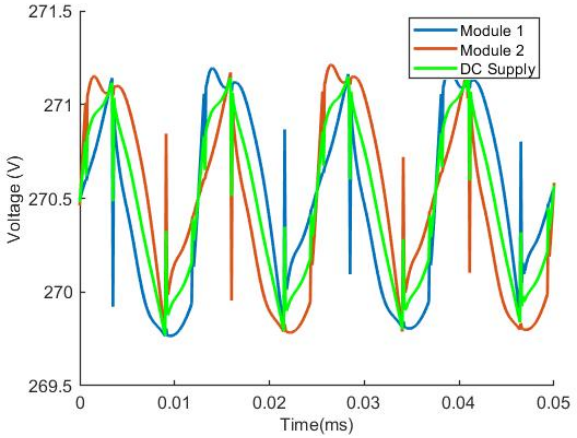


Fig. 9: DC bus voltage ripple in parallel connected modules

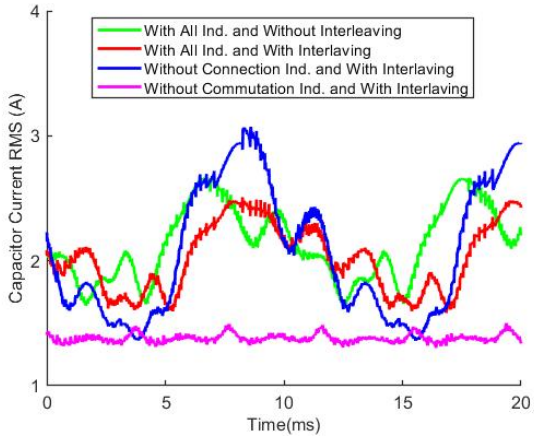


Fig. 10: Variation of DC bus capacitor current RMS in parallel connected modules

4.2 Parallel Connection

The parallel connection is usually favored to reduce the size of DC bus capacitors with interleaving. However, when gate signals of two modules are phase shifted with proper angle, transition (circulating) currents between modules emerge, as shown in Fig. 7. The reduction on the capacitor current stress when interleaving is applied in parallel connected modules has been shown for different number of modules and phase shift angles in [3]. However, this analysis is only valid for ideal case where commutation and connection inductances are ignored. The RMS of capacitor currents with and without interleaving and parasitic inductances suggest that actual RMS current is much larger as shown in Fig. 10. On the other hand, the voltage ripple is reduced with interleaving.

5 Conclusion

In this paper, the effects of parasitic inductances on a modular motor drive are investigated. Device stress is only affected by power loop inductances, whereas capacitor stress is caused by the commutation inductances. In series connected converters, interleaving has no useful effect on the capacitor stress and module voltage ripple. On the other hand, capacitor stress can be reduced in parallel connection with interleavig. However, the capacitor RMS currents are not significantly reduced when parasitic inductances are taken into account.

In the final paper, a complete analytical model will be introduced including parasitic inductances, number of modules and interleaving effects. The aforementioned IMMD prototype is currently on its testing stage. The power distribution architecture is designed such that 4 inverter modules will be tested with all-series, all-parallel or 2-series and 2-parallel connections. All the simulation results presented in this manuscript will be validated via experiments and presented in the final paper.

References

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