VUB MOBILITY, LOGISTICS & AUTOMOTIVE
TECHNOLOGY RESEARCH CENTRE

Double Pulse Test MATLAB/Simulink Model

HAKAN POLAT

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1 Introduction

Double pulse test (DPT) is a standard test to measure the switching characteristics of a power semiconductor. It has a wide range of applications, ranging from measurement of parasitic capacitances to measuring the turn-on and turn-off losses of the device under test (DUT) for various drain-source voltages V_{ds} and drain-source currents I_{ds}. According to [1], double pulse test allows identifying the technical issues at an earlier stage of the project. Testing the semiconductors under worst-case scenarios allows precautions to be taken, which may cause delays in the timeline.

2 Double Pulse Test

A DPT circuit consists of a loading inductor, a freewheel diode, and the DUT given in Fig. 1. Often the same semiconductor is used as a freewheeling diode to measure losses on the body diode.

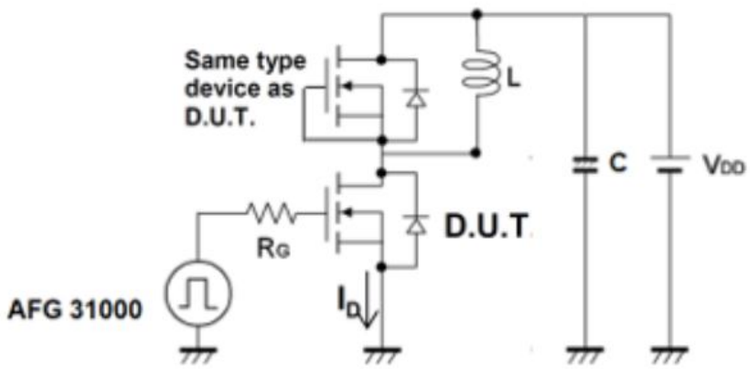


Figure 1: DPT test circuit.

The gate-source voltage (V_{gs}) of the high side semiconductor is smaller than the threshold voltage V_{th}. To avoid false turn-on during hard switching conditions, a negative voltage is applied for SiC and GaN devices since the parasitic gate-source capacitance (C_{gs}) is much smaller than conventional Si devices. The load inductor is first charged to the desired current. Then the DUT is turned off, and the load current flows from the freewheeling body-diode. In order to observe the turn-on characteristics, the DUT is turned on and off once more. By controlling the switching times, the DUT characteristics can be measured in a controlled manner. A typical DUT I_{ds} current is shown in Fig. 2 [1]. Here it is important to list a few features of the load inductor:

- The load inductor should not saturate for the currents under testing.
- The inductor should be far away from the half-bridge configuration to avoid EMI.
- The current pulse should be small as possible to avoid heating of the junction, which changes the switching characteristics.

3 Simulink Model

Prior to real testing, a simulation model is necessary for the initial evaluation of the semiconductor. Therefore, it is essential to model the DPT with DUT in a simulation environment. In this report, a Matlab 2020b/Simulink DPT model is built.

The 900 V, 23 A SiC MOSFET with manufacturer part number C3M0120090D is selected as DUT [2]. The Simulink model is presented in Fig. 3. The DC link capacitance is neglected from the model for simplicity. However, during actual experimental testing, the

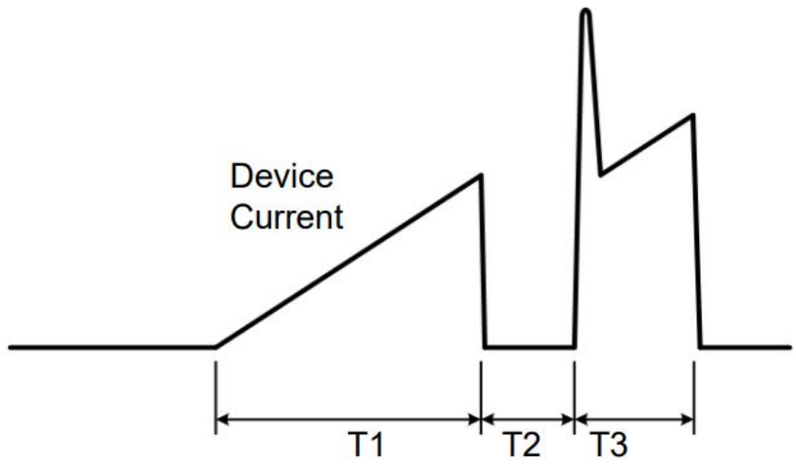


Figure 2: DPT DUT I_{ds} representation.

DC-link capacitance should be chosen such that no voltage sags are observed during switching transients.

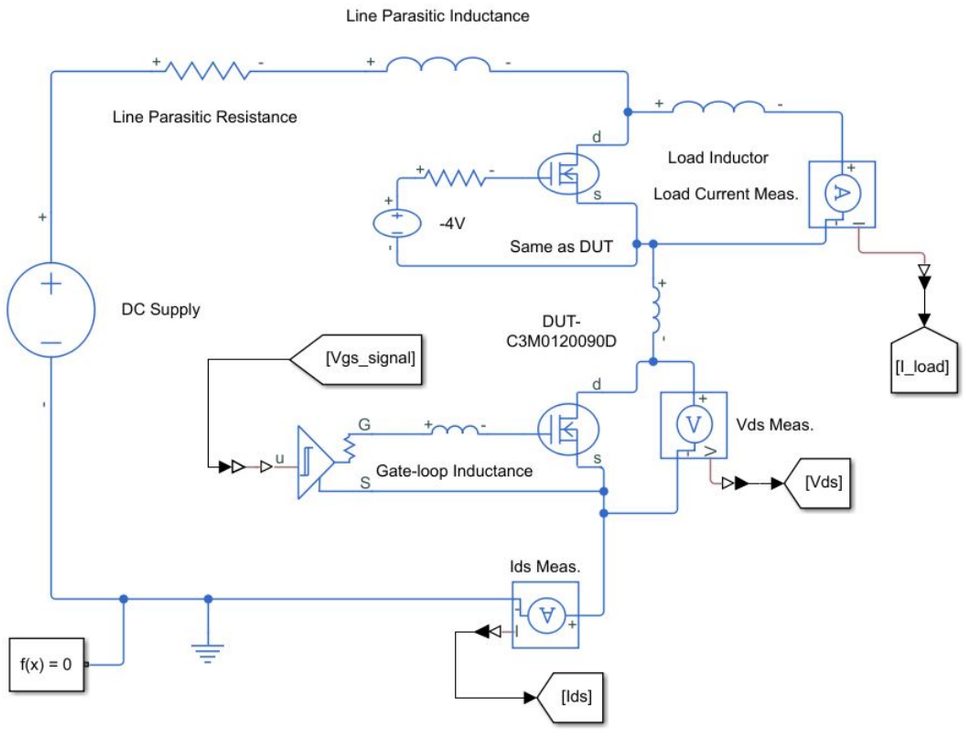


Figure 3: Simulink DPT model for C3M0120090D SiC MOSFET.

The line parasitic resistance ($R_{par,line}$) and line parasitic inductance ($L_{par,line}$), are parasitic impedances in the AC power loop. Another important parameter is the parasitic inductance between the two semiconductors. This parasitic impedance (L_{HB}) is crucial since it directly affects the turn-on and turn-off LC oscillations. For simplicity, it is taken as 1 nH.

3.1 Gate Driver Parameters

The gate driver parameters are taken from UCC21530 gate driver, which was given in the reference designs from Texas Instruments [3]. The gate driver parameters are presented in Table 1. The turn on-off voltages are taken from the datasheet presented in [2]. The gate loop parasitic inductance is taken as 7 nH, which is an acceptable value in SiC drives. If desired, the parasitic gate loop inductance can be measured using RLC meter with proper PCB measurement probes or calcualted using FEA simulation in ANSYS Maxwell Q3D. The top freewheeling SiC device is supplied with -4 V which ensures that the gate stays closed at all times. While the diode characteristics also changes with applied gate voltage, -4 V

is selected to match the results in the manufacturer datasheet. (The DPT circuit in the datasheet also applies the same gate voltage to the top semiconductor.)

Table 1: Gate Driver Parameters

Gate Driver model	UCC21530
Turn-on delay time ($t_{on,delay}$)	19 ns
Turn-off delay time ($t_{on,delay}$)	19 ns
Turn on external gate resistance (R_on, ext)	5 Ω
Turn-off external gate resistance (R_off, ext)	5 Ω
Gate-source turn-on voltage ($V_{gs,on}$)	15 V
Gate-source turn-off voltage ($V_{gs,off}$)	-4 V
Gate loop parasitic inductance (L_{gate})	7 nH

3.2 Semiconductor Model

The simulink MOSFET model requires the parameters presented in Table 2.

Table 2: C3M0120090D SiC MOSFET Parameters

Semiconductor	C3M0120090D SiC MOSFET
Drain-source on state resistance ($R_{ds,on}$)	120 $m\Omega$
I_{ds} for $R_{ds,on}$	15 A
V_{ds} for $R_{ds,on}$	15 V
Gate threshold voltage (V_{th})	2.1 V
Input capacitance (C_{iss})	Piecewise linear function wrt. V_{ds}
Output capacitance (C_{oss})	Piecewise linear function wrt. V_{ds}
Reverse transfer capacitance (C_{rss})	Piecewise linear function wrt. V_{ds}

The parasitic capacitances presented in Table 2, are taken as piecewise linear function wrt. the V_{ds}. In Fig. 4, the change of the parasitic capacitances is presented. These parameters can also be given as constant. However, the transient response will deviate slightly from realistic results.

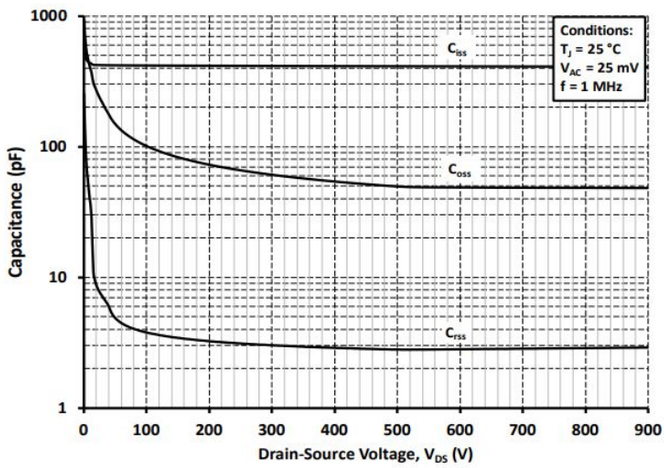


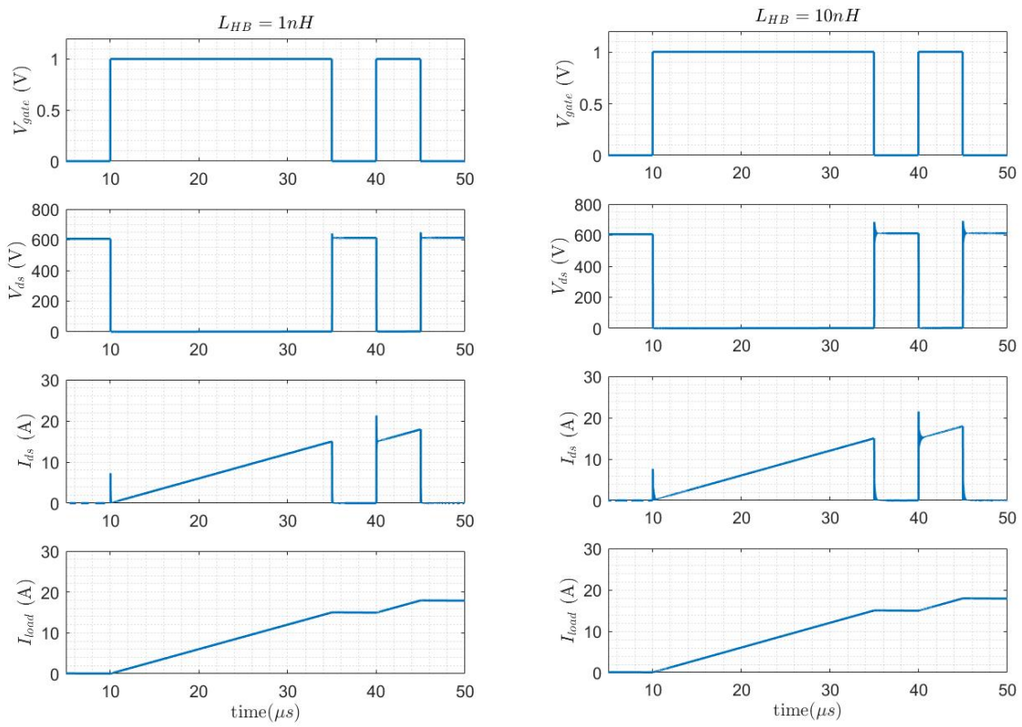
Figure 4: C3M0120090D SiC MOSFET parasitic capacitances with respect to V_{ds}. [2]

4 Results

The DPT parameters are listed in Table 3. The gate signal (V_{gate}), V_{ds}, I_{ds} and I_{load} are presented for different parasitic inductances in Fig. 5. The turn on and off switchings are presented in Fig. 6 and Fig. 7. The turn on and turn off energies are calculated as 76 μJ, 18 μJ, respectively.

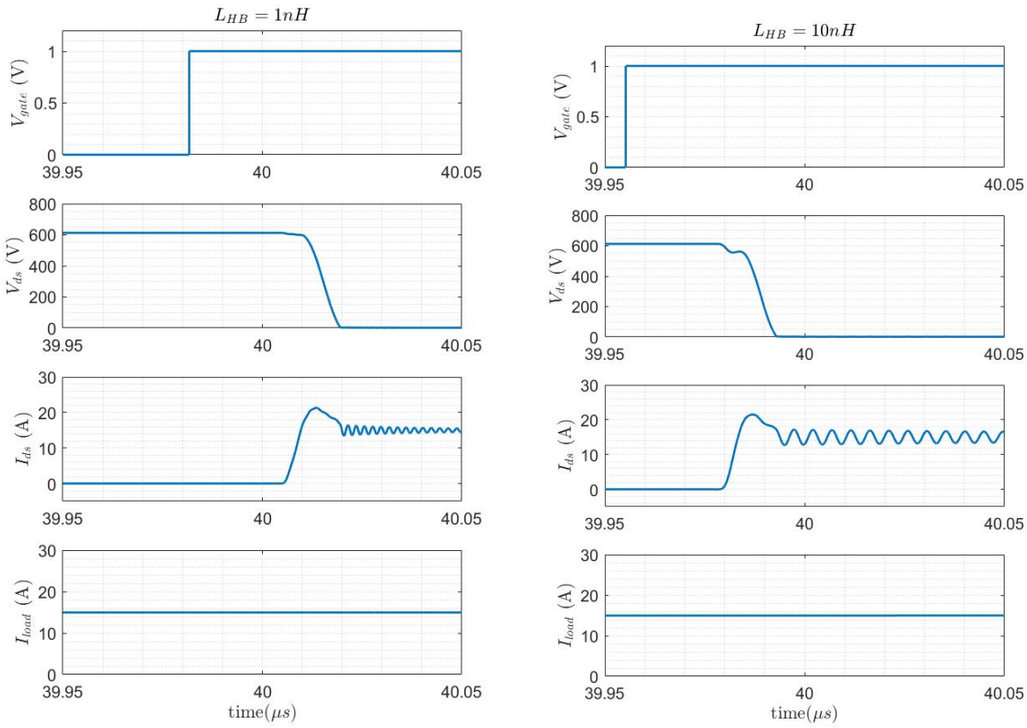
Table 3: DPT Parameters

Semiconductor	C3M0120090D SiC MOSFET
$V_{dc,link}$	600 V
I_{load}	15 A
L_{load}	1 mH



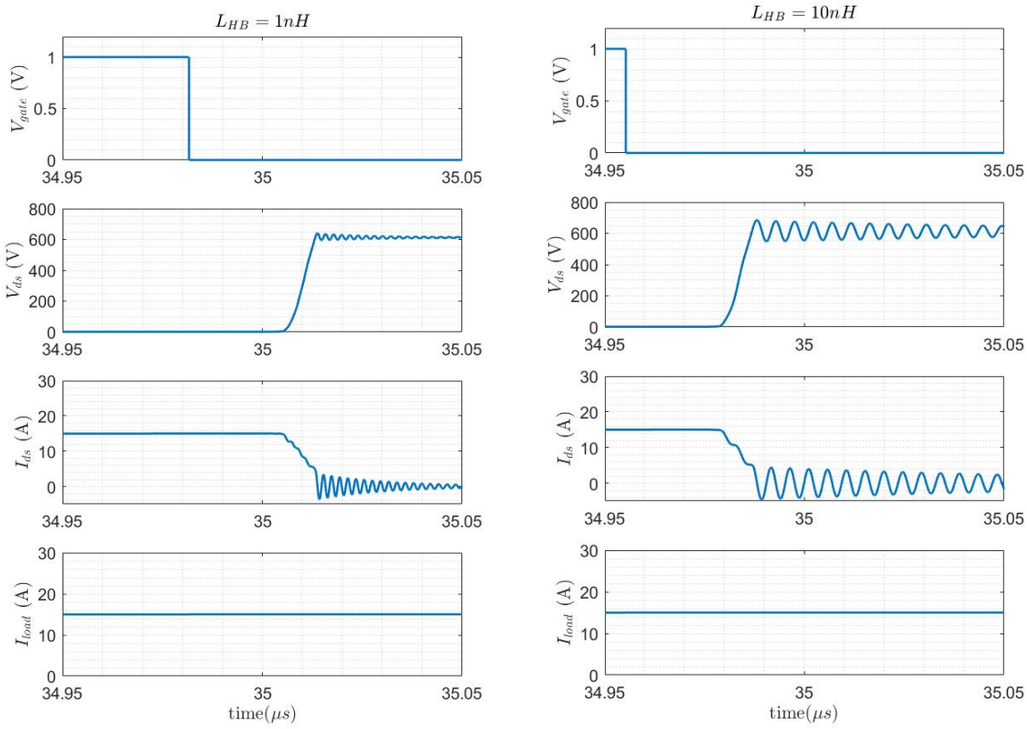
(a) (b)

Figure 5: Effect of parasitic inductance on the switching overshoots. Notice the increased oscillation and voltage peak on V_{ds} and I_{ds} during turn on and off.($V_{dc,link} = 600V$, $I_{load} = 15A$)



(a) (b)

Figure 6: Effect of parasitic inductance on the switching overshoots during turn on. ($V_{dc,link} = 600V$, $I_{load} = 15A$)



(a) (b)

Figure 7: Effect of parasitic inductance on the switching overshoots during turn off. ($V_{dc,link} = 600V$, $I_{load} = 15A$)

5 Possible Improvements

5.1 GaN Modeling

Modeling GaN transistors are a bit problematic. While the forward conduction characteristics are like regular MOSFET's the reverse conduction characteristics depend on the applied V_{gs} voltage, and since there is no body diode in a GaNFet [4]. Therefore, it is not possible to perfectly model GaNFet using Simulink built-in MOSFET.

5.2 SiC Modeling

The SiC Simulink model can further be improved to improve the transient simulation and experimental agreement. The required parameters can be extracted from manufacturer datasheets using curve fitting functions as in [5] and each internal parasitic element can be modeled analytically.

6 Short Summary

In this report, a MATLAB Simulink model is built to simulate a double pulse test for a specific device. While C3M0120090D-Silicon Carbide Power MOSFET is selected as the device under test, by changing the parameters, it is possible to simulate various semiconductors. The found switching losses are lower than the ones presented in the manufacturer's datasheet. This is because of not being able to perfectly model the turn on and off delay times, source/sink currents of the gate driver circuit, or the line parasitic inductance values.

References

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