MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EE464 Simulation Project-2 Report

Isolated Converters & Controller Design

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1. Introduction

In this project, we are required to design an isolated DC-DC converter and a controller, respectively. For DC-DC converter, we are supposed to use the topology that we chose for our hardware project. Therefore, since we have chosen to use flyback converter for our hardware project, firstly we need to design a transformer for our flyback converter. Secondly, we are supposed to observe the voltage-current stress in the switches and decide to use any snubber. Also, we are objected to choose our components for our converter. Moreover, we are supposed to design a converter for our specifications in the hardware project and obtain its bode plot and transfer function. Lastly, we are supposed to design a Type-2 controller.

Our converter specifications are as follows.

Vin (Vdc)	Vout (Vdc)	Pout (W)	Topology
12	24	80	Flyback

2. Results

Q1) Isolated Converter Simulation

a)

The given constraints of the Flyback converter is 80W of output power rating, input voltage of 24V and output voltage of 12V. To achieve that we have decided upon the following specifications for our converter. Calculation of values (Lm,C) and the choice of the elements are provided in the following sections.

Table 1.1: Chosen element list

	Value	Voltage Rating	Current Rating
C	470µF	50V	-
Lm (core)	256µH	-	$8.33A_{avg}$
Mosfet	-	100V	13.2A
Diode	-	45V	20A

In the steady state under full load, we have designed our converter achieve CCM under full load. The switching frequency is chosen as 10kHz in order to achieve greater efficiency. Low switching frequency is compensated by using a bigger core and larger number of turns. Output capacitor is chosen large deliberately in order to achieve low voltage ripple at the output. Since the voltage ratings are low size of the capacitor is not a big issue in this converter. Moreover, there is no limitation in the size as well. The transformer ratio is chosen as N1/N2 = 2.

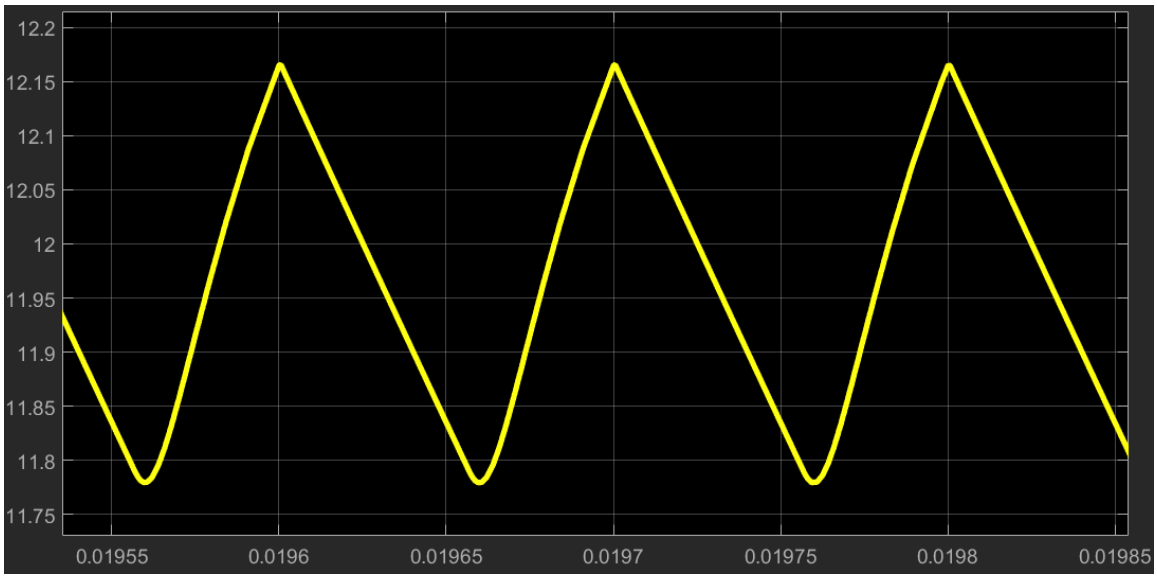

Figure 1.1: Output voltage waveform at the steady state

b) Transformer design

In this part, and most of the parts, the calculation is done using MATLAB. You can reach to the related m file in our Github repository.

Transformer is the key component in a flyback converter. It should be capable of storing and delivering enough energy to the output in a switching cycle. As the switching frequency increases Lm value can be reduced because the ripple current on the Lm is directly related to the switching frequency. Before starting to the transformer design, ripple of the current flowing through the Lm is assumed to have a ripple of 40%. Using this constraint following values are calculated. Moreover, duty cycle is chosen as 0.4, which is a reasonable duty ratio.

Note that, as duty cycle gets too close to 0 or 1, operation of any converter is affected badly since the inductor is charged or discharged for a very short amount of time, proper operation may not be achievable.

$Ripplepercent = 0.4;$

$$I_{Lmavg} = \frac{Vo^2}{Vs * D * Rload} = 8.33A$$

$$I_{Lmmax} = I_{Lmavg} + I_{Lmavg} * \frac{Ripplepercent}{2} = 10A$$

$$I_{Lmmin} = I_{Lmavg} - I_{Lmavg} * \frac{Ripplepercent}{2} = 6.67A$$

$$L_m = \frac{V_s * D}{\Delta I_{Lm} * fsw} = 288\mu H$$

To achieve 288µH, a core with a high A_L value should be chosen. Core should be gapped in order to store more energy. To achieve the given specifications, we have chosen the core with the chosen specifications. To reach to the datasheet, you can click here.

Table 2: Specifications of the transformer core

Flux Density	0.49T
Effective Core Area (A_e)	200mm^2
Effective Length (l_e)	70mm
Inductance Factor (A_l)	160nH
Effective Permeability (μ_e)	45
Effective Magnetic Volume (Ve)	14000mm^3
Material	N41

Number of turns required for to reach to the calculated Lm value:

$$N1 = \sqrt{\frac{L_m}{\text{Al}}} = 42$$

Based on this calculation, N1 chosen as 40 turns. The current flowing in the primary side is calculated as half of the load current (since N1/N2 = 2 chosen) that is 3.33A. Referring to the table in this link, AWG 16 cable can carry 3.7A of current which has 1.29mm of diameter. The window area of the core is given as 20.8*7mm^2. Fill factor of the core is:

$$Fill\ Factor = \frac{N*CableArea}{Window\ Area} = 0.36$$

With the addition of the secondary side cables, FF value will be around 0.7, which is achievable.

The core also should not get saturated the maximum value of the Lm value. Peak value of the flux density of the is calculated as:

$$B_{peak} = \frac{N1*I_{Lmmax}}{\text{Effective Core Area}*\text{Core Reluctance}} = 0.32T$$

From the datasheet, it can be seen that the loss coefficient at 0.3T and 10khz is around 100kW/m^3.

$$CoreLoss = 100\frac{kW}{m^3} * Effective\ Magnetic\ Volume = 14\ Watts$$

c) DCM occurs when I_{Lmmin} reaches zero. Assuming current ripple on the Lm is constant, then ILm=1.667A at the boundary of the DCM. Also, we know that Is=D*ILm = 0.4*1.667 = 0.667A. Therefore when the load current goes below N1/N2*Is = 2*0.667 = 1.333A, the converter goes into the DCM.

d)

Due to the energy stored in the leakage inductance, when the switch goes off, large di/dt rate causes very high voltage peaks. To overcome this problem, the transformer can be designed to have smallest leakage inductance, or the switch be chosen very large to suppress the extra voltage stress. We have modeled our leakage inductance as 2.3µH on the primary side. The voltage across the switch element is shown in Figure 1.2. Note that in order to model the chosen switching element, R_{dson} value of the mosfet is set, and a parallel capacitance of 930pF is put across the mosfet for the C_{gs} capacitance modeling.

The formulas used in this part is taken from here.

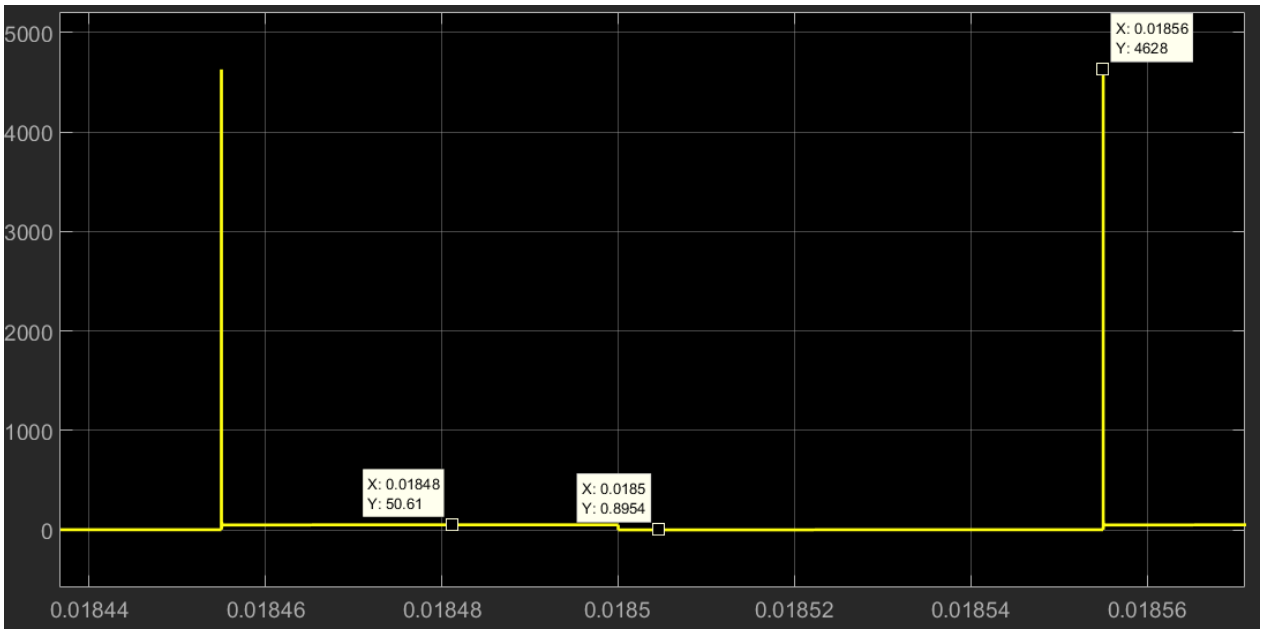

Figure 1.2: Voltage across the switch in the steady state

During the turning off, the voltage across the switch reaches up to 4.6kV. Choosing a switching element at that rates is not a viable solution for such a low powered application. Therefore, we have designed an RCD snubber circuit in order to reduce the voltage stress across

the switch. The schematic of the RCD snubber circuit and its connection to the flyback converter is given in Figure 1.3.

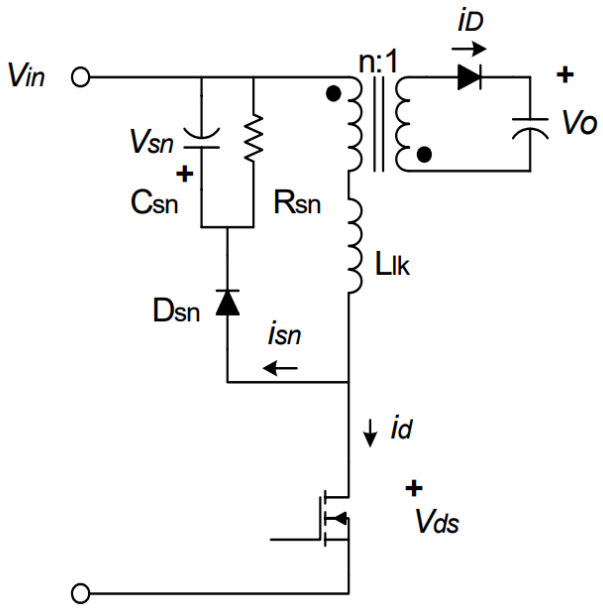

Figure 1.3: Flyback converter with RCD snubber(source)

To design the snubber, we have followed the steps provided in the application note of the ON Semiconductor. You can reach the application from here.

Before starting the calculations, we have given some predetermined values to the Csn and Rsn to determine Vsn value. The waveform of Vsn is shown in Figure 1.4.

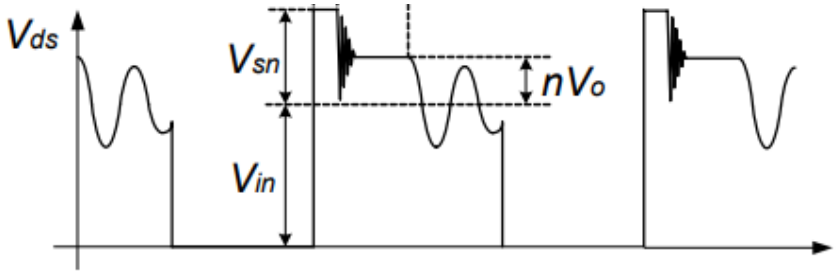

Figure 1.4: Vsn waveform(source)

These values are found by trial and method and Csn =2µF Rsn=25Ω. After finding suitable values for Csn and Rsn in order to determine Vsn value, we have followed following steps. Note that peak value of the iD current (Figure 1.3) is also determined for this purpose.

$$t_s = \frac{L_{lk1}}{V_{sn} - nV_o} * i_{peak}$$

$$R_{sn} = \frac{{V_{sn}}^2}{\frac{1}{2} L_{lk1} {i_{peak}}^2 \frac{V_{sn}}{V_{sn} - nV_o} f_{sw}} = \frac{54.5^2}{\frac{1}{2} * 2.3\mu H * 39.4 * \frac{54.5}{54.5 - 2 * 12} 10kHz} = 93.44\Omega$$

Assuming 10% voltage ripple across the Csn capacitor;

$$C_{sn} = \frac{1}{R_{sn} \frac{\Delta V_{sn}}{V_{sn}} f_{sw}} = \frac{1}{93.44 * 0.1 * 10000} = 10.7\mu F$$

When have simulated for Rsn = 93.44Ω and Csn = 10.7µF.

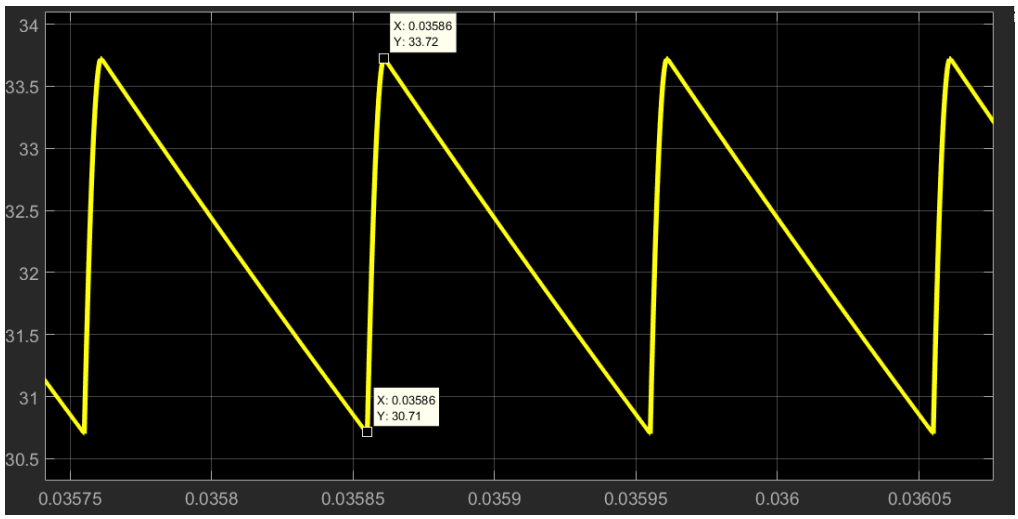

Figure 1.5: Voltage across the Csn capacitor

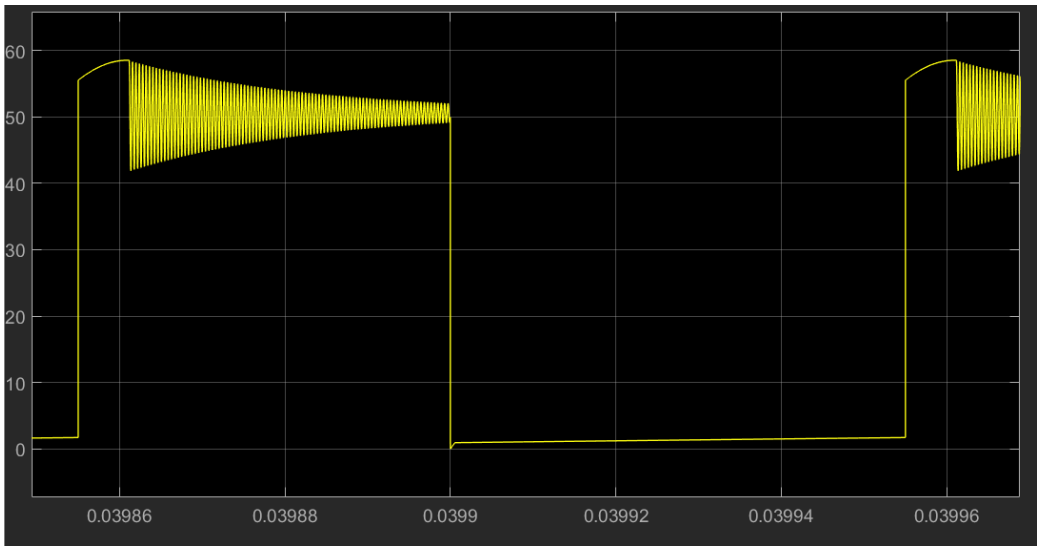

Figure 1.6: Voltage across the switch element

Using the designed RCD snubber circuit, it can be seen that the voltage stress across the switching element is reduced to 50V. Even though there is still some resonance, the high voltage peaks are eliminated.

d) Efficiency

The change in the load current changes the I_{Lm} value, which varies the core losses value as well. Using the created m file, the calculated values are as follows

Table 1.3: Loss and Efficiency table.

Load	B_{mean}	Core loss	Total Switch loss	Diode loss	Copper loss	Efficiency
80W	0.27T	14W	1.39W	4.4W	2.54W	78%
60W	0.20T	7W	0.78W	3.3W	1.42W	83%
40W	0.135T	2.8W	0.35W	2.2W	0.63W	87%
20W	0.08T	0.7W	0.09W	1.1W	0.15W	91%
0W	0T	0W	0.005W	0W	0W	100%

e) Components

The rating values of the component is provided in part a Table 1.1. The choice of these elements is made according to the simulation results. The waveforms of the mosfet and the diode are as follows.

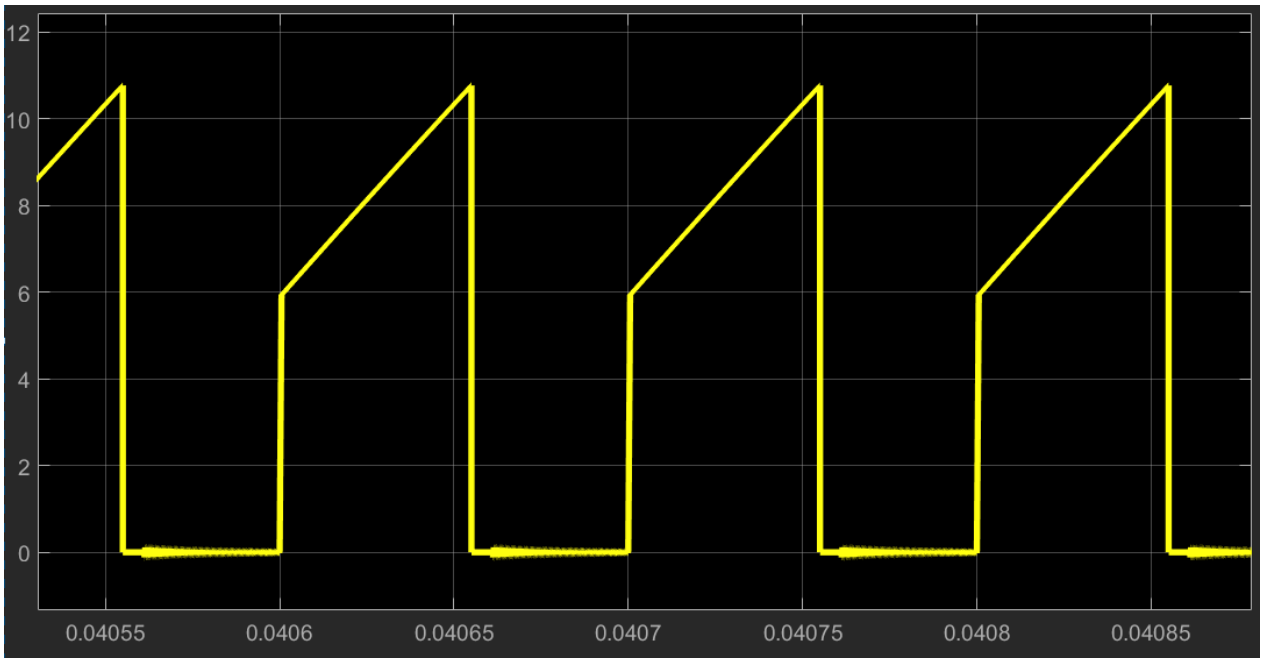

Figure 1.7: Mosfet current waveform

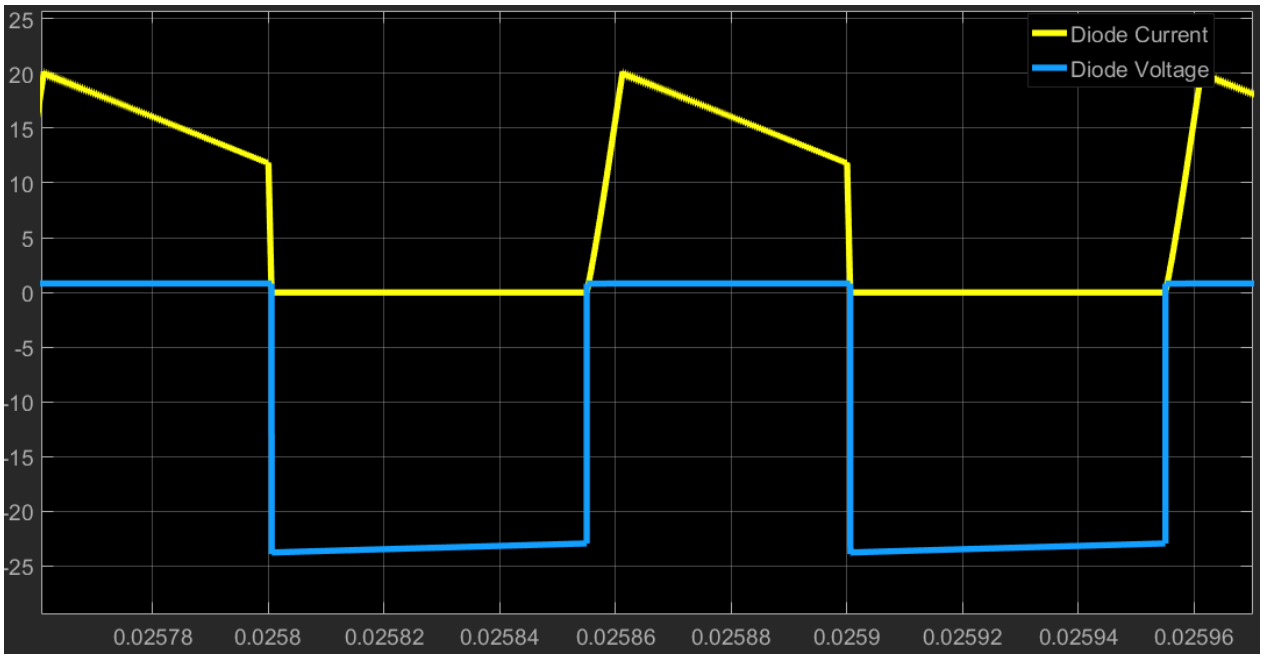

Figure 1.8: Diode voltage and current waveforms

Mosfet current has a mean value of 4.55A with the addition of the losses, however its peak reaches 10.76A. During this peak value, mosfet can get heated up which can burn the device, therefore it should either be cooled down properly or chosen larger that peak value. In Figure 1.8,

the maximum voltage across the mosfet is measured as around 60V.The datasheet of the chosen mosfet can be reached from here.

Diode current swings between 20A and 0 and has a mean value of 6.8A. Moreover, maximum reverse voltage is around 24V. Considering these, we have chosen this diode.

The capacitance value was calculated to get a output voltage ripple of 10%, which resulted in 222µF. To decrease the ripple further, we have chosen output capacitor as 470µF.

The rated values of the elements are provided in the Table 1.1 along with the links to their datasheets.

2) Controller Design

In this part, we designed a buck converter with input voltage of 24 V, output voltage of 12 V and power rating of 80 W, therefore same specifications is provided with the chosen Hardware Project. It is considered to have such numerical values for passive elements;

Inductance: 1 mH and Equivalent Series Resistance (ESR): 10 mΩ

Capacitance: 470µ F and Equivalent Series Resistance (ESR): 10 mΩ

a)

In this part, a buck converter transfer function is obtained analytically. In order to make the model realistic ESR values of both inductor and capacitor is added to converter schematic as seen in Figure xx. As marked in the schematic, there are two state variables in the buck converter namely inductor and capacitor current.

$\dot{X} = AX + BVd$ and Vo = C*X where $X = \begin{bmatrix} iL \\ Vc \end{bmatrix}$ So, aim is finding A, B,C vectors.

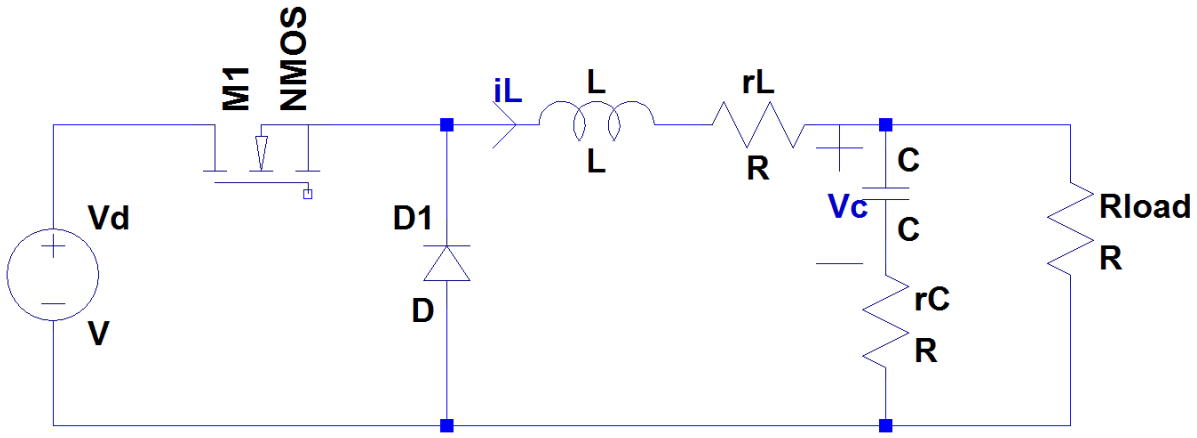

Figure 2.1: Realistic buck converter

On State of buck converter

As known, LCR circuit is connected to Vd through MOSFET in on state. Hence two mesh equations can be written such that one of them is covering outer mesh which consists of input voltage, inductor and load resistor and other one is covering capacitor and load resistor.

Kirchoff Voltage Law on outer mesh:

$$-Vd + L * \dot{\imath L} + rL * iL + Rload * (iL - C * \dot{V}c) \quad (1)$$

Kirchoff Voltage Law on small mesh:

$$-Vc - C * \dot{V}c * rC + Rload * (iL - C * \dot{V}c) \quad (2)$$

From 2nd equation;

$$\dot{V}c = iL * \frac{Rload}{C(rC+Rload)} - Vc * \frac{1}{C(rC+Rload)} \quad (3)$$

From 1st and 3rd equation;

$$\dot{\imath L} = -iL * \frac{Rload*rC+Rload*rL+rC*rL}{L*(Rload+rC)} - Vc * \frac{Rload}{L*(Rload+rC)} + Vd * \frac{1}{L} \quad (4)$$

Hence A_1 and B_1 matrices can be constructed as follows

$$A_1 = \begin{bmatrix} -\frac{Rload*rC+Rload*rL+rC*rL}{L*(Rload+rC)} & -\frac{Rload}{L*(Rload+rC)} \\ \frac{Rload}{C(rC+Rload)} & -\frac{1}{C(rC+Rload)} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

Output voltage equation;

$$Vo = Rload * (iL - C * \dot{V}c) = iL * \frac{Rload * rC}{Rload + rC} + Vc * \frac{Rload}{Rload + rC}$$

$$\text{So;} \qquad C_1 = \begin{bmatrix} \frac{Rload*rC}{Rload+rC} & \frac{Rload}{Rload+rC} \end{bmatrix}$$

Off State of buck converter

At off state, LCR circuit is short circuited through diode. Note that off state is exactly same with on state with Vd short circuited. So $A_2 = A_1$ and $B_2 = 0$. Also output voltage equation is same which yields $C_2 = C_1$.

Resultant matrices;

$A = A_1 = A_2$ $\qquad$ $B = B_1 * D$ $\qquad$ $C = C_1 = C_2$

As ESR of the inductor and capacitor is usually in mΩ range and minimum Rload is about 1.8Ω a reasonable assumption can be done with Rload >>rC,rL also Rload>>rC+rL. Resultant matrices can be constructed as follows;

$$A = \begin{bmatrix} -\frac{rC+rL}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \qquad B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} * D \qquad C = \begin{bmatrix} rC & 1 \end{bmatrix}$$

Obtaining Transfer Function

From Mohan's book at page 325 this transfer function formula can be seen;

$$T_p(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \mathbf{C}[s\mathbf{I} - \mathbf{A}]^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_d] + (\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}$$

By substituting matrices found before it can be expressed as follows;

$$Tp(s) = \begin{bmatrix} rC & 1 \end{bmatrix} * \begin{bmatrix} s + \frac{rC+rL}{L} & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{1}{CR} \end{bmatrix}^{-1} * \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} * Vd$$

Taking inverse of middle matrices;

$$Tp(s) = \begin{bmatrix} rC & 1 \end{bmatrix} * \frac{1}{s^2 + \frac{s}{CR} + s\frac{rC+rL}{L} + \frac{rC+rL}{LCR} + \frac{1}{LC}} \begin{bmatrix} s + \frac{1}{CR} & -\frac{1}{L} \\ \frac{1}{C} & s + \frac{rC+rL}{L} \end{bmatrix} * \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} * Vd$$

Hence;

$$Tp(s) = Vd\frac{1 + s * rC * C}{LC(s^2 + s(\frac{1}{CR} + \frac{rC+rL}{L}) + \frac{rC+rL}{LCR} + \frac{1}{LC})}$$

Substituting numerical values; C =470 μF, L =1 mH, rC =10 mΩ, rL = 10 mΩ and R =1.8 Ω

$$Tp(s) = 24\frac{1 + s * 4.7 * 10^{-6}}{470 * 10^{-9}(s^2 + s(1182 + 20) + 2.36 * 10^4 + 2.13 * 10^6)}$$

Note that the terms results from rC and rL makes very small effect in denominator, but rC results a zero which may cause considerable differences at high frequencies. Bode plot of this transfer function is obtained using MATLAB, related result can be seen in Figure 2.2. Some comments can be done here as follows. Transfer function has fixed gain and small phase at low frequencies. Magnitude makes a fall with -40 dB/decade beyond the cut off frequency which is located at √(1/LC) and phase approaching -180°. Then slope decreased to -20 dB/decade where zero introduced by capacitor ESR and phase goes to -90°.

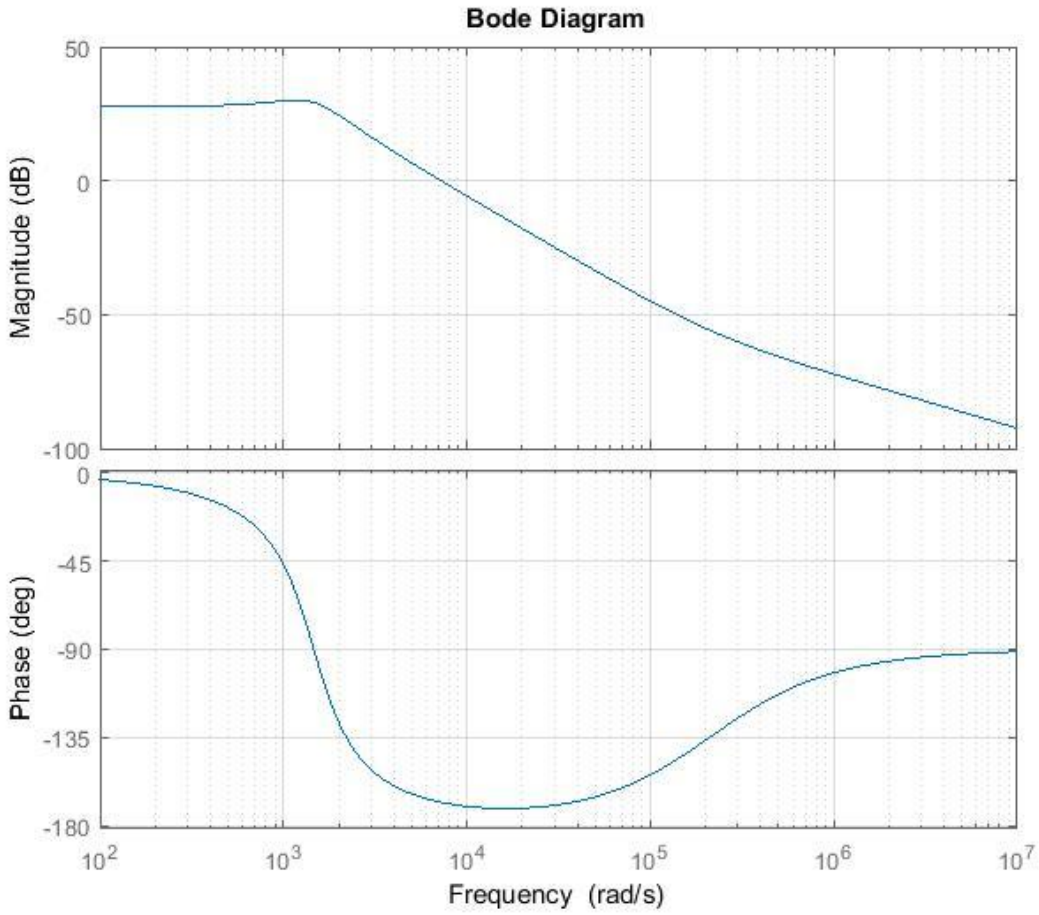

Figure 2.2: Bode plot of analytically calculated transfer function

b)

In this part, transfer function of the buck converter is simulated in order to obtain same transfer function with previous part. PSIM is chosen as simulation environment. The schematic which can be seen in Figure 2.3 is constructed by following procedure explained by official PSIM account on YouTube. As a result, bode plot which can be seen in Figure 2.4 is obtained.

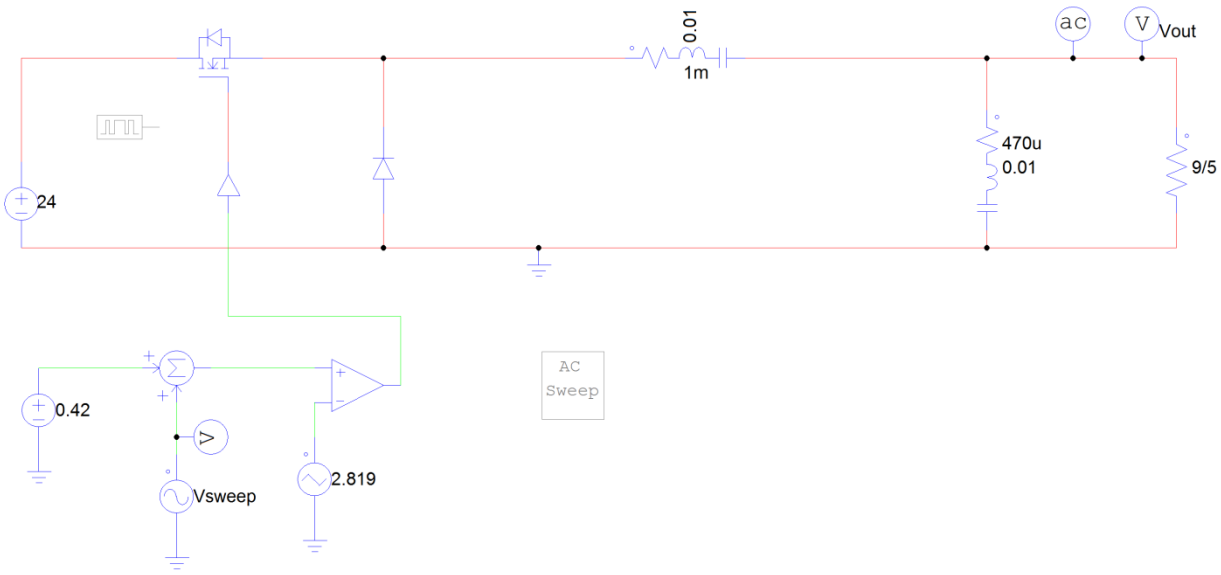

Figure 2.3: The schematic circuit of the designed Buck Converter

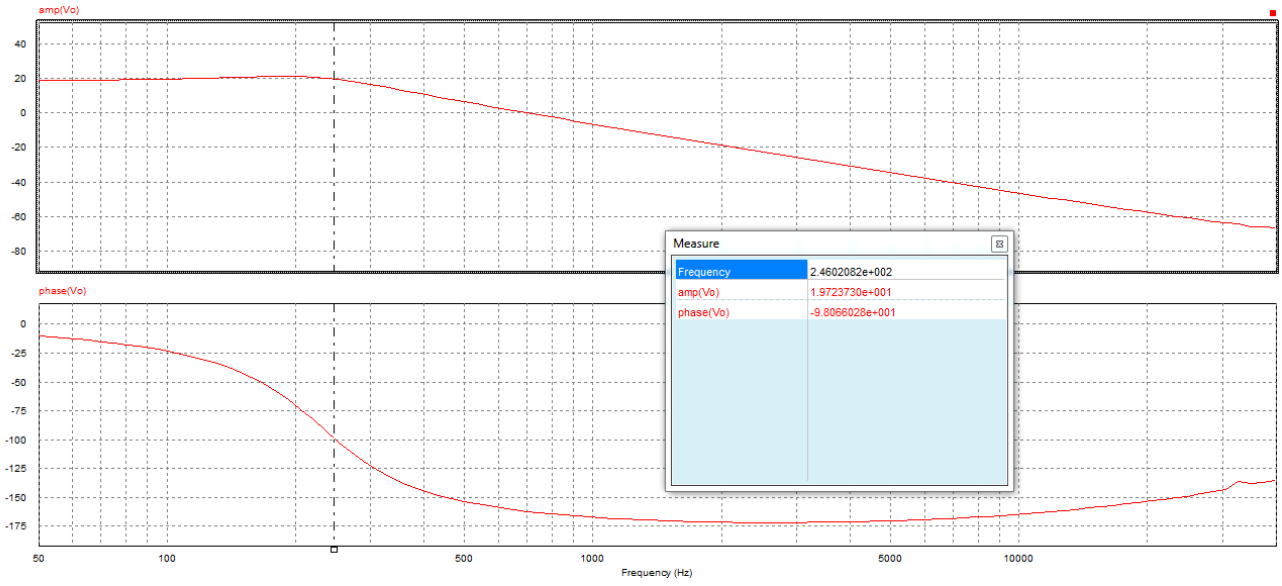

Figure 2.4: The Bode plot of the simulated Buck Converter

As can be seen in both bode plot graphs namely Figure 2.2 and Figure 2.4, they are same noting that one of them is plotted to rad/s while other is plotted to Hz. As a consequence, it can be noted here that phase margin of the converter is about 20° and it should be improved by adding phase at the gain cross over frequency with the Type-2 controller in order to have more stable converter and better transient performance.

c)

In this part, Type-2 controller will be constructed in order to increase phase margin of the converter. Therefore, transient stability can be provided.

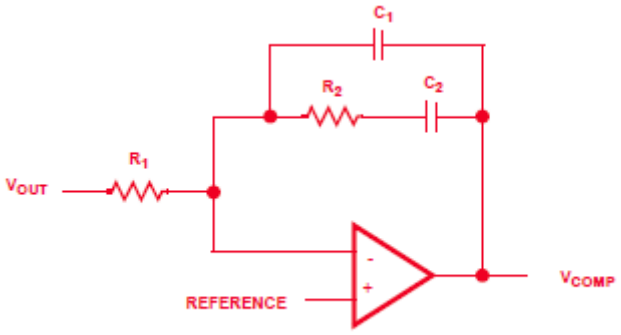

Figure 2.5: Type-2 compensator

Transfer function of the compensator is

$$G(s) = \frac{sC_2R_2 + 1}{R_1C_1s(s\frac{C_1C_2}{C_1 + C_2}R_2 + 1)}$$

This transfer function has one zero at $1/C_2R_2$ and two poles at 0 and$1/\frac{C_1C_2}{C_1+C_2}R_2$. In order to increase the phase margin of the converter bode plot which is in Figure 2.2, zero of the compensator should located around 10^3 rad/s and nonzero pole should be located around 10^5-10^6 rad/s. Let choose R_2 = 1kΩ so C_2 = 1μF and C_1 =1nF. Note that R_1 is just adjusting gain. As R_1 should be very large in order to have very low gain where gain is constant, let R_1 = 100MΩ. The resultant bode plot can be seen in Figure 2.6.

From this point on, simulations are conducted on SIMULINK.

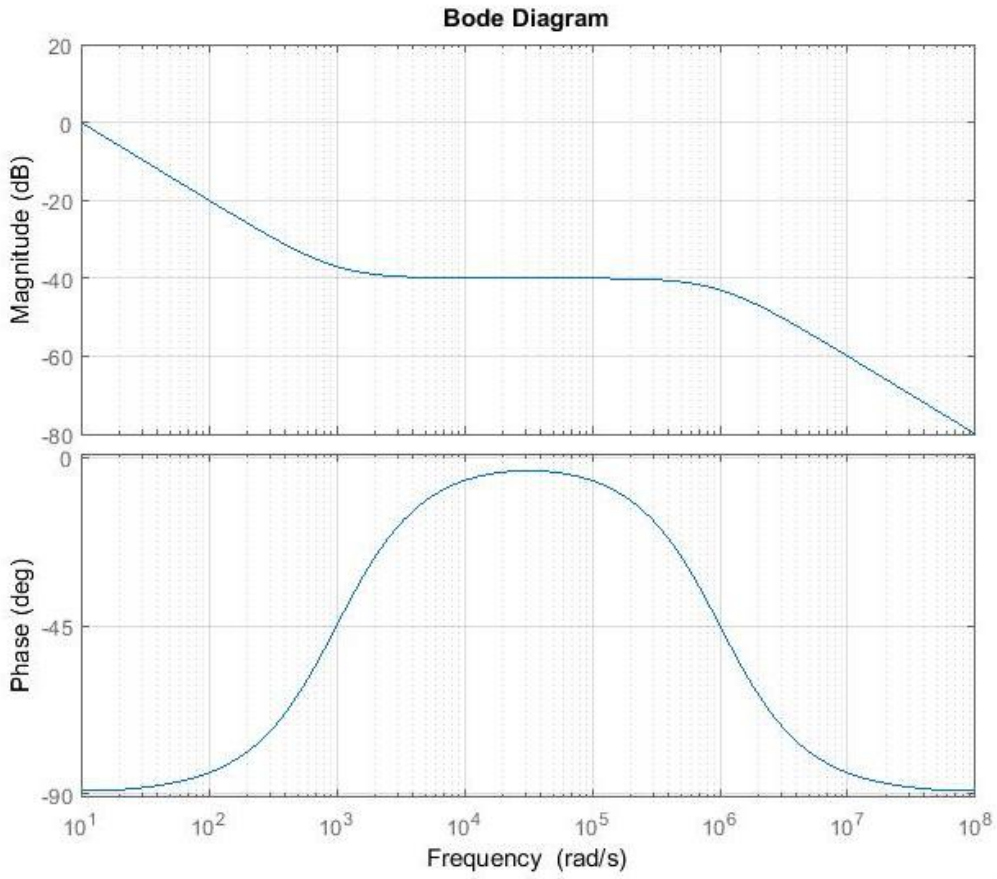

Figure 2.6: Bode plot of the designed Type-2 compensator

From this point on, simulations are conducted on SIMULINK. As SIMULINK does not have opamp model, compensator is implemented as transfer function block and the resultant SIMULINK model can be seen in Figure 2.7.

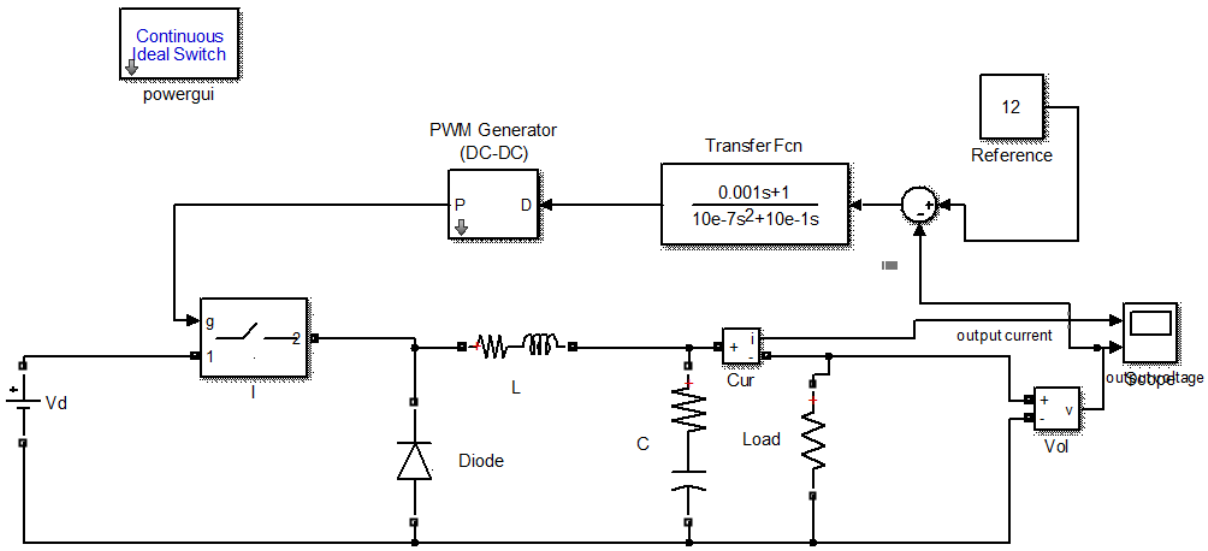

Figure 2.7: SIMULINK blocks of the buck converter with compensator

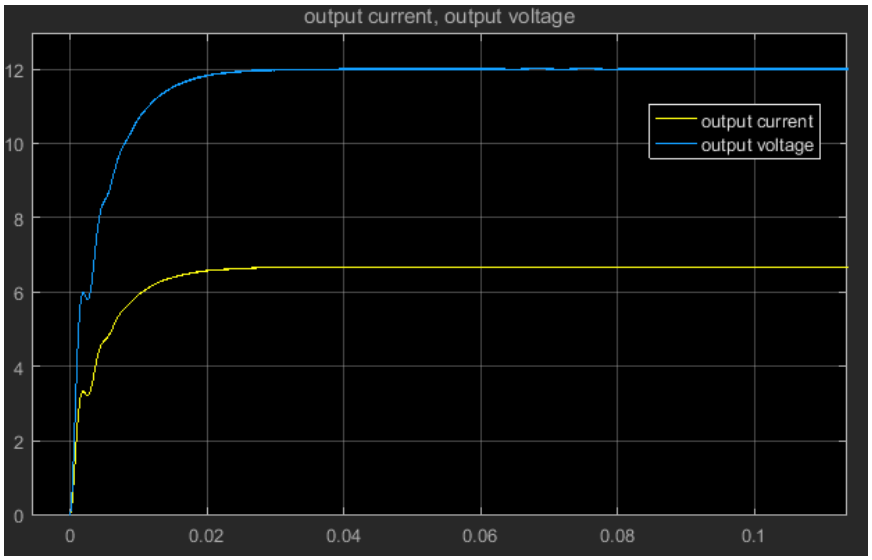

Figure 2.8: Transient response of the converter with compensator

Transient response of the converter with compensator can be seen in Figure 2.8. As can be seen in this figure, converter voltage rises the desired value at 0.02 s with no overshoot and oscillation and zero steady state error. Therefore, transient response of this converter-compensator pair can be considered as stable and enough for many applications.

d)

In order to verify the performance of the controller, load increased half to full suddenly in this step. As seen from Figure 2.9 SIMULINK blocks are constructed in such way that at t=3 load side switch is closed, and output load resistor decreased to 1.8Ω to 3.6Ω. The resultant output voltage and current waveforms can be seen in Figure 2.10. As seen from this figure, it responses very little overshoot and sits to steady state value in very short time. Therefore, controller can be considered as suitable in terms of output load fluctuations.

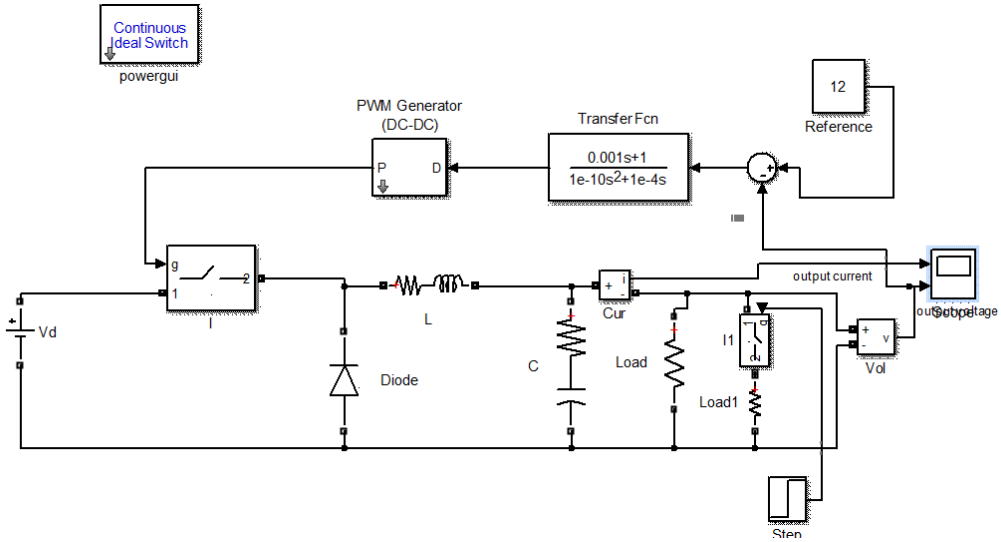

Figure 2.9: SIMULINK blocks of implementing step change to full load from half load

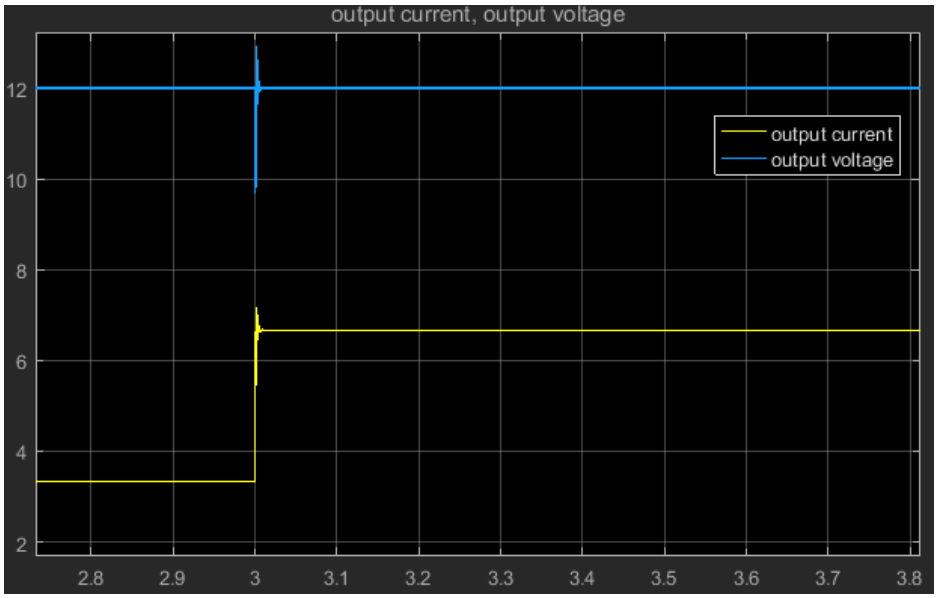

Figure 2.10: The change in the output waveforms when step change to full load from half load

In order to point out the converter output response at some instant input changes SIMULINK blocks which can be seen in Figure 2.11. As seen from this figure input voltage is controlling by two switches and up to t = 4 s input voltage is connected to Vd which is 24 V, after t = 4 s input voltage is connected to Vd-Vd*0.1 which is 21.6. As seen from Figure 2.12, controller behaves very fast and accurate to this input change without any overshoot and oscillation.

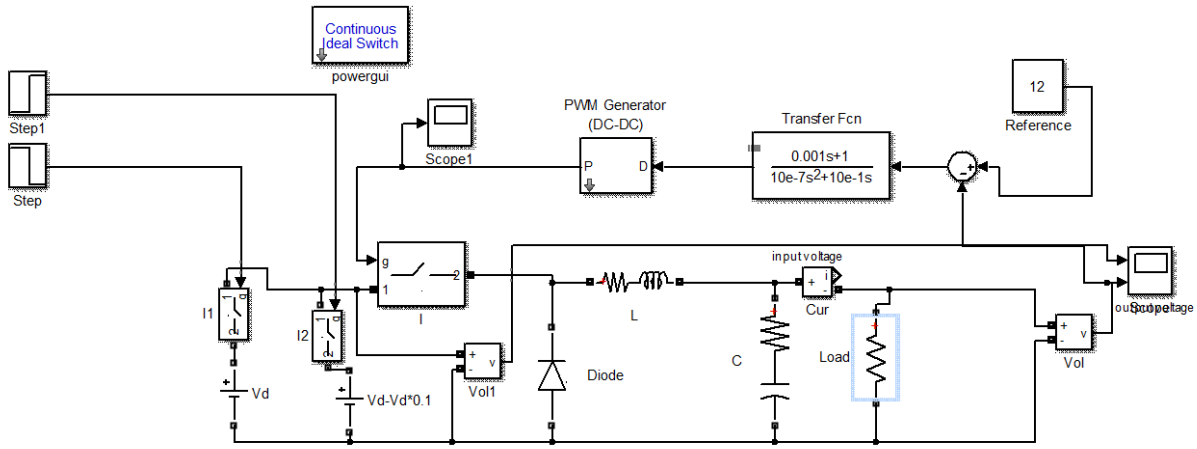

Figure 2.11: SIMULINK blocks of implementing step change to decreased input voltage

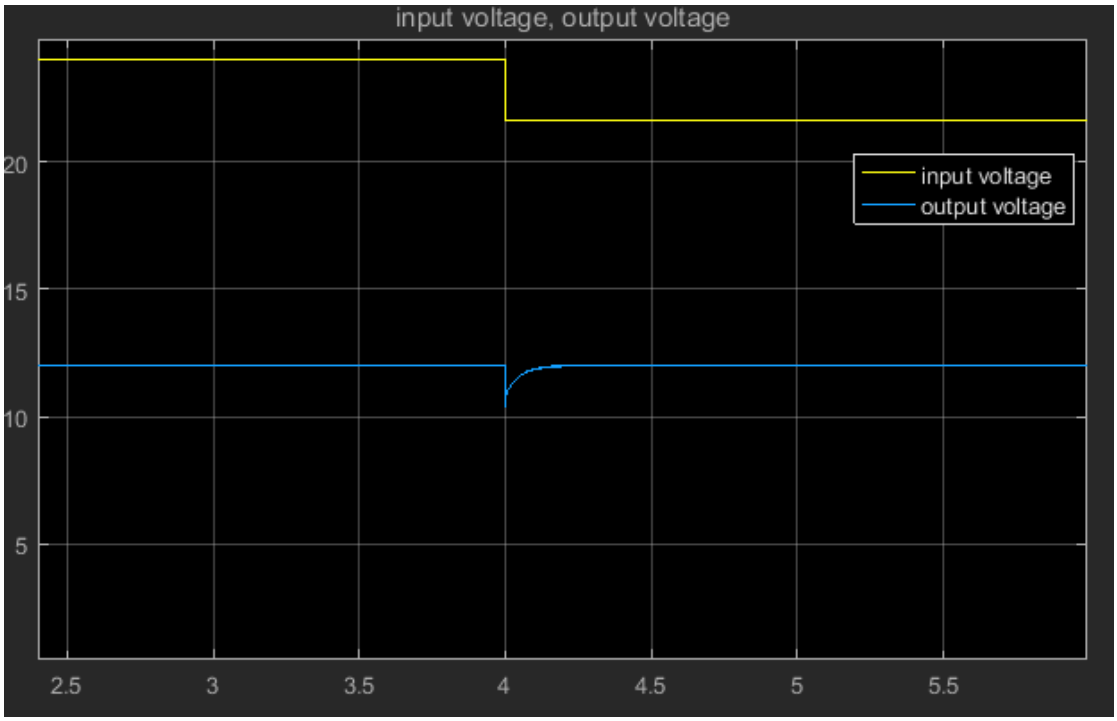

Figure 2.12: The change in the waveforms when step change to decreased input voltage

e)

During the fast changes in the load or supply voltage, the output voltage is changed for a little while and settled to the desired values quite fast. The values of the capacitors and the resistors determines the poles and the zeros of the controller, which are directly determines the performance of the system. The DC gain of the controller can be modified to have a smaller or larger phase margin. We have used type 2 (PI) controller to decrease the steady state error and increase the stability further. However, type of the controller can be chosen differently. For example, PID controller may be chosen if there is a high frequency swing at the output however, settling might be affect with this type of controller.

3. Conclusion

In this project, we have examined different aspects of designing a power supply. In the first part design of a flyback converter is studied. There are several important points in designing of a flyback converter. One of them is the leakage inductance of the transformer causes overvoltages across the switching elements. This effect can be reduced with a better transformer design, however snubber design seems to be necessary to overcome this problem. The other one can be the design of the transformer. The core must be capable of carrying the load current without getting saturated and core loss must be high for the efficiency and cooling considerations.

In the second part, the design of a buck converter and its controller design is examined. The controllers are necessary for the power circuits because in the real life load current or the input voltage is not constant. We have used analog controller because they are simpler to implement and have faster response then the digital controllers. The transfer function of the buck converter is obtained including the parasitic resistances of the passive elements. Depending on this transfer function, bode plots are drawn. To improve the phase margin and reduce the steady state error, a type 2 controller is implemented which is a PI controller. Depending on the values of the resistances and the capacitances of the controller, pole locations can be set and desired bode plot can be obtained. By choosing these values properly, the converters stability can be increased, and the steady state error can be decreased.