Part-A: SSP

1. Is the complete design functional (FIFOs, Logic)?

If not, what issues did you face? Which design blocks are incorrect?

A signal may be following a wrong clock

Yes and no. It follows the specifications, but there are two things about the design:

- I think it takes more a delay of 40 to complete the operations, so you can only see the correct value for the first as I use a lot of clock cycles to synch modules
- Attached screenshots of it working separately under forced inputs
- Attached screenshot of it passing the correct value for the first valid input

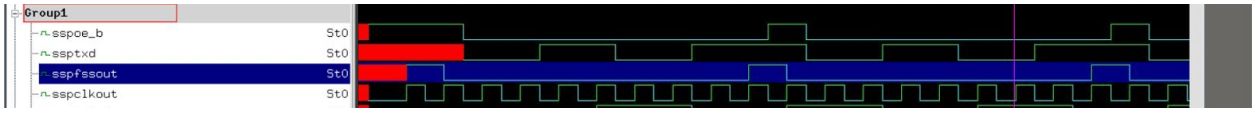
2. Synthesis Results:

	Area	**Arrival Time**
No Optimization	2669.84	-1.19
Area Optimization	2582.55	.45
Timing Optimization	2639.34	-.65

3. Brief description of the strategy used for design:

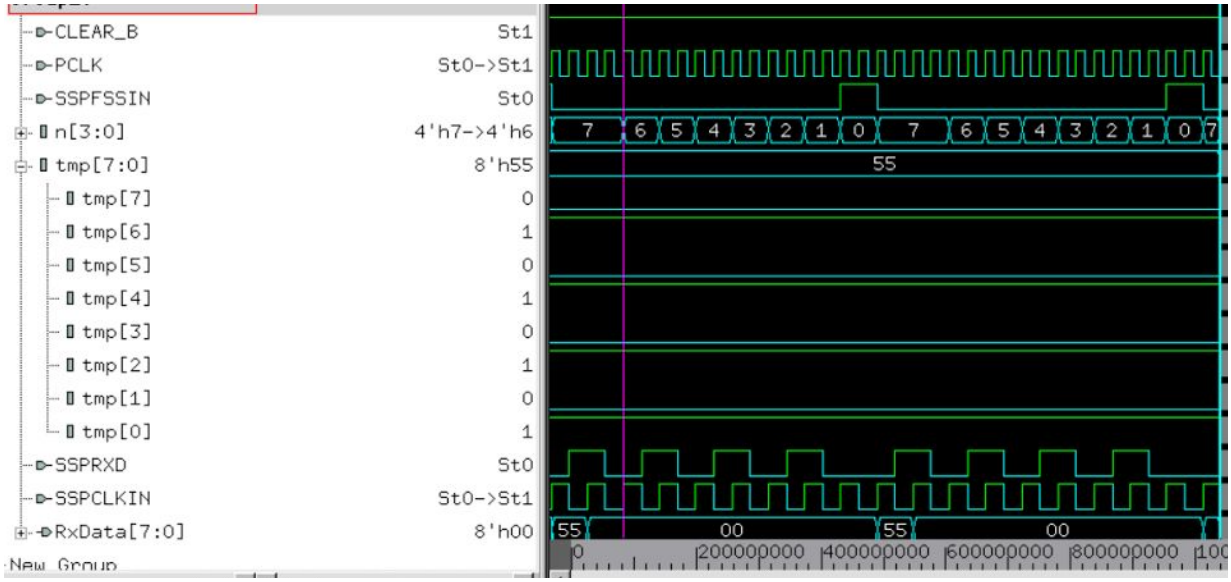
No latches because they are glitchy and slow. Flip Flops rule the design and the course.

Proof of Transmit Works: (feed 00110011)



Proof that FIFO Works:

Proof that Receiver Works and Connected to Transmitter (Transmitted 00110011):



F0 From Testbench: