EE 460R - Lab 1 Report

Name : Haley Alexander (ha5722)
Verified by (TA) :
Date (TA) :

Inverter Characterization:

1. Please fill this table from your simulation results: Truthful

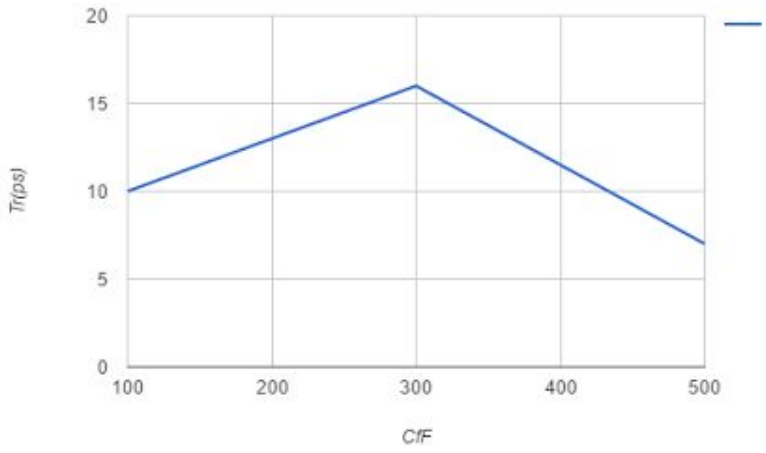
C(fF)	Slew(ps)	Tr(ps)	Tf(ps)
100	10	10	7.02
100	30	9.9	10.26
100	50	33	9.33
300	10	16	3.9
300	30	29.8	21.99
300	50	7.02	22.15
500	10	7.01	7.02
500	30	7.02	6.71
500	50	9.33	10.96

Please fill this table from your simulation results: Theoretical

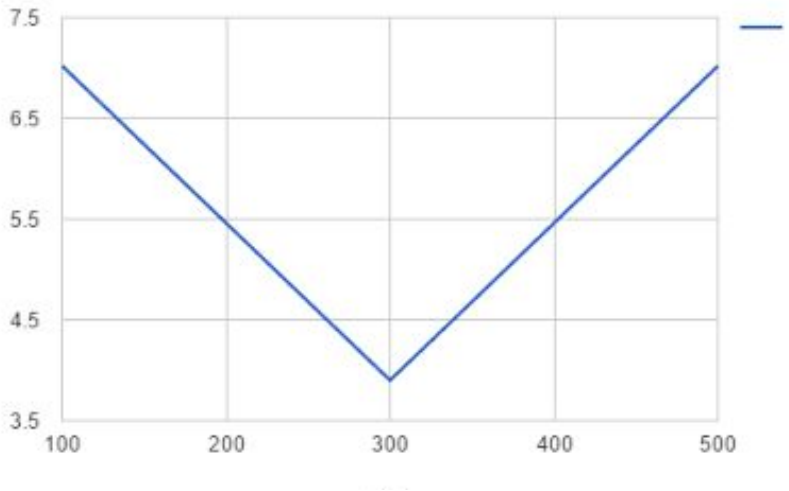
C(fF)	Slew(ps)	Tr(ps)	Tf(ps)
100	10	10	10.02
100	30	9.9	10.26
100	50	10.01	9.33
300	10	16	12.2
300	30	19.8	11.99
300	50	17.02	12.15
500	10	17.01	17.02
500	30	17.02	16.71

500	50	17.33	17.96

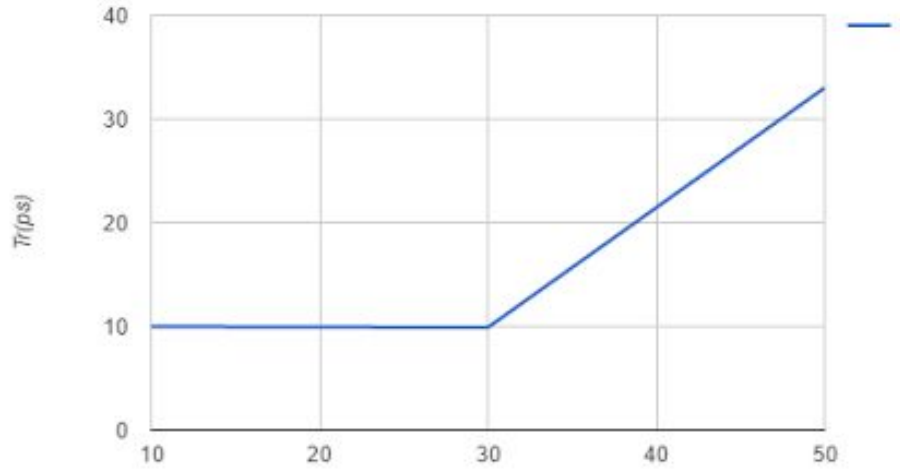
2. Attach the following 4 graphs with this report:
Graph A1: plot Tr against C (keeping slew constant)
Used Slew of 10



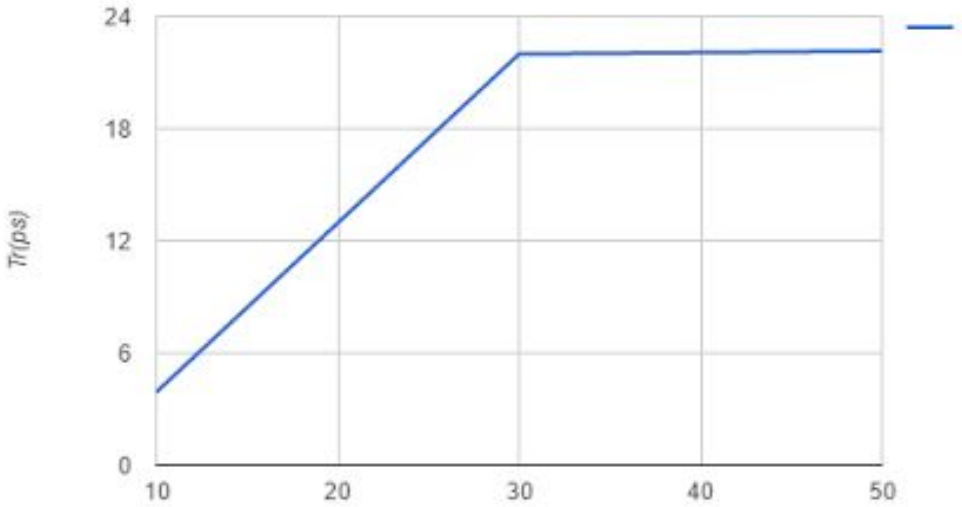
Graph A2: plot Tf against C (keeping slew constant)
Used Slew of 10



Graph B1: plot Tr against slew (keeping C constant)
Used 100fF



Graph B2: plot Tf against slew (keeping C constant)
Used 300fF



Memory Cell:

1. Area of the 4-bit cell
    a. Length of the cell: _9.98_____ um
    b. Width of the cell: __16____ um
    c. Final Area: __159.68_____ sq microns

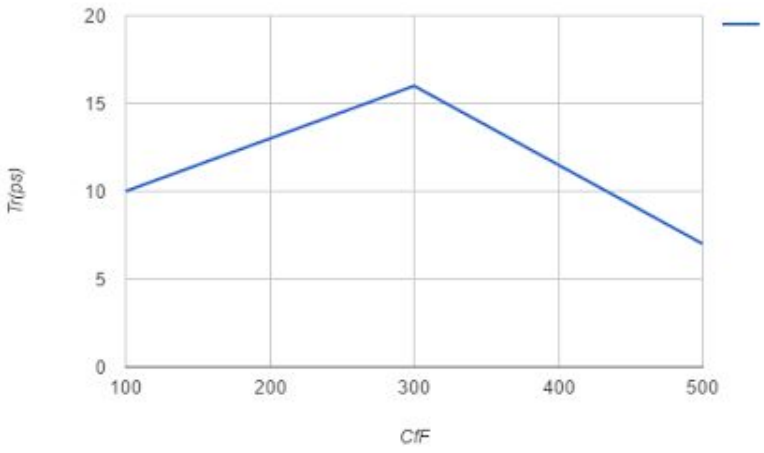
2. Describe the techniques used for area minimization:
    a. Minimize the length of wires for the inputs
    b. Tried to combine transistors together
    c. Used different metal layers to allow crossovers which minimize width
    d. Sharing wells
    e. Using HVH design protocol

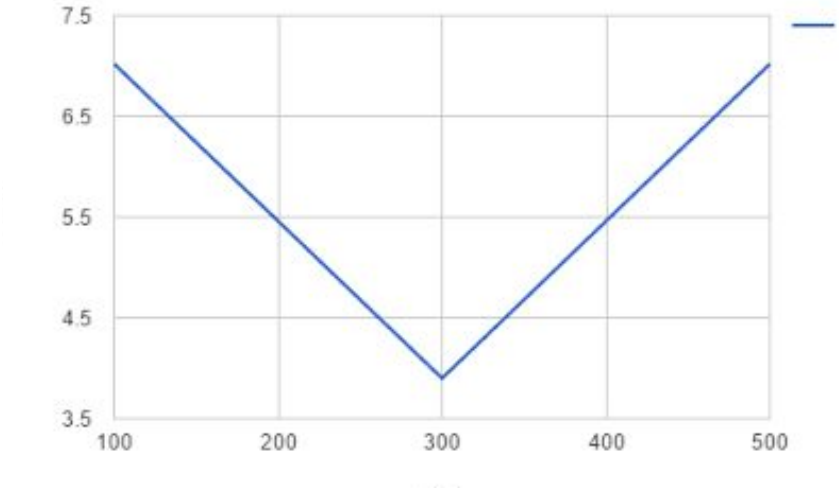
3. Testing of the 4-bit cell:
    a. DRC Pass (Yes/No):
    b. LVS Pass (Yes/No):
    c. Extract Report Clean (Yes/No):
    d. Cell works for “writing 0011 - reading - writing 0101 - reading” (Yes/No):

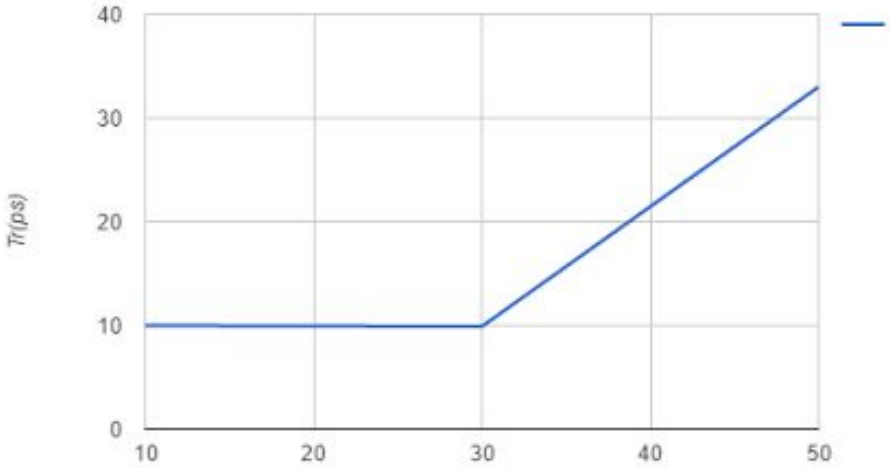
If any answer above is “No”, please explain the issues faced:

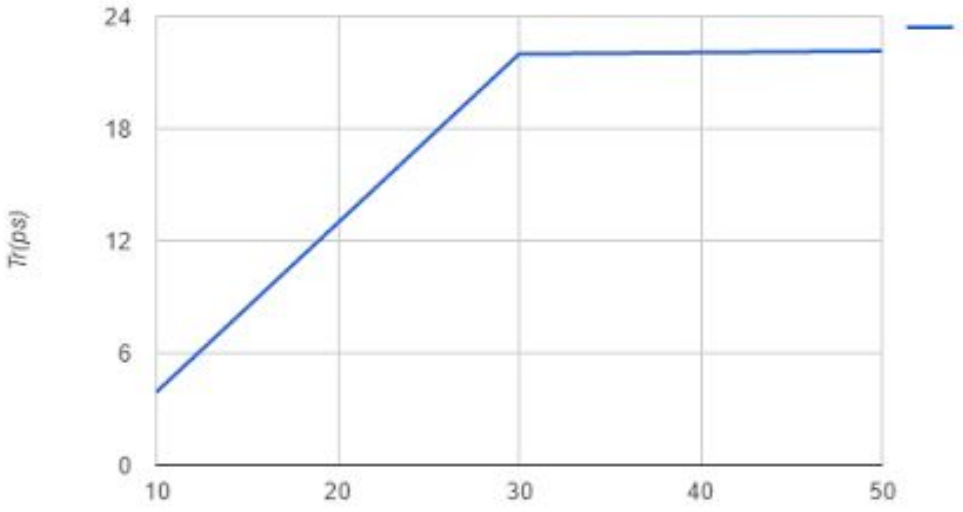
Enclosures Required: (In this order)

1. The 4 graphs as required by “Inverter Characterization” for Tr and Tf

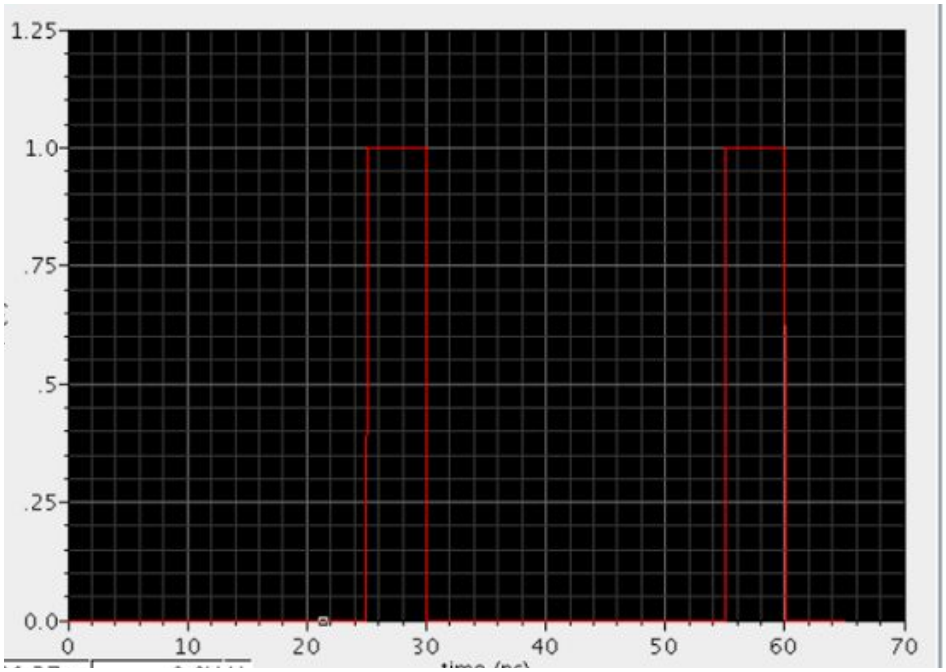


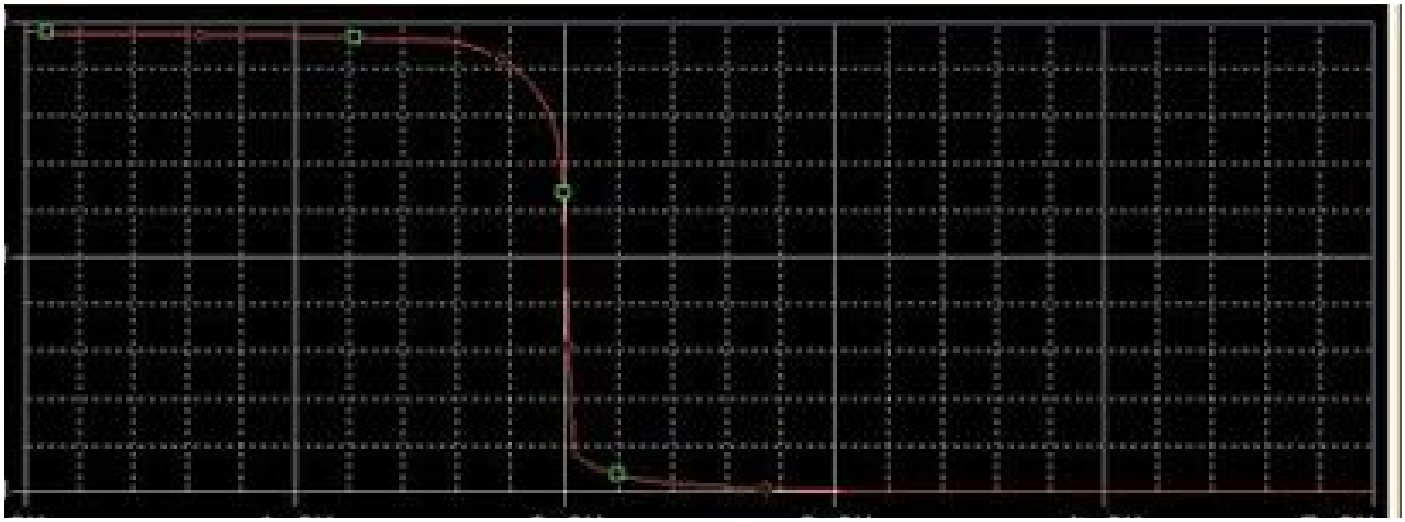

7.5
6.5
5.5
4.5
3.5
100
200
300
400
500


40
30
20
10
0
Tr(ps)
10
20
30
40
50



2. HSPICE waveform for (Tr,Tf) for the ‘max load and max slew case



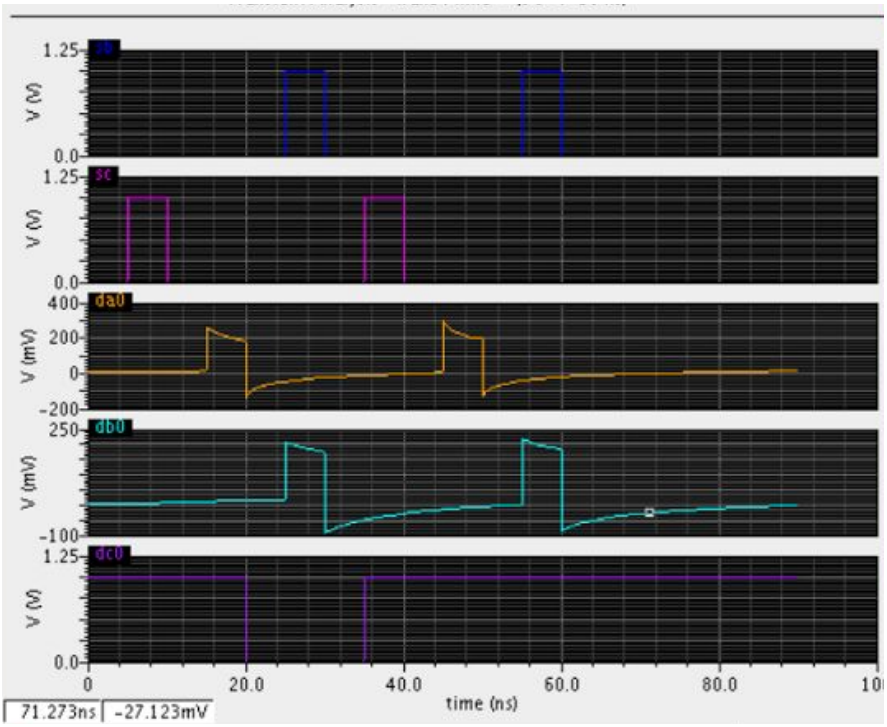


3. *.sp file used in HSPICE to test the 4bit SRAM cell

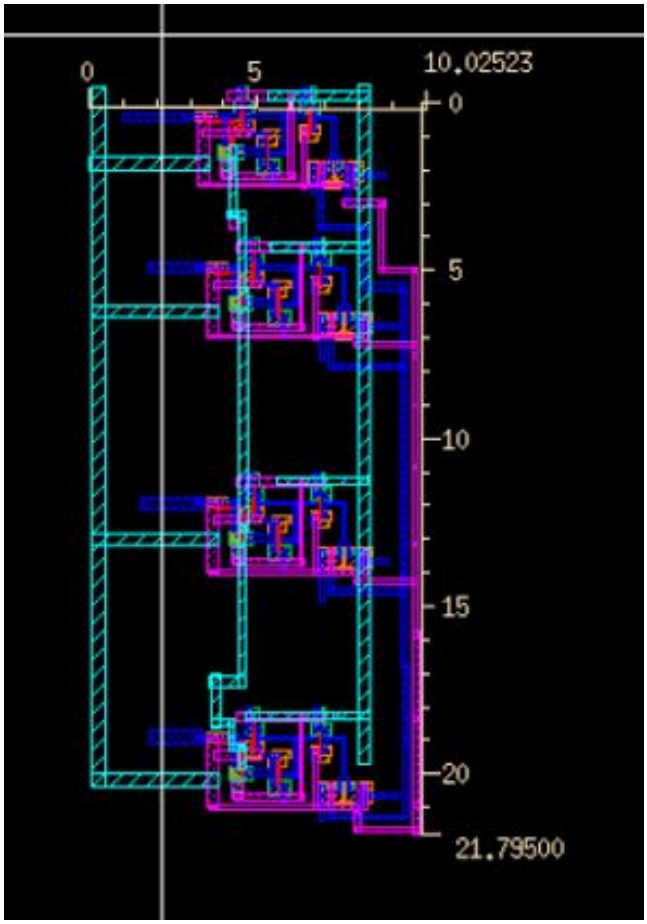
```
************************************

.global

***********change the slew**********
*.param risefall = 10p
************************************

**********change the cap************
*capout INV_OUT 0 100f
************************************

*********Pin Specification**********
** Pin orders should be matched with 'inverter.pex.netlist' ****
x1 SC SA DC0 DC2 DC1 DC3 DB0 DB3 DB1 DB2 DA0 DA1 DA3 DA2 SB GND! VDD!
FourBitMem
************************************

VGND GND! 0 0
VVDD VDD! 0 1

.TEMP 25


Vdc3 dc3 0 pwl (0n 0 0.05n 0 20n 0 20.05n 1 35n 1 35.05n 0 50n 0 70n 0)
Vdc2 dc2 0 pwl (0n 0 0.05n 0 20n 0 20.05n 0 35n 0 35.05n 1 50n 1 70n 1)
Vdc1 dc1 0 pwl (0n 1 0.05n 1 20n 1 20.05n 0 35n 0 35.05n 0 50n 0 70n 0)
Vdc0 dc0 0 pwl (0n 1 0.05n 1 20n 1 20.05n 0 35n 0 35.05n 1 50n 1 70n 1)
```

```
Vsc sc 0 pwl (0n 0 5n 0 5.05n 1 10n 1 10.05n 0 35n 0 35.05n 1 40n 1 40.05n 0 70n 0)
Vsa sa 0 pwl (0n 0 15n 0 15.05n 1 20n 1 20.05n 0 45n 0 45.05n 1 50n 1 50.05n 0 70n 0)
Vsb sb 0 pwl (0n 0 25n 0 25.05n 1 30n 1 30.05n 0 55n 0 55.05n 1 60n 1 60.05n 0 70n 0)

******** Adjust stop time for the simulation to get the waveform you want **************
.tran 10p 90n
************************************


.op
.option post

.END
```

4. HSPICE waveform for 4bit SRAM cell



5. Layout with rulers showing the width and length of the 4bit cell



Prepare to demo/show:

1. 1-bit SRAM schematic and Layout
2. 4-bit SRAM schematic and Layout
3. DRC/LVS/Extraction Report for the 4bit SRAM cell