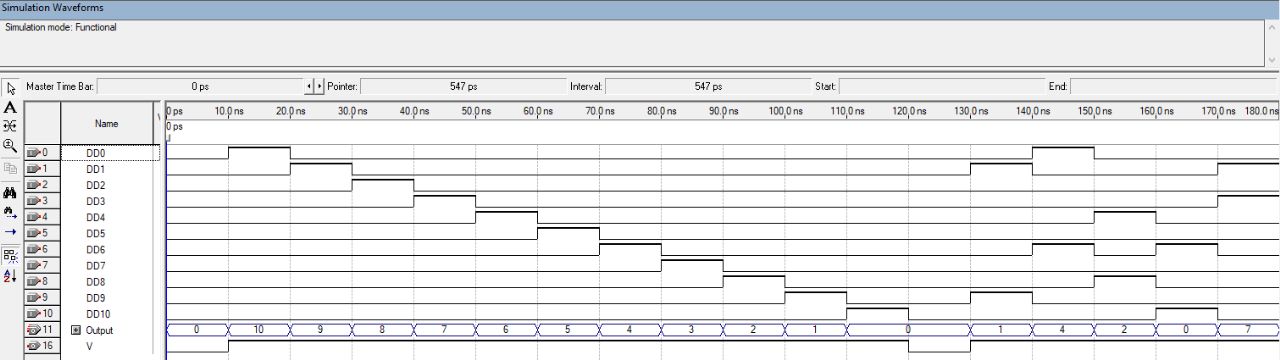
Request Switched:

The input of the floor request switches is connected to an 11-4 decoder that outputs the binary digits of the floor requested and whether the input was valid (invalid encoder input is when all inputs are set to zero), the output of the Encoder is connected to a register that saves the value of the requested floor.

Below is the waveform simulation of the encoder



the waveform of the 4-bit Register

Graphical user interface, diagram

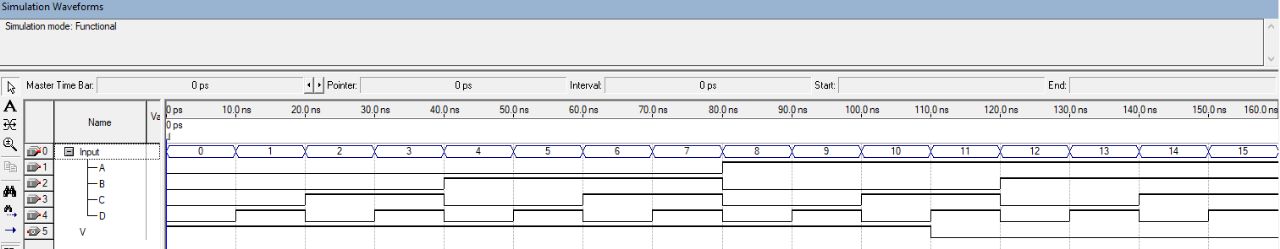
Description automatically generated with medium confidence

Control Switches :

The input of the Control Switches is saved in a register after being checked for valid

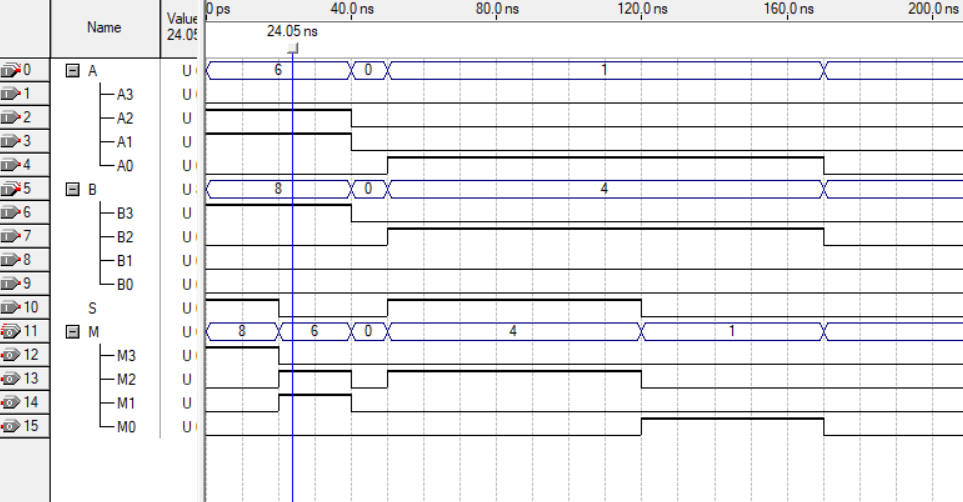
Input between the range of (0-10).

Waveform of the valid input circuit



Our circuit counts to the chosen floor whether it was from the request or control switches, in order to choose between the different inputs they are both connected to a 4-input 2-bit Mux, the Mux’s select line is connected to a negative triggered master-slave d flip-flop that saves the input from the go switch and outputs 1 if the Go switch was turned on, if the Go-Switch was switched on the Control Switch inputs are selected otherwise the Request inputs are.

Waveform of the quad Mux



The “next floor” output coming from the mux will then enter a comparator, if the requested floor is bigger than the current floor the comparator will signal to the counter to count up, if it is equal it will hold the value of the current floor, otherwise it will count down.

Waveform of the comparator

A picture containing graphical user interface

Description automatically generated

Waveform of the counter

Graphical user interface

Description automatically generated with medium confidence

The Output of the counter is connected to the 7-Segment drivers and to a Decoder that signals to the LED light switch of the current floor to turn on

Waveform of the left 7-Segment driver

Graphical user interface, application, table

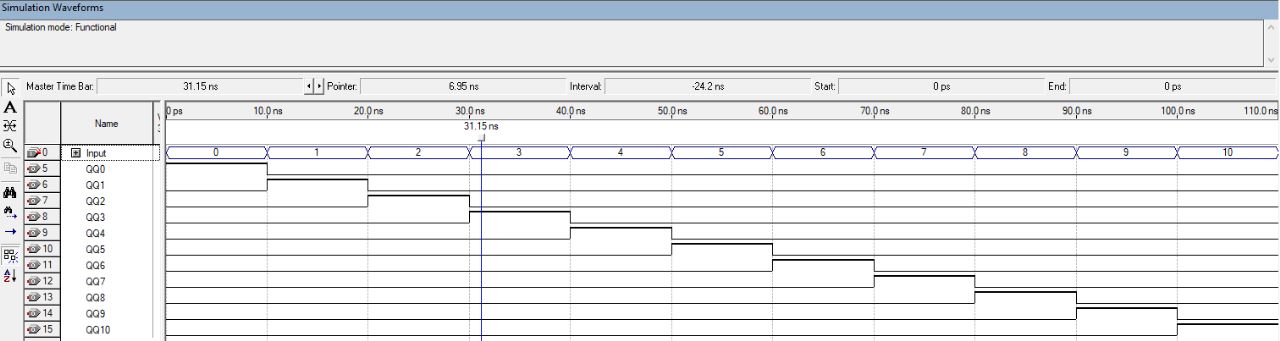
Description automatically generated

Waveform of the right 7-Segment driver

Graphical user interface, application

Description automatically generated

Waveform of the 4-11 Decoder



Waveform of the final circuit

A picture containing table

Description automatically generated

Tasks Timeline

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 20/12 | 21/12 | 22/12 | 23/12 | 24/12 | 25/12 | 26/12 | 27/12 | 28/12 | 29/12 |
| Othman  Milad | Discussing the Design of the circuit:  -Components to be used  -Connections between the component | | | Up-Down Counter | 11-4 Encoder | | Left 7-Segment driver | 4-11 decoder | Testing on FPGA  And preparing the report | |
| Hala  Alfaris | 4-bit Comparator | | Waveform simulation | Revising and making small changes to connections |
| Mustafa  Abu-Obeid | Dff,  4-bit  register | | Valid input circuit | Right 7-  Segment  driver |