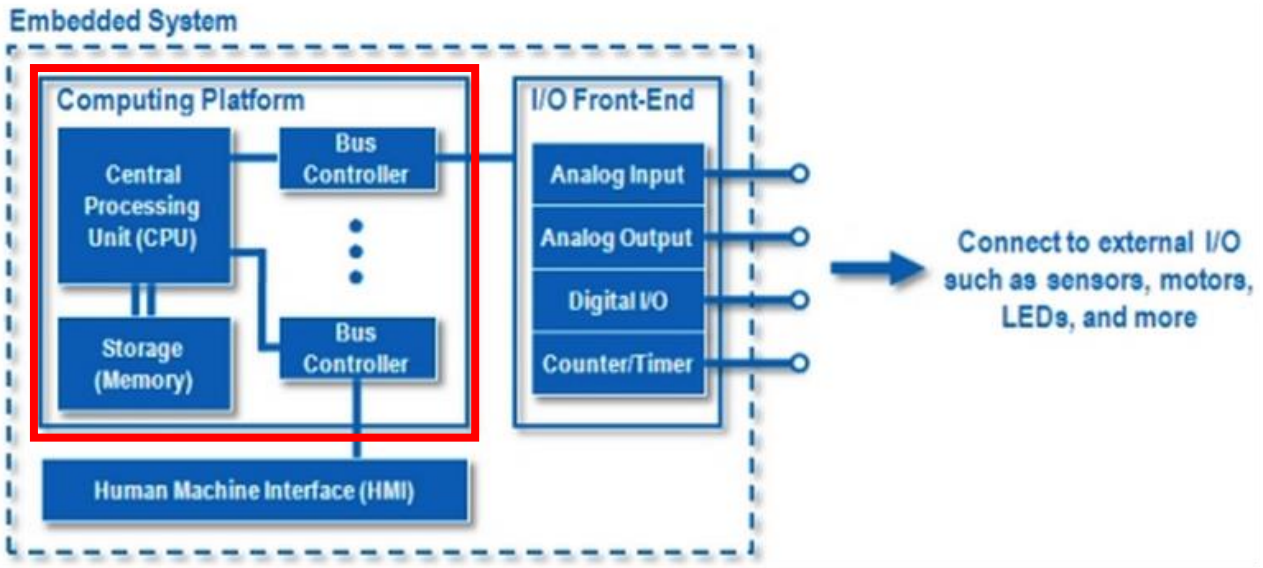
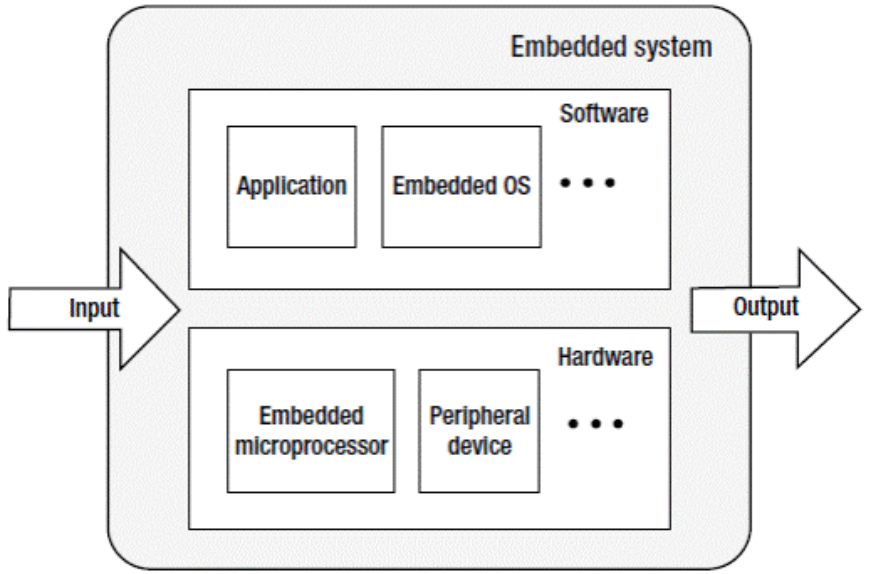
CO3053 – Embedded Systems

2. Embedded Platform Architecture





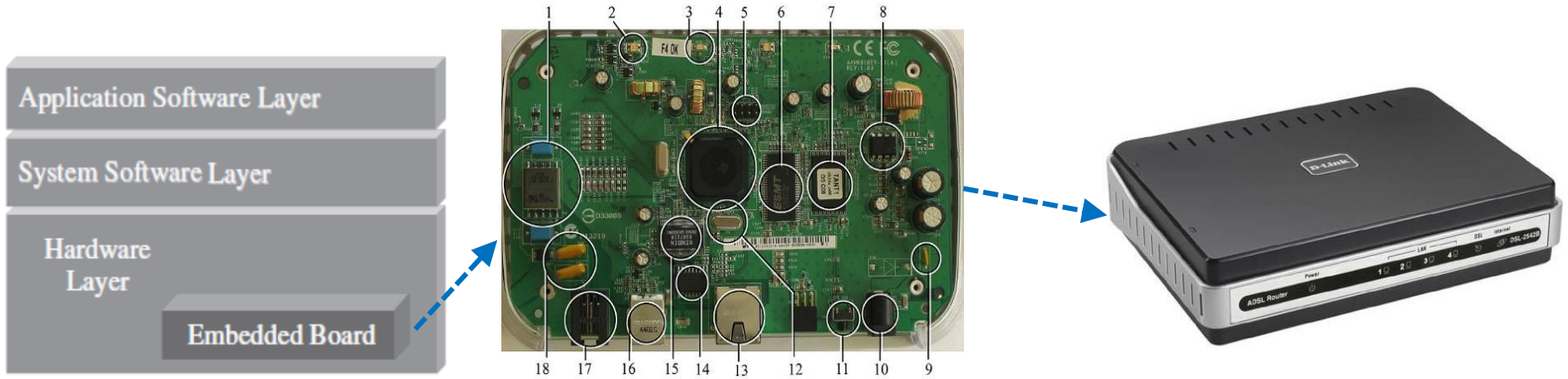
Contents

- Embedded hardware overview
- Processor
- Memory
- Buses

Embedded Board

- In embedded devices, all electronics hardware resides on a **embedded board** or Printed Circuit Board (**PCB**).

- All of hardware on an embedded board is located in hardware layer of **Embedded System Model**



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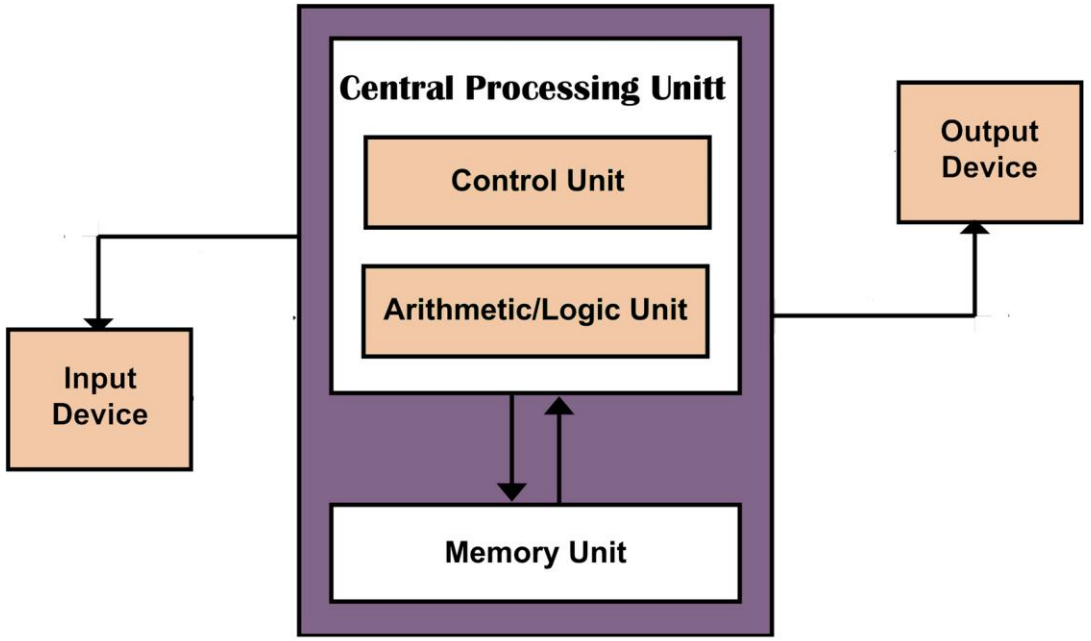
Hardware Block Architecture

- **Central Processing Unit (CPU)**
  - The master processor.
- **Memory**
  - where the system's software is stored.
- **Input Device**
  - Input slave processors and relative electrical components.
- **Output Device**
  - Output slave processors and relative electrical components.
- **Bus**
  - Interconnect the other components includes any wires, bus bridges, bus controllers.



Von Neumann Architecture

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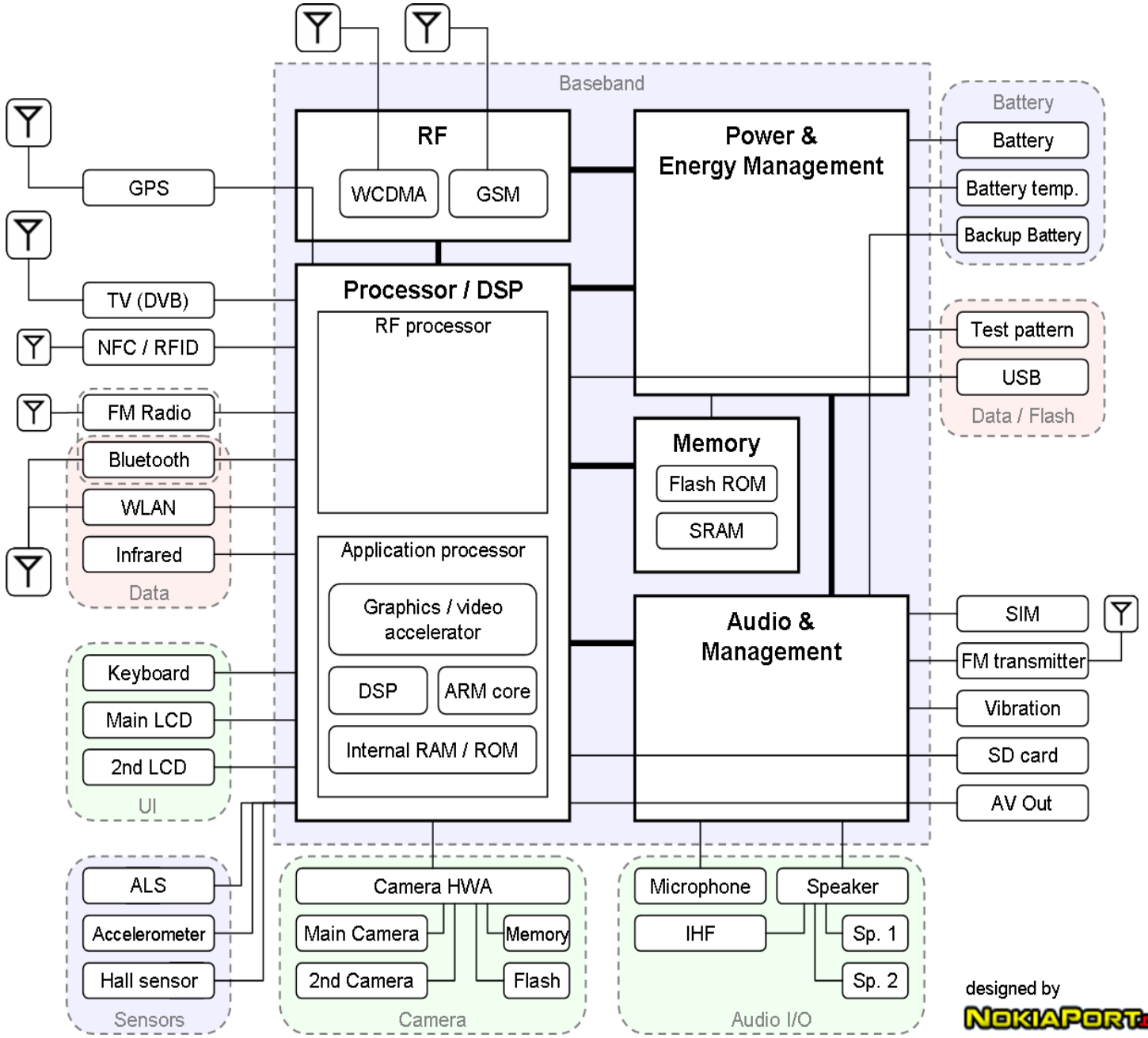

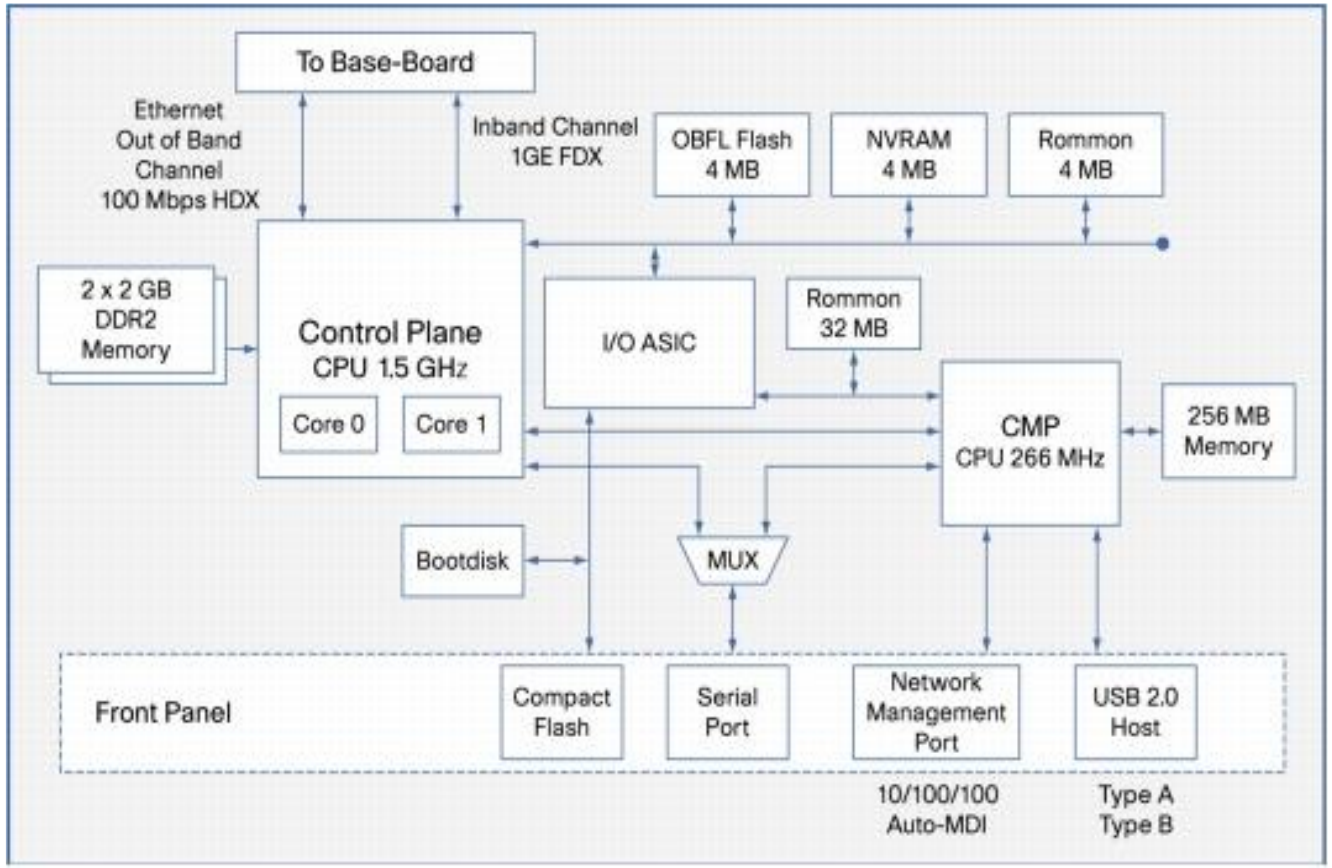

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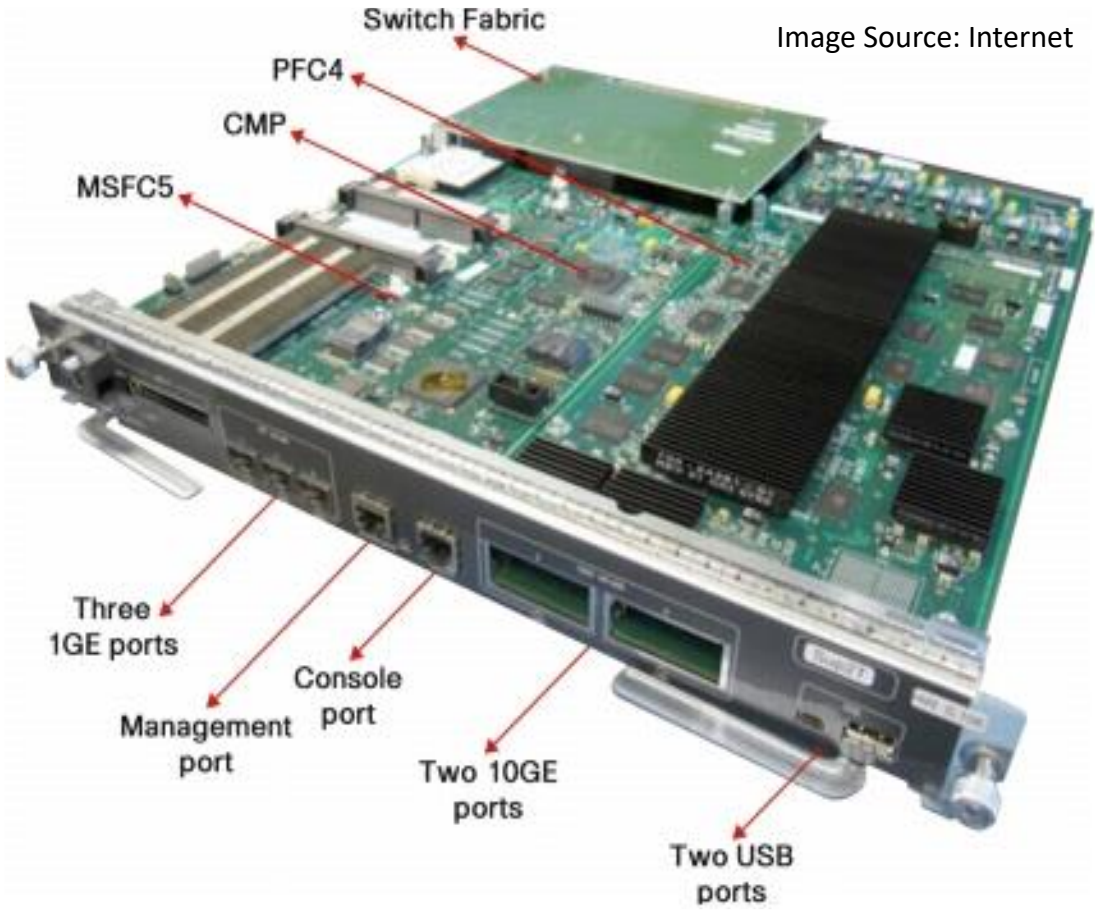

Cisco Catalyst 6500 Supervisor 2T

IPhone 5S

anhpham@hcmut.edu.vn

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Processors

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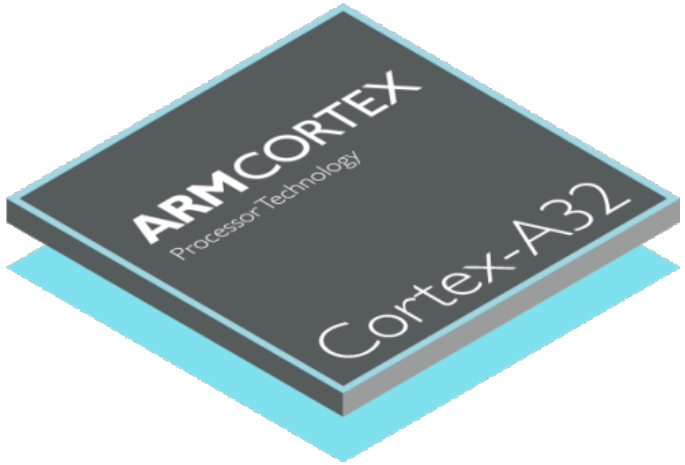
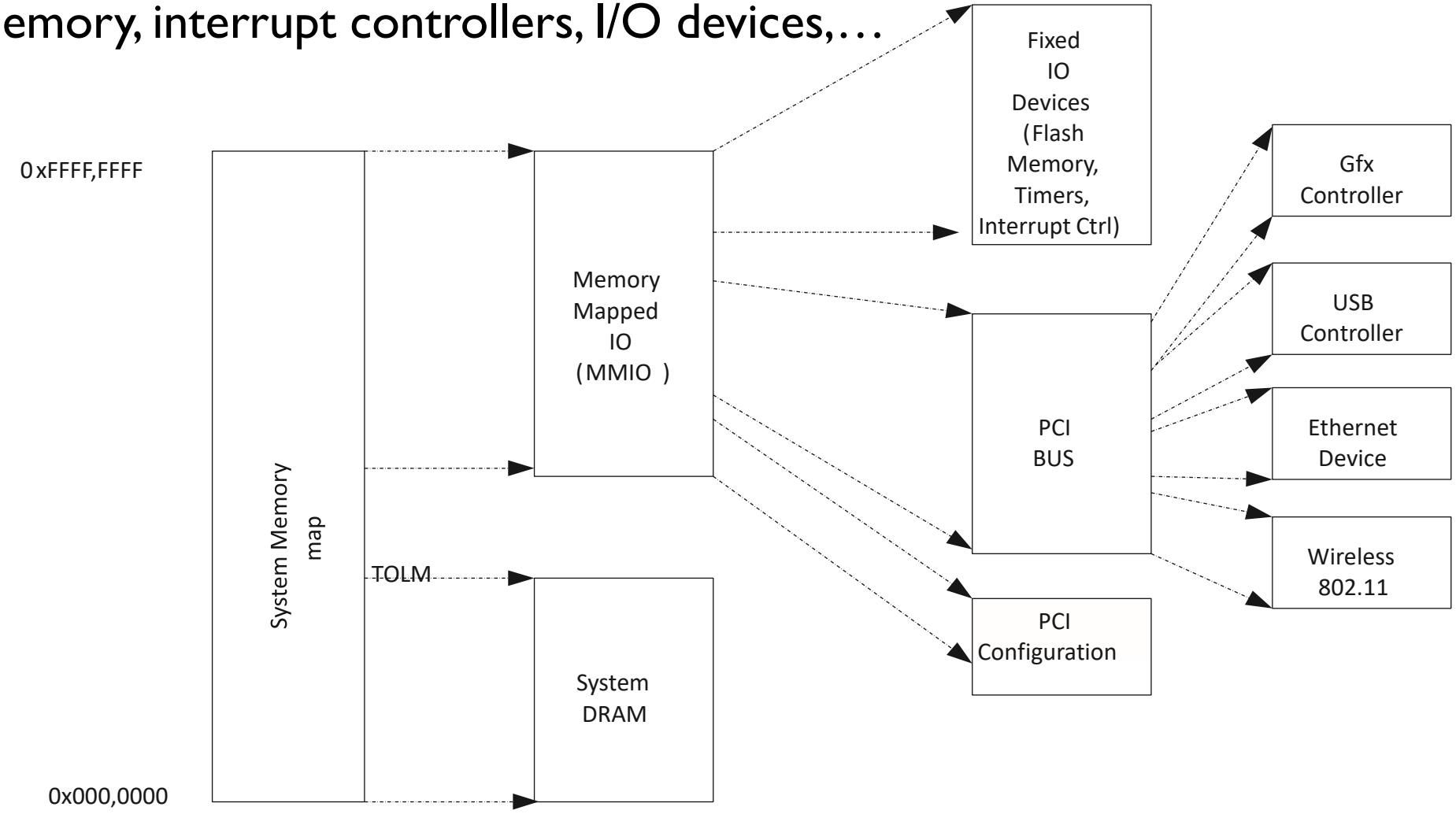
- **The center of the platform.**
  - **32 bit** or **64** bit processor
  - Complex Instruction Set Computer (**CISC)**
    - Example: Intel processor
  - Reduced Instruction Set Computer (**RISC)**
    - Example: ARM, MIPS, Power PC
  - **Scalar** or **superscalar** architecture.
    - SISD vs. MIMD



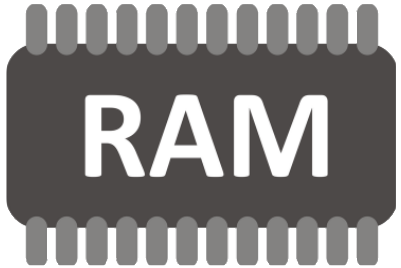
System Memory Map

- Memory map is a list of physical addresses of all the resources on the platform
  - DRAM memory, interrupt controllers, I/O devices,…

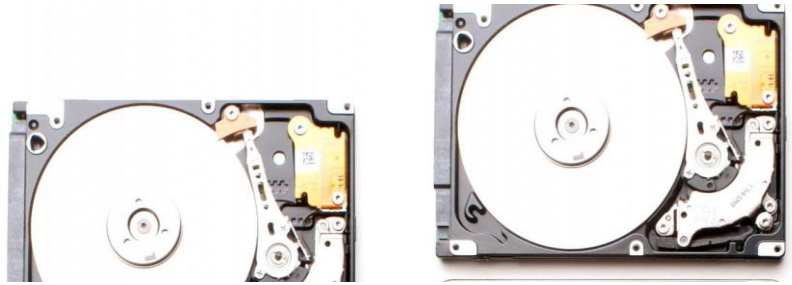


Volatile Memory Types

- Volatile Memory
  - Static Random Access Memory (SRAM)
    - Generally expensive.
    - Used inside processors.
  - Dynamic Random Access Memory (DRAM)
    - Longer access times than SRAM.
    - Used as main memory in computer systems.
    - SDR SDRAM, DDR, DDR2, DDR3



- Nonvolatile Memory (Storage)
  - Retain data even when the power is removed from the device
    - OS, application, configuration, user data, …
  - Varying storage
    - Capacities, densities, performance reliability, and size
  - Two primary nonvolatile storages
    - Solid state memory (SSD): NOR flash, NAND flash.
    - Magnetic storage media: hard drives (HDD).



Buses

- All of major components are interconnected via buses.
  - Bus is simply a collection of wires carrying various data signals, addresses, and control signals (clock, ack, data type).
- On more complex boards, multiple buses can be integrated on one board.
- **Bus Types**
  - System buses
  - Backplane buses
  - I/O buses
- **Bus Expansion**
  - PCMCIA, PCI, IDE, SCSI, USB
  - I2C, SPI
- **Bus Arbitration & Timing**

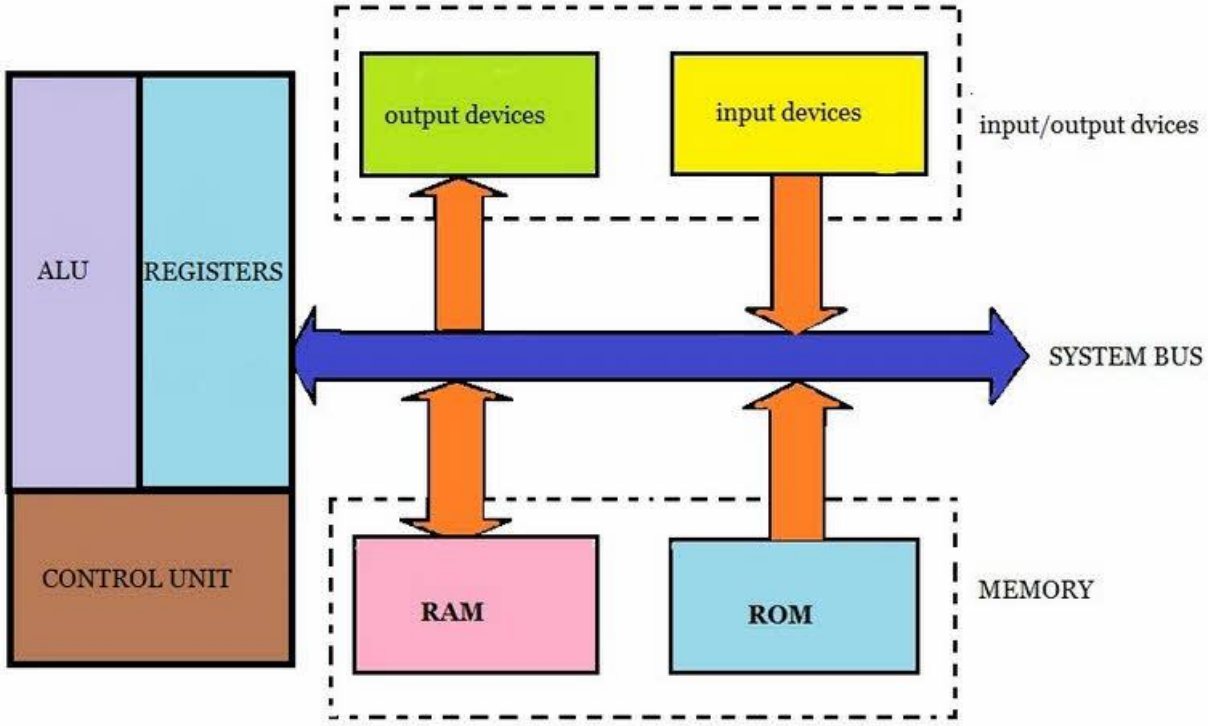


Image Source: Internet

Bus Types

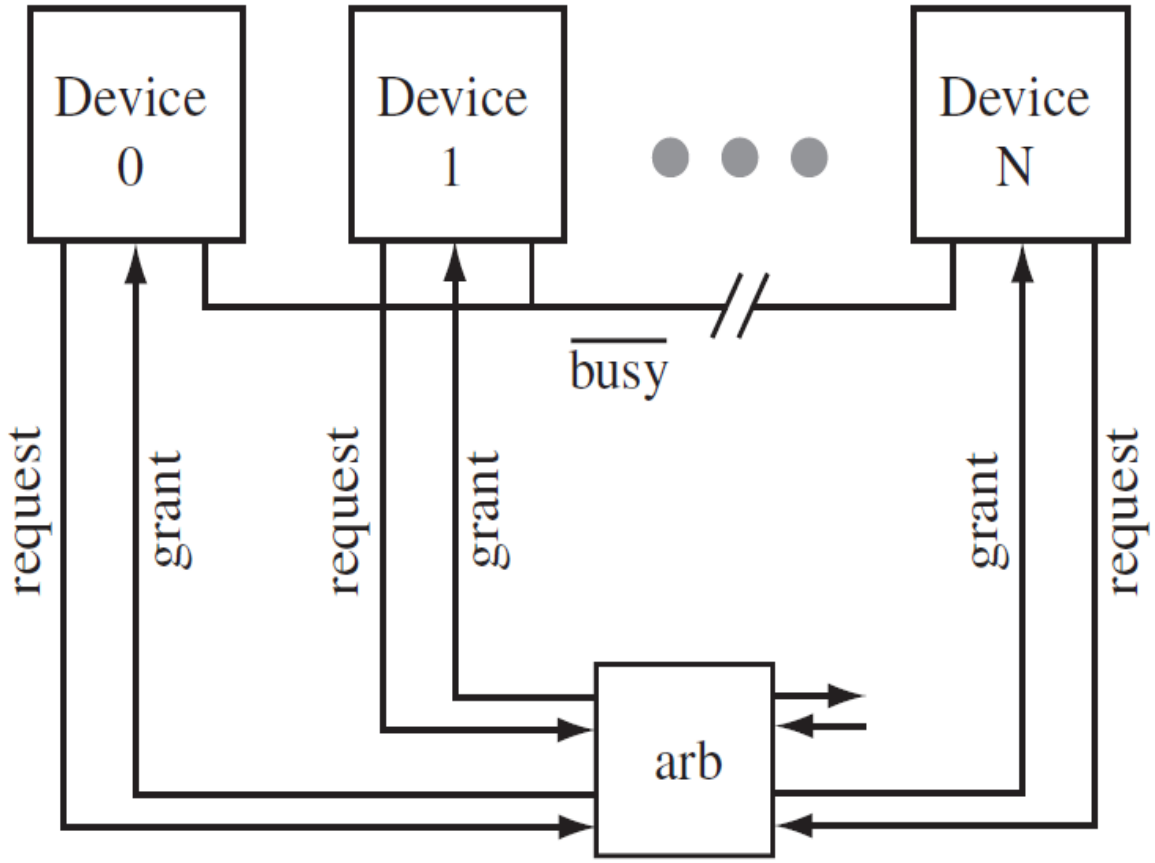
- System buses
  - Interconnect external main memory and cache to the master CPU and any bridges to other bus.
  - Typical short, high speed.
- Backplane buses
  - All in one bus, interconnect memory, master processor, I/O devices.
- I/O buses
  - Extensions of the system bus to connect I/O devices to system bus via bridge or processor I/O ports.

Bus Arbitration and Timing

- Every bus includes some type of protocol that defines bus **arbitration**, **handshaking** and **signals**.
- Bus arbitration - process of gaining access to the bus, determine by bus's arbitration scheme
- Bus handshaking – way to communicate over the bus, determine by bus's timing scheme
- Bus arbitration scheme
  - Master devices, devices that can initiate a bus transaction.
  - Slave devices, devices that can only gain access to a bus in response to master device's request.
  - Multiple master scheme require arbitrator

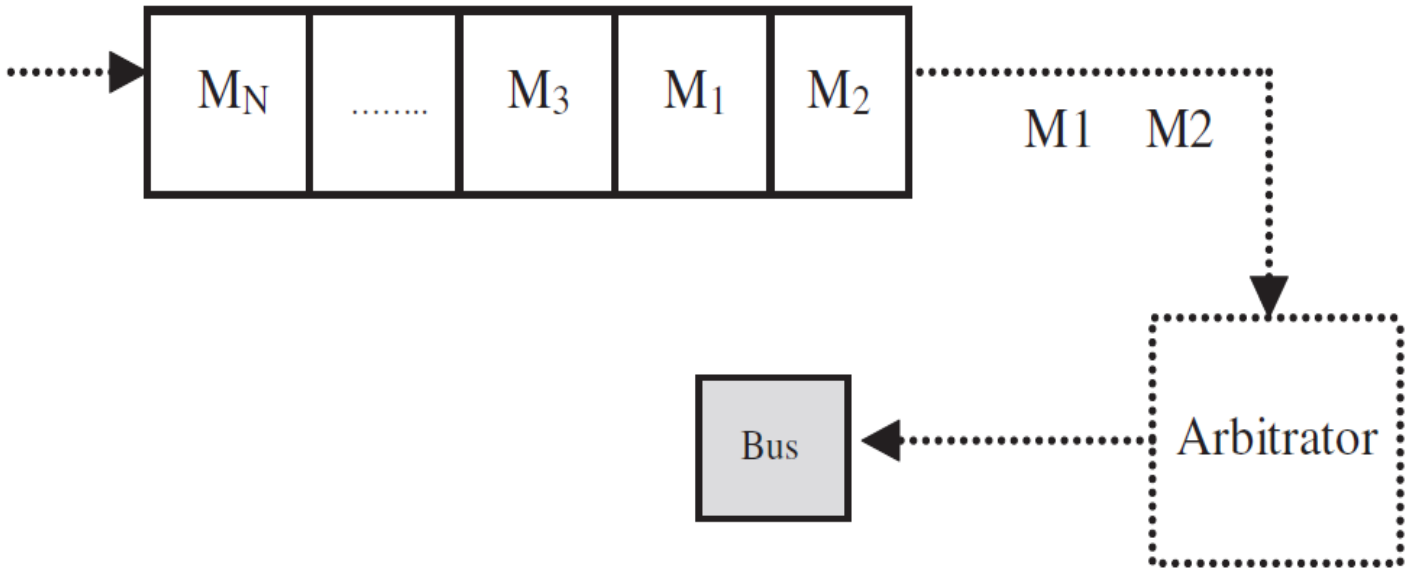
Bus Arbitration - Dynamic Central Parallel Scheme

- Arbitrator is centrally located, all bus masters connect to the central arbitrator.
- Masters are granted access to the bus via **FIFO** or **Priority-based** system.



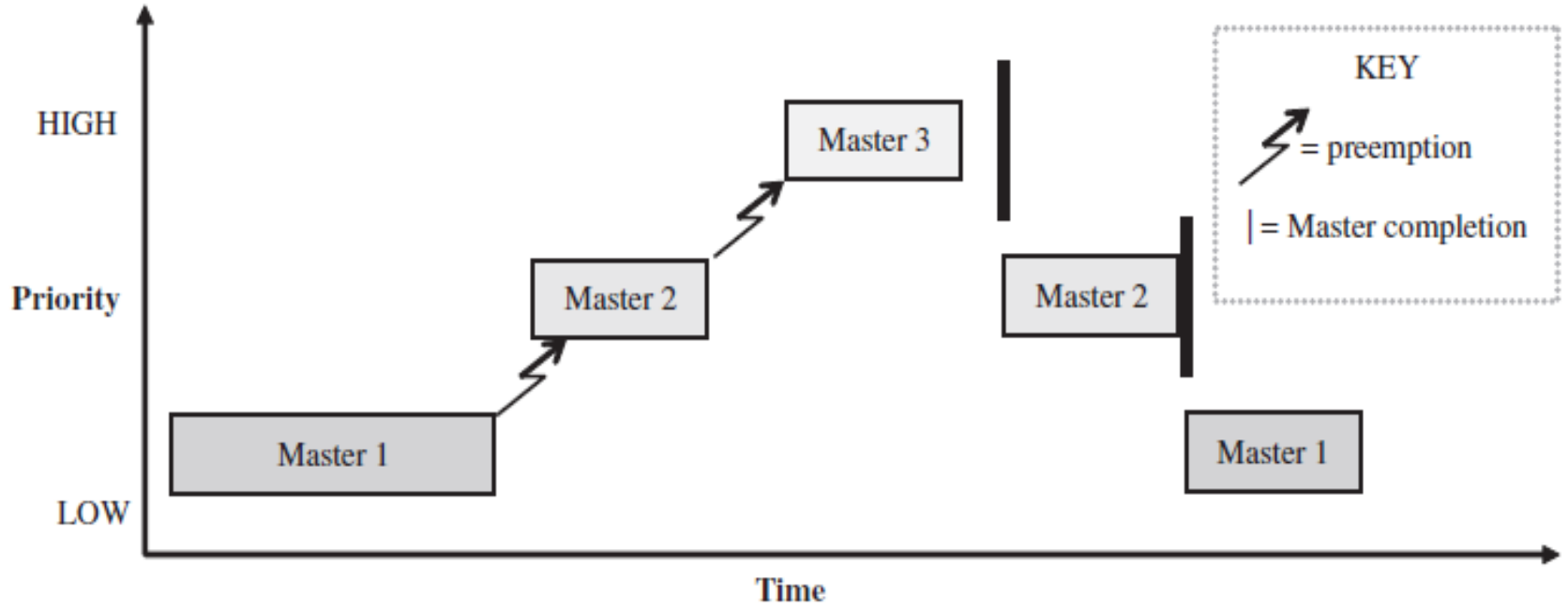
FIFO-based Arbitration

- FIFO queue stores list of master devices ready to use the bus in order of bus requests.
- Master device is allowed access bus from the start of the queue.
- However, arbitrator don't intervene even if the master at the front never release its control.



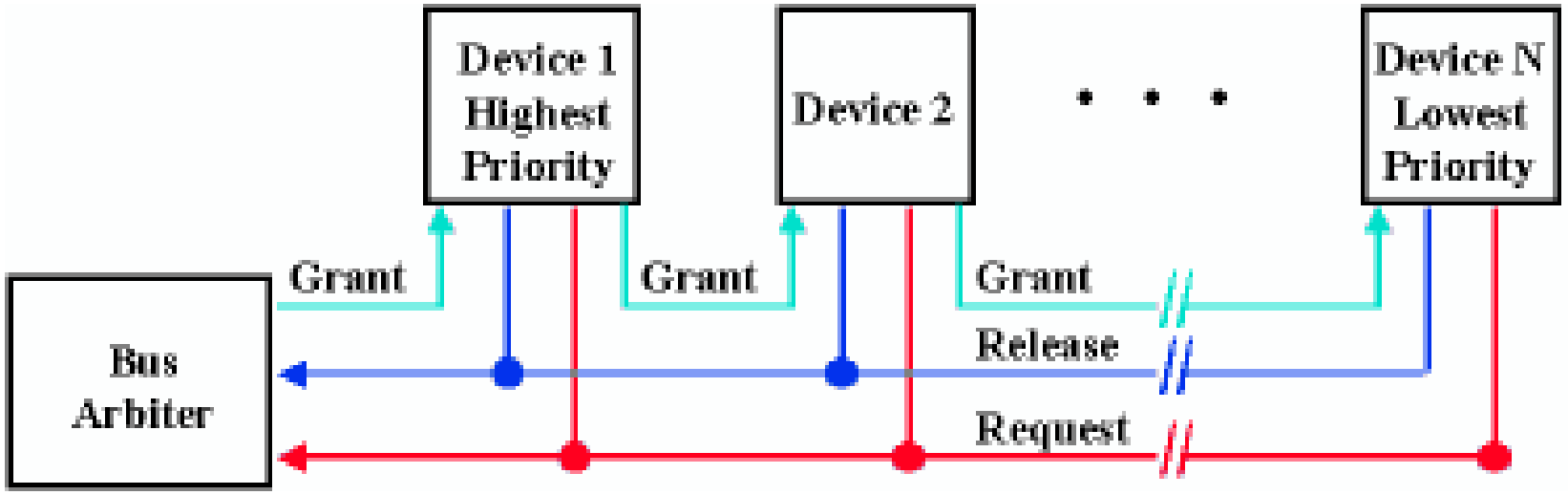
Priority-based Arbitration

- Every master device is assigned a priority.
- For preemptive priority-based, the master with highest priority can preempt lower priority devices.



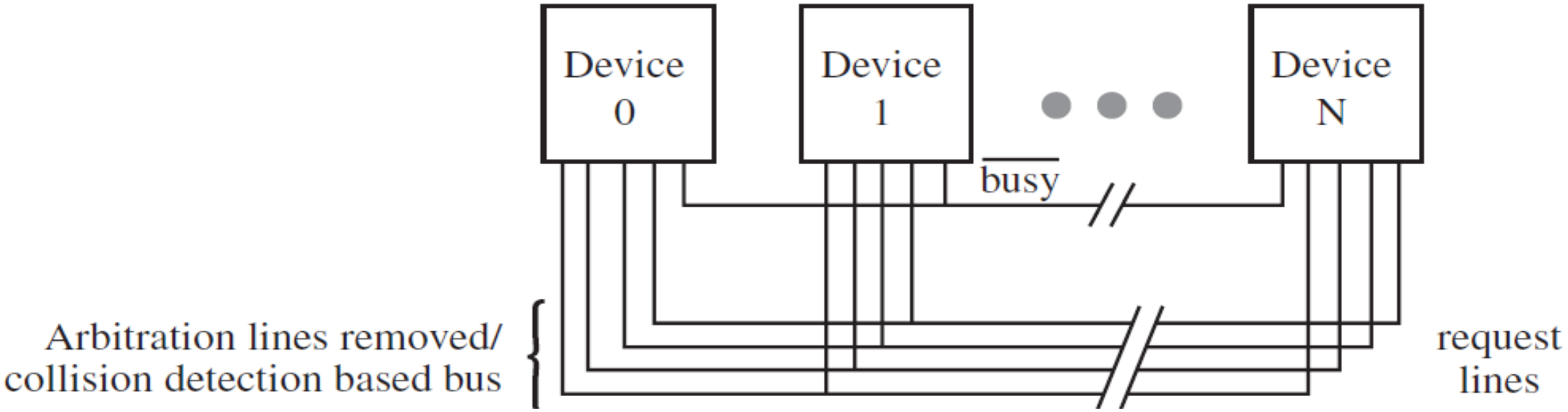
Bus Arbitration - Central-serialized Scheme

- **Central-serialized (daisy-chain) arbitration**
  - Arbitrator is connected to all masters, and the masters are connected in serial.
  - The first master in chain is granted the bus, and pass the "bus grant" on the next master when the bus is no longer needed.



Bus Arbitration - Distributed Arbitration Scheme

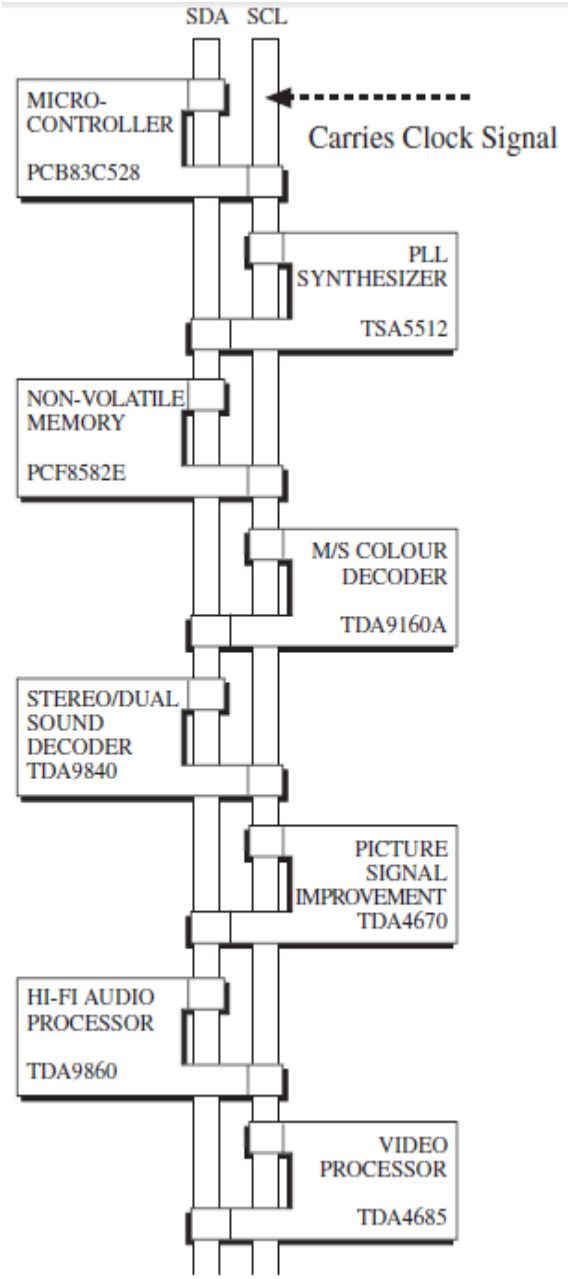
- No central arbitrator and no additional circuitry.
- Master arbitrate themselves by trading priority information.
- Or could remove arbitration lines and listen to collision.



Bus Timing Scheme

- **Synchronous timing scheme**
  - A synchronous bus includes a clock signal.
  - All components run at the same clock rate as bus.
  - Data is transmitted either on the rising or fallings edge.
  - Problem with long bus and high clock rate, potential of a skew in the synchronization.

- **Asynchronous timing scheme**
  - Using "handshaking" signals instead of clock signal.
  - More complicate in handling request and reply command.
  - Could support long bus and larger number of components.
  - Need other "synchronizer" to manage the exchange of information.



Bus Expansion

- **Expandable bus**
  - PCMCIA, PCI, IDE, SCSI, USB
  - Additional components can be plugged into the board on-the-fly.
  - More expensive to implement.

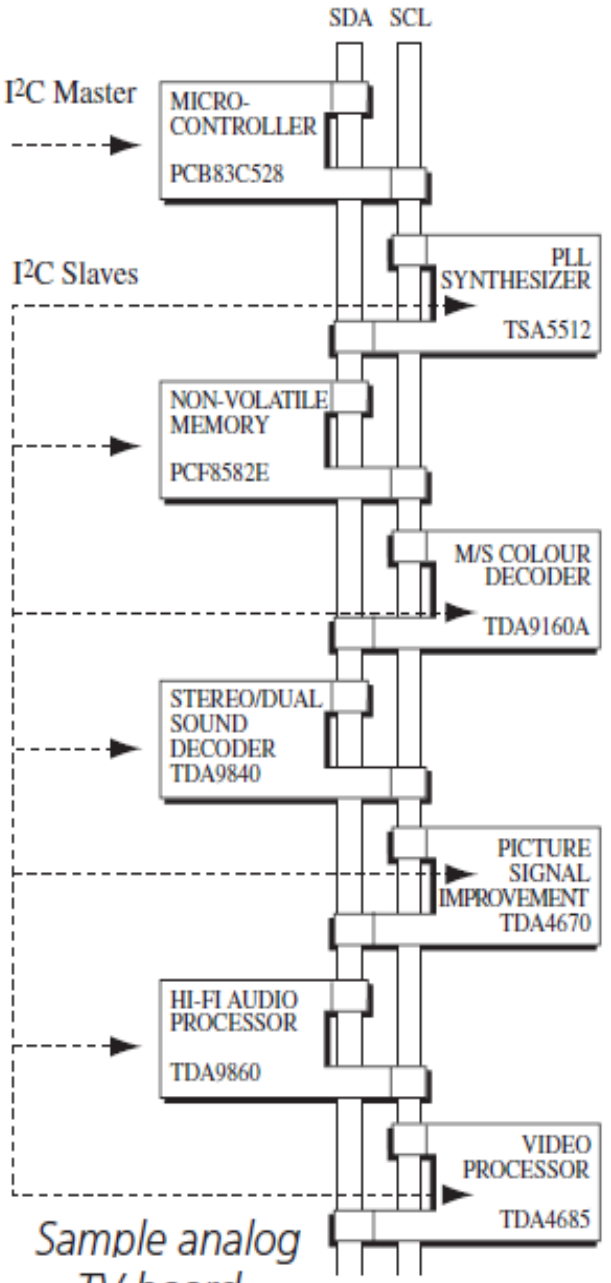
- **Non-expandable bus**
  - Additional component cannot be simply plugged into and communicate to others over that bus.
  - DIB, VME, I2C

PCI Bus

- Peripheral Component Interconnect (PCI)
  - Synchronous bus
    - 33 MHz – 66 MHz
  - Bus width
    - 32 bits – 64 bits.
  - Throughput
    - 132 MB/s (33MHz, 32bits)
    - 528 MB/s (66Mhz, 64 bits)
- Two connection interfaces
  - Internal interface that connects it to the main board via EIDE channel
  - Expansion interface, which consist of the slots.

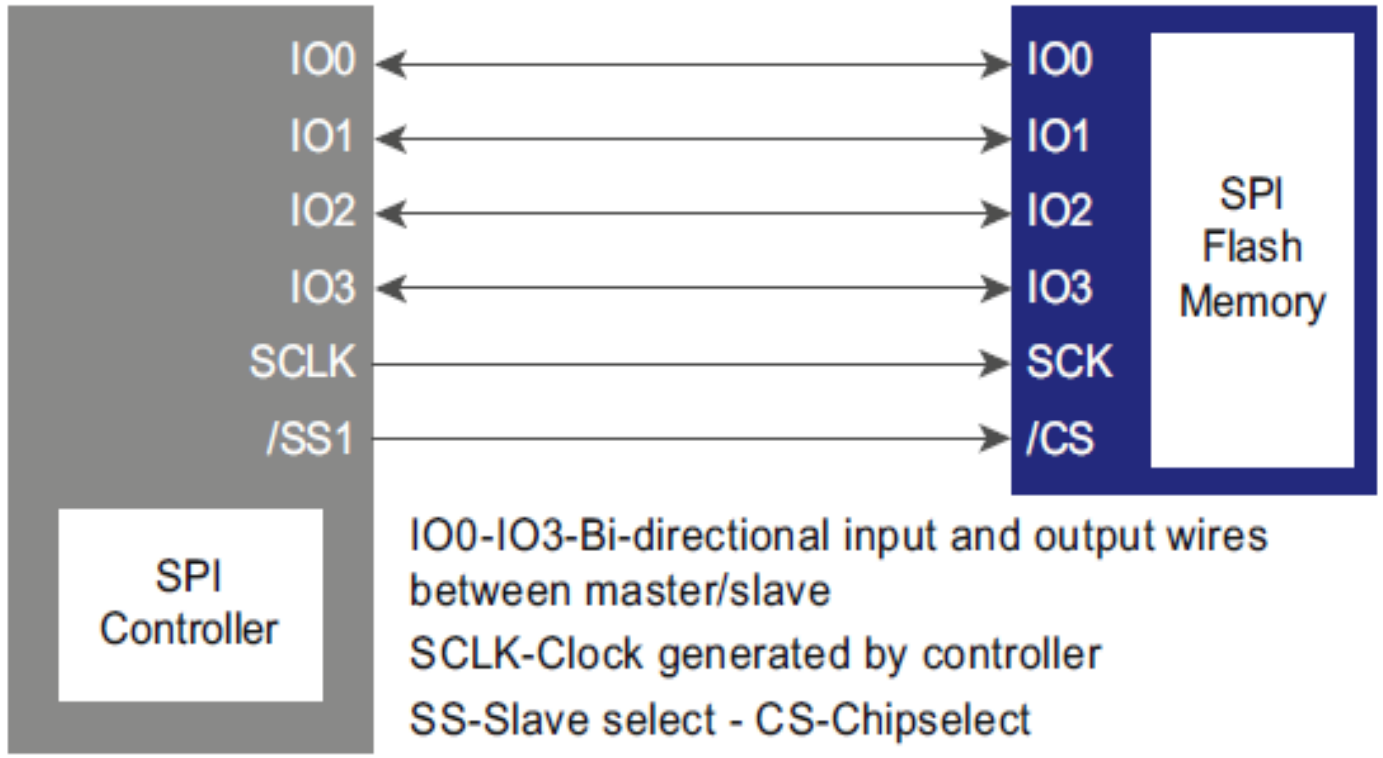
I2C Bus

- 2 wires bus
  - Serial data line (SDA)
  - Serial clock line (SCL)
- Master/Slave relationship
  - Master initiates data transfer
  - Generate clock signals.
- I2C is a serial, 8-bit bus.
  - Only one byte of data is transferred at one time



SPI Bus

- Four-wire bus
  - Serial clock
  - Master output/slave input
  - Master input/slave output
  - Device select.
- Speed up to 80MHz



- Used to connect to serial flash for initial boot code in Intel platforms.

Summary

- QnA

- Further Readings
  - https://www.sciencedirect.com/topics/engineering/embedded-system-architecture