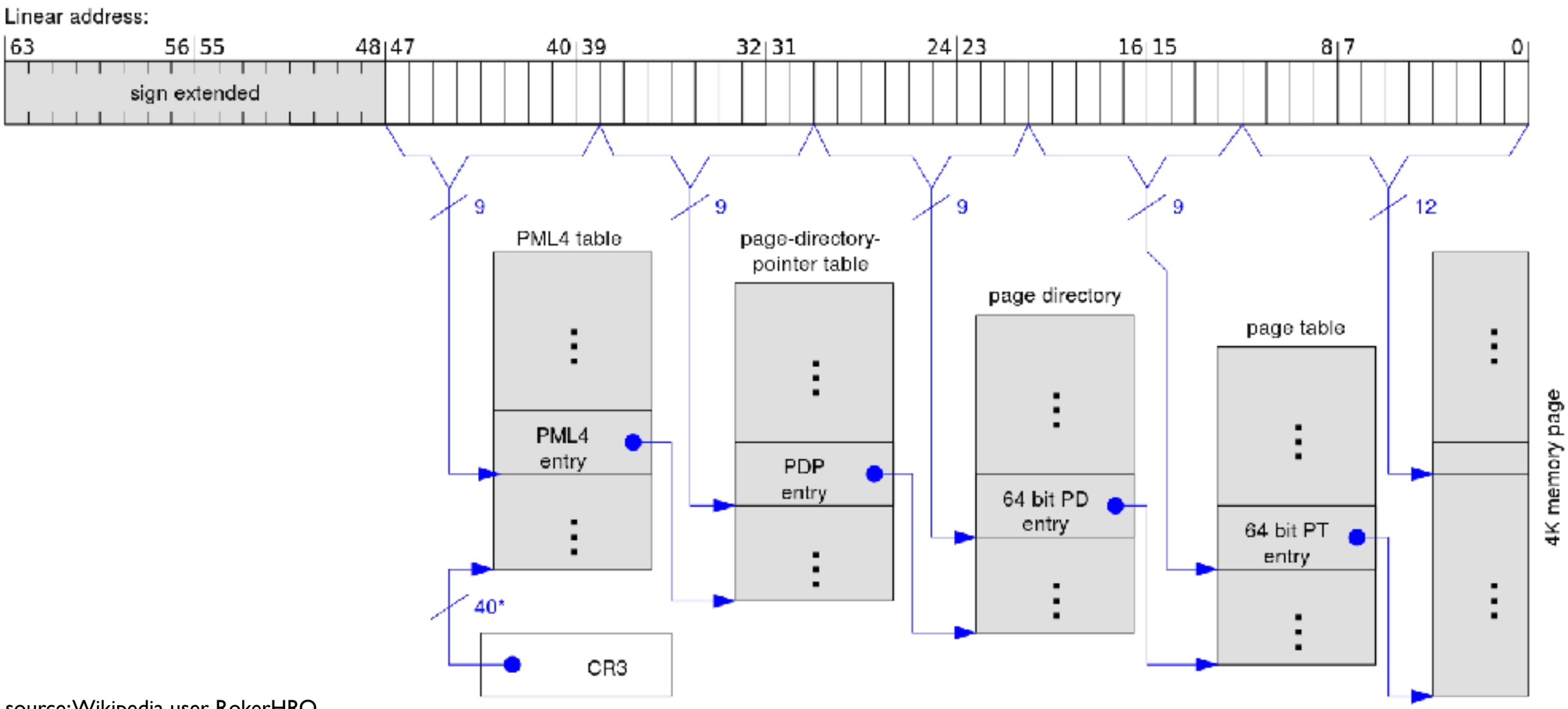
Address Translation

Protection and Performance

Hammurabi Mendes

Fall 18

Superpages



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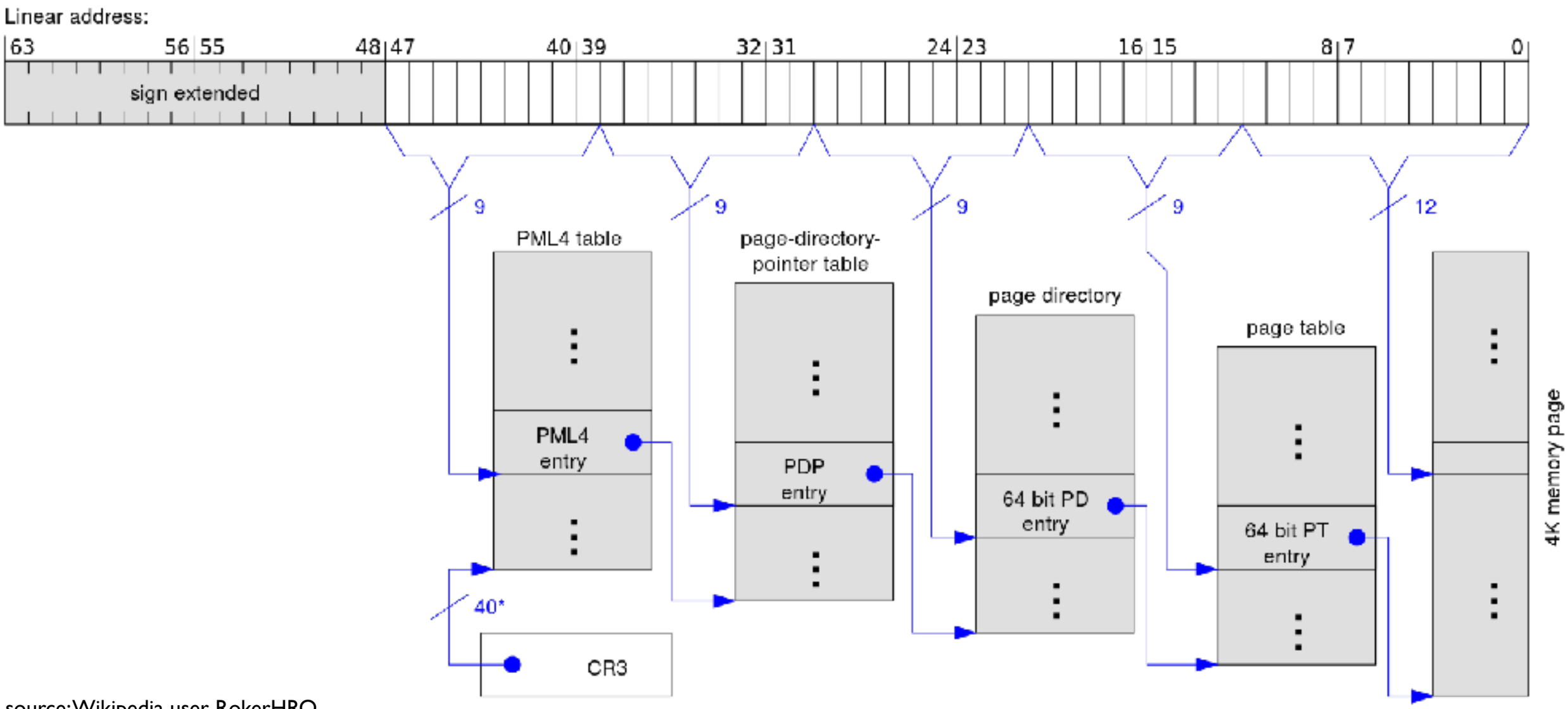
Superpages

Use one entry to map a single 1GB chunk

without allocating the $2^9 \times 2^9$ entries (2^9 tables) underneath



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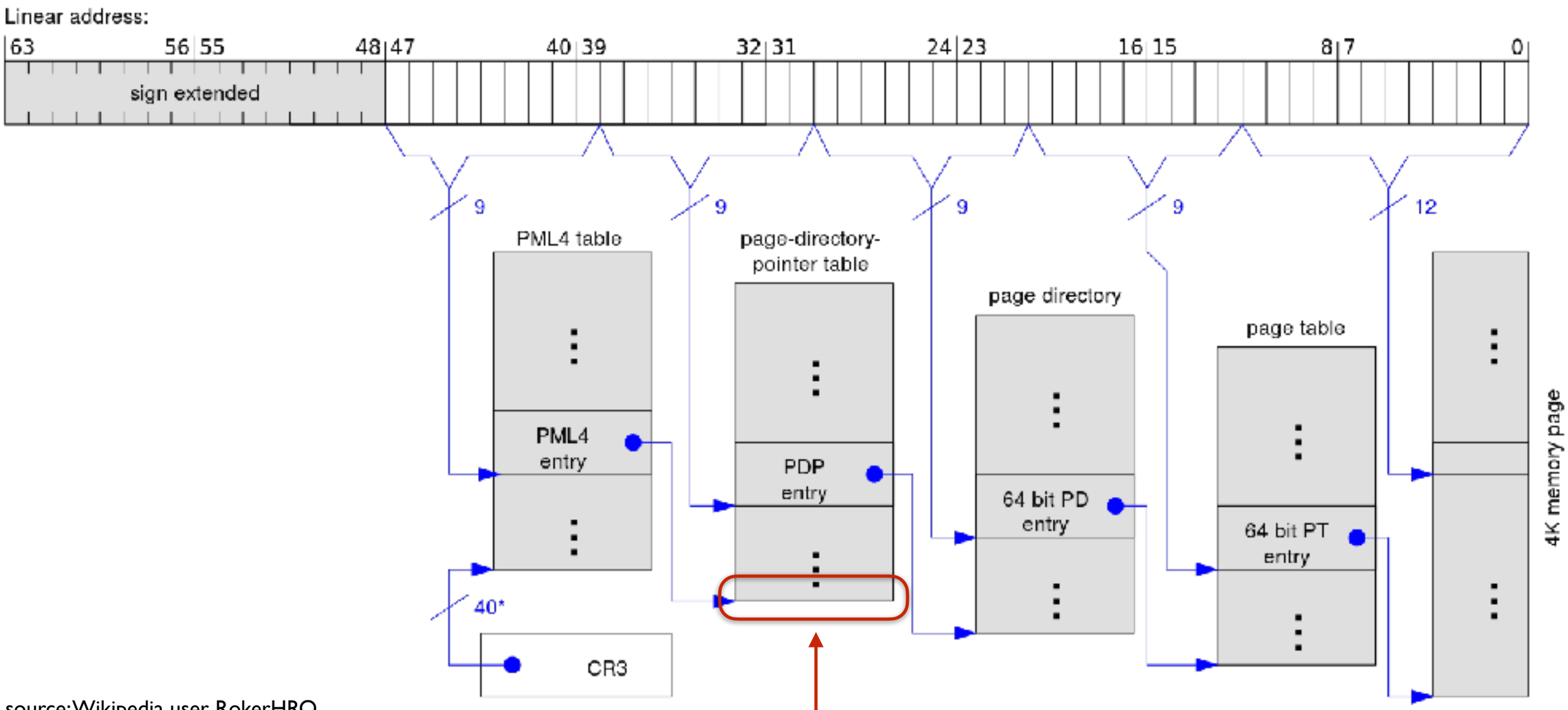

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Entries have flags - set the flag for "superpage"

Need for Speed

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  - Consulting page tables makes memory references cost *3* or *4* times as much (*600 cycles!*)

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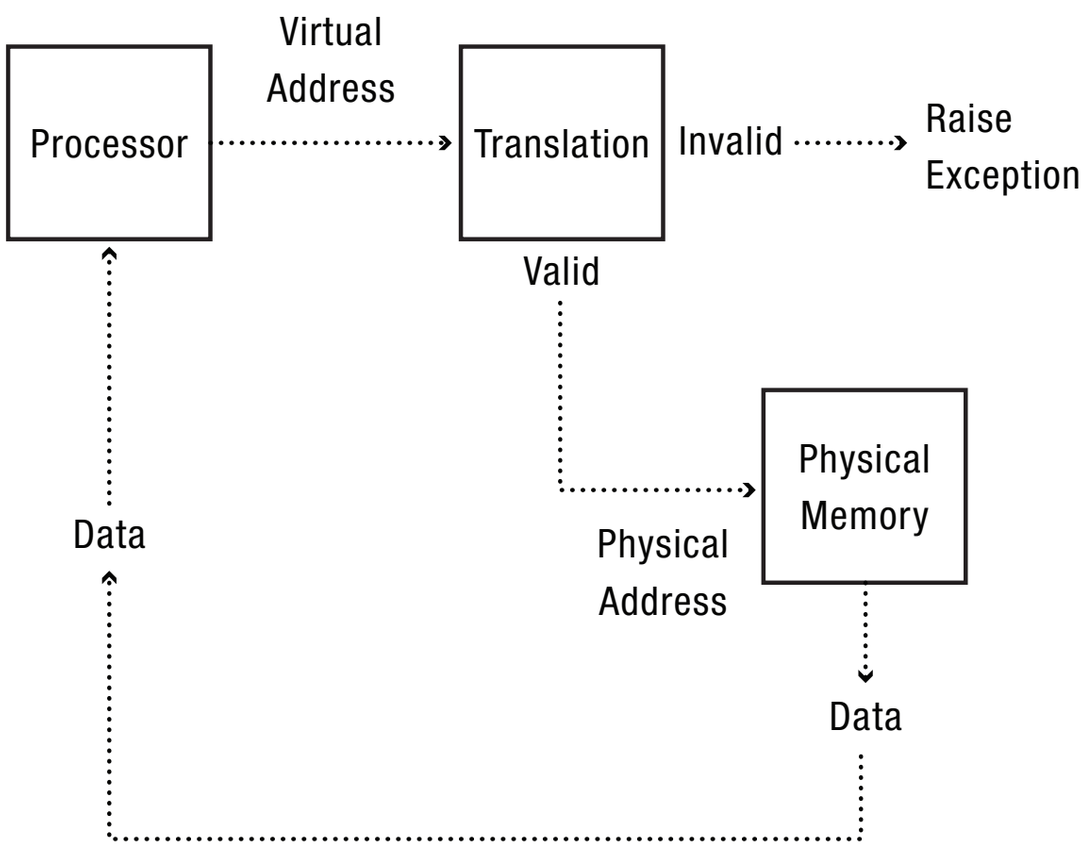
So Far…


Processor
Virtual
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Translation
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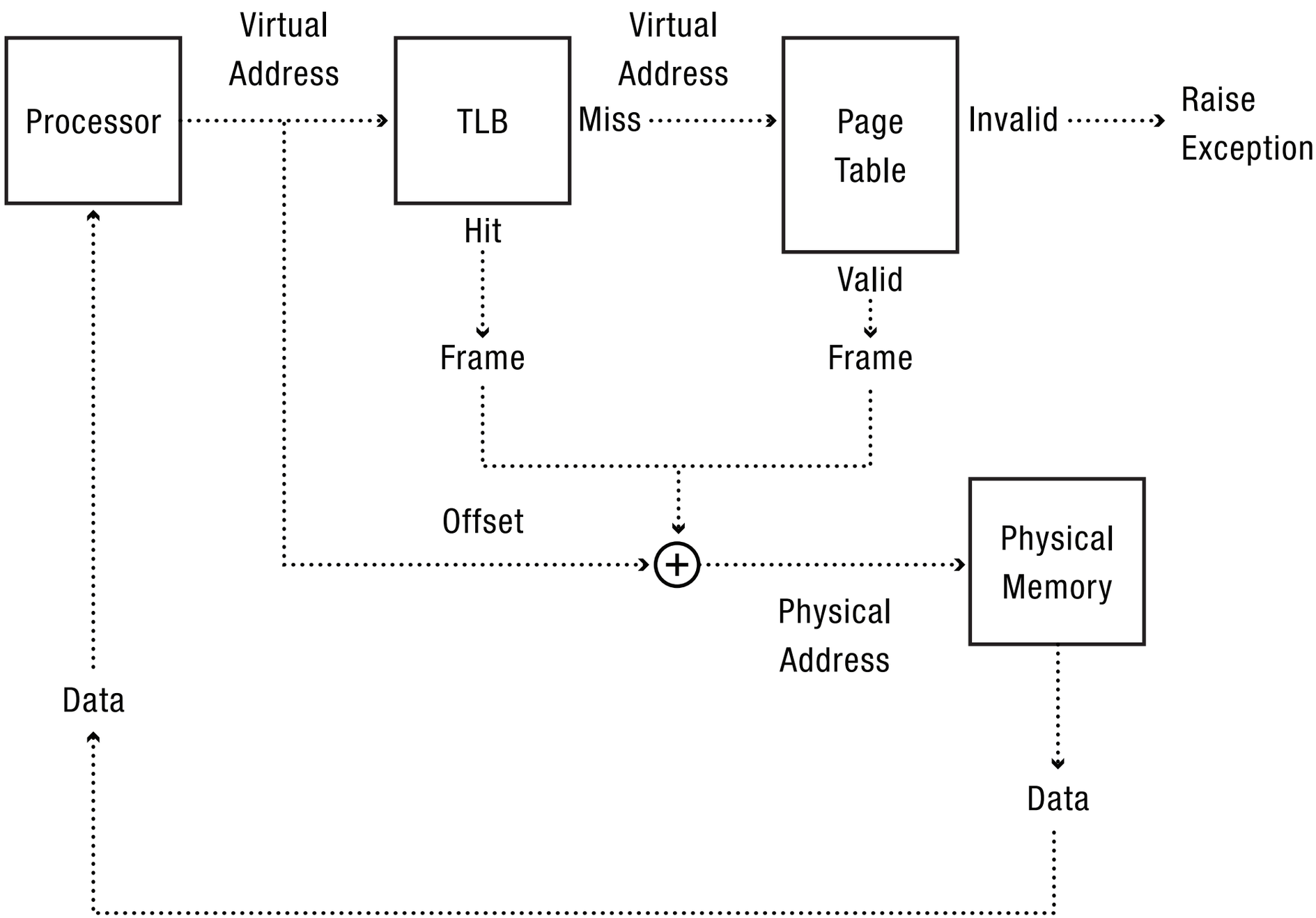
Caching: TLB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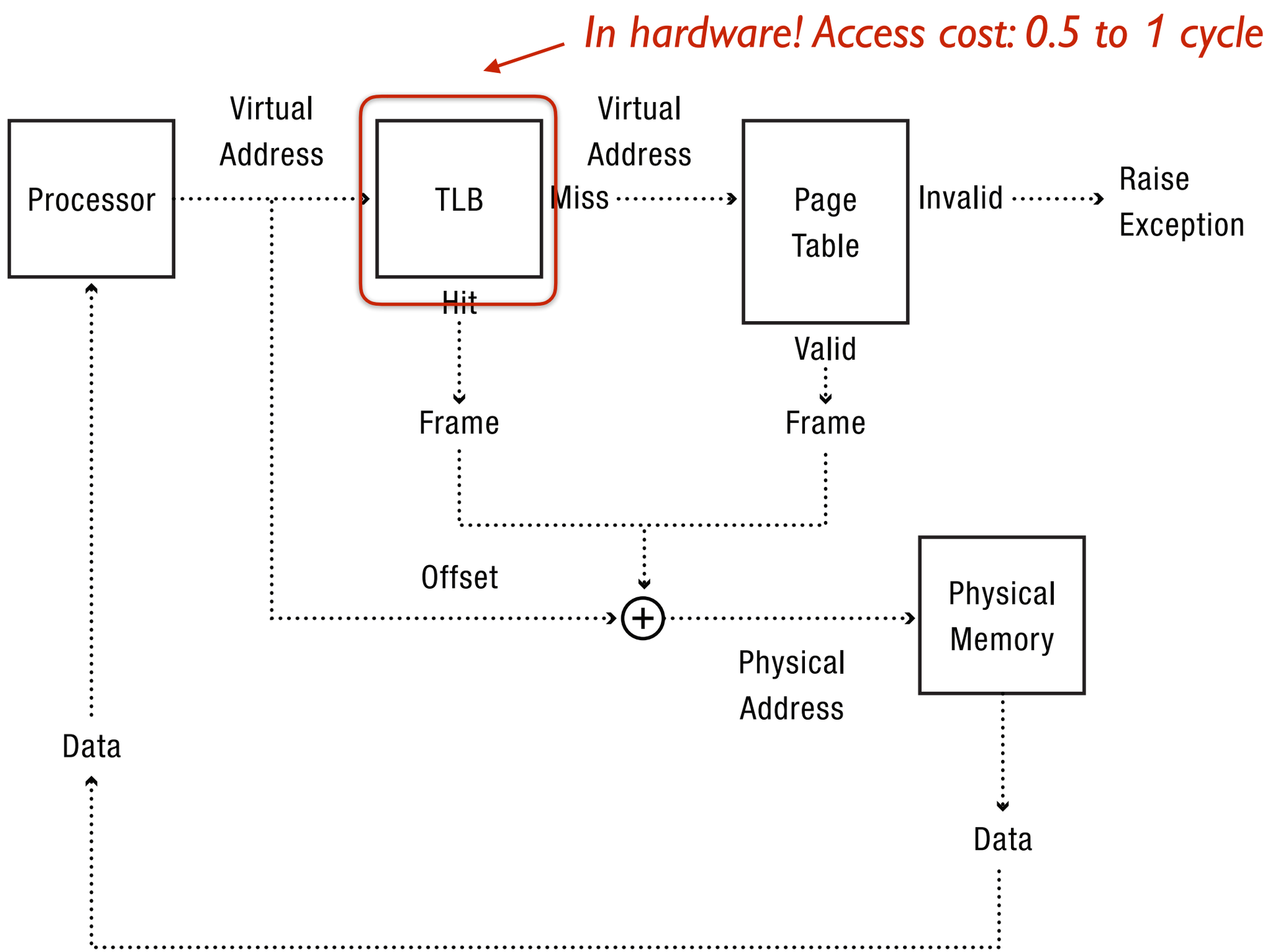
In hardware! Access cost: 0.5 to 1 cycle
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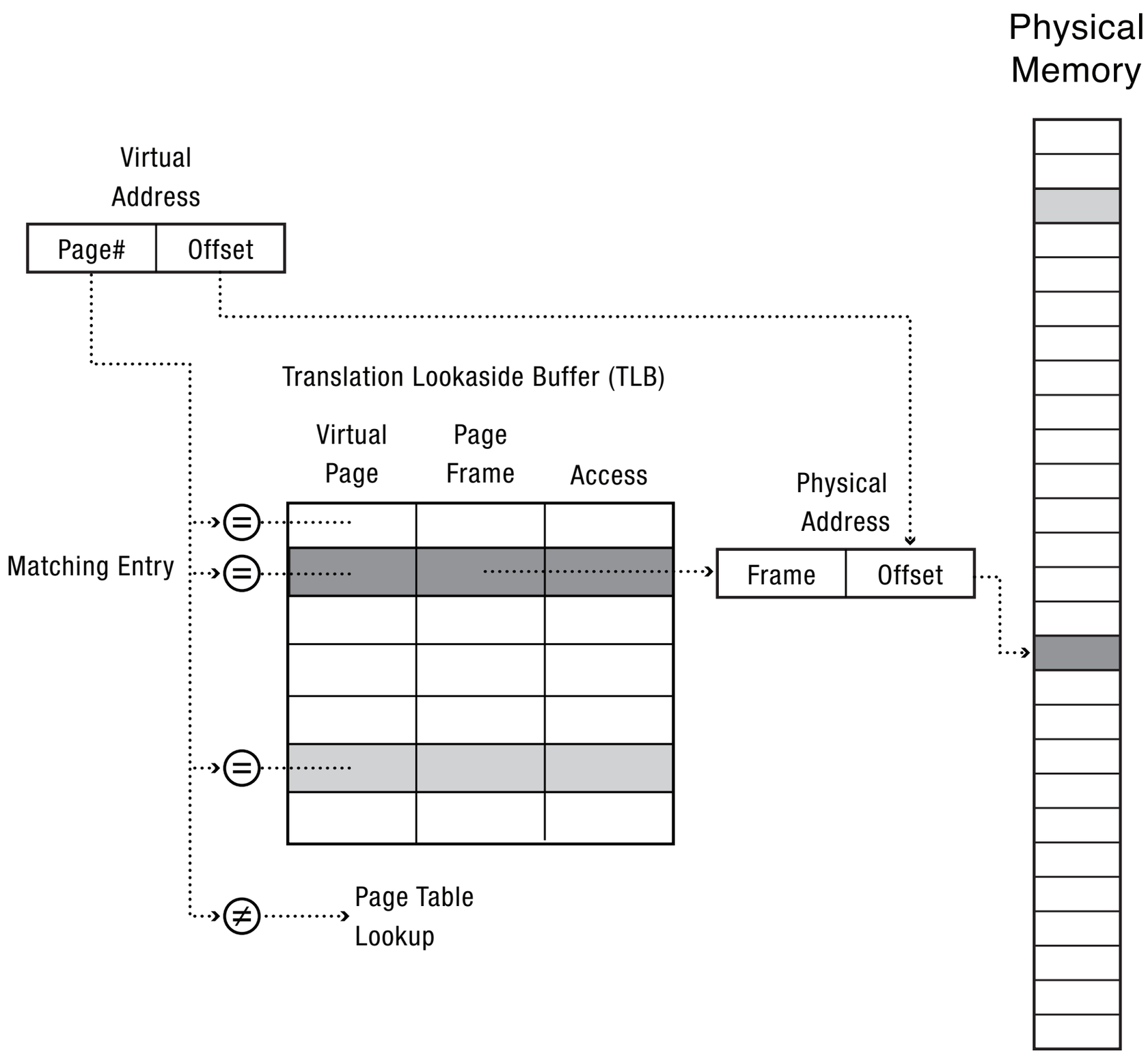

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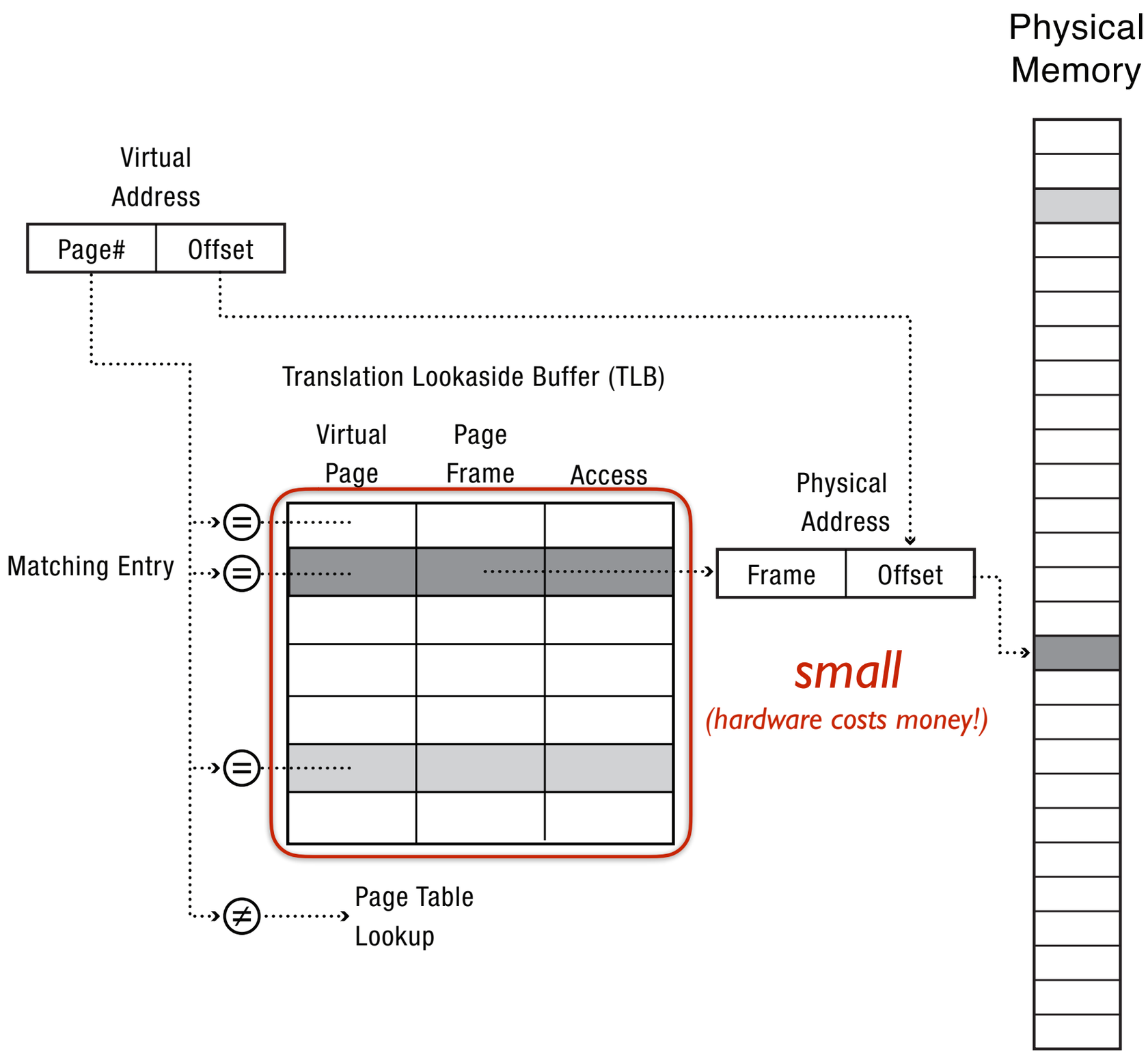

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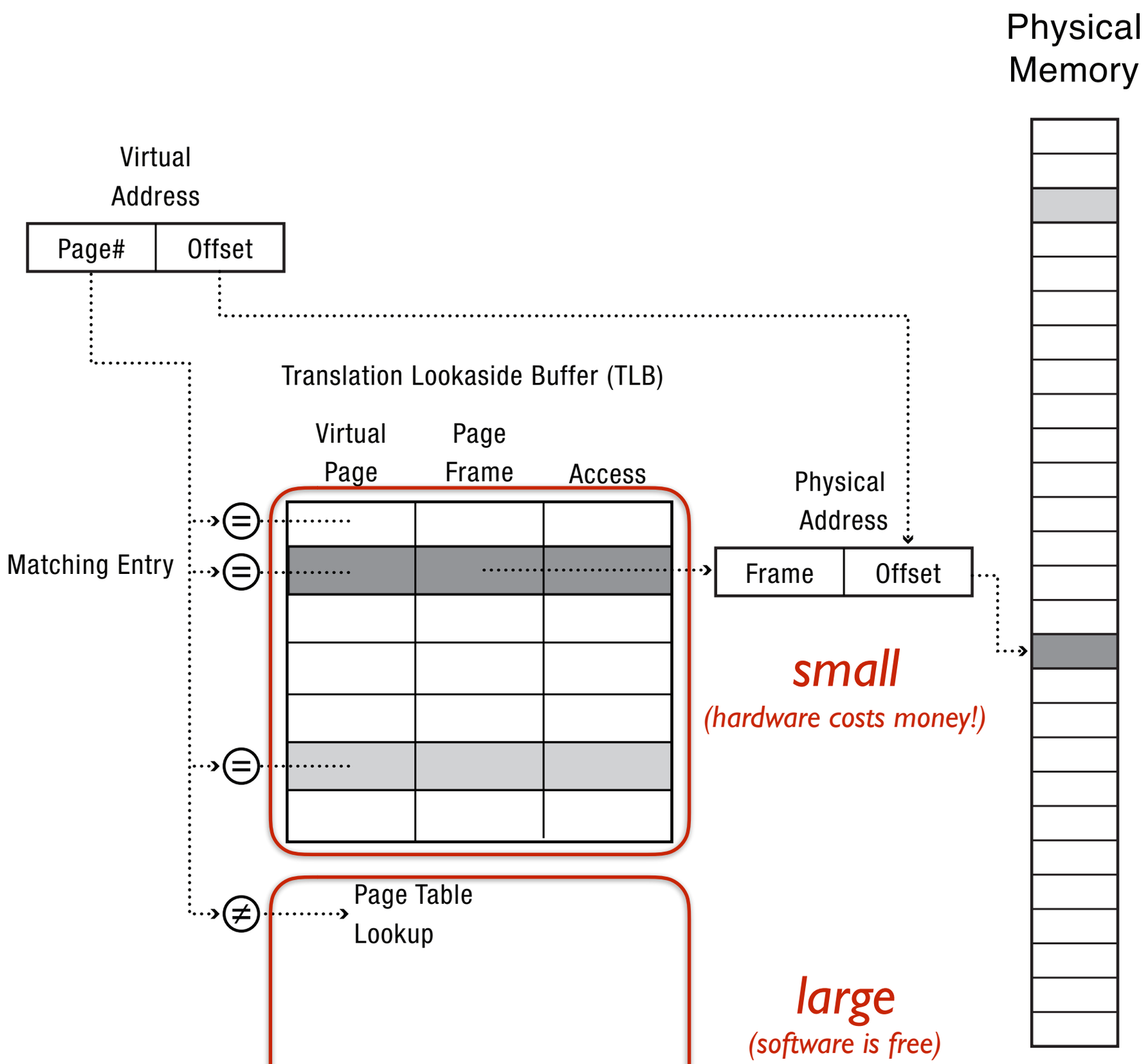

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  - *Replacement policy*
  - LRU — least recently used (note the practical implementation considerations)

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- **Tricky Q**: How does hardware enforces LRU?
  - It doesn't. Usually hardware implements NRU
  - *Not recently used:* set a timestamp for each entry and retire old entries

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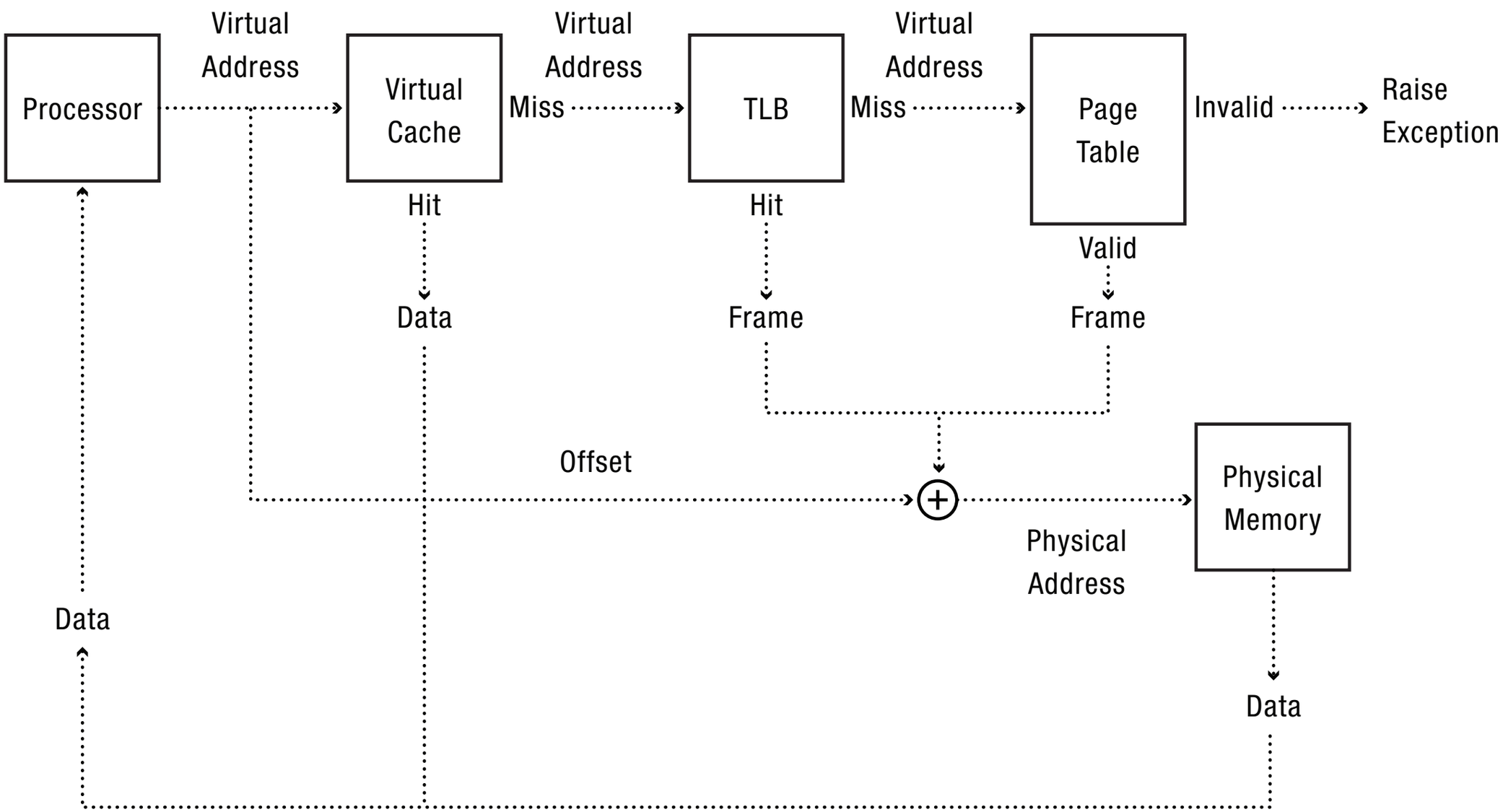
    - Injury: it's slow
    - Insult: the more the #CPUs, the worse the problem

Virtually-Addressed Caches



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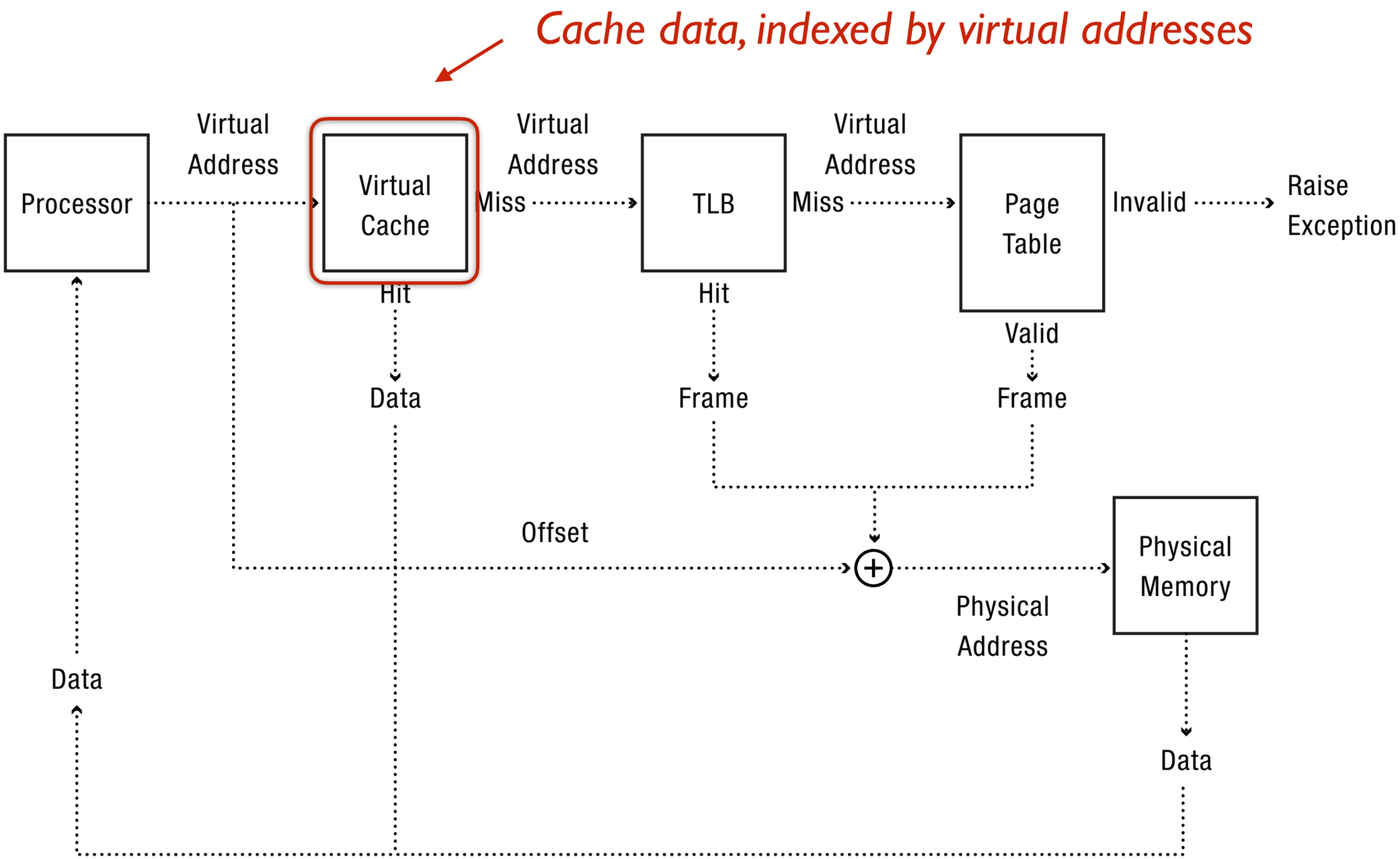

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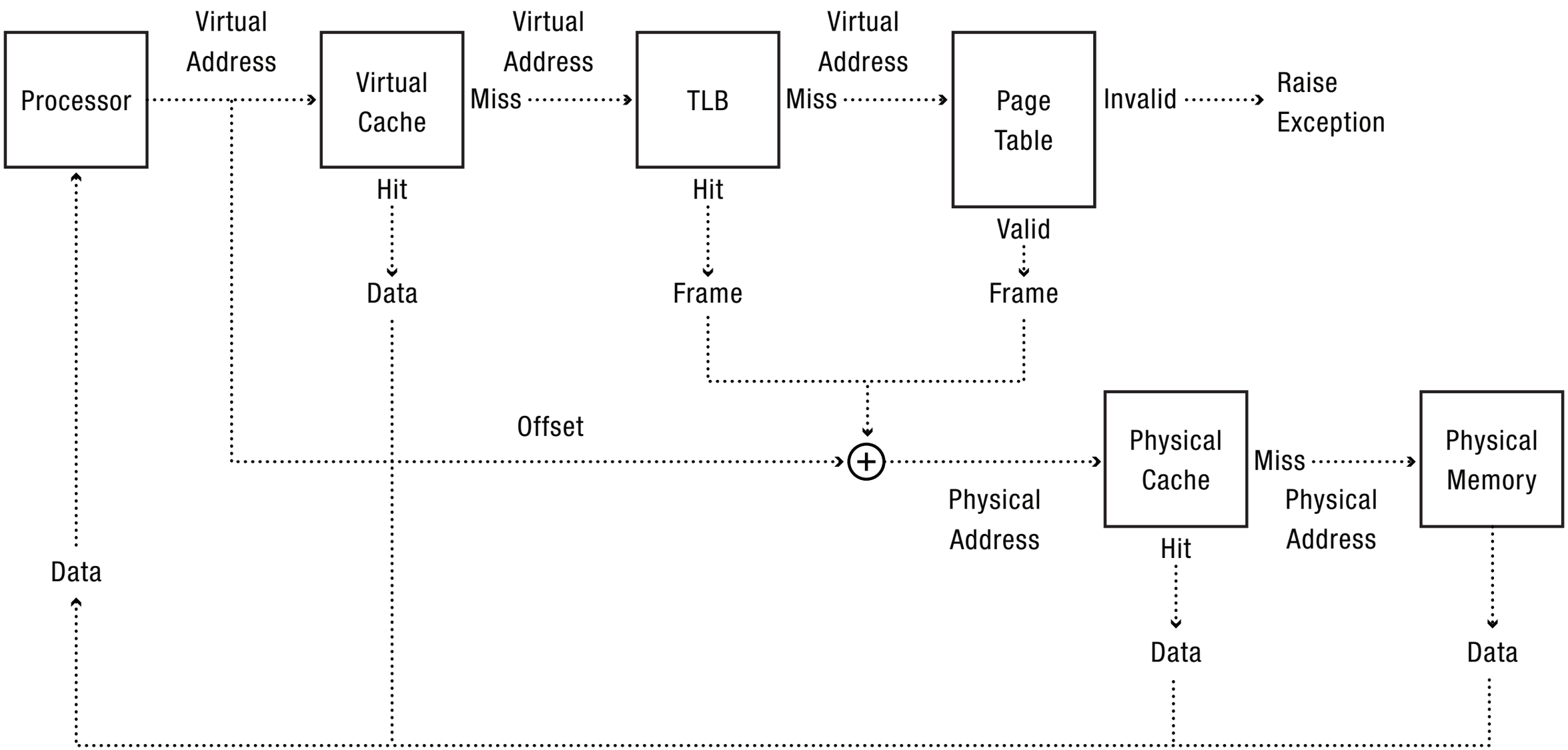
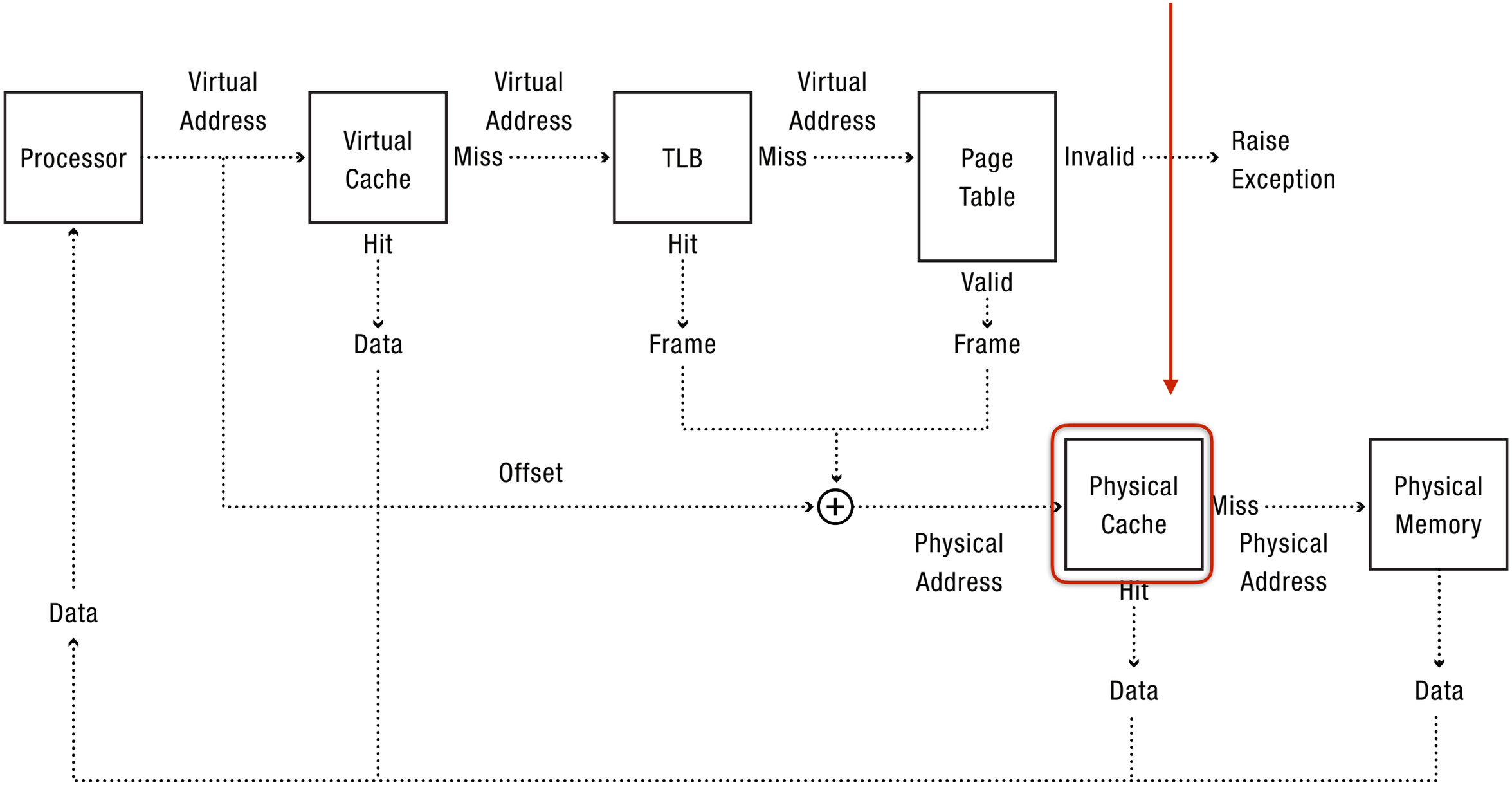


Physically-Addressed Caches

Trick: pin the most used page tables here!
Translation done on-chip even with TLB misses!



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They are *incredibly* efficient

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- With a TLB hit ratio of 98% (typical):
  - $(65+1)$ x $0.98 + (4*65 + 1)$ x $0.02 = 69.9\text{ns}$

Fim

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