DAVIDSON

Address Translation
Introduction

Hammurabi Mendes
Fall 18

Paging

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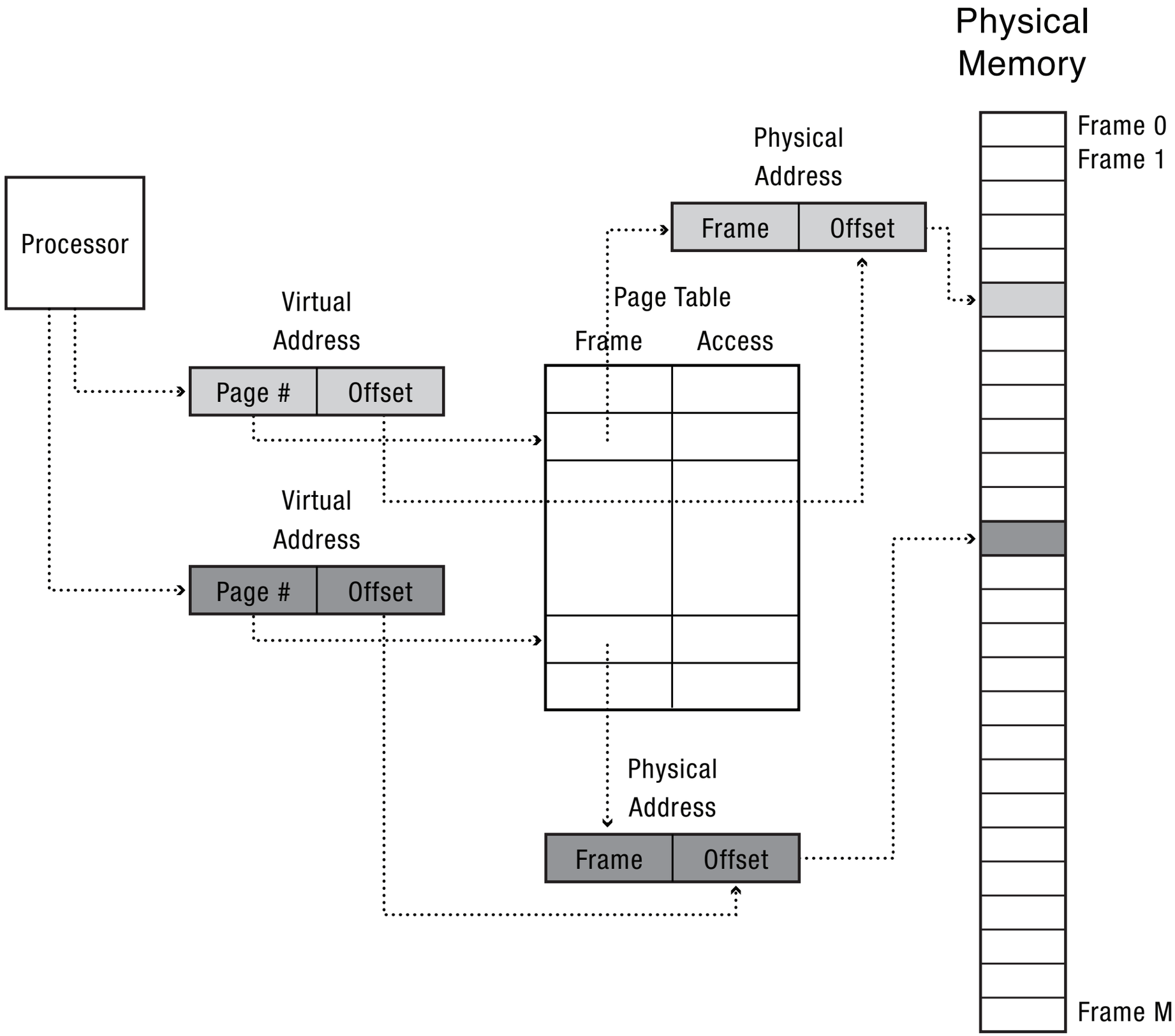
  - This prevents external fragmentation!

Paging


Physical
Memory
Frame 0
Frame 1
Frame M
Processor
Virtual
Address
Page #
Offset
Page Table
Frame
Access
Physical
Address
Frame
Offset
Virtual
Address
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Physical
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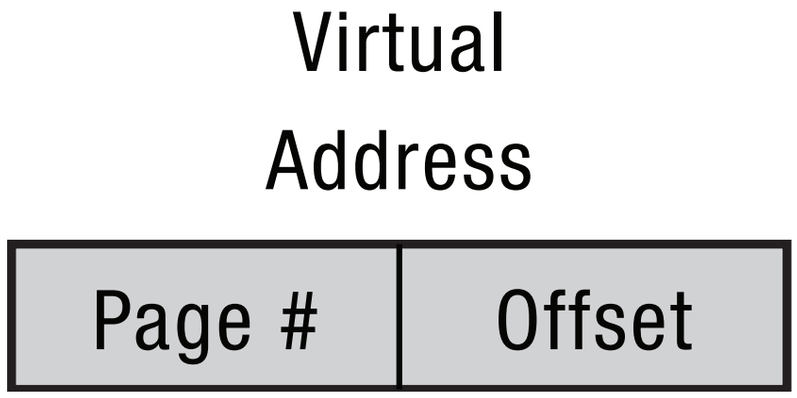
x86-64 gives you a 48-bit virtual address space:



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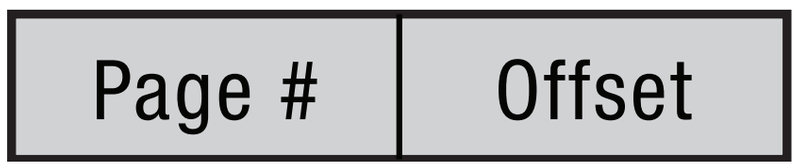

12 bits

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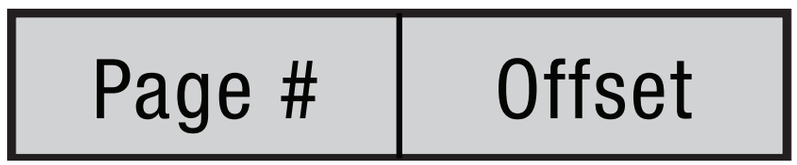

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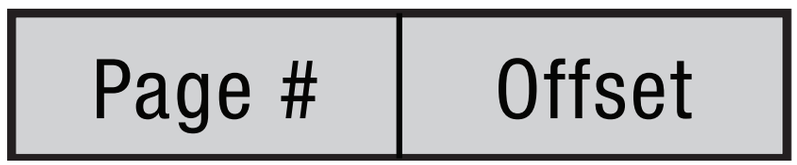

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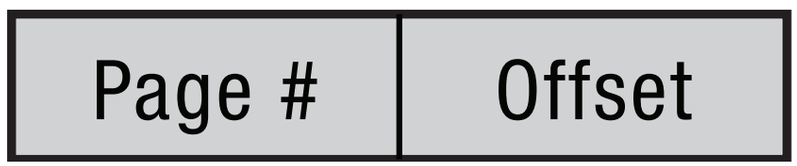

Page size:
2^{12} = 4096 B

Maximum process image:
2^{48} = 281474976710655 B = 256 TB

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  - Out of memory? Store unused pages in the disk!

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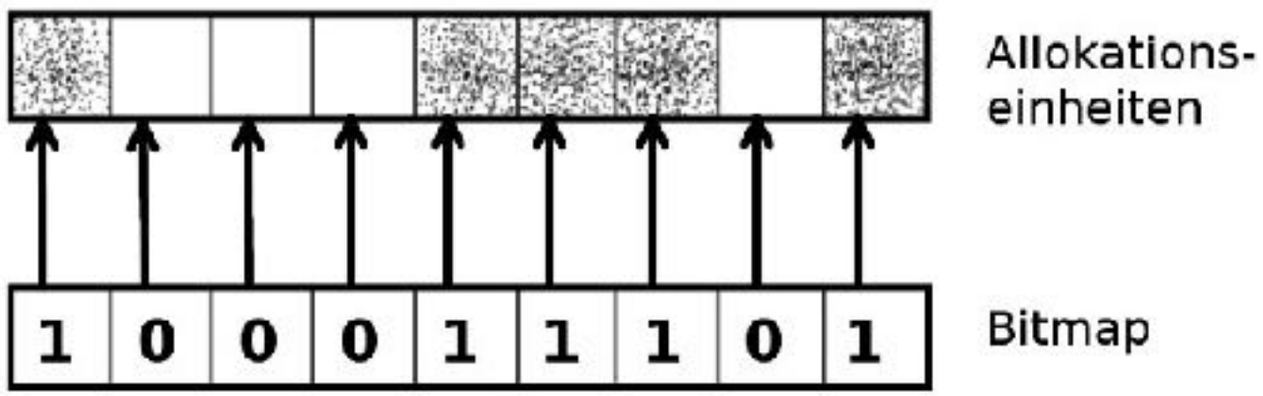

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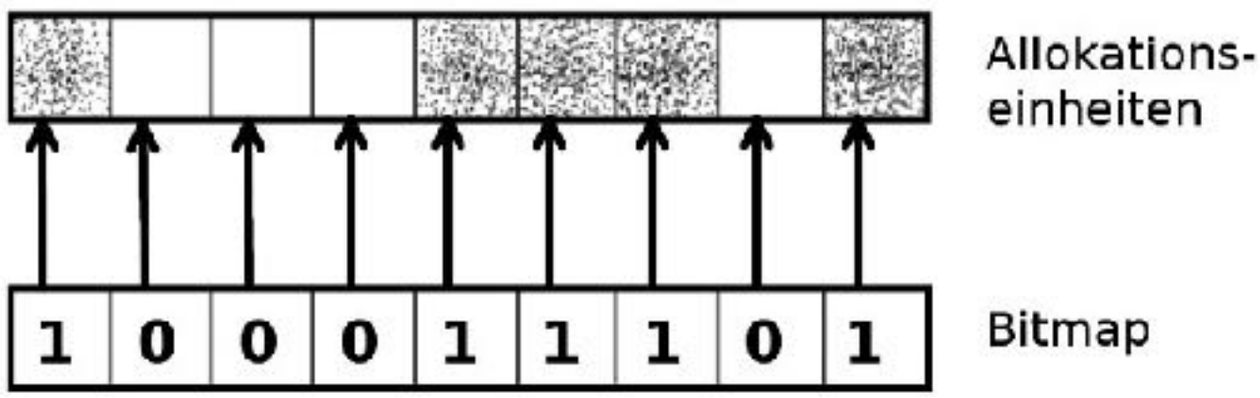

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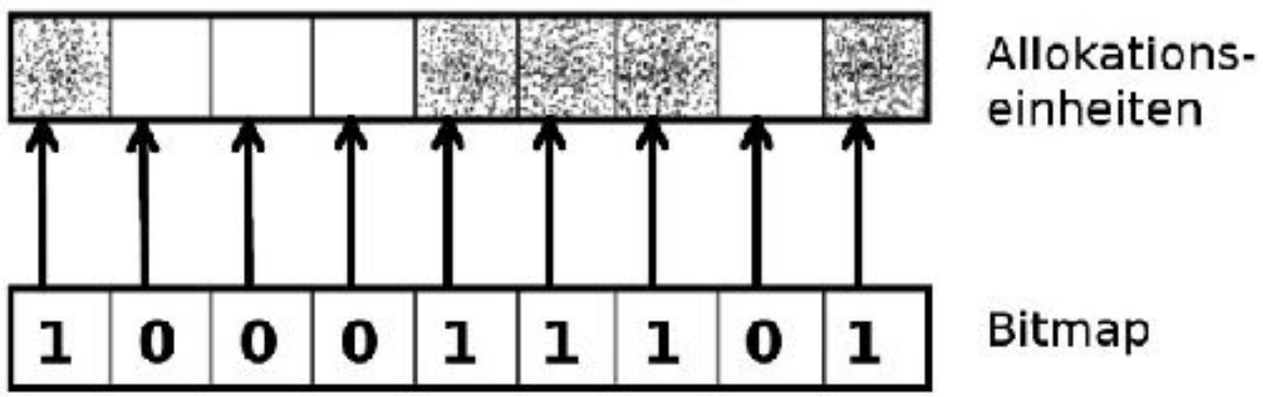

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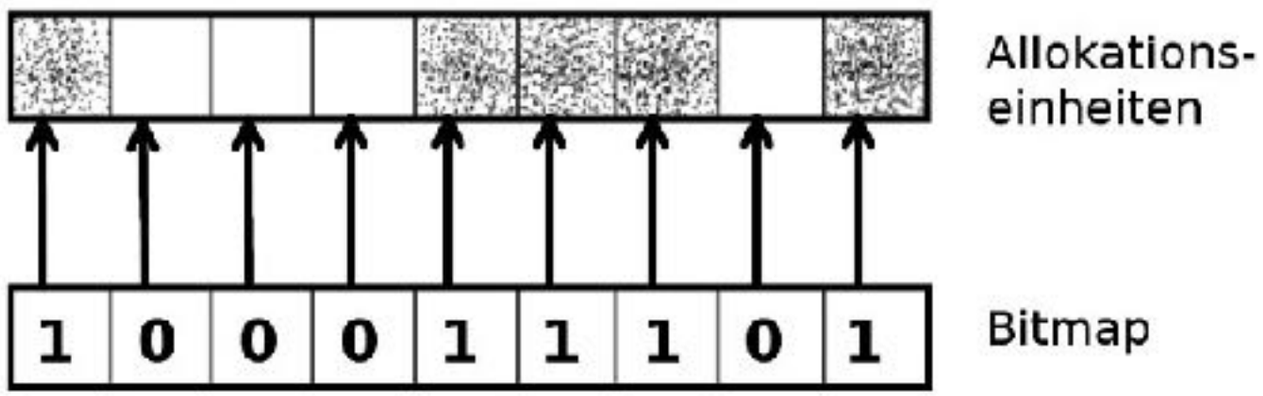

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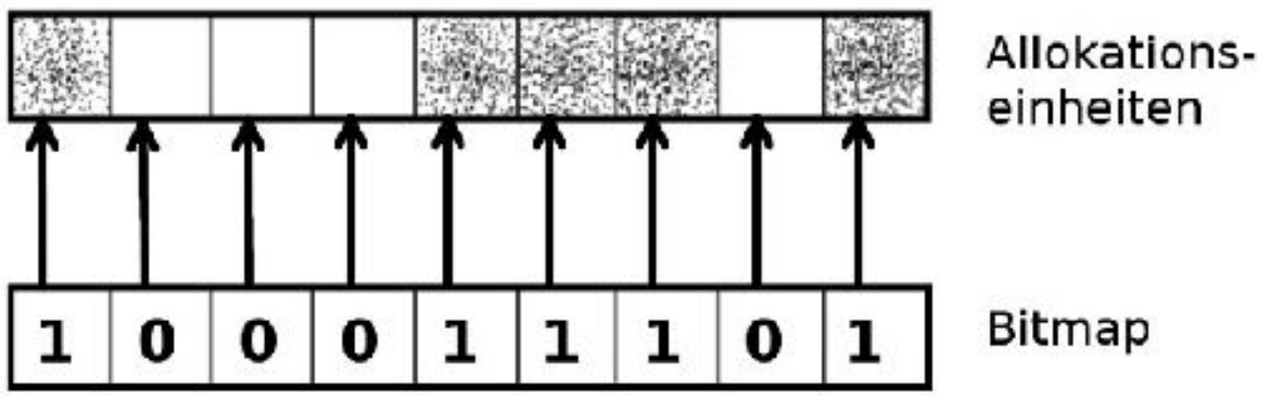

Of course

we will use better data structures
to tackle both problems

Multilevel Paging

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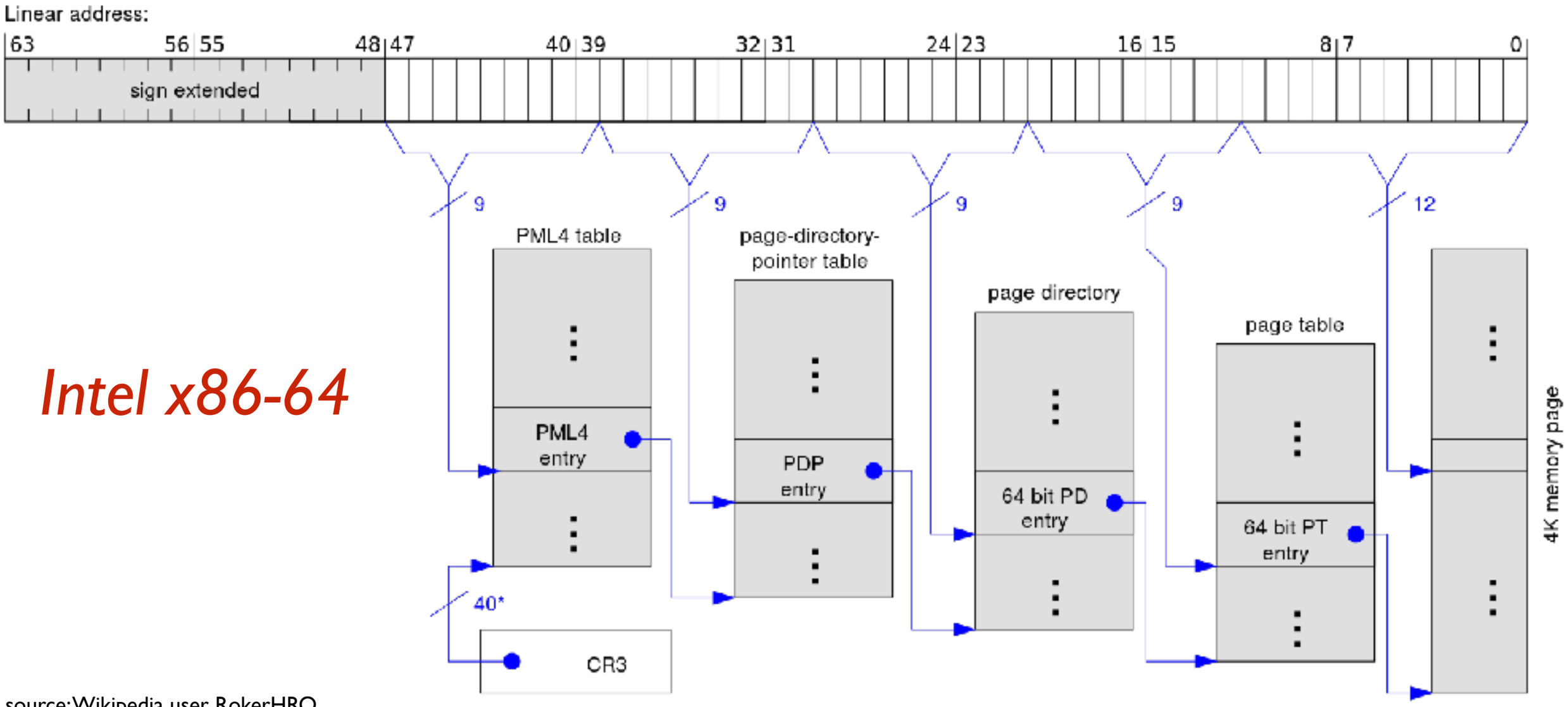

* source: Wikipedia user RokerHRO

Multilevel Paging

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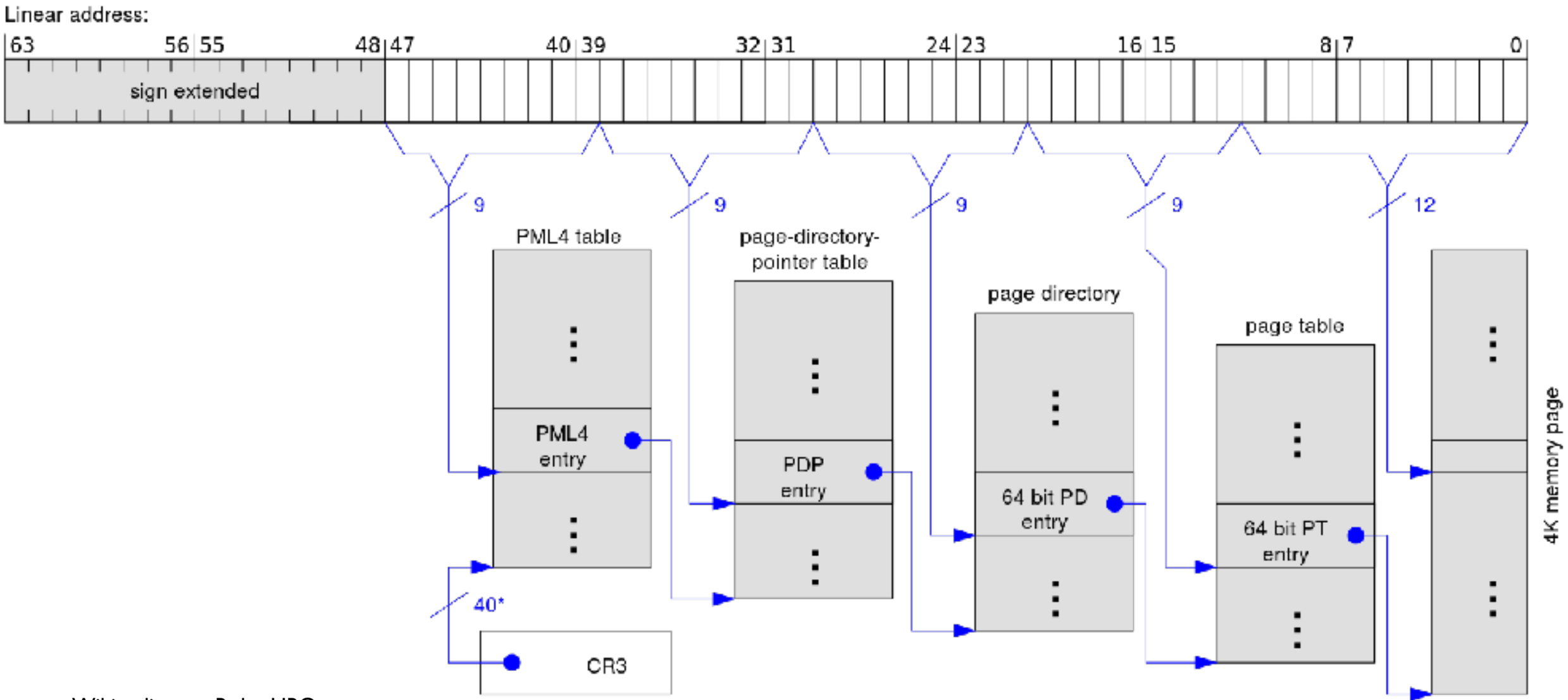

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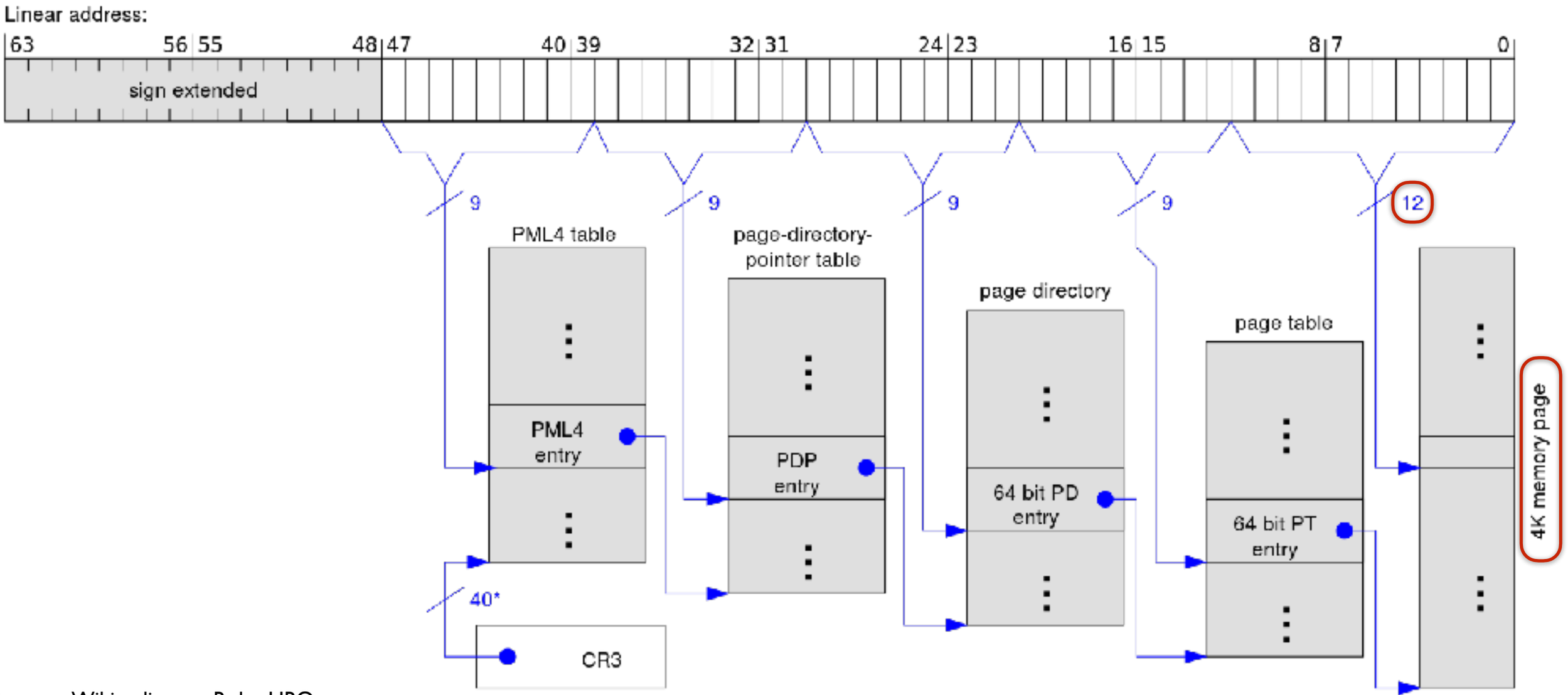

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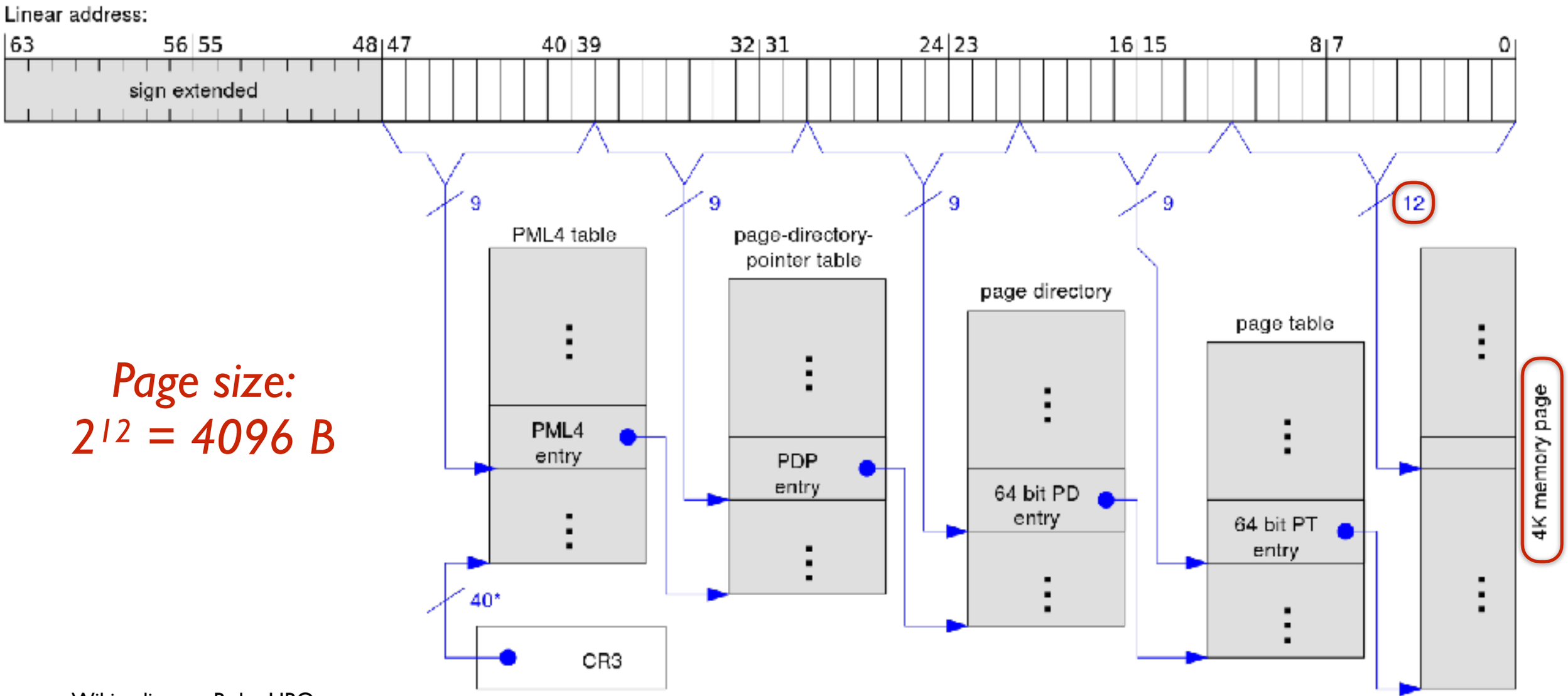

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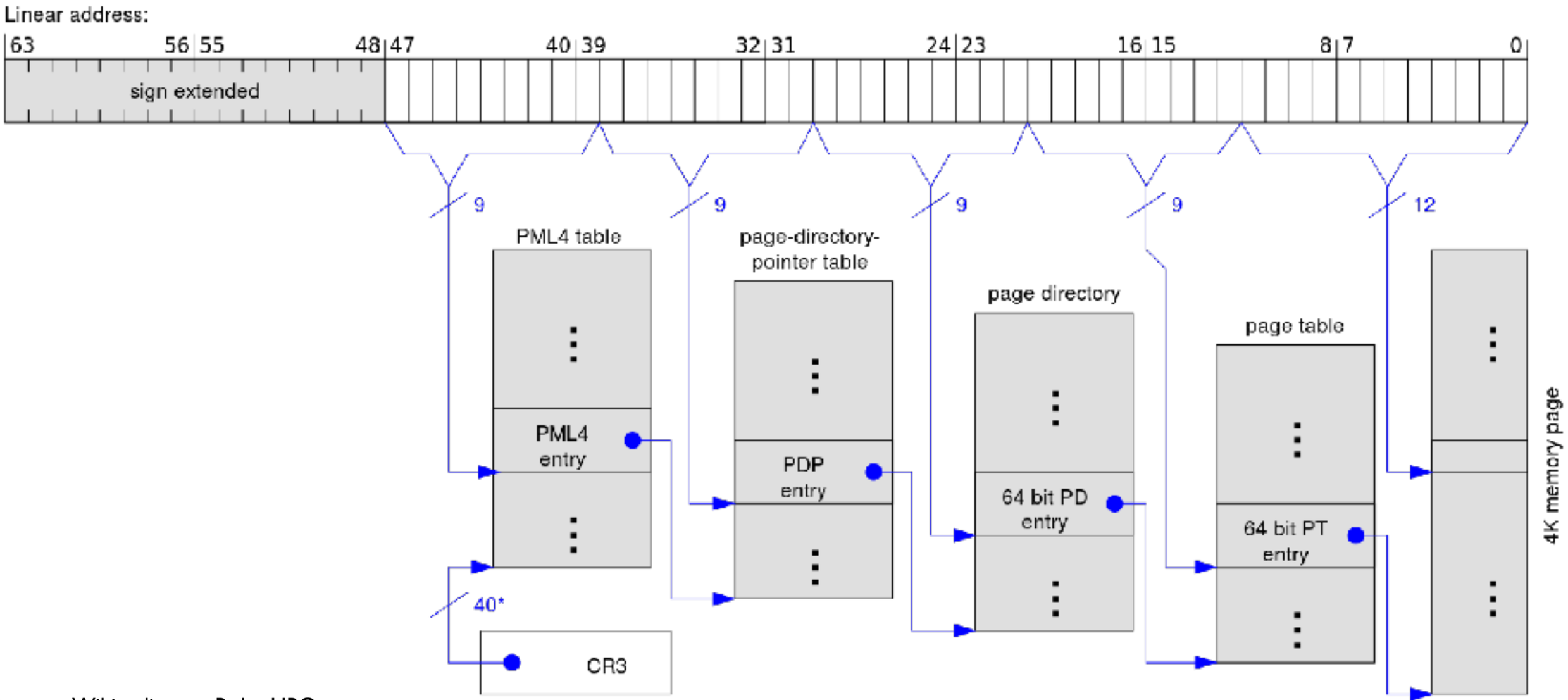

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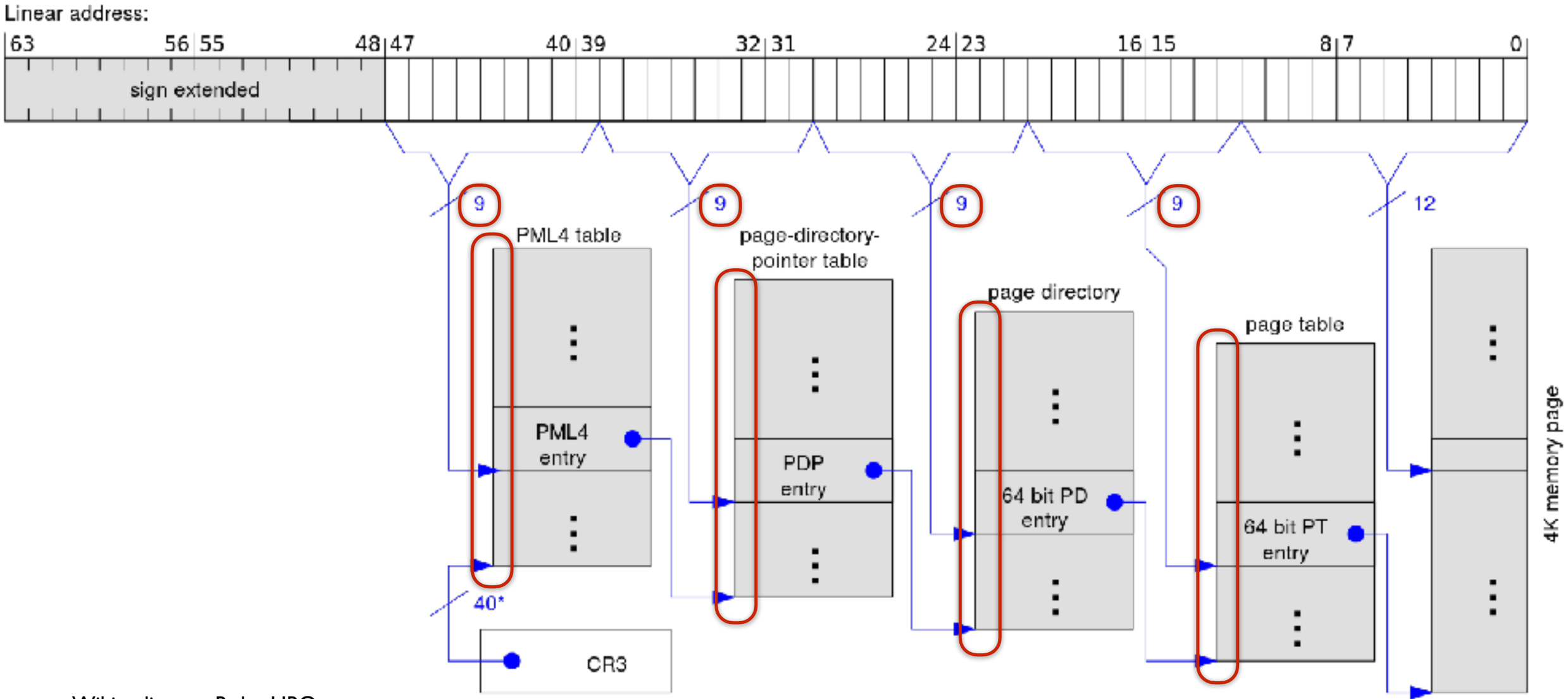

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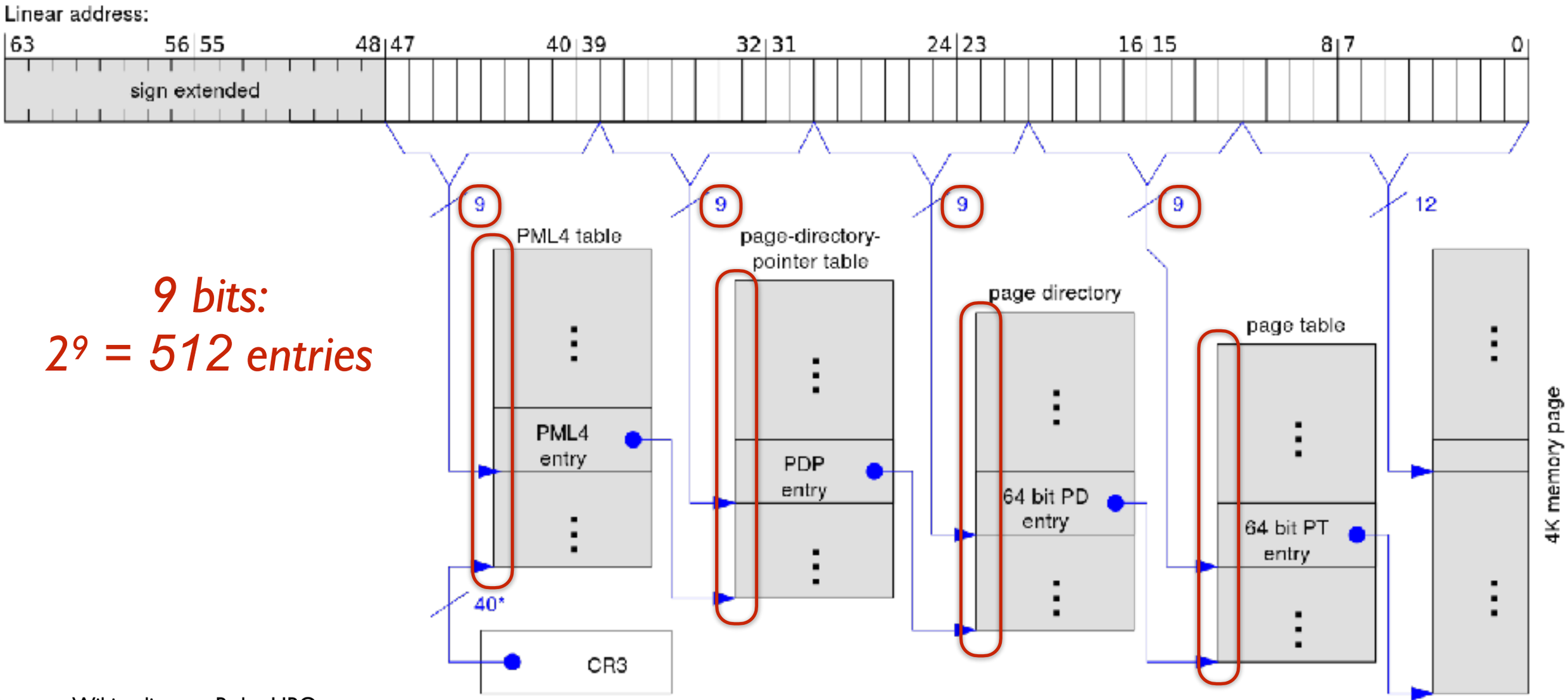

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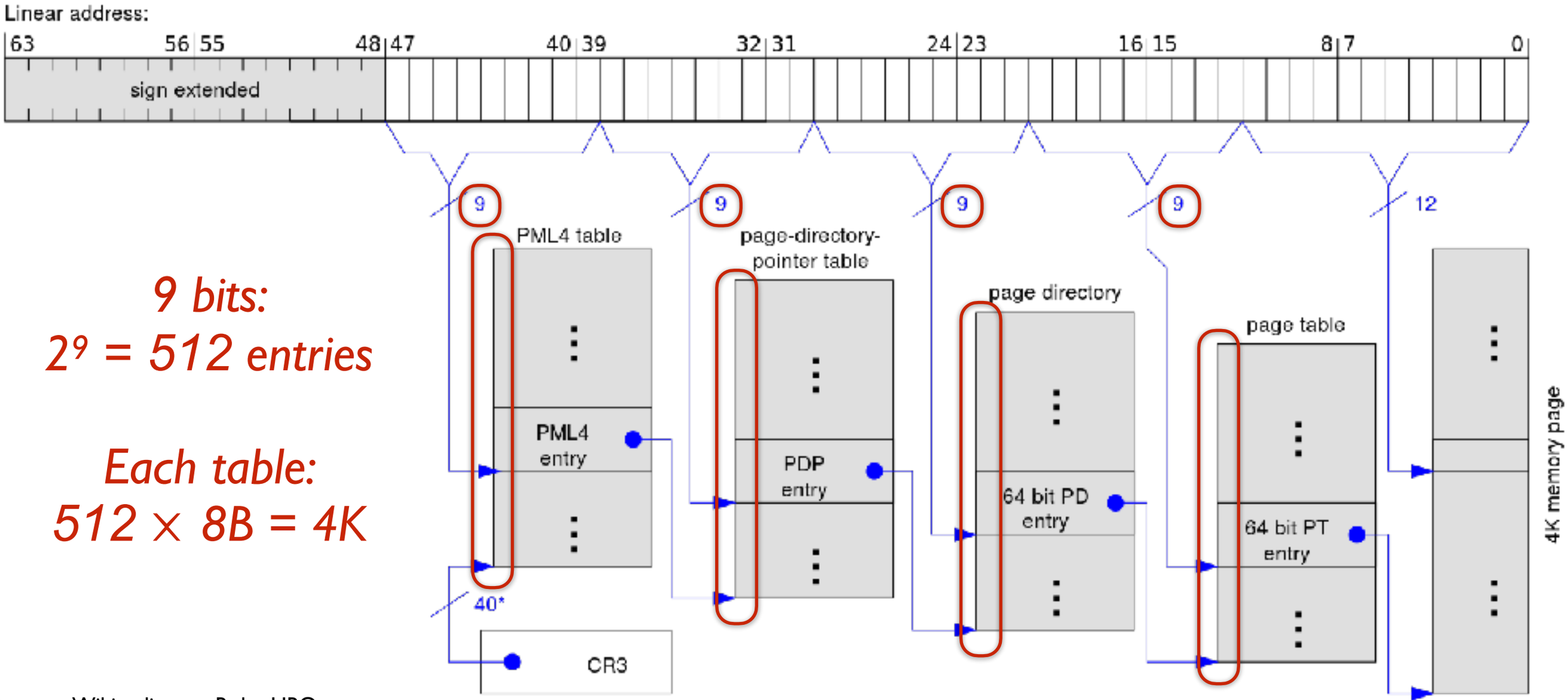

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Each table:
512 × 8B = 4K

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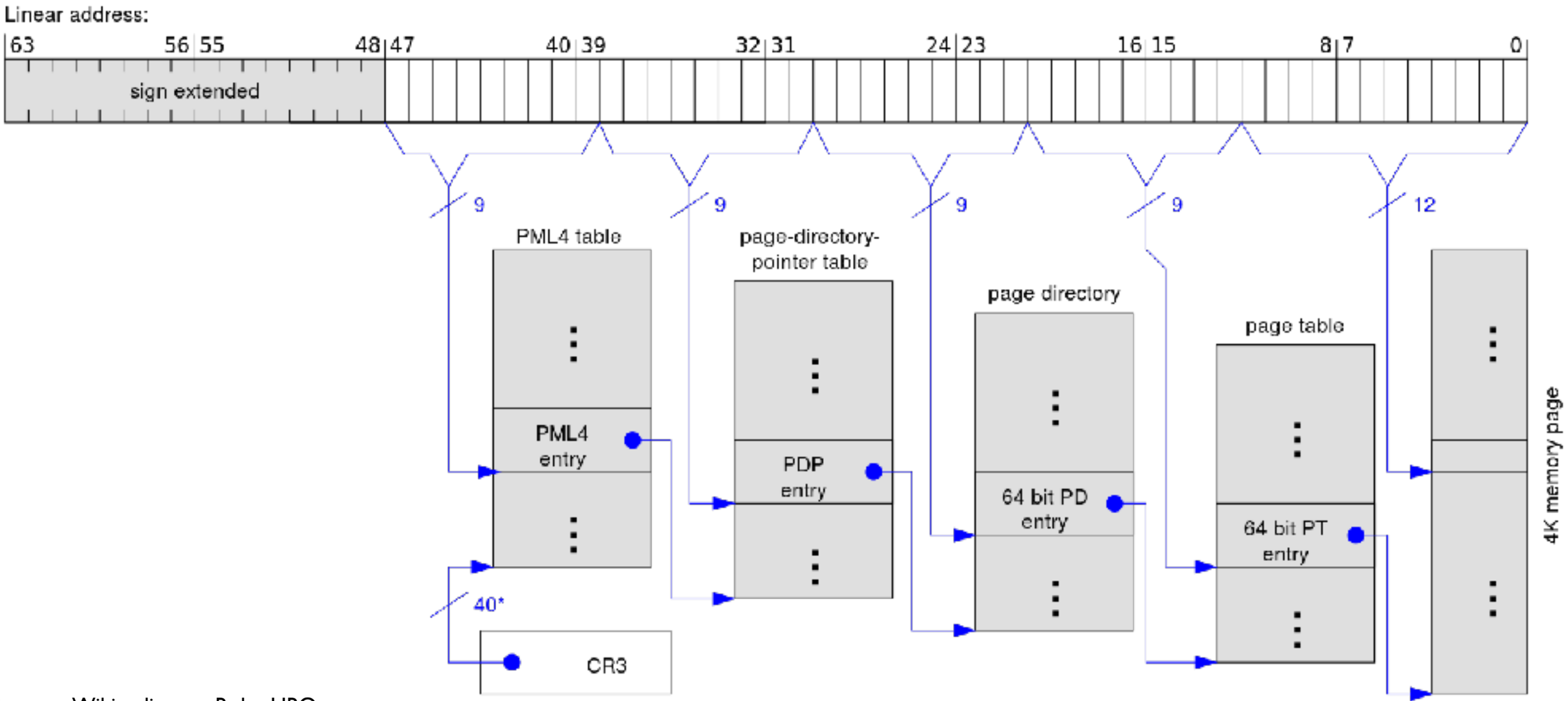

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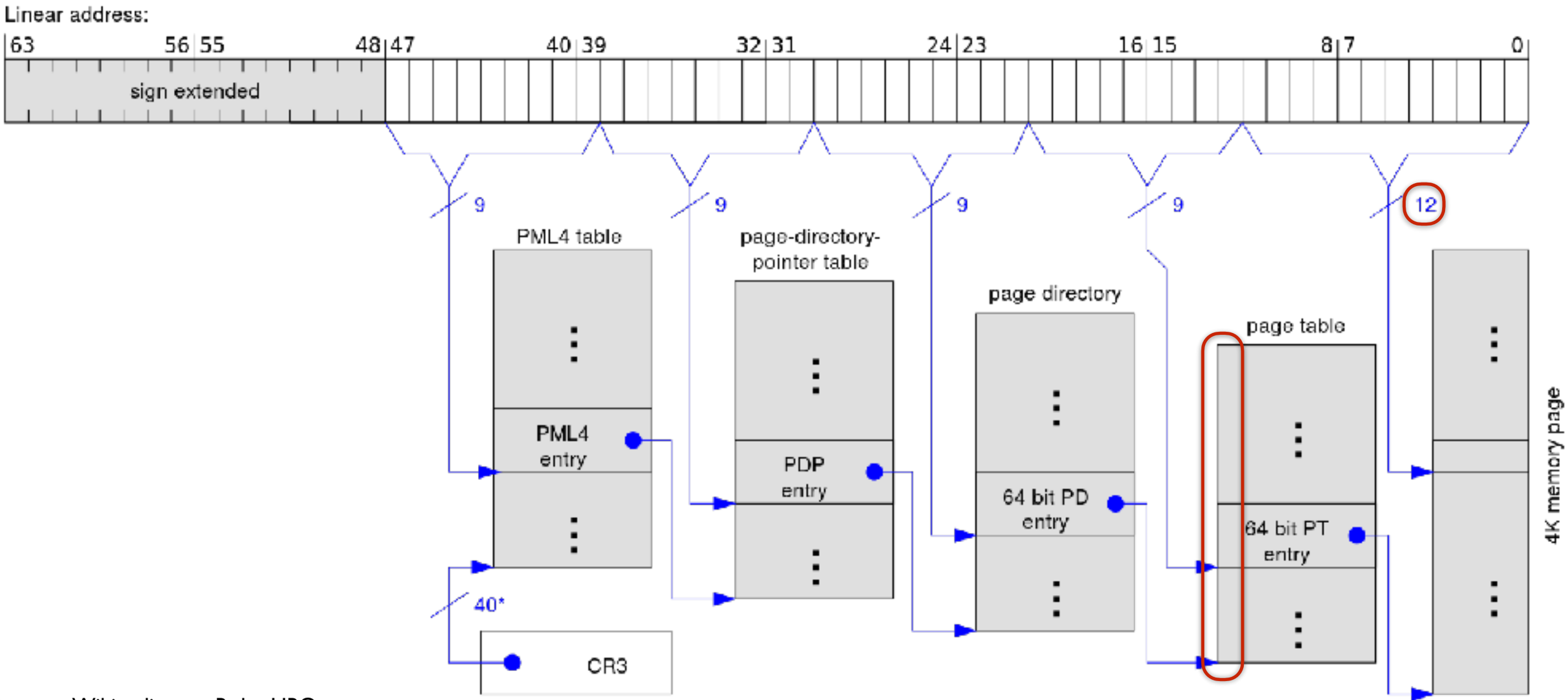

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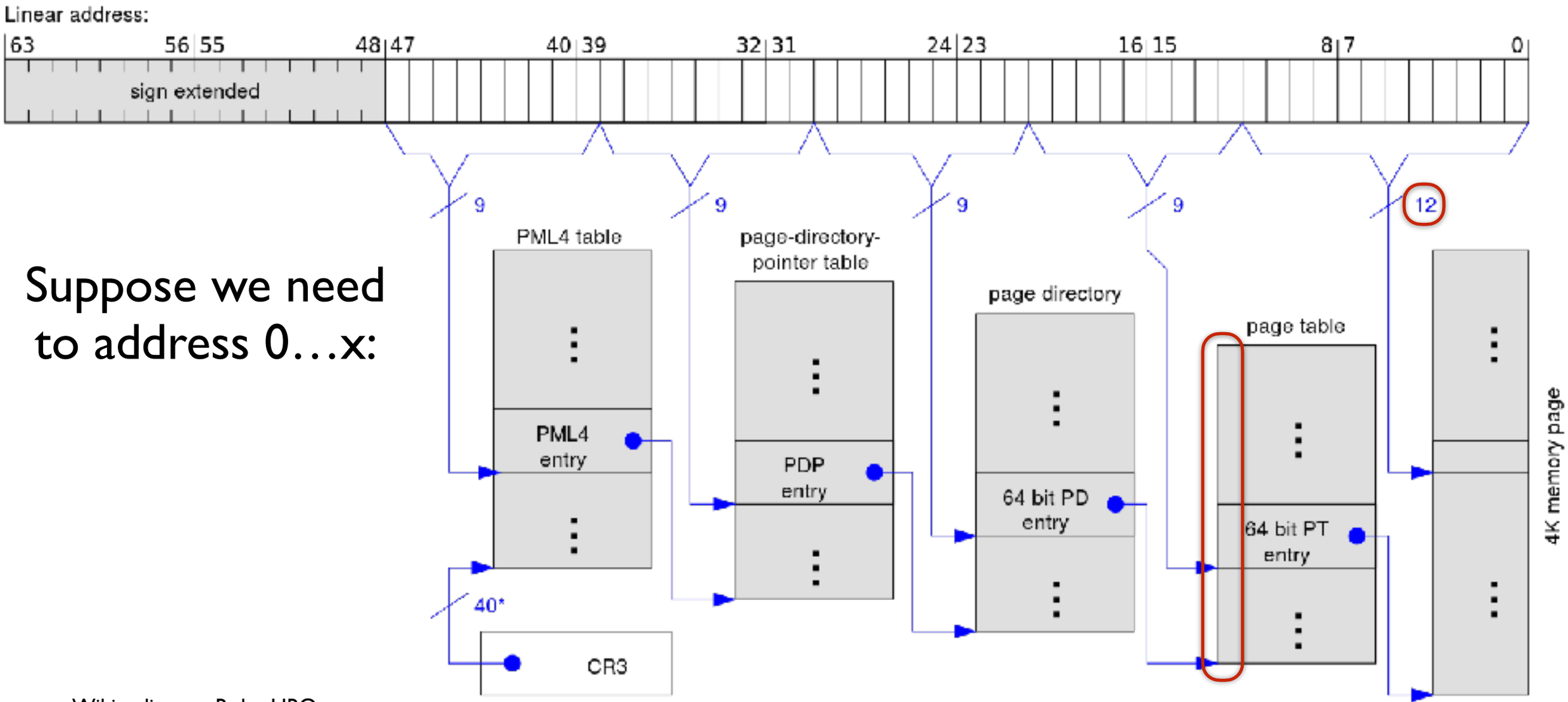

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Multilevel Paging

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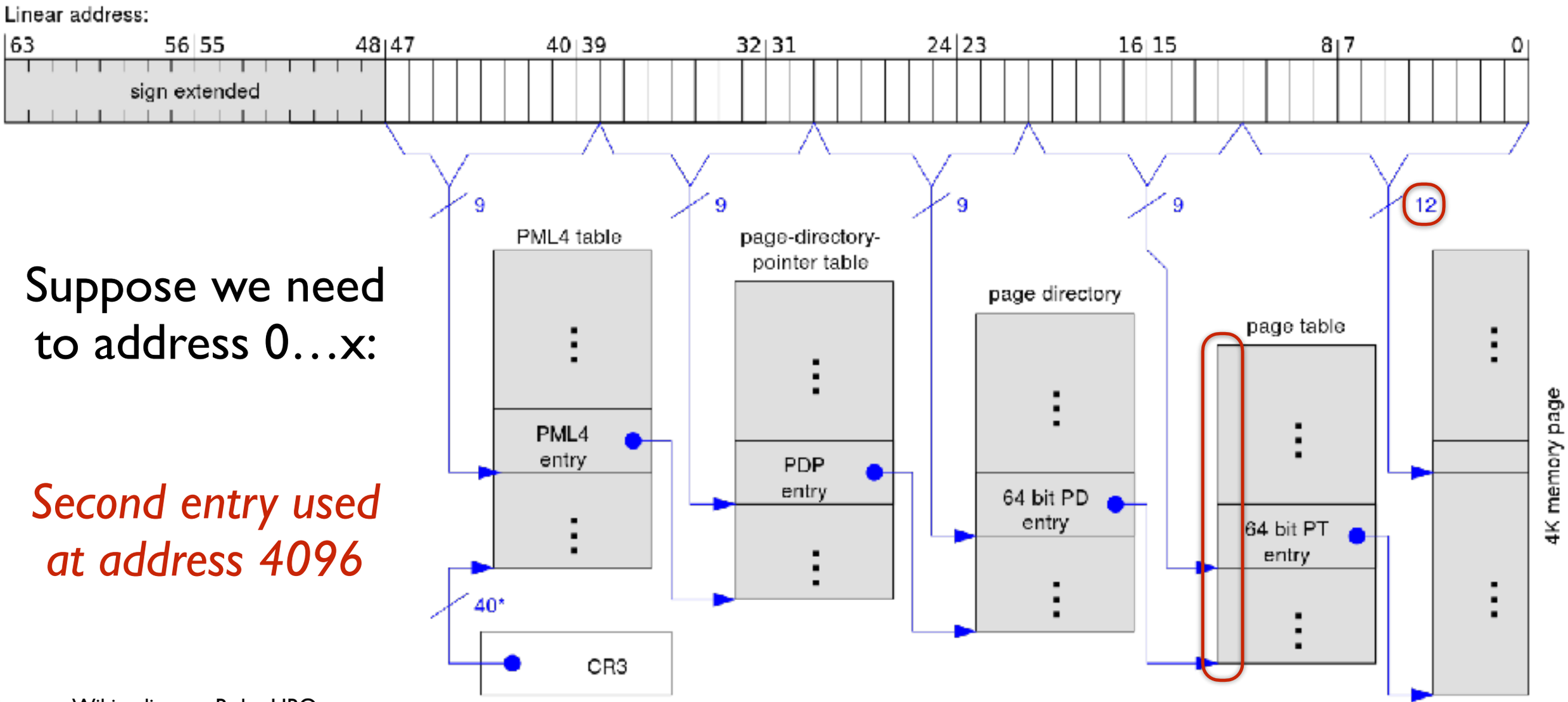
Suppose we need to address 0…x:

Second entry used at address 4096



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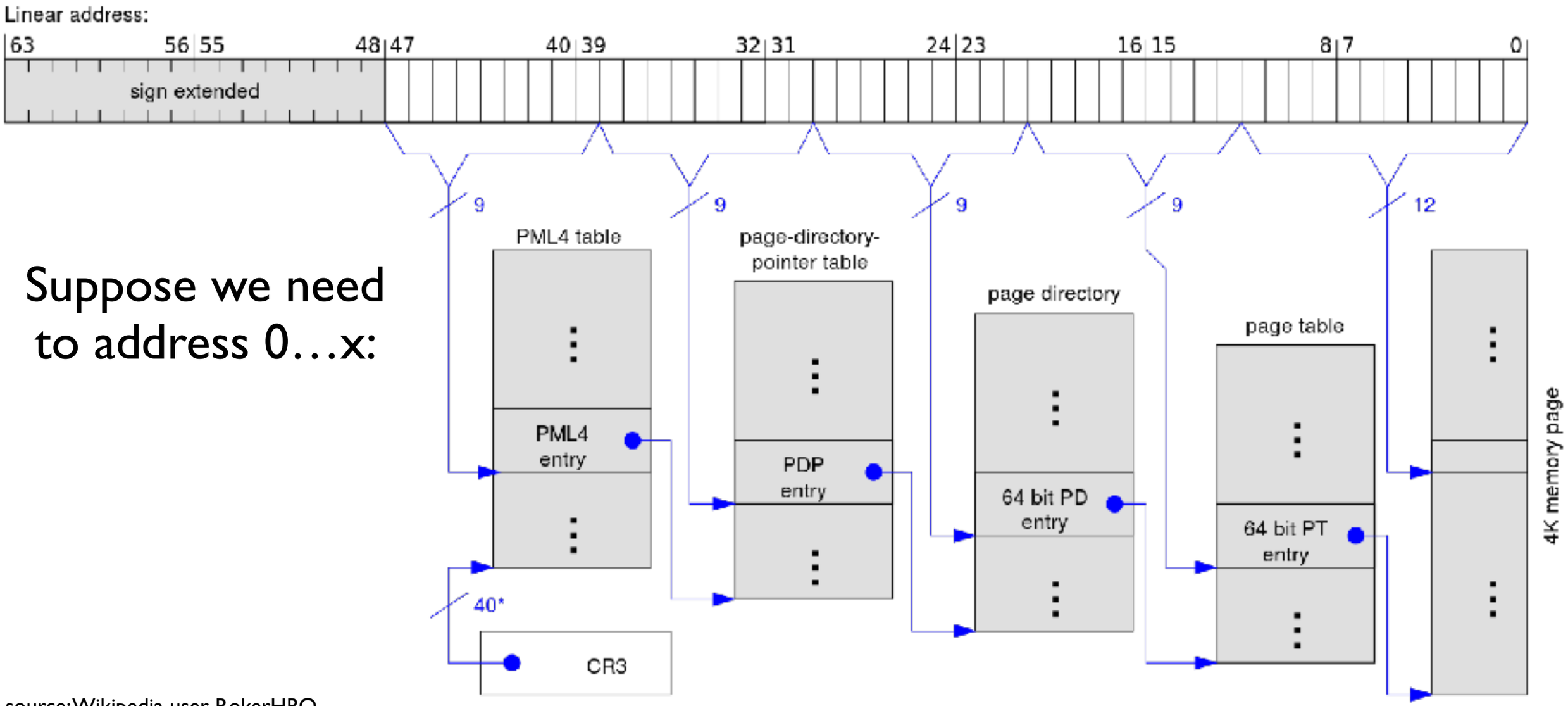

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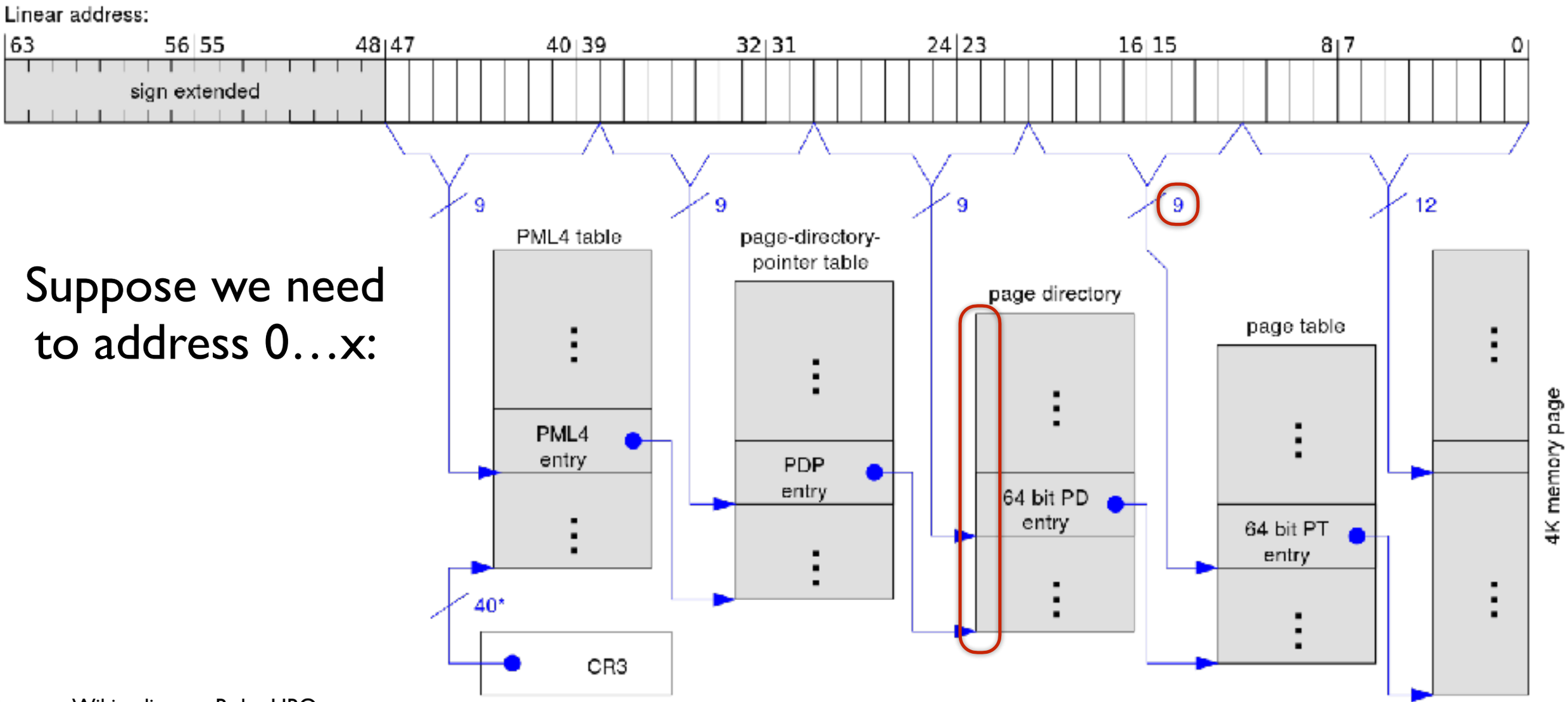

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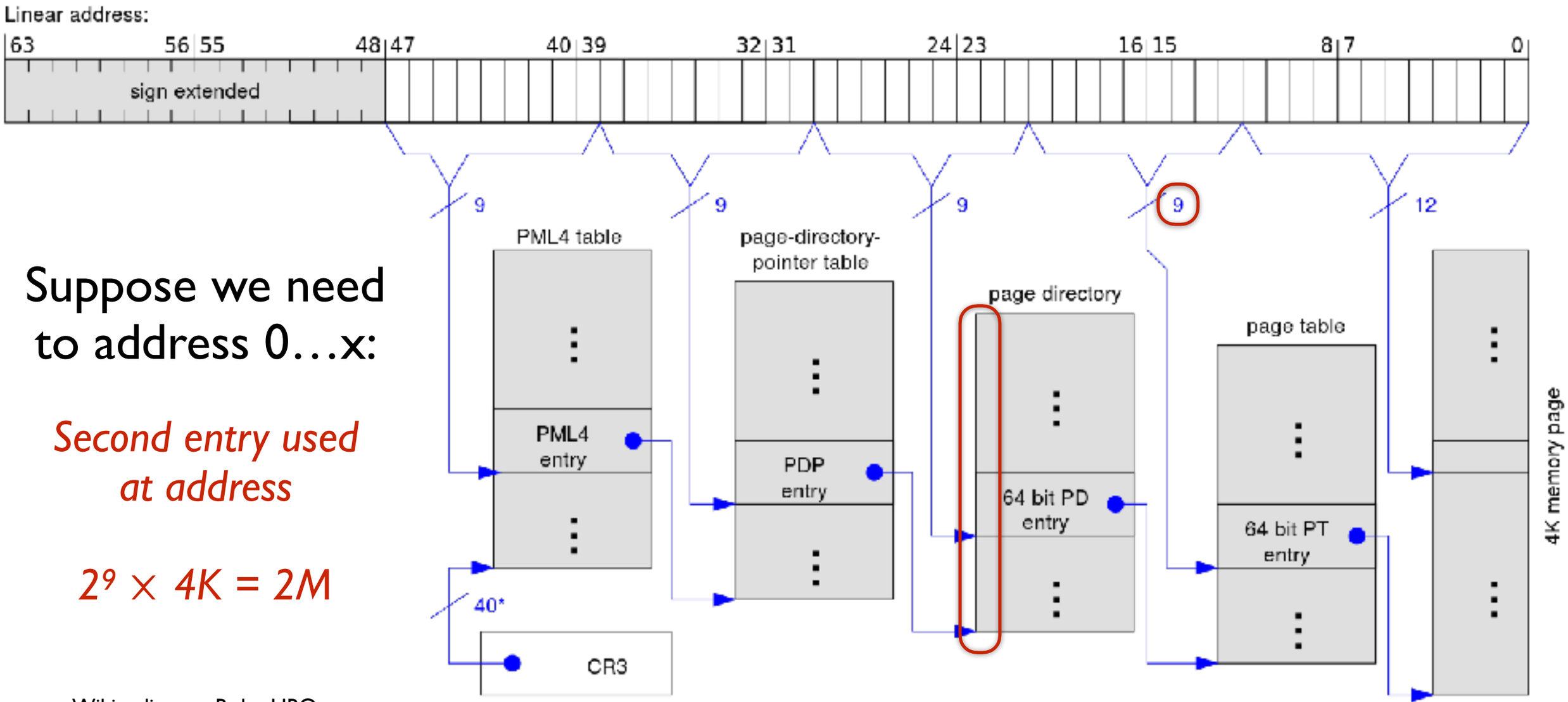
$2^9 \times 4K = 2M$



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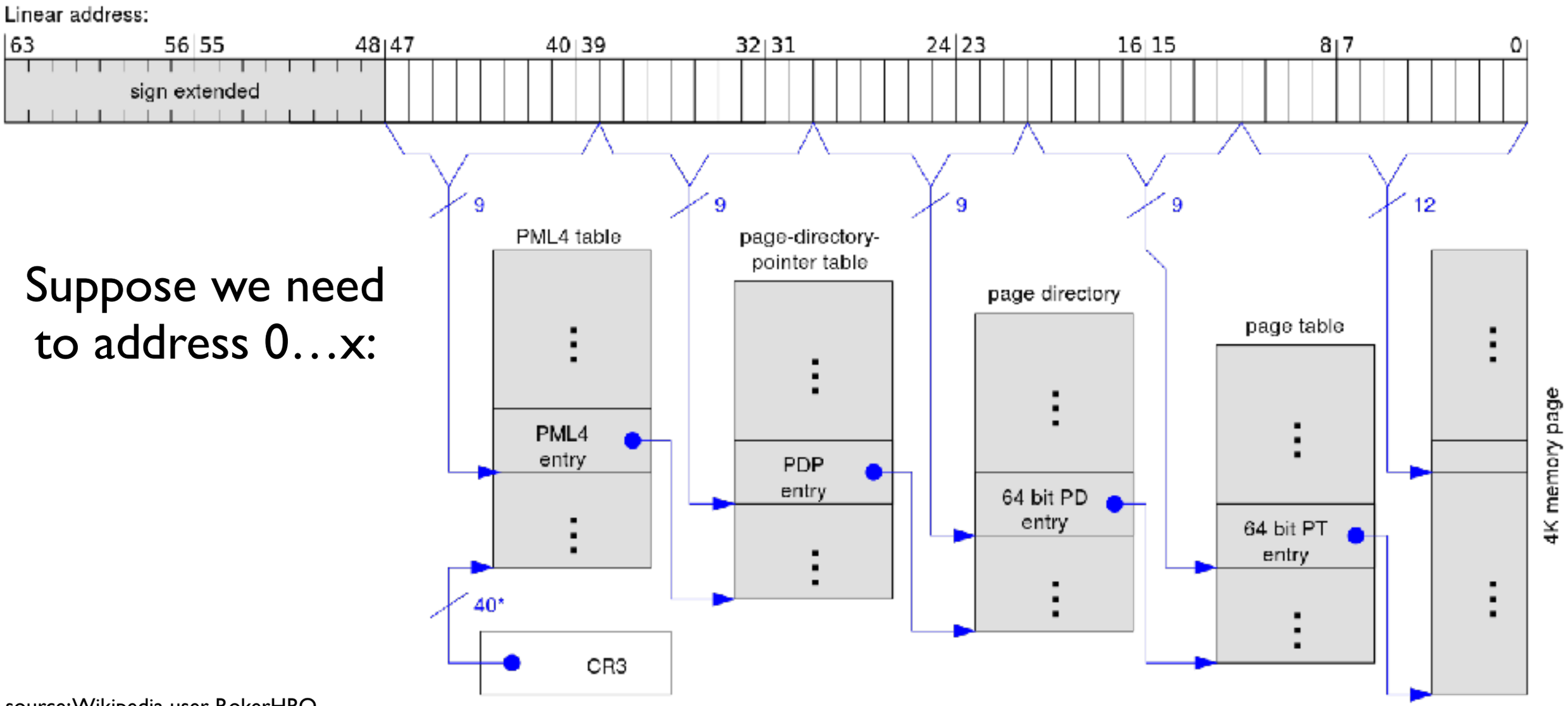

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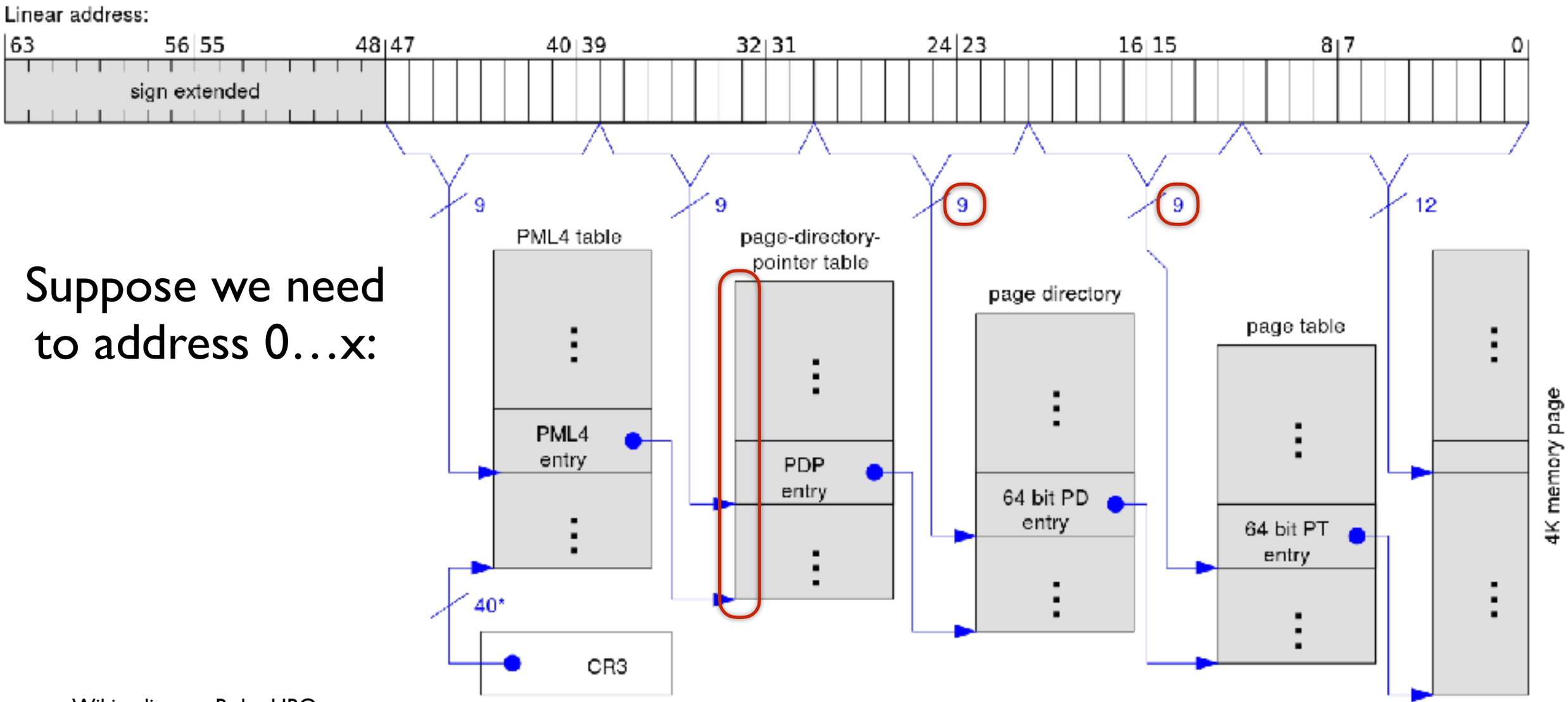

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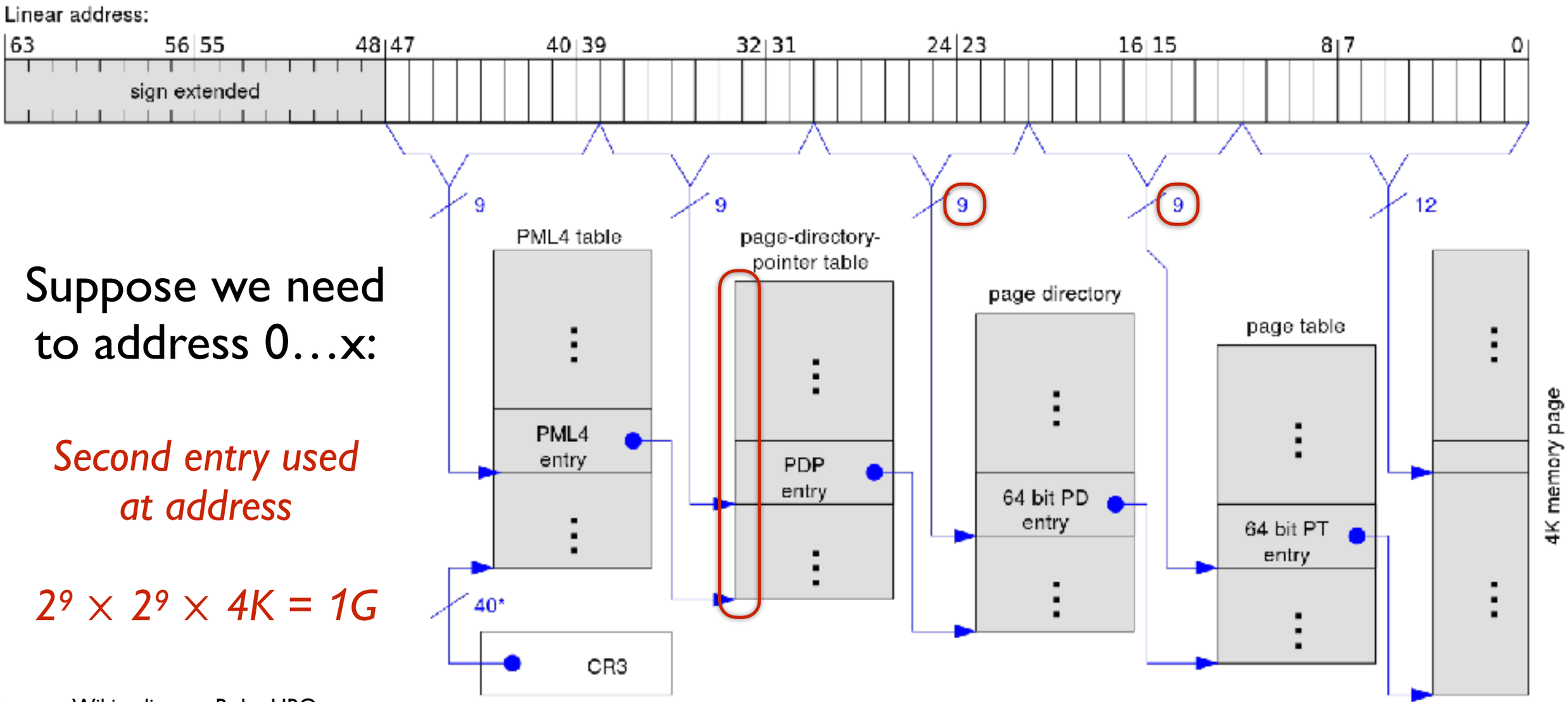
Second entry used at address

$2^9 \times 2^9 \times 4K = 1G$



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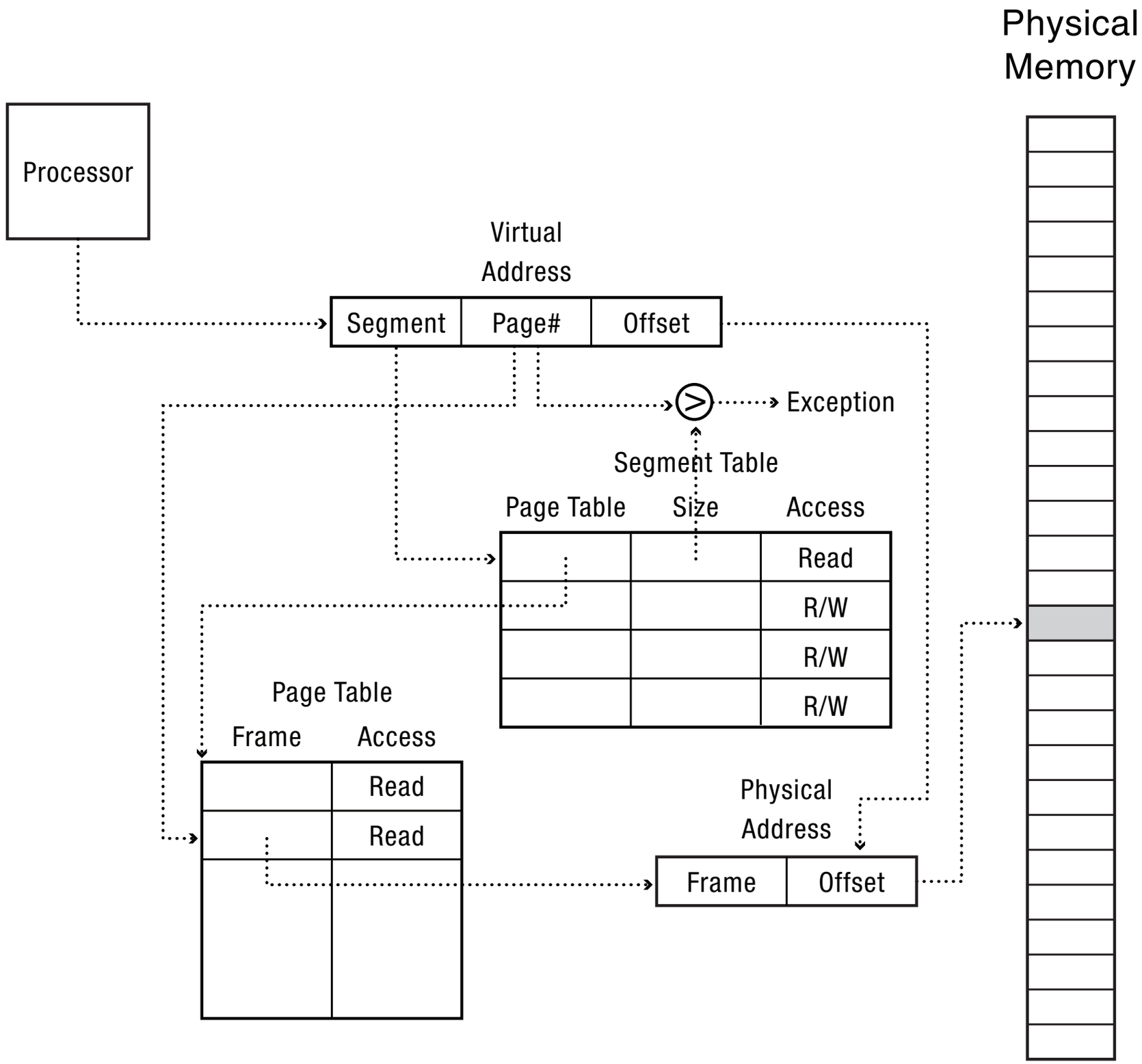
  - One-shot change

Alternative

(less important)

Paged Segmentation



Fim

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