Address Translation

Introduction

Hammurabi Mendes

Fall 18

Goals

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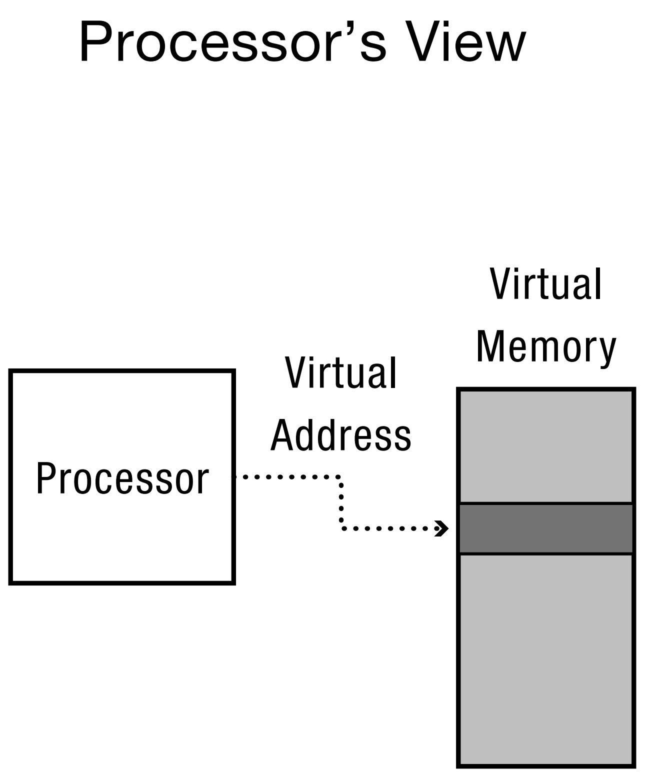
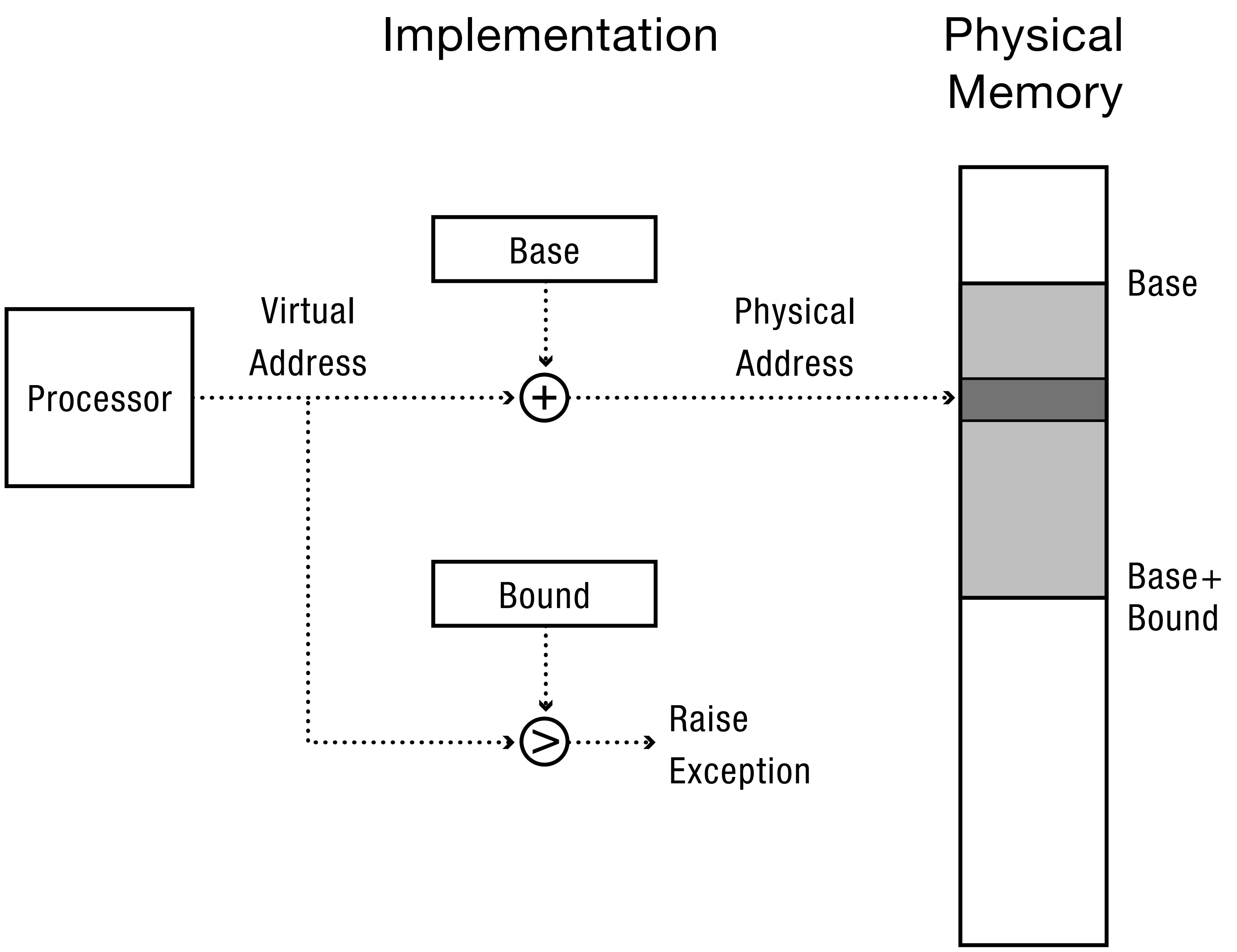
- Relocation Features
  - We want programs to be allocated in memory *fast*

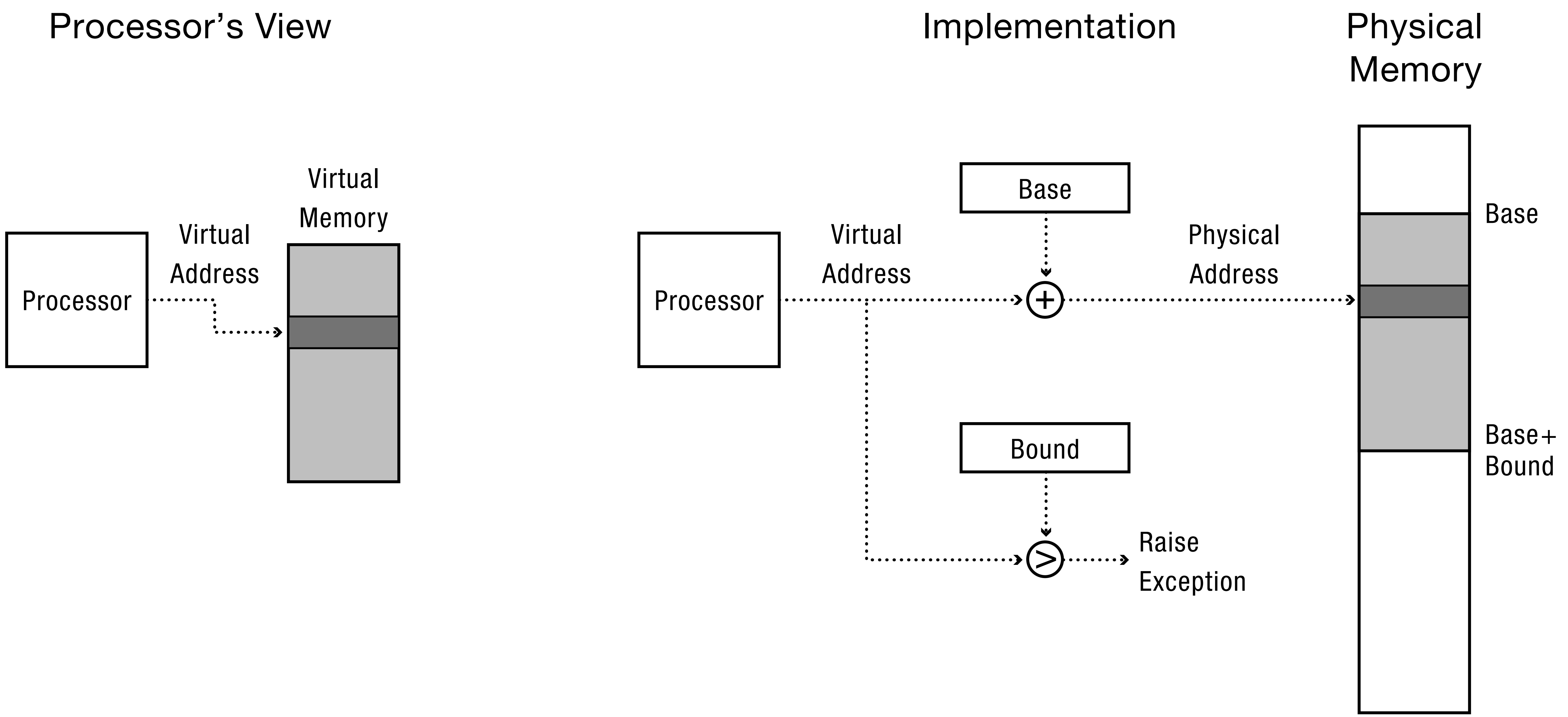
Approach 1: Base & Bound

Base & Bound


Processor's View
Virtual Memory
Processor
Virtual Address

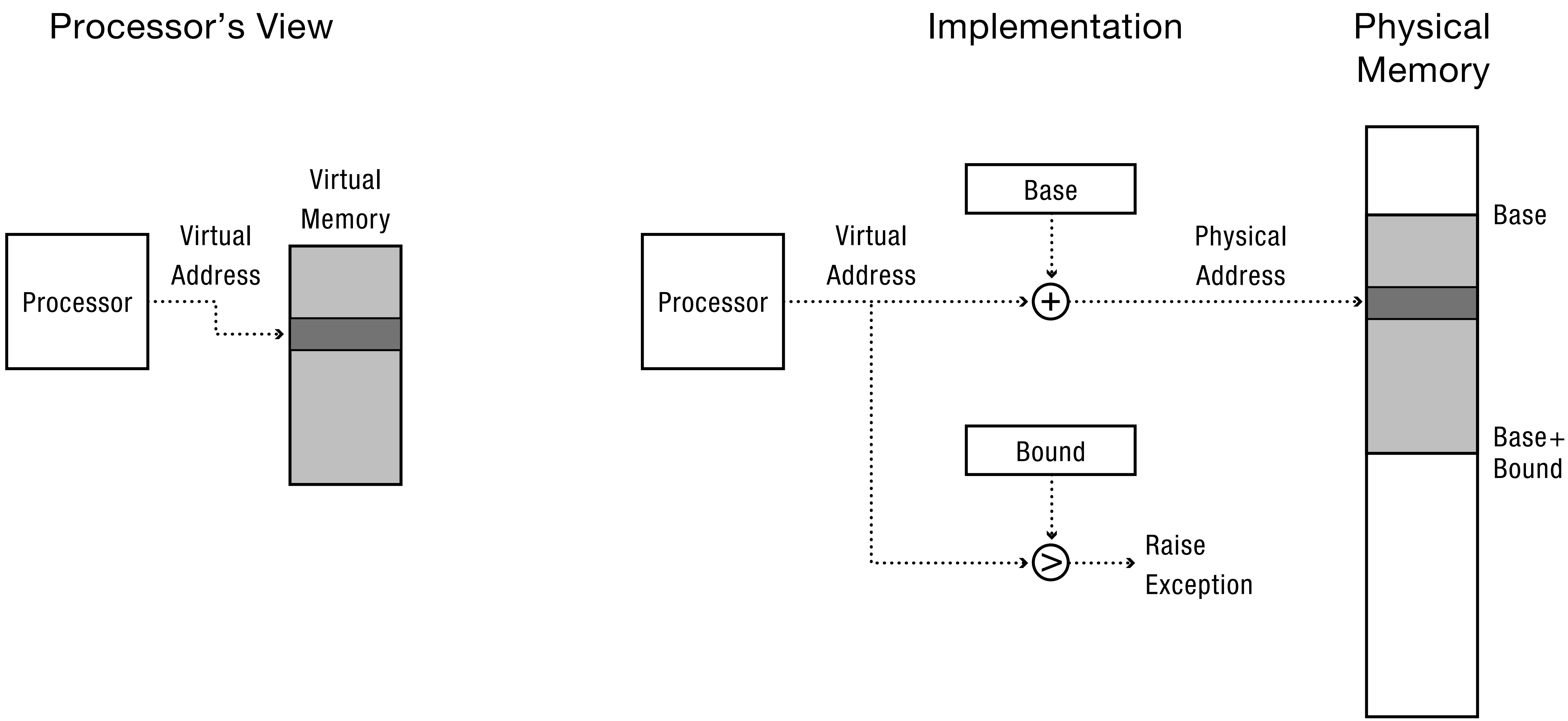

Implementation
Physical Memory
Processor
Virtual Address
Base
Physical Address
Bound
Raise Exception
Base
Base+ Bound

Base & Bound



- A program cannot see past its own memory!

Base & Bound



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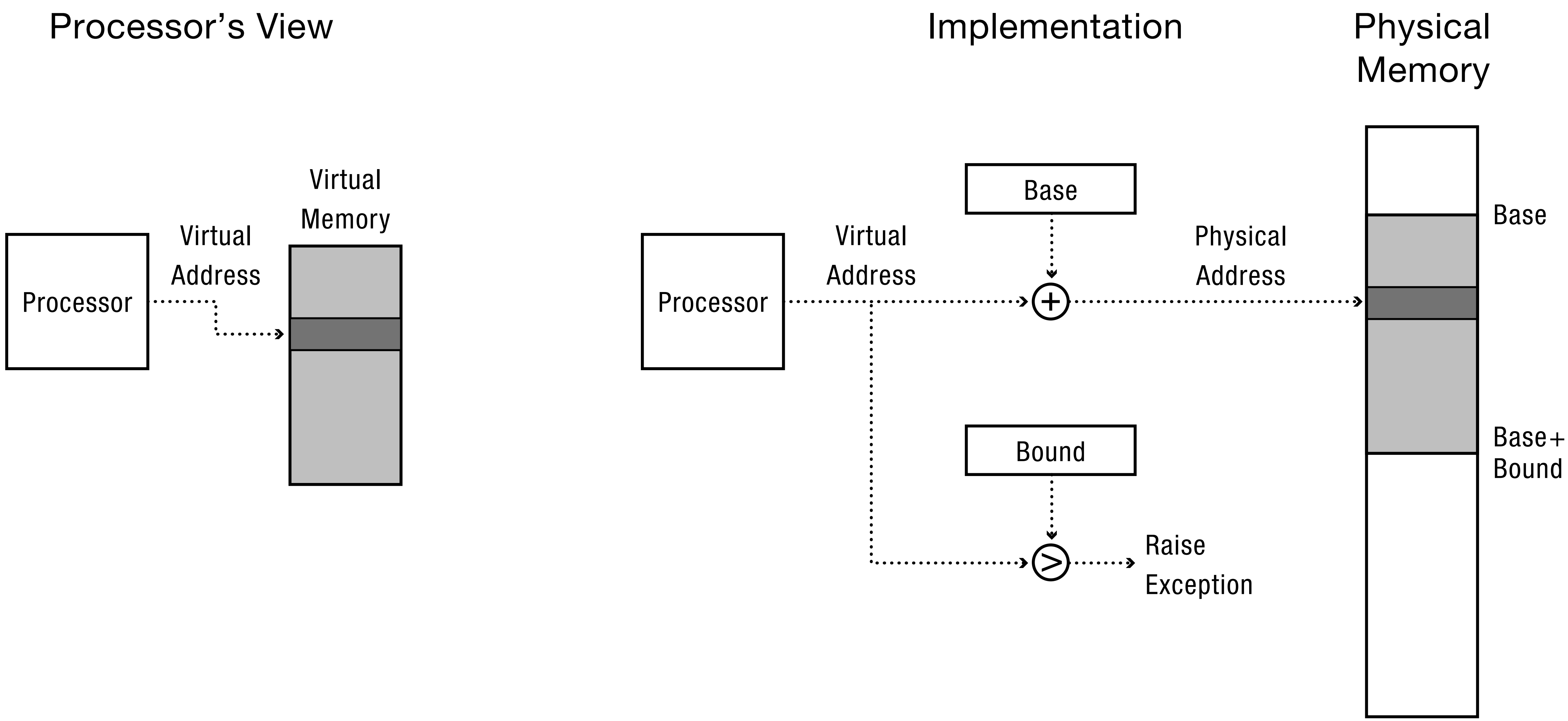
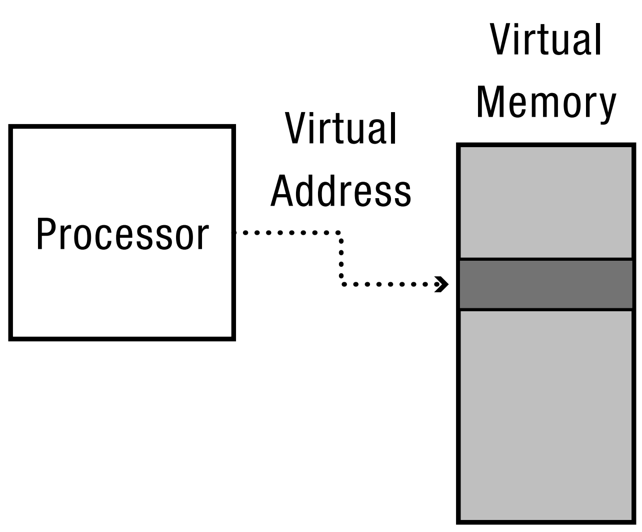


- A program cannot see past its own memory!
- No more need for relocating loader!
- Context switch: just change base & bounds

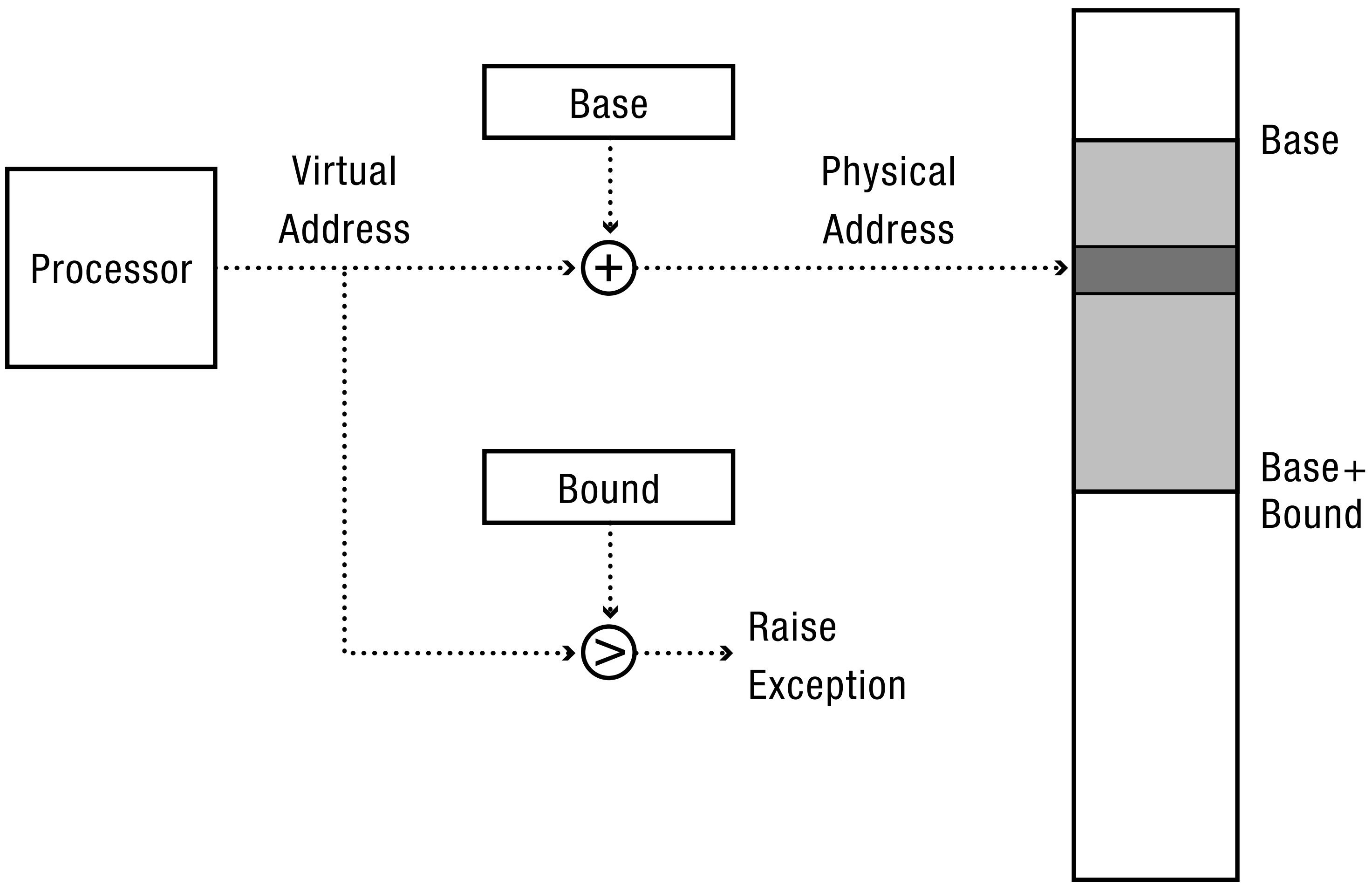
Base & Bound

Processor's View

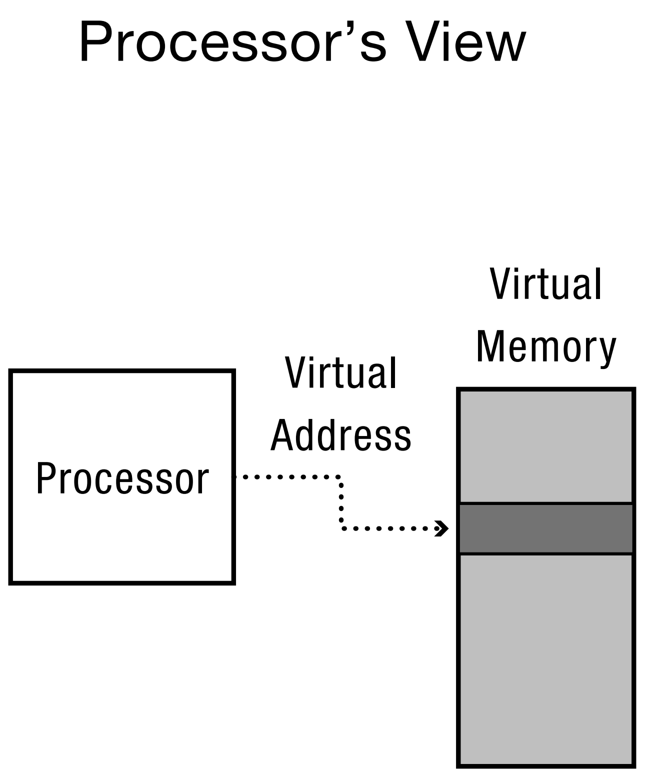


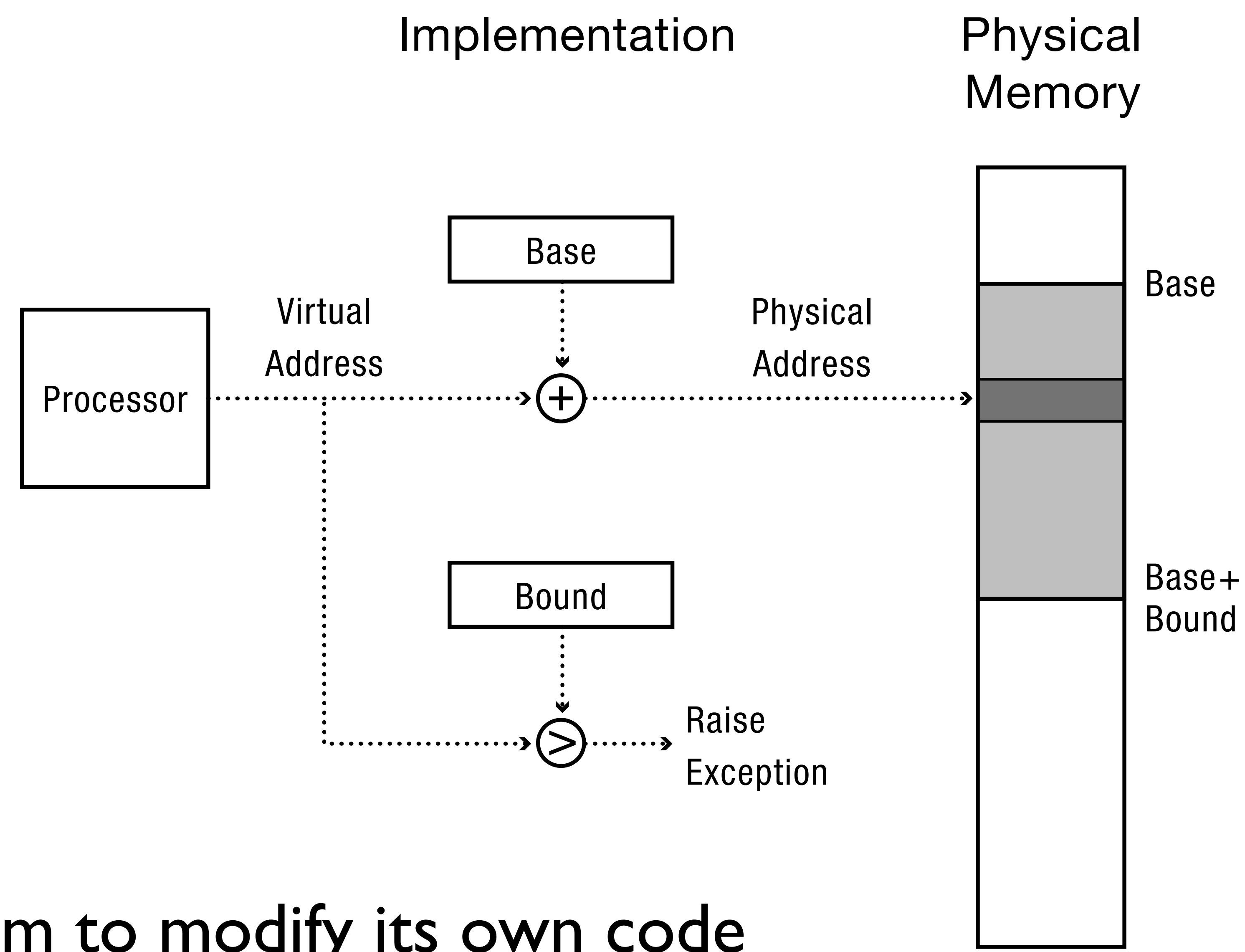
Implementation

Physical Memory



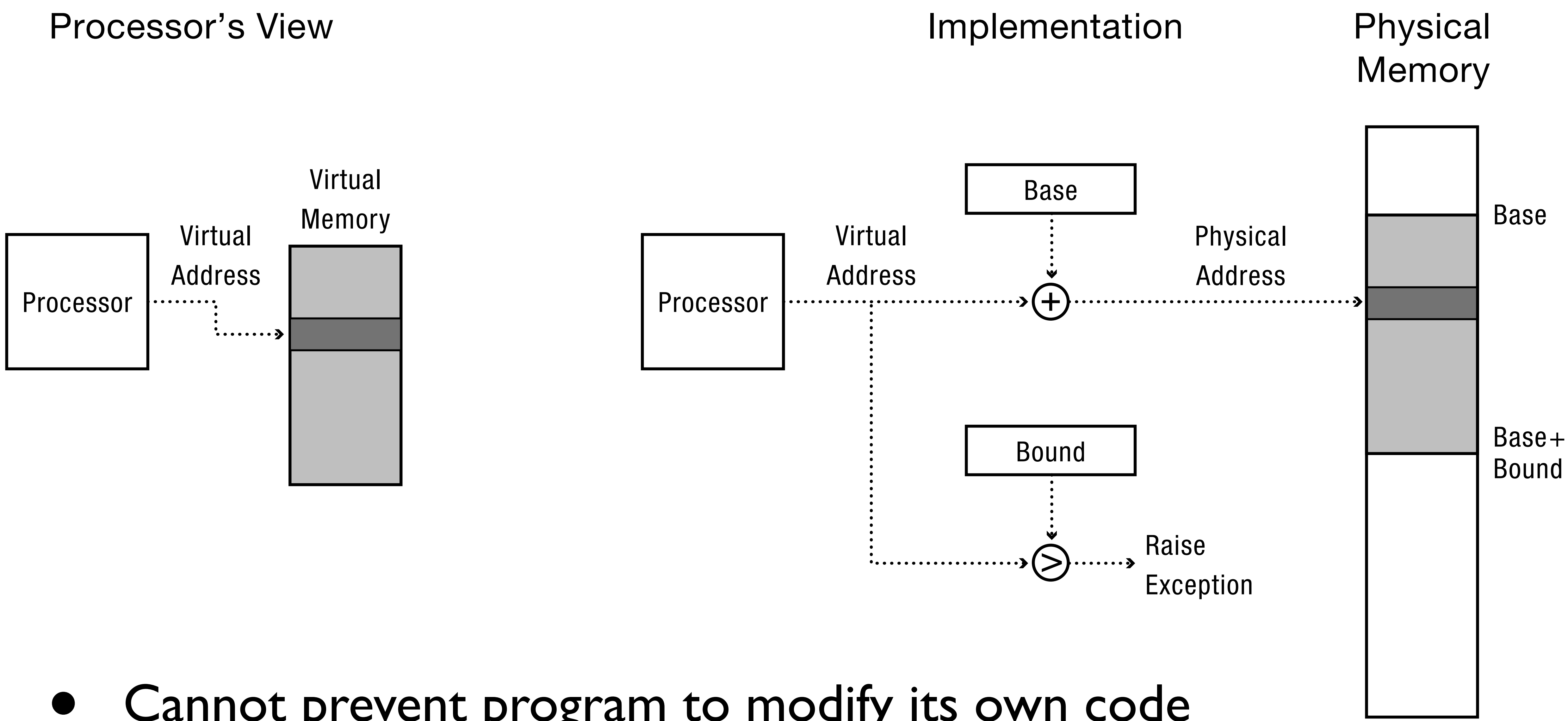
Base & Bound





- Cannot prevent program to modify its own code

Base & Bound



- Cannot prevent program to modify its own code
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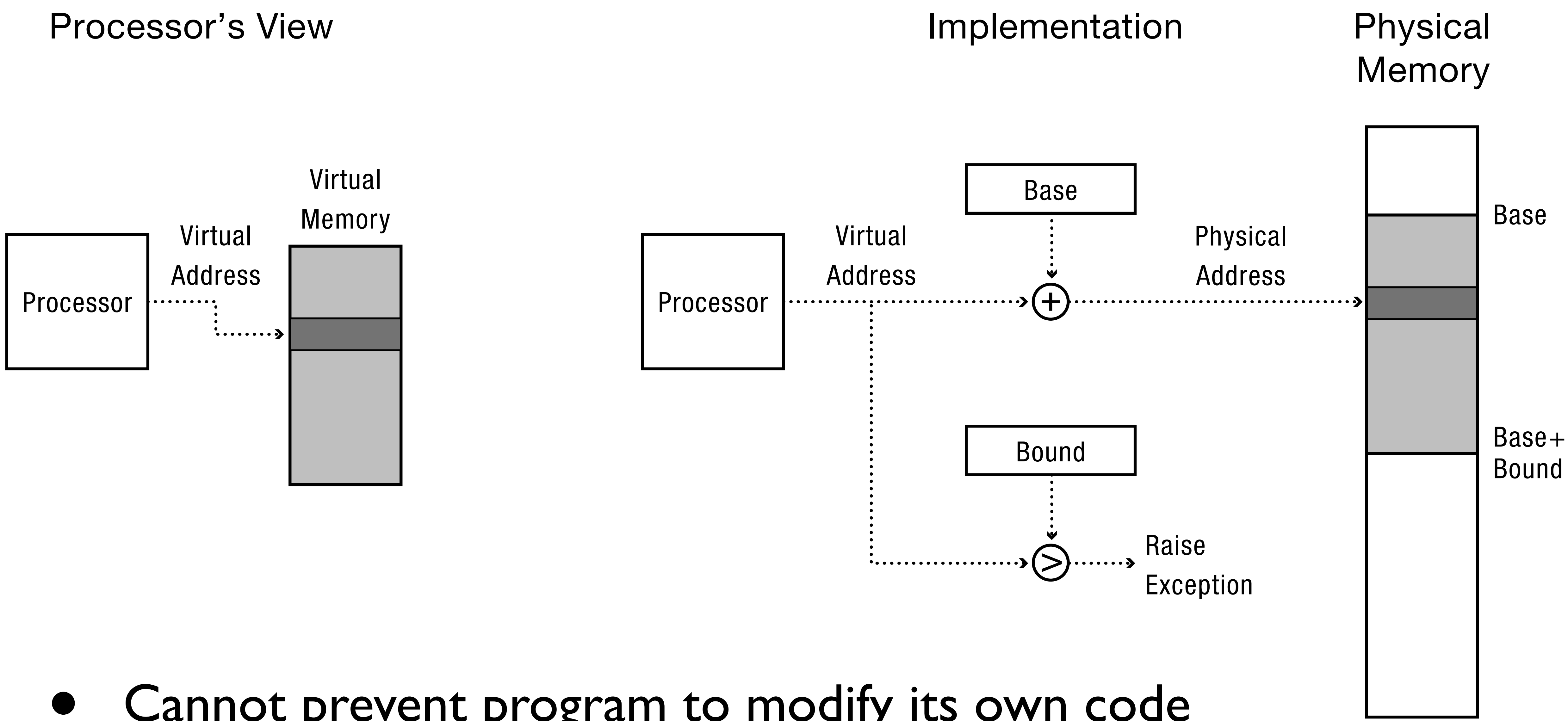
Base & Bound



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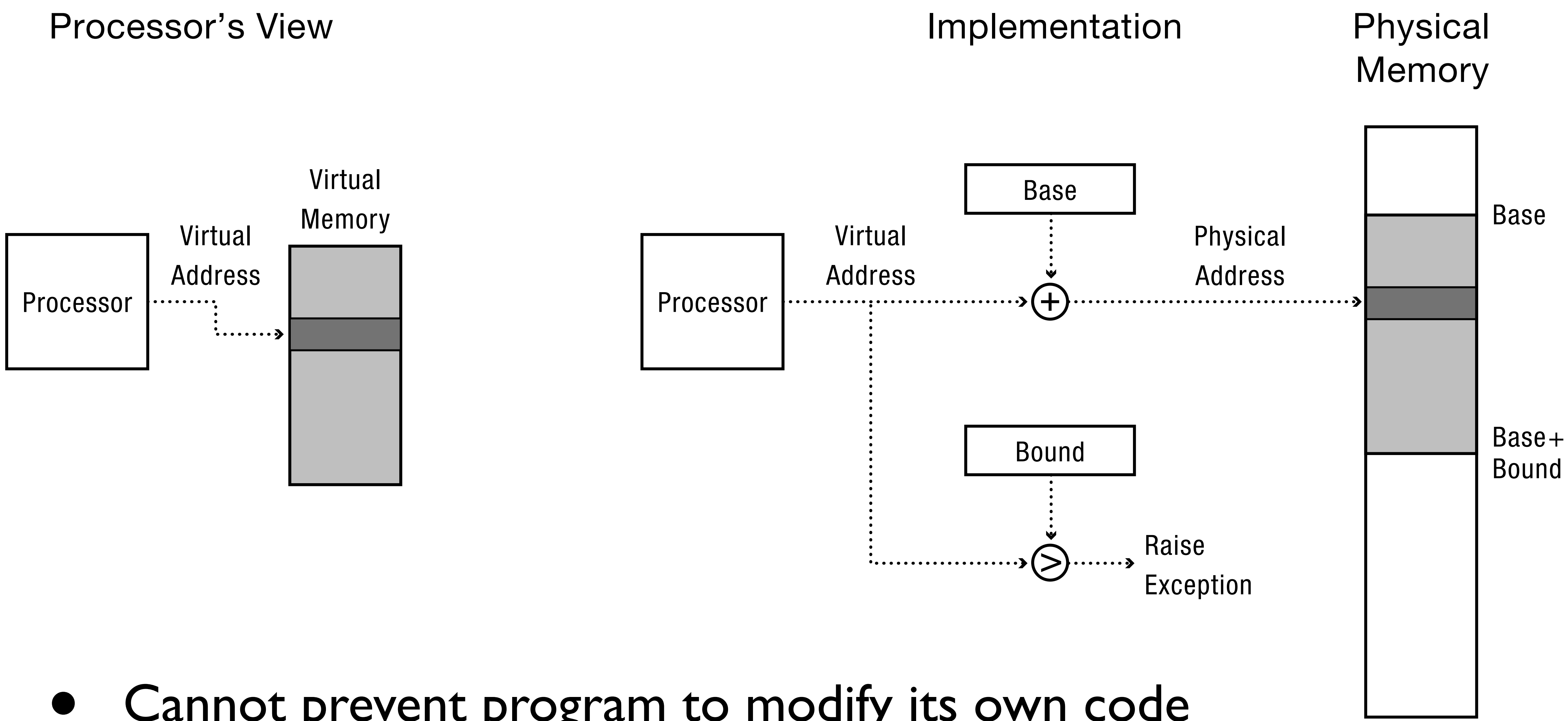
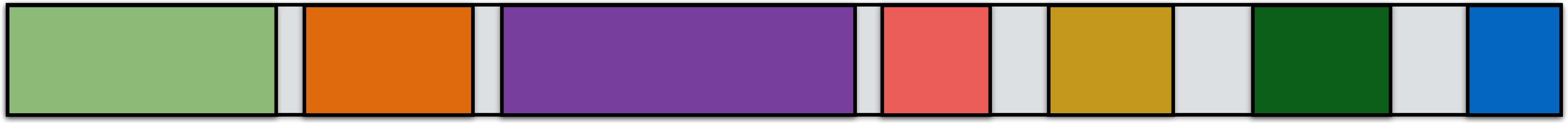
Base & Bound



- Cannot prevent program to modify its own code
- No sharing!
- No expandable heap/stack
- External fragmentation

External Fragmentation

Suppose your memory looks like this



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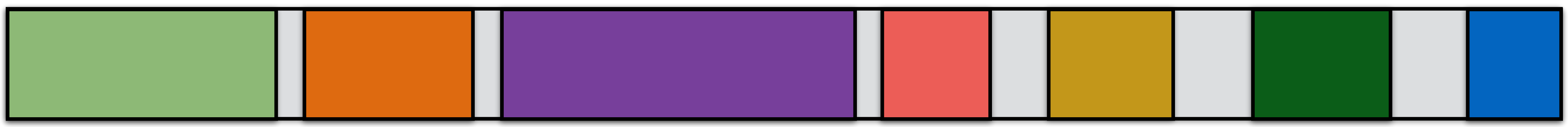
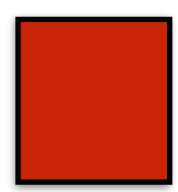


Allocate this



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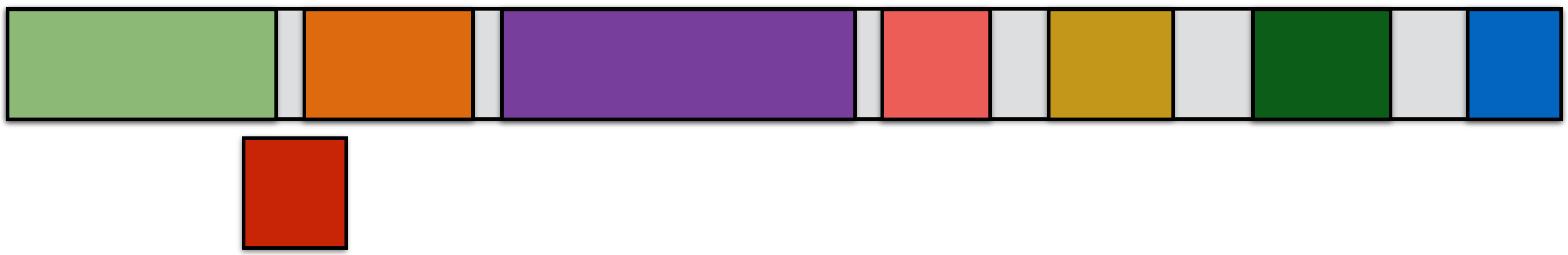

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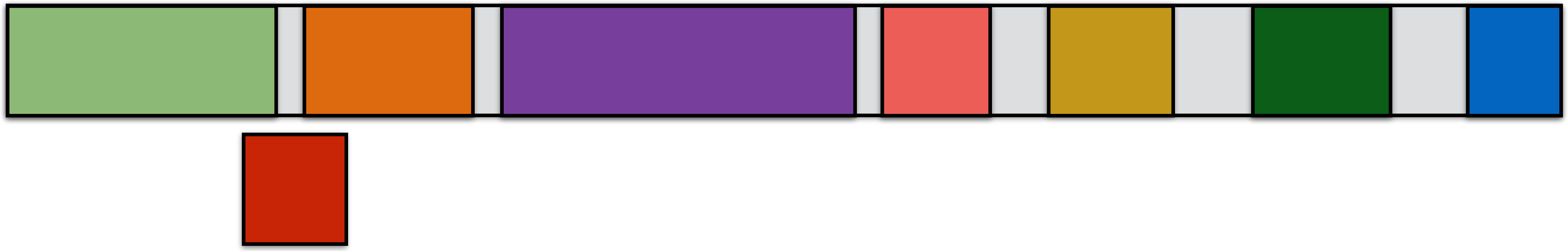

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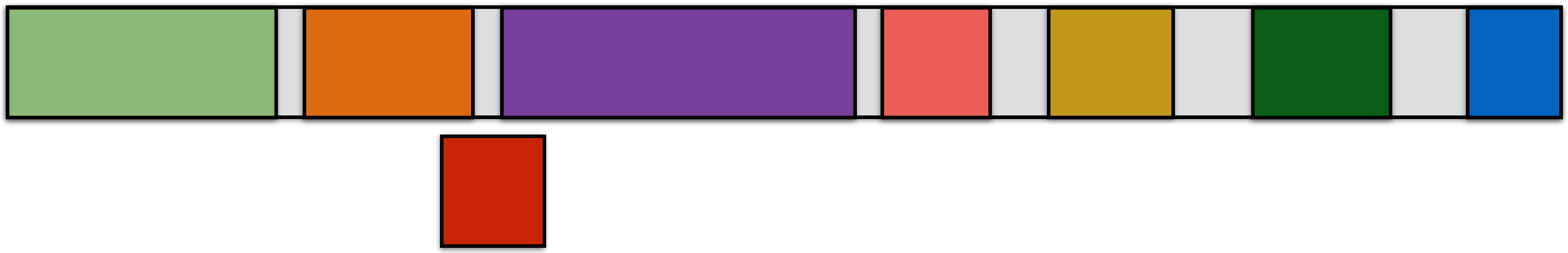

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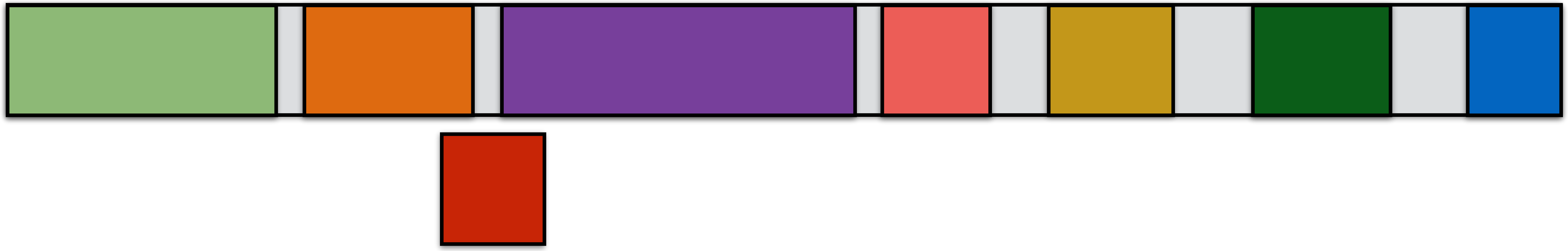

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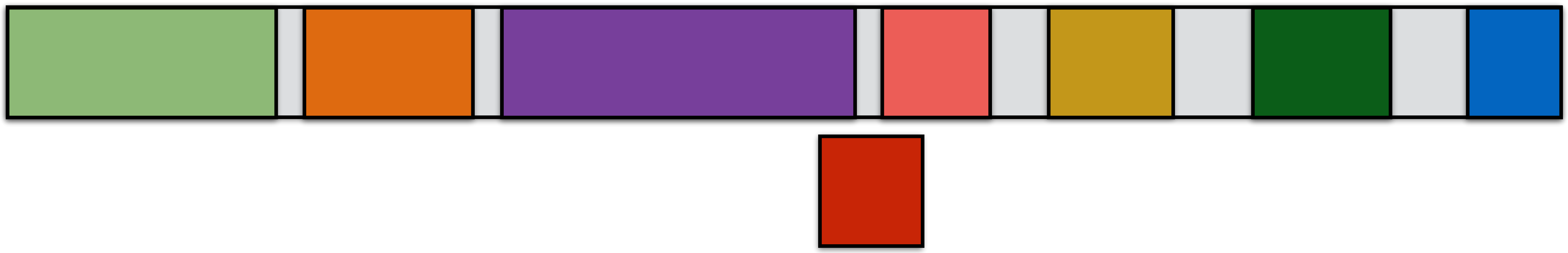

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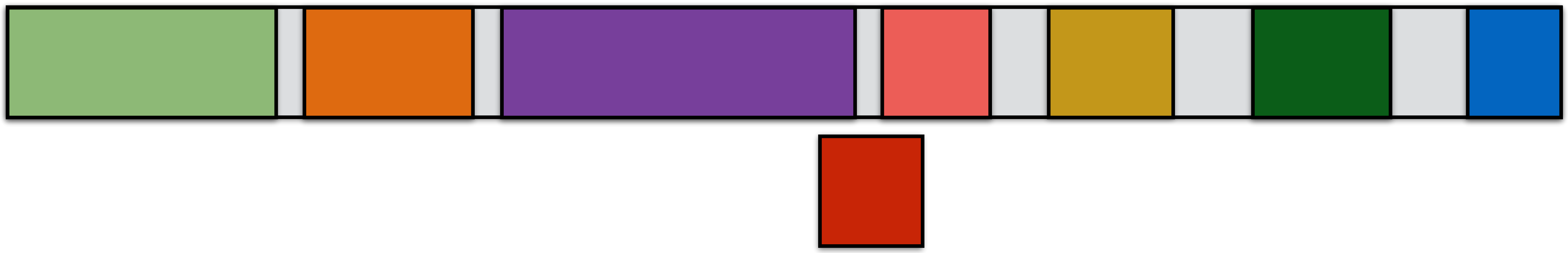

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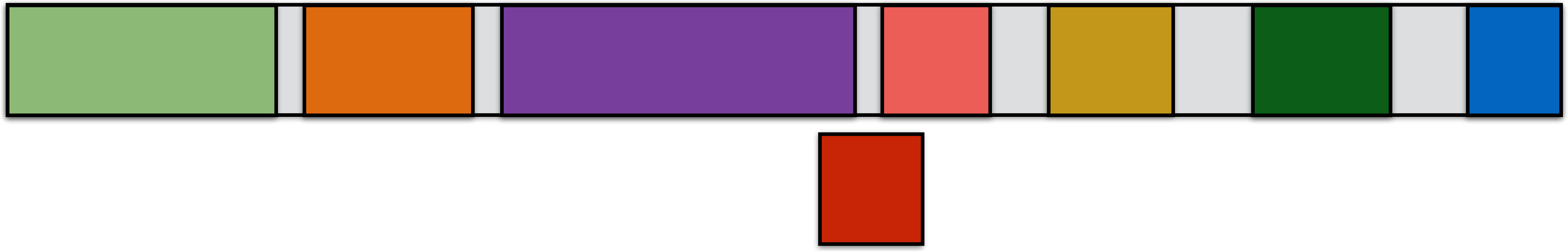

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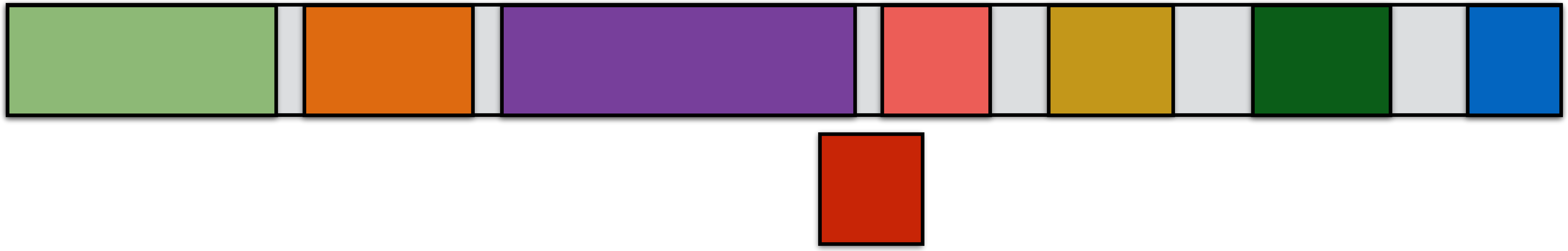


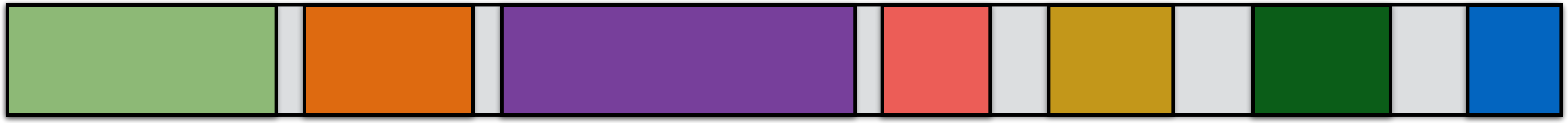
Nope… you get the idea

You suffer from *external fragmentation:*

You have enough space available, but not contiguously!

External Fragmentation

Defragment memory is costly…



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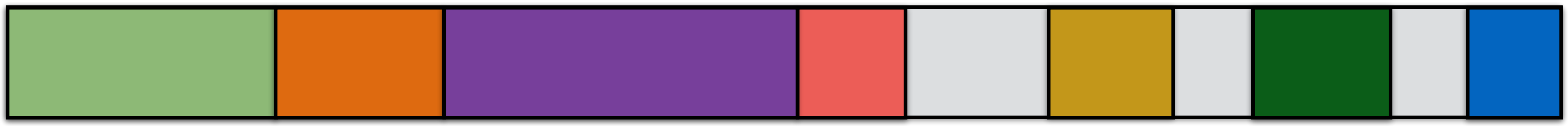

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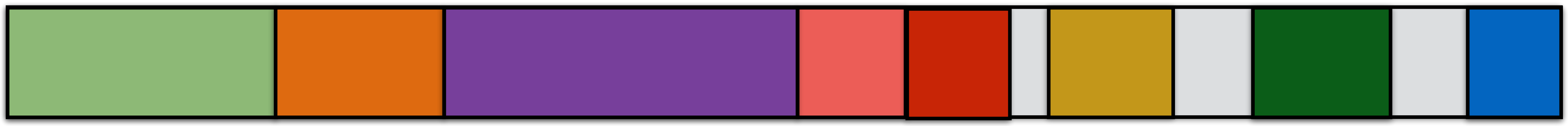

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External Fragmentation

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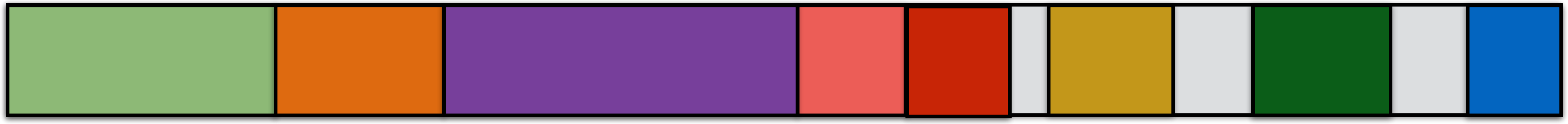


Aha!

Much better to *avoid* ever having to do that!

Approach II: Segmentation

Segmentation

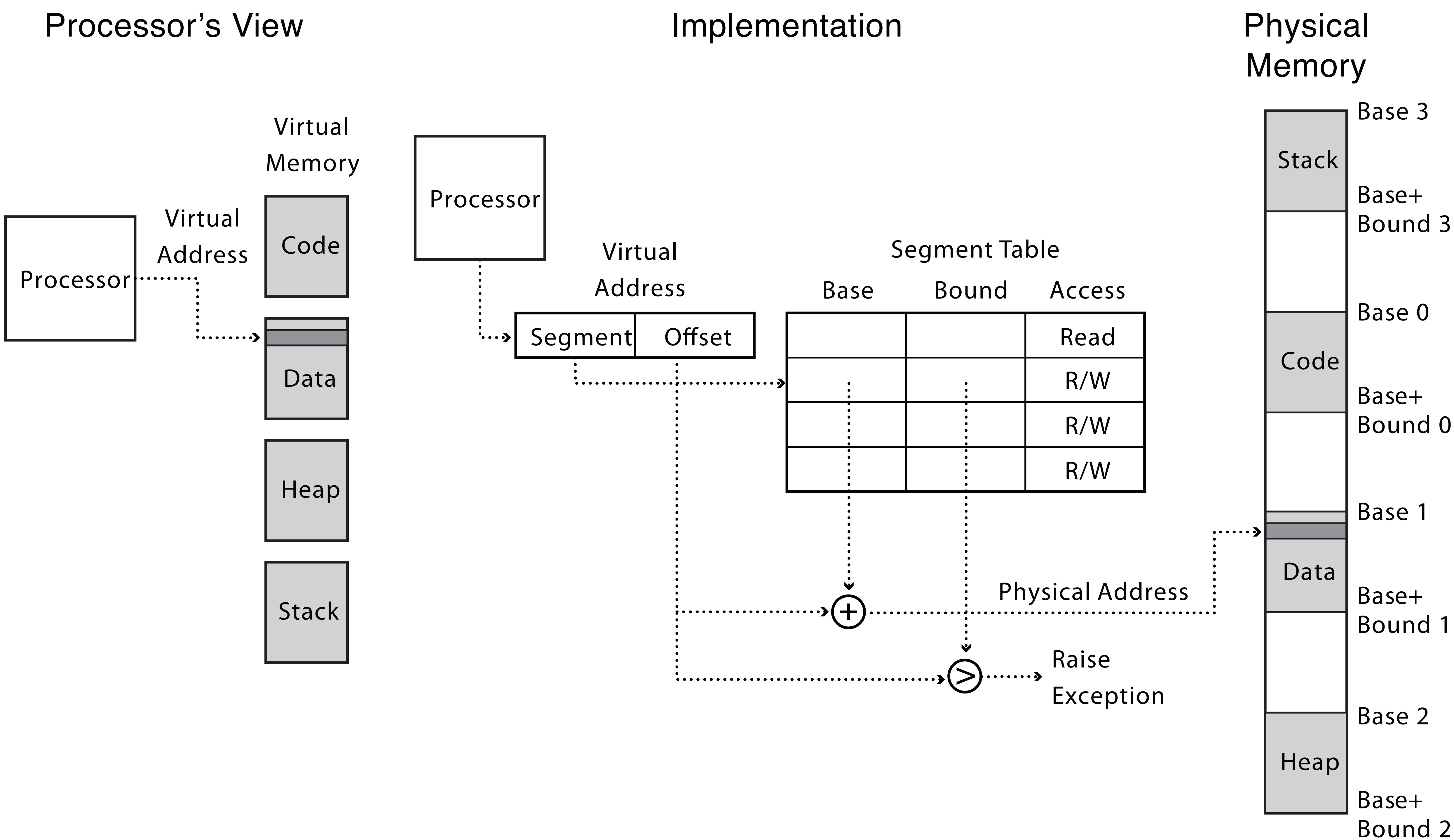
Segmentation

- Multiple base & bound registers

Segmentation

- Multiple base & bound registers
- On Intel x86:
  - Code (CS)
  - Data (DS)
  - Stack (SS)
  - Extra segment (ES)
  - Two general-purpose segments (FS, GS)

Segmentation



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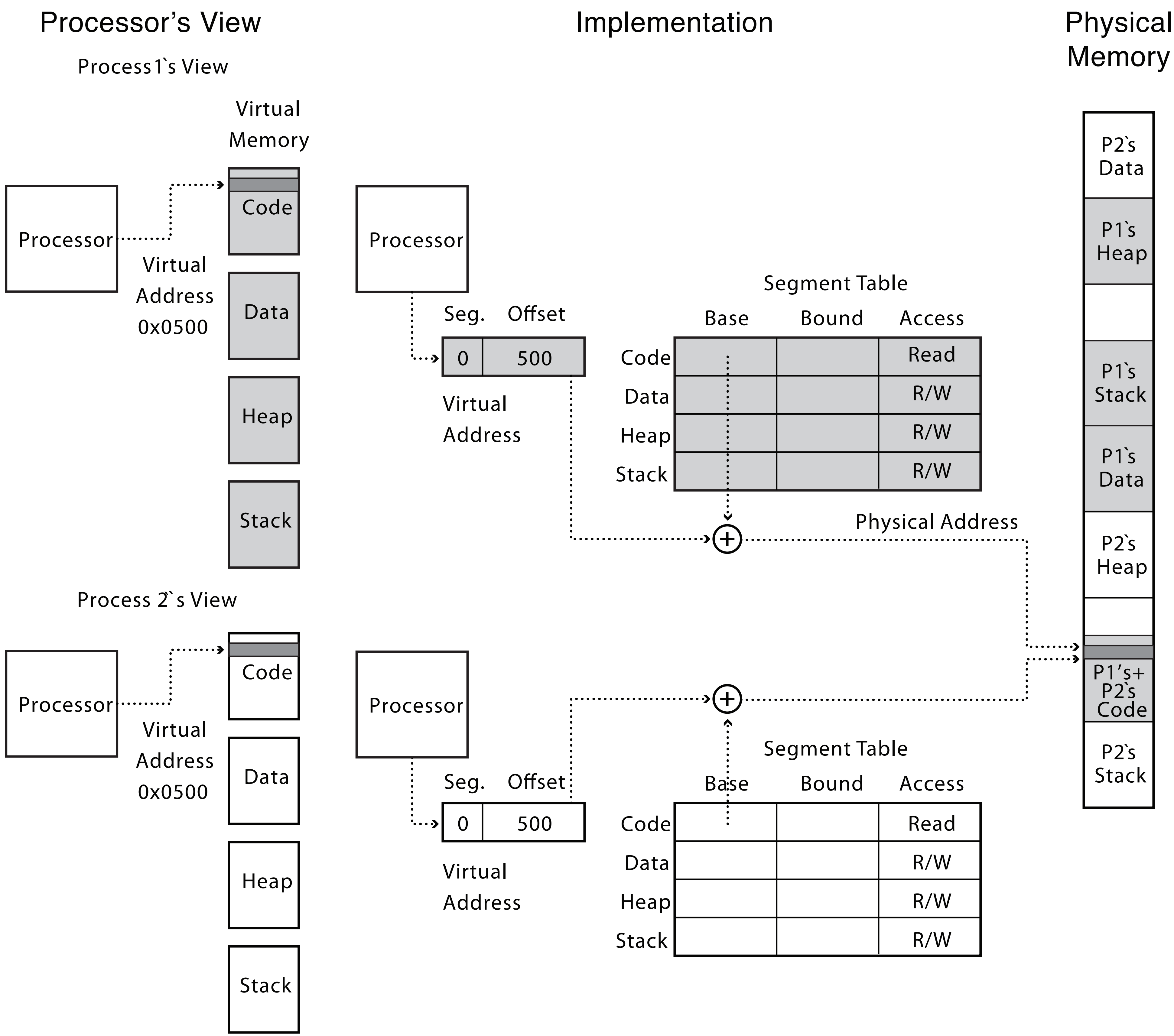
  - Save the segment table contents
- Sharing is allowed!

* source: Wikipedia user Sander van der Wel

Segment Sharing



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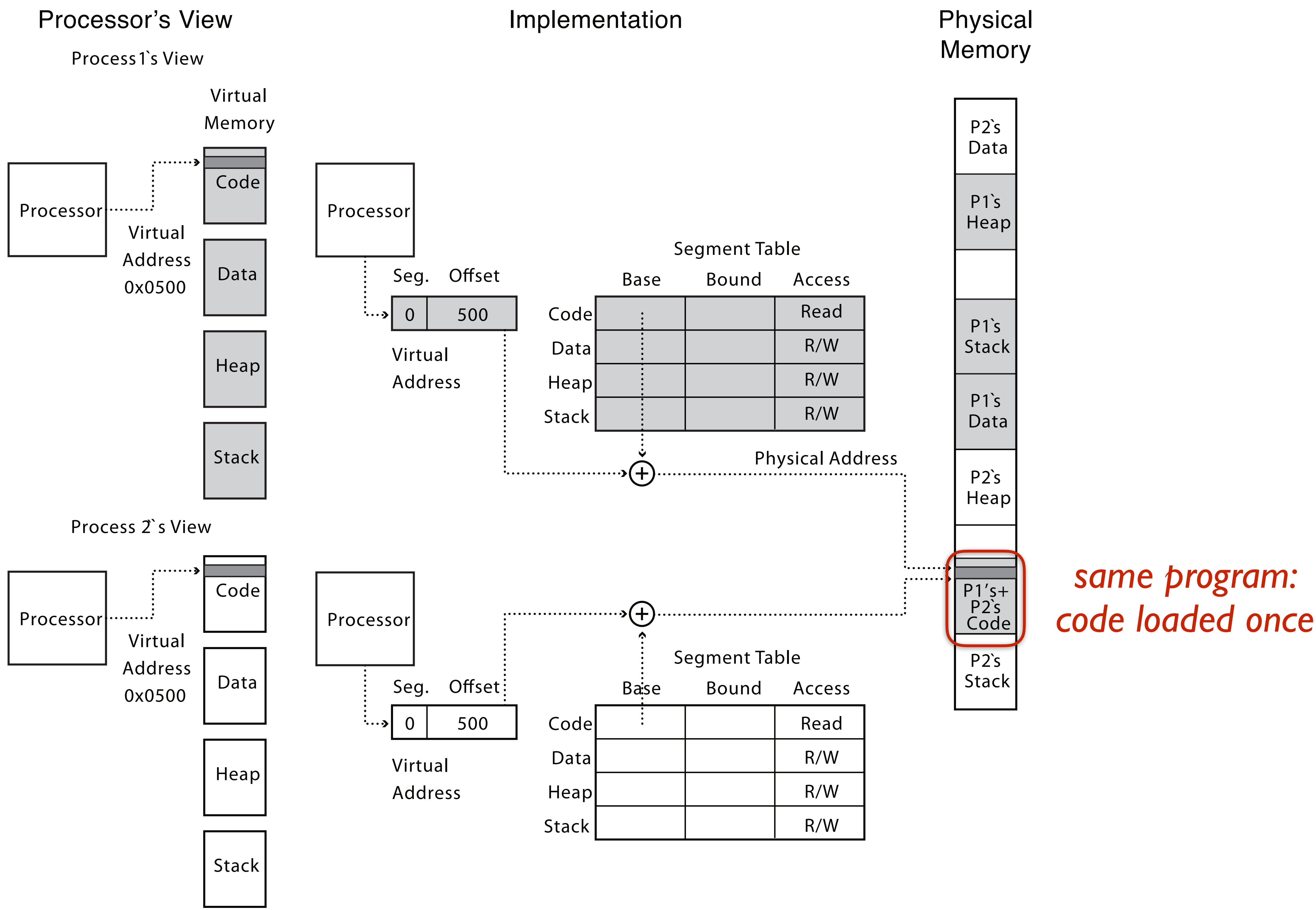

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** opportunistic understood in a good sense.

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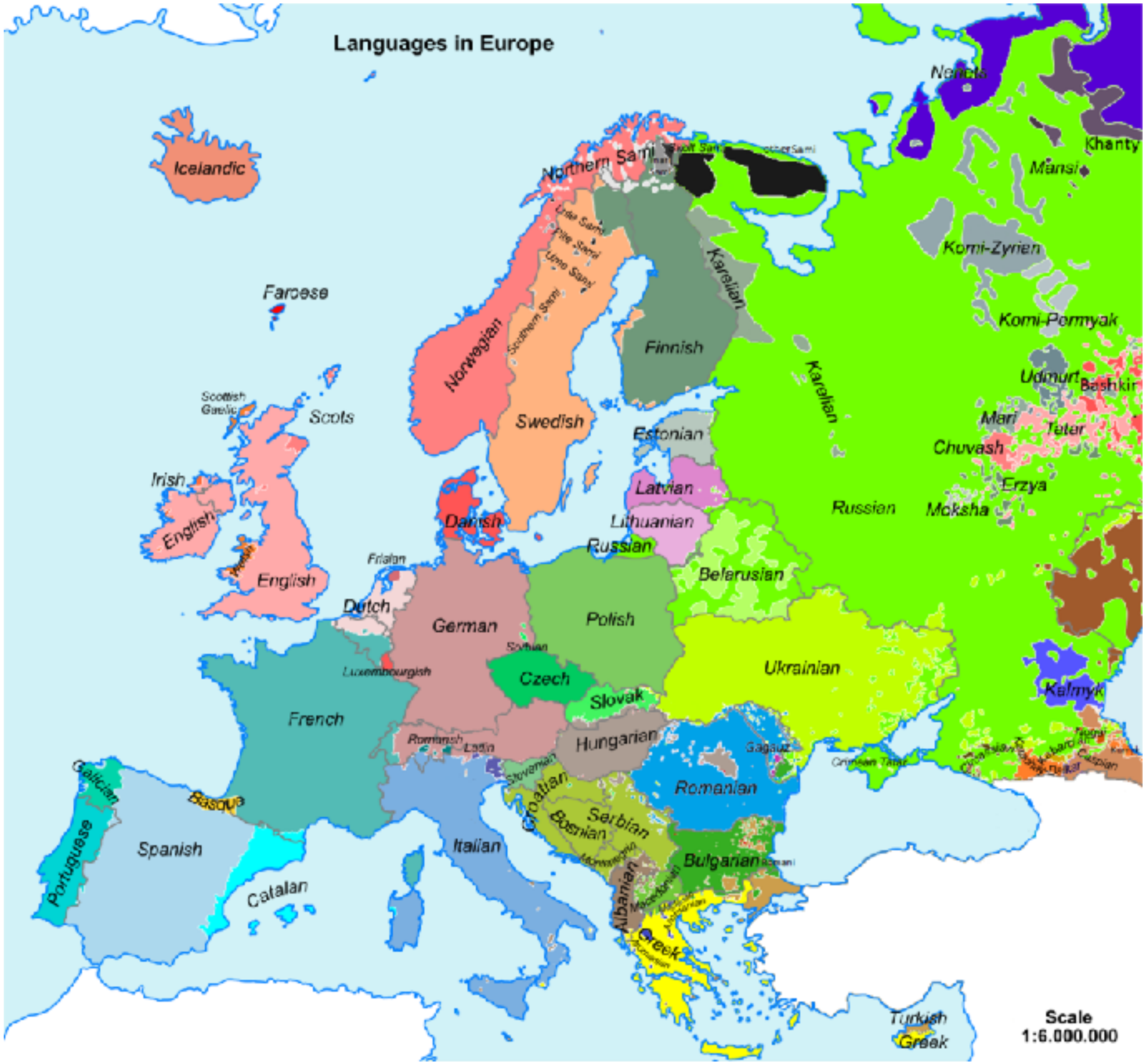
But…

External Fragmentation



Approach III: Paging

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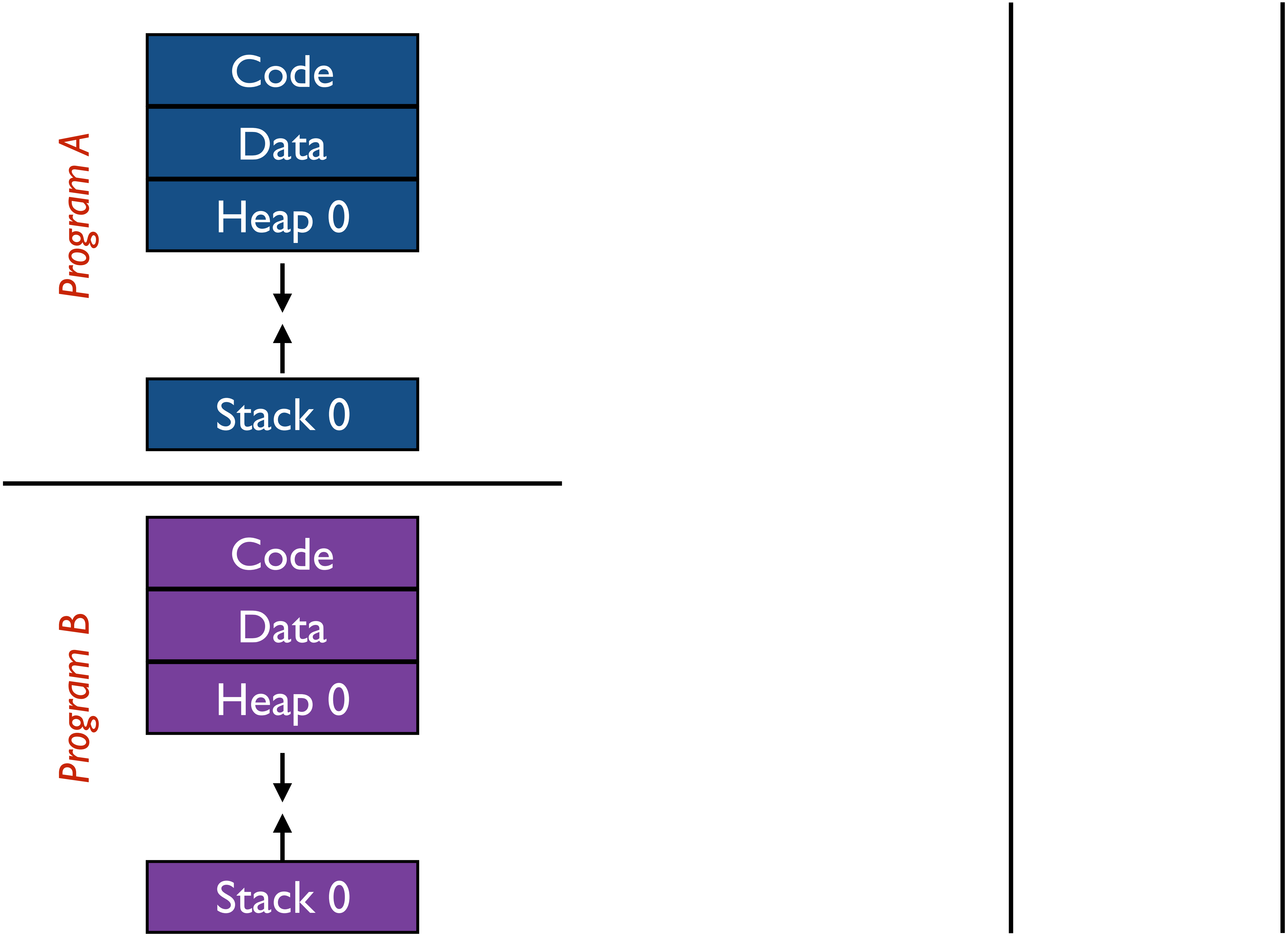
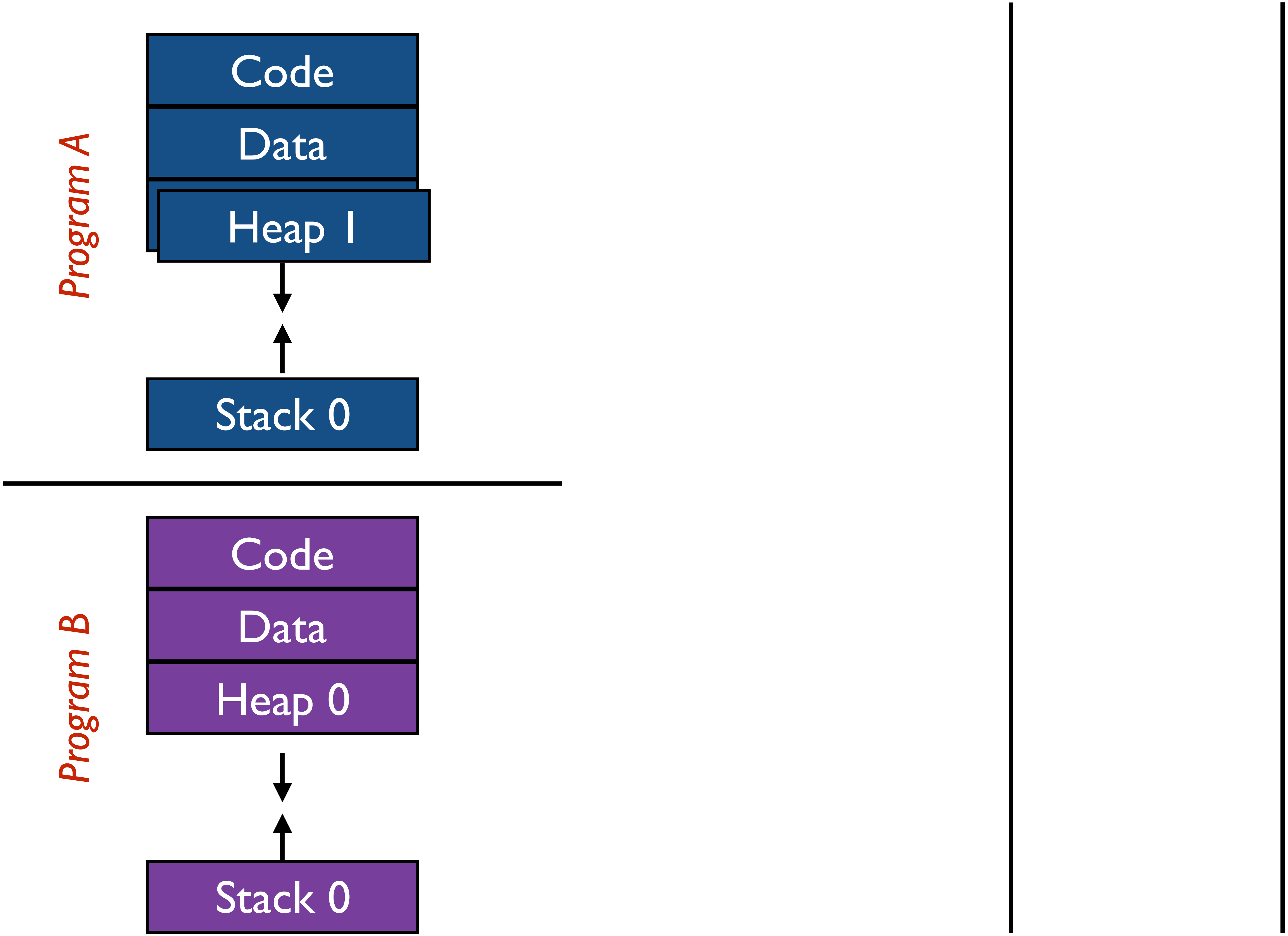
deja vu

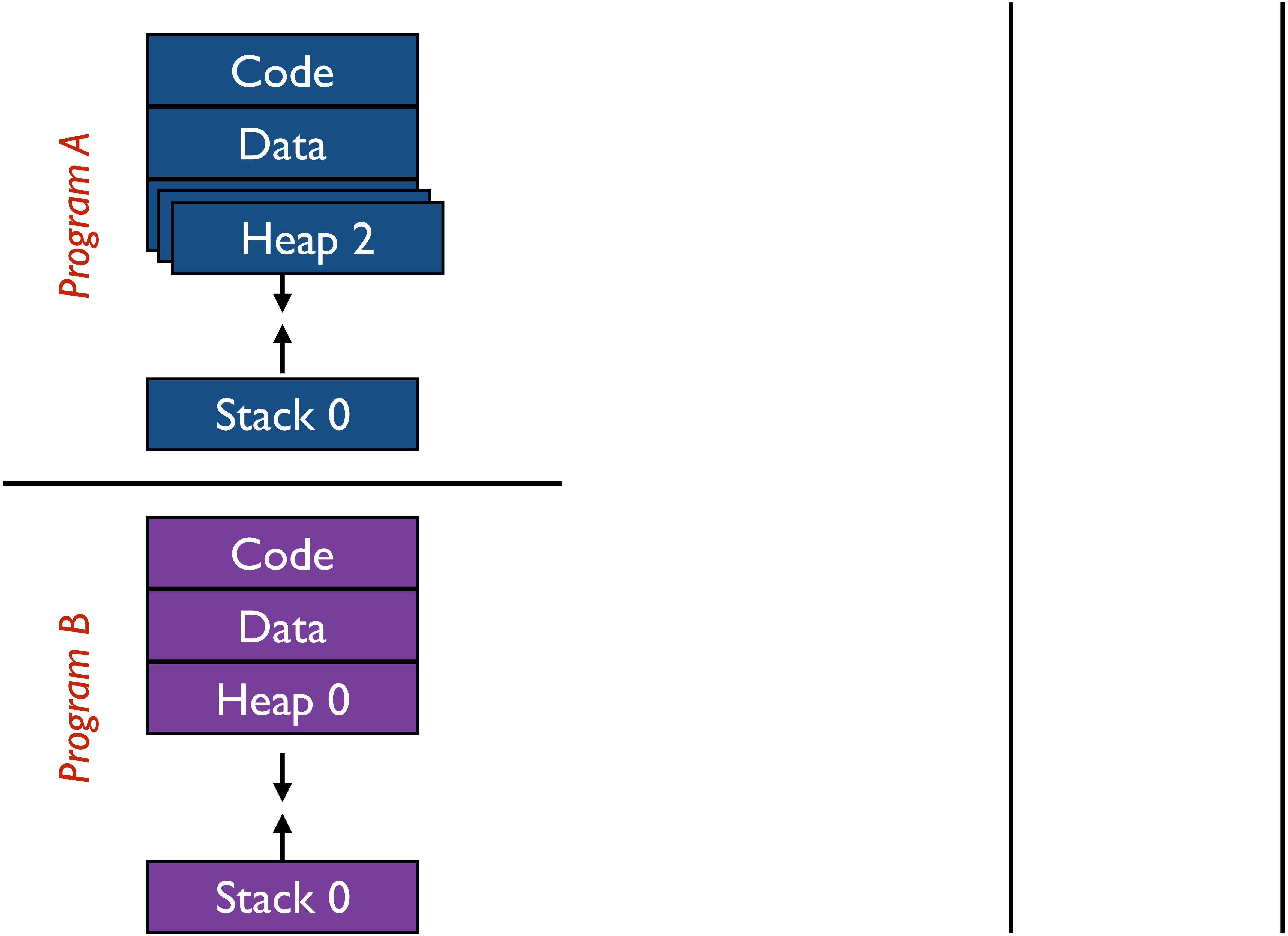
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0

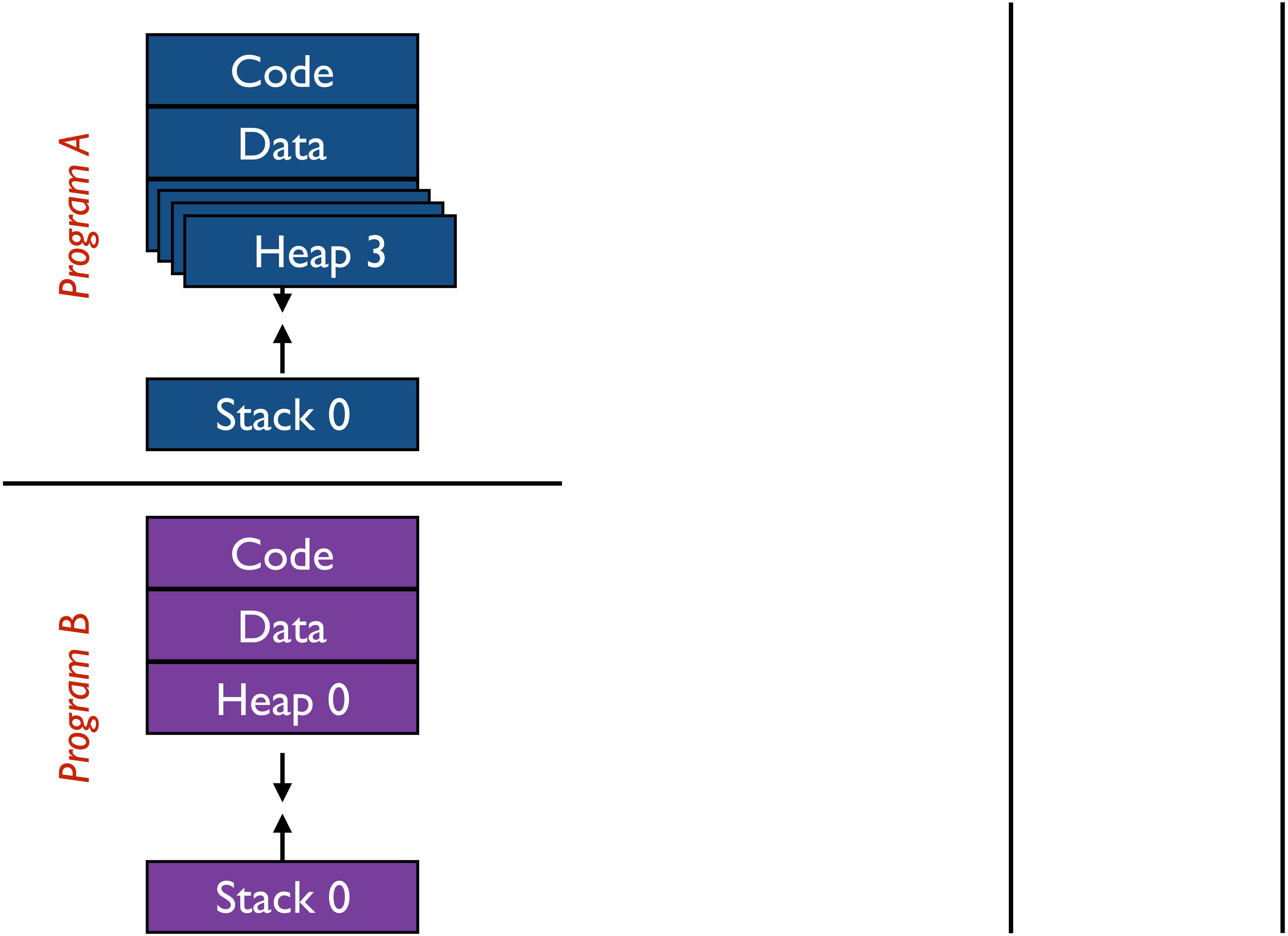
Paging


Program A
Code
Data
Heap 1
Stack 0
Program B
Code
Data
Heap 0
Stack 0

Paging

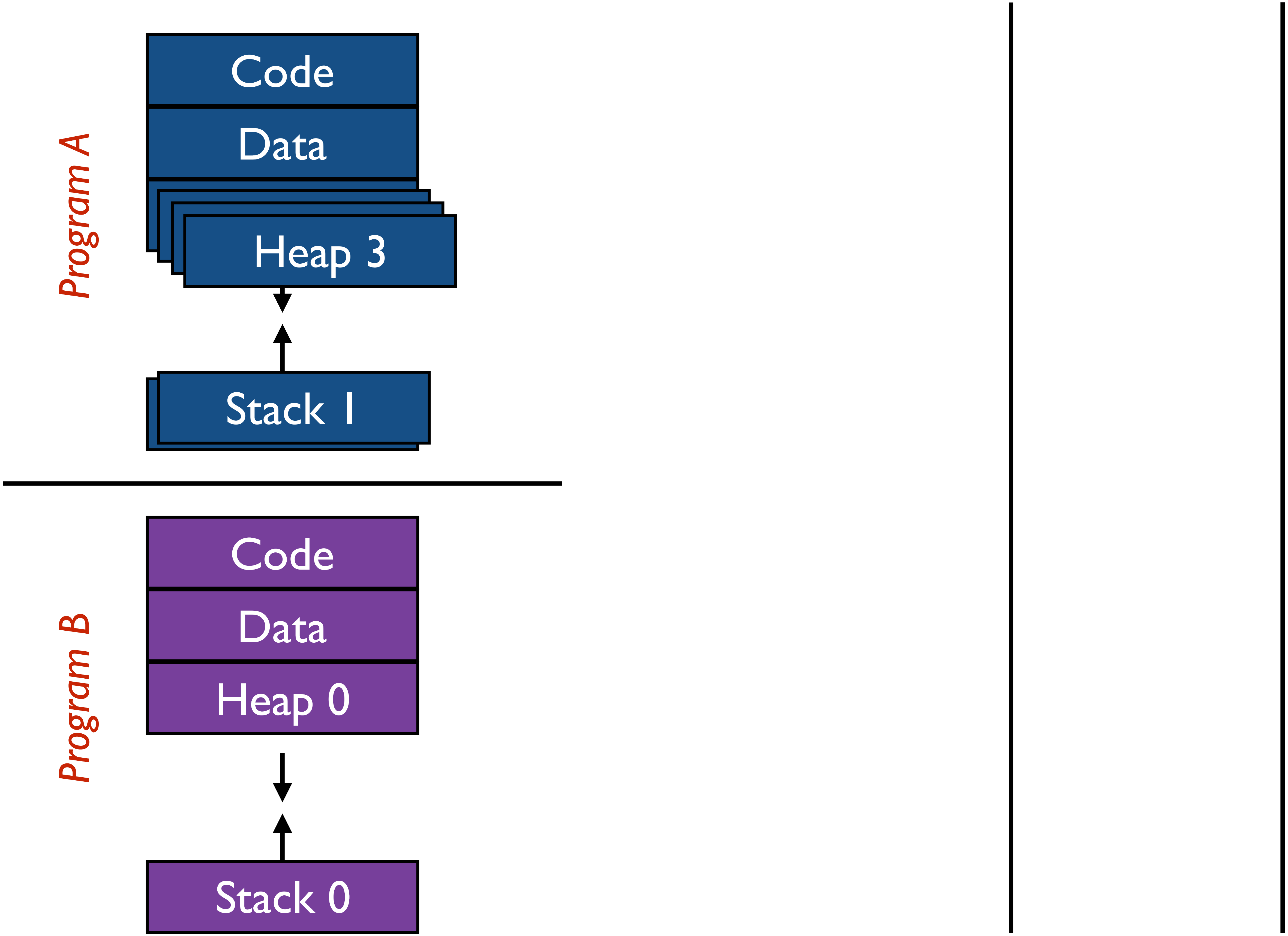

Program A
Code
Data
Heap 2
Stack 0
Program B
Code
Data
Heap 0
Stack 0

Paging

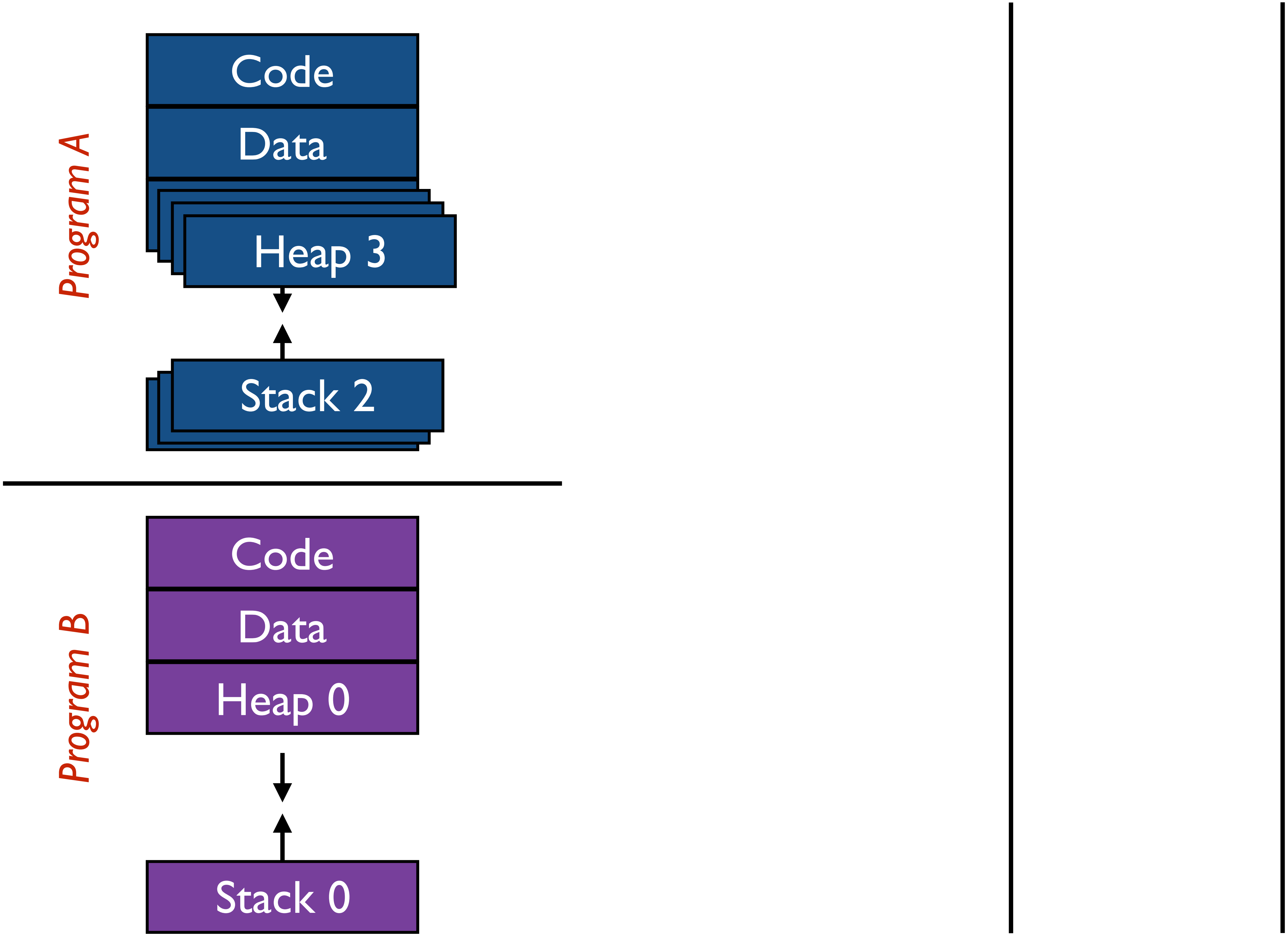


Program A
Code
Data
Heap 3
Stack 0
Program B
Code
Data
Heap 0
Stack 0

Paging

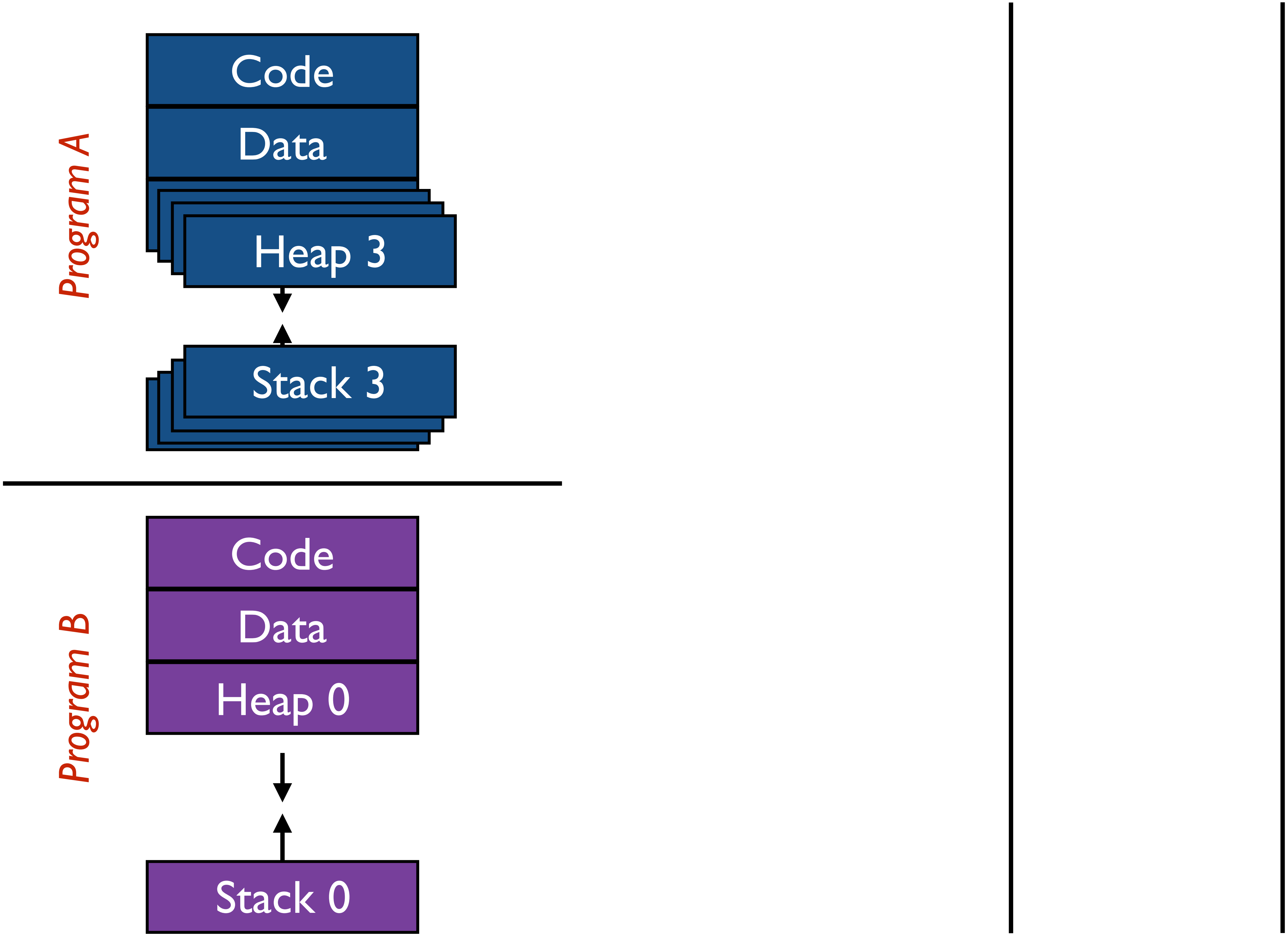

Program A
Code
Data
Heap 3
Stack 1
Program B
Code
Data
Heap 0
Stack 0

Paging

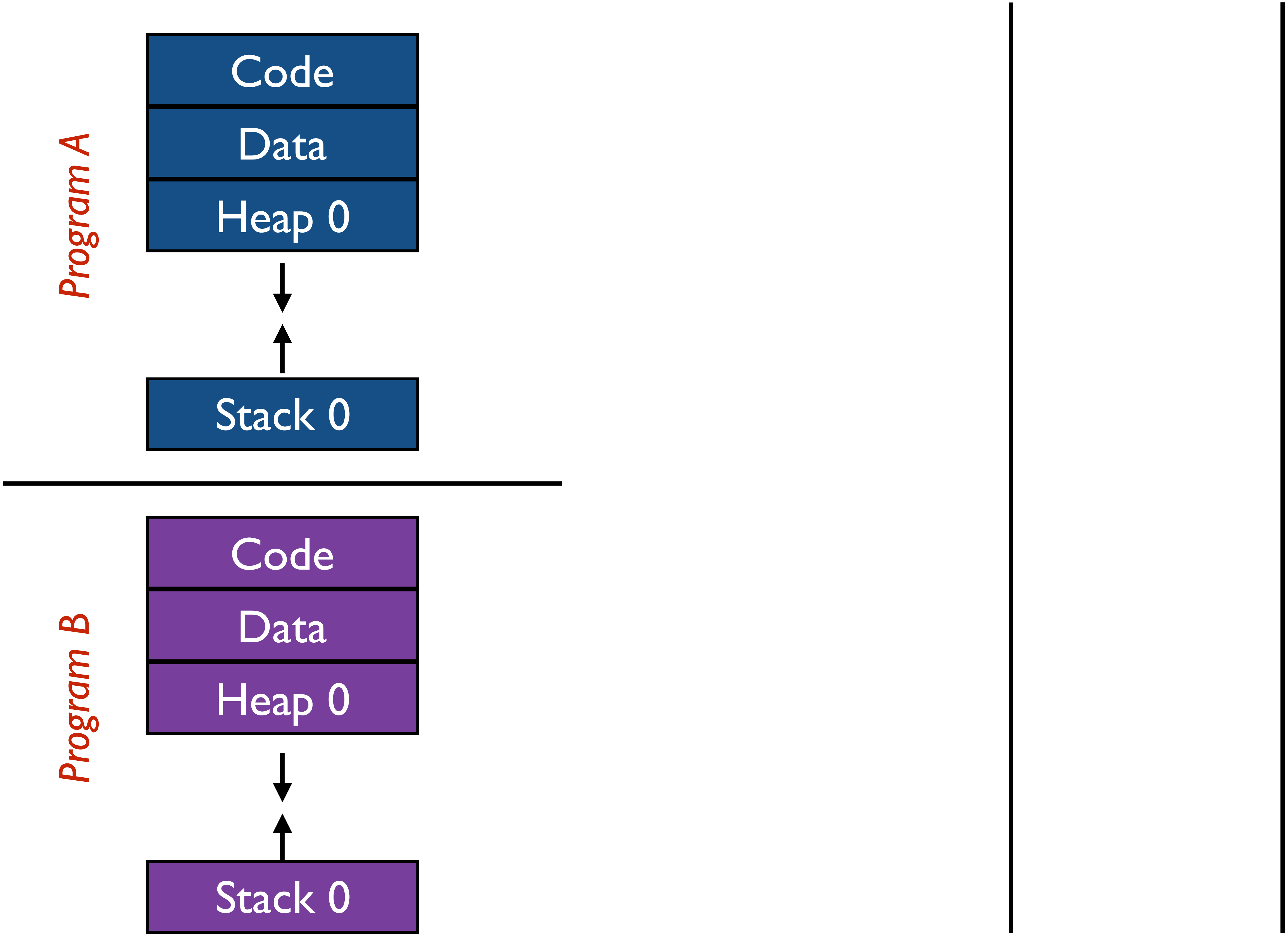


Program A
Code
Data
Heap 3
Stack 2
Program B
Code
Data
Heap 0
Stack 0

Paging


Program A
Code
Data
Heap 3
Stack 3
Program B
Code
Data
Heap 0
Stack 0

Paging



Program A
Code
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Heap 0
Stack 0
Program B
Code
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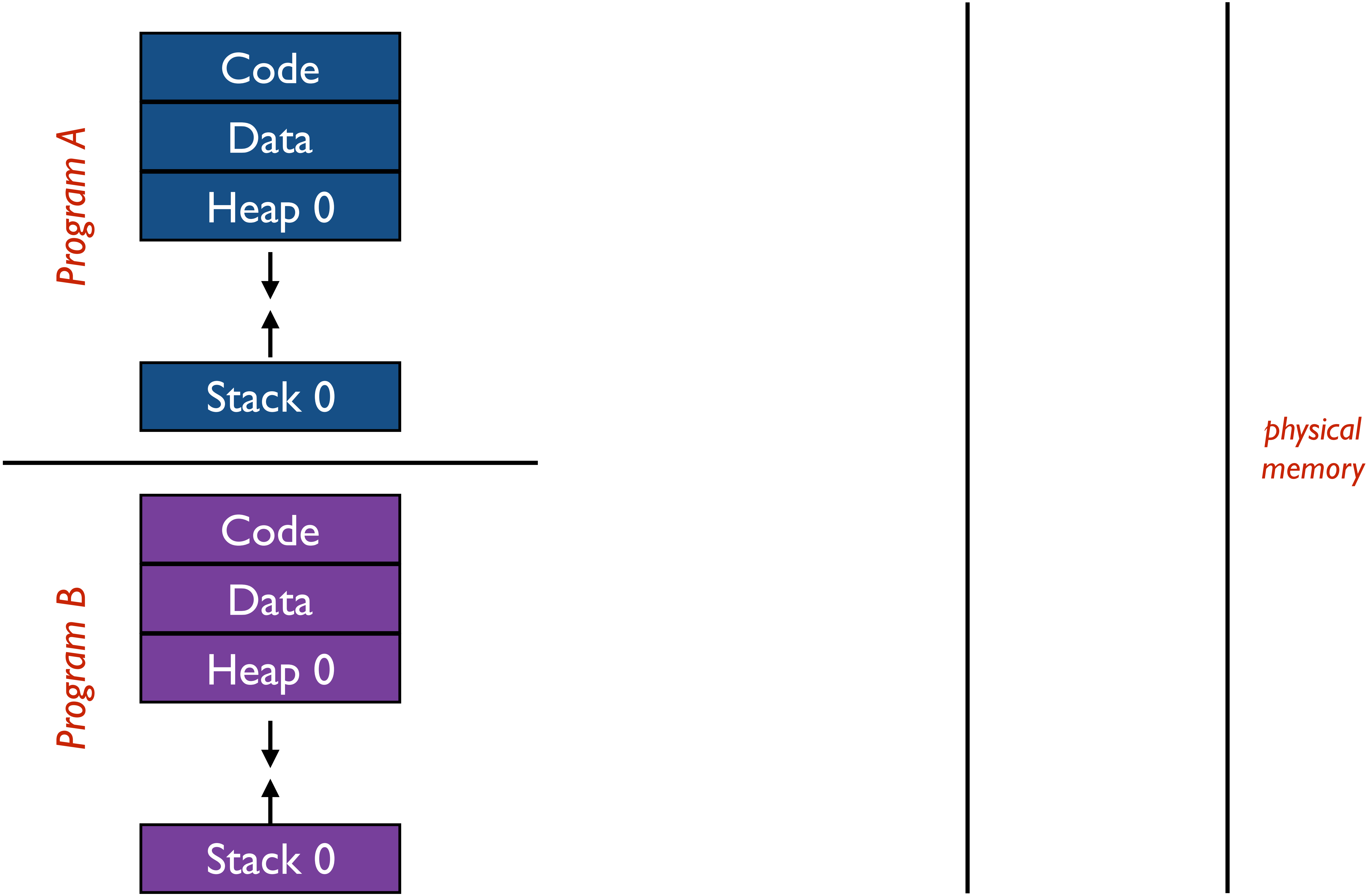
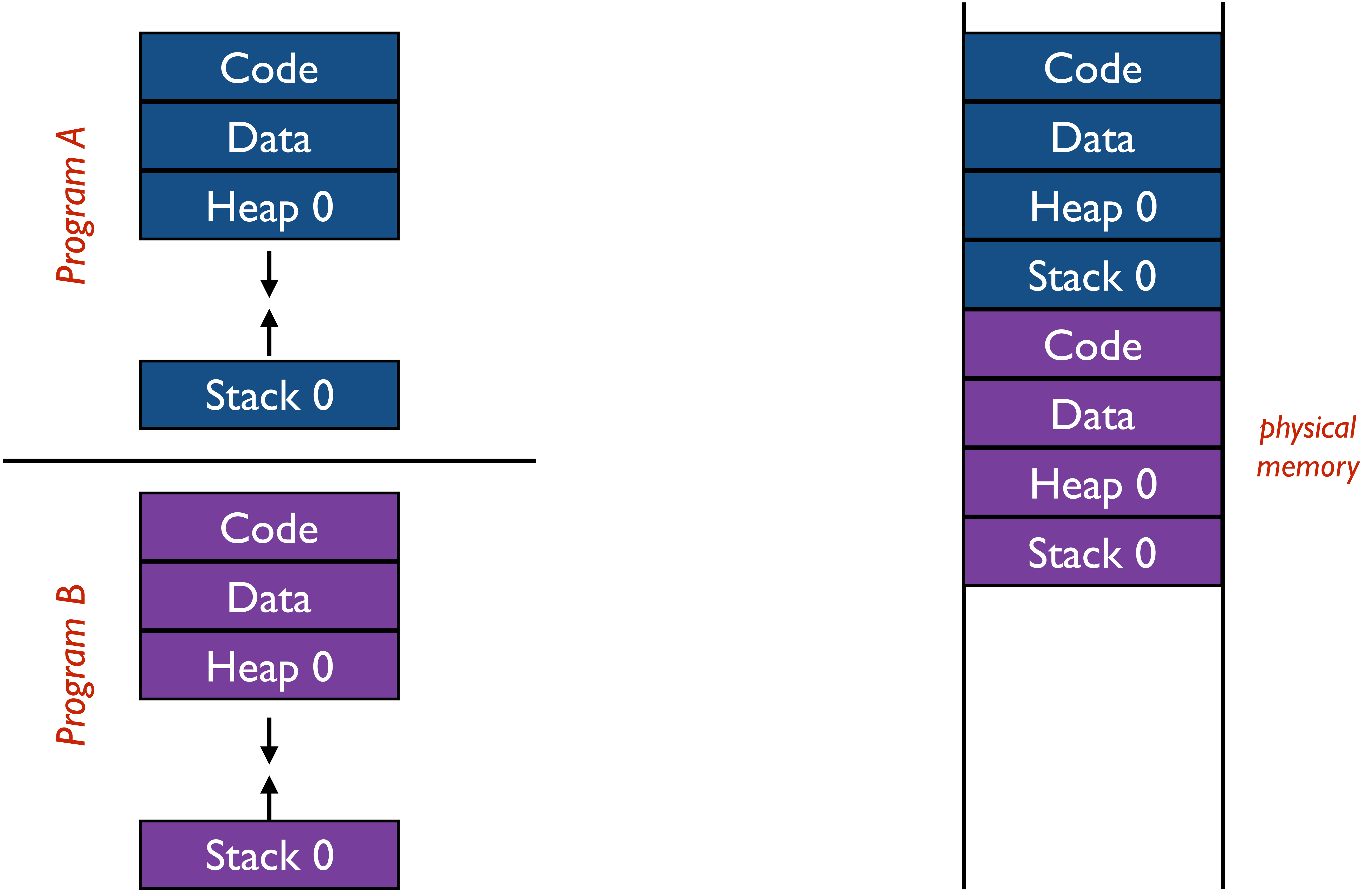
Heap 0
Stack 0

Paging



Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
physical memory

Paging


Program A
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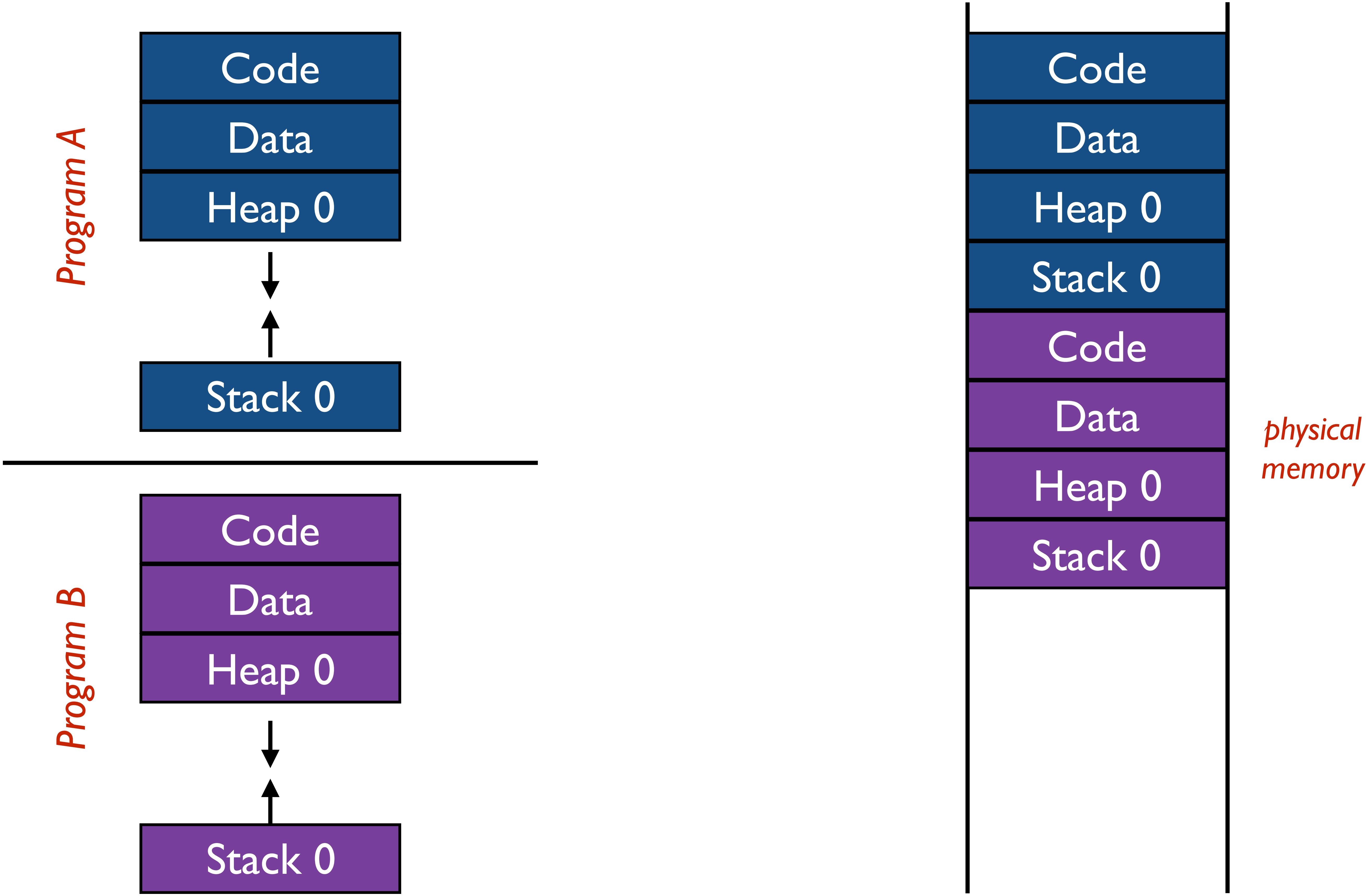
physical memory

Paging



Program A
Code
Data
Heap 0
Stack 0
Program B
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Data
Heap 0
Stack 0
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Heap 0
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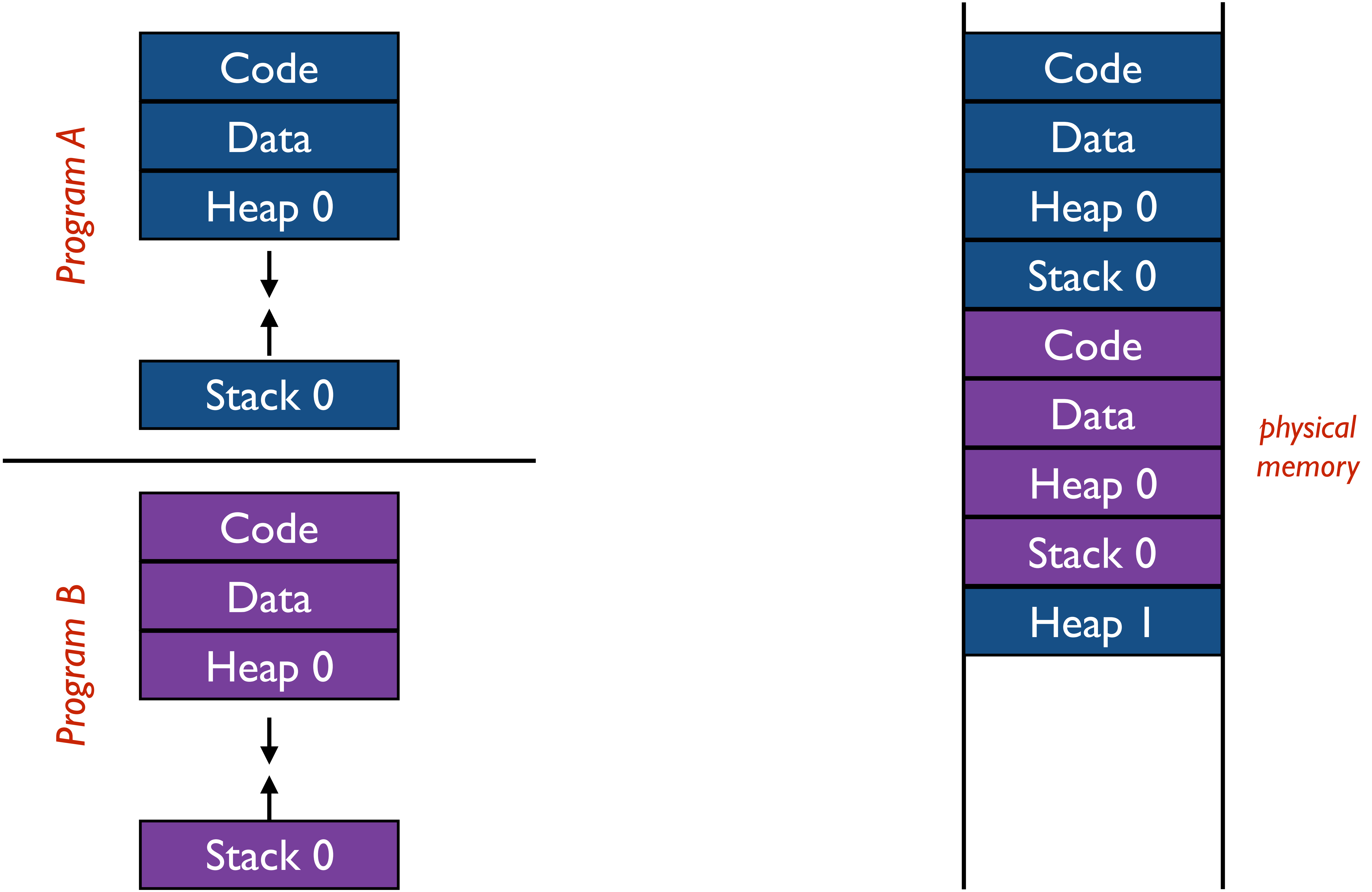
physical memory

Paging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Data
Heap 0
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Program B
Code
Data
Heap 0
Stack 0
Code
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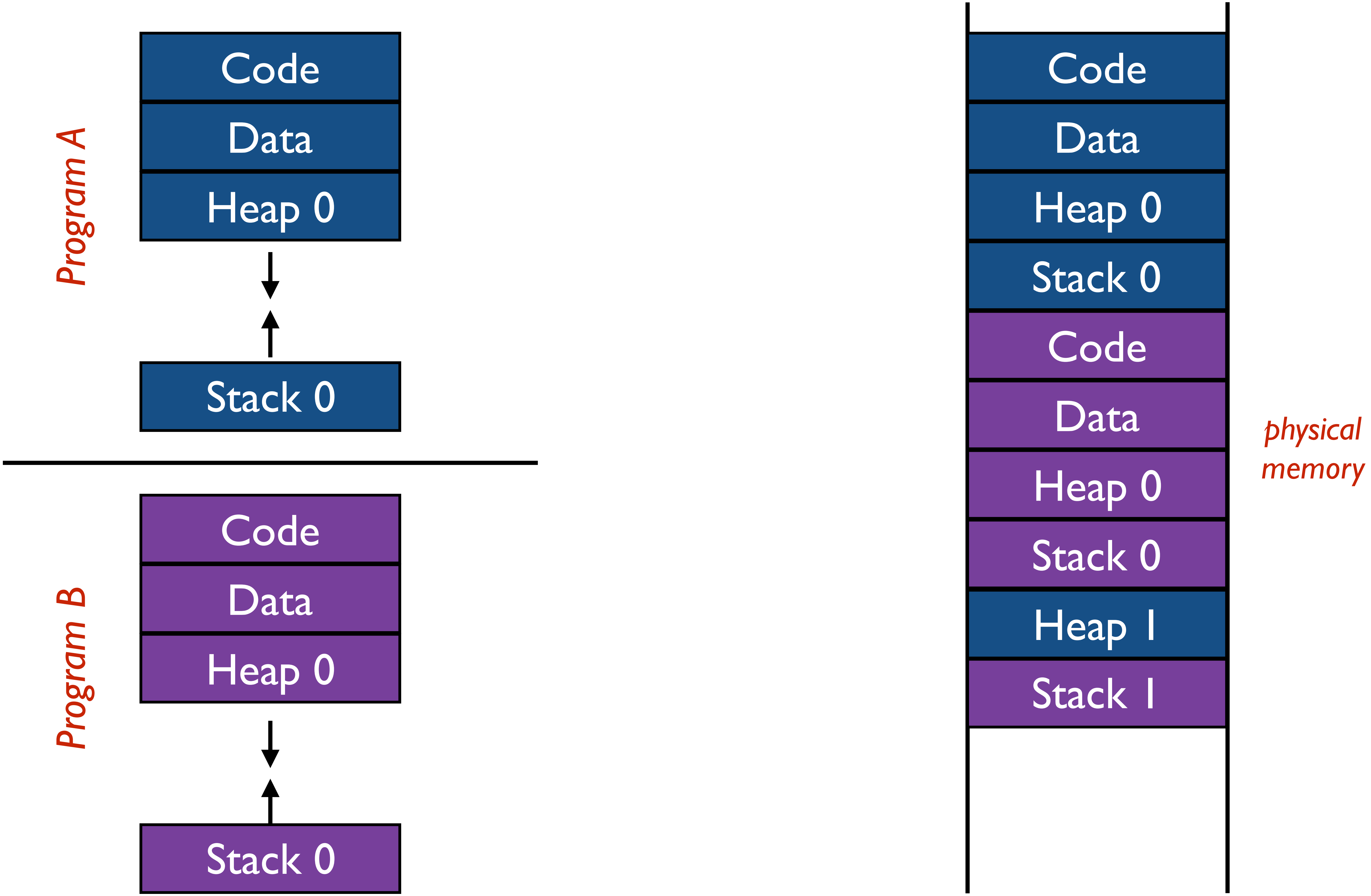
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 1
physical memory

Paging



Program A
Code
Data
Heap 0
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Program B
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Code
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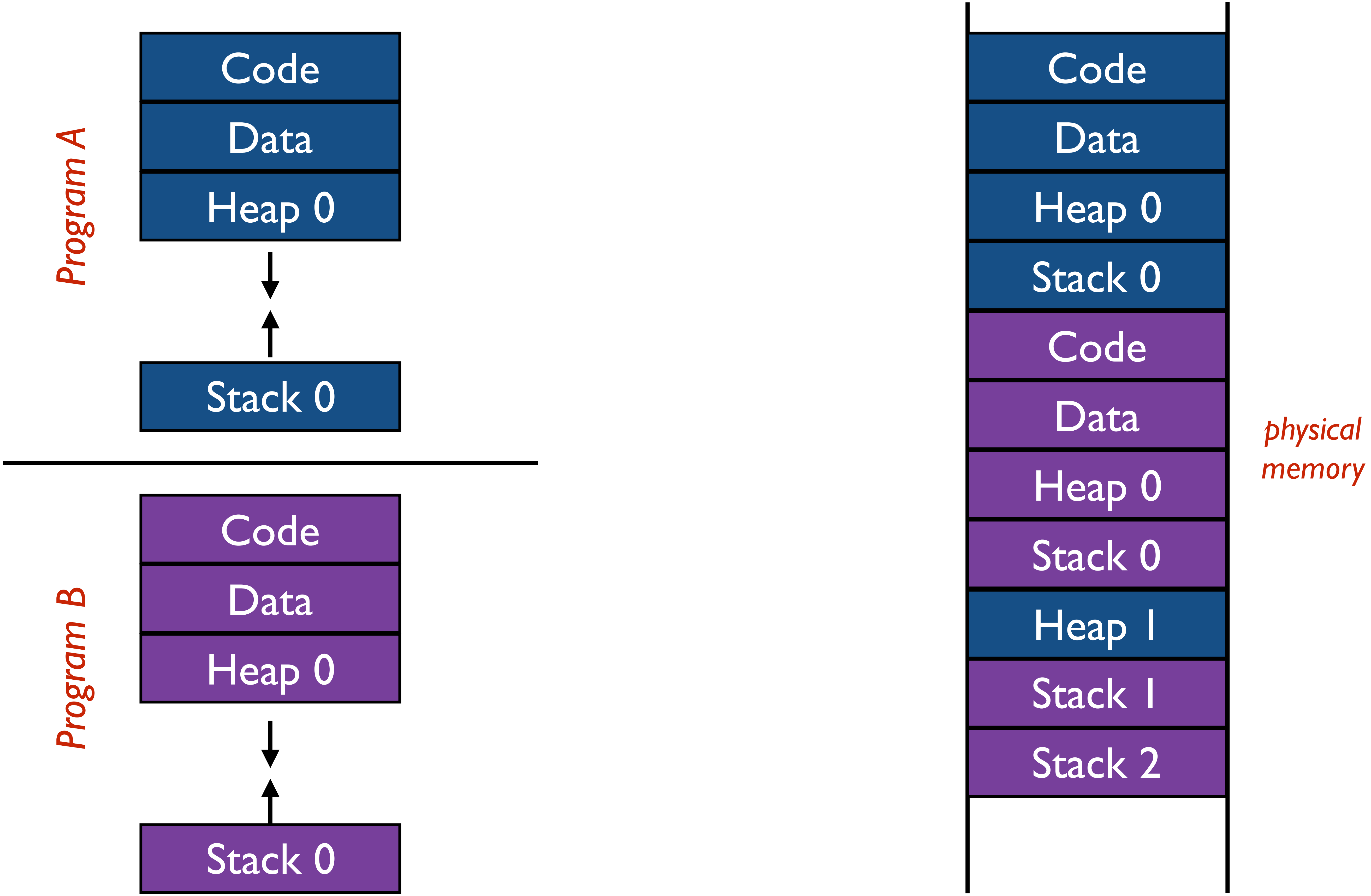
Data
Heap 0
Stack 0
Heap 1
Stack 1
physical memory

Paging



Program A
Code
Data
Heap 0
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Program B
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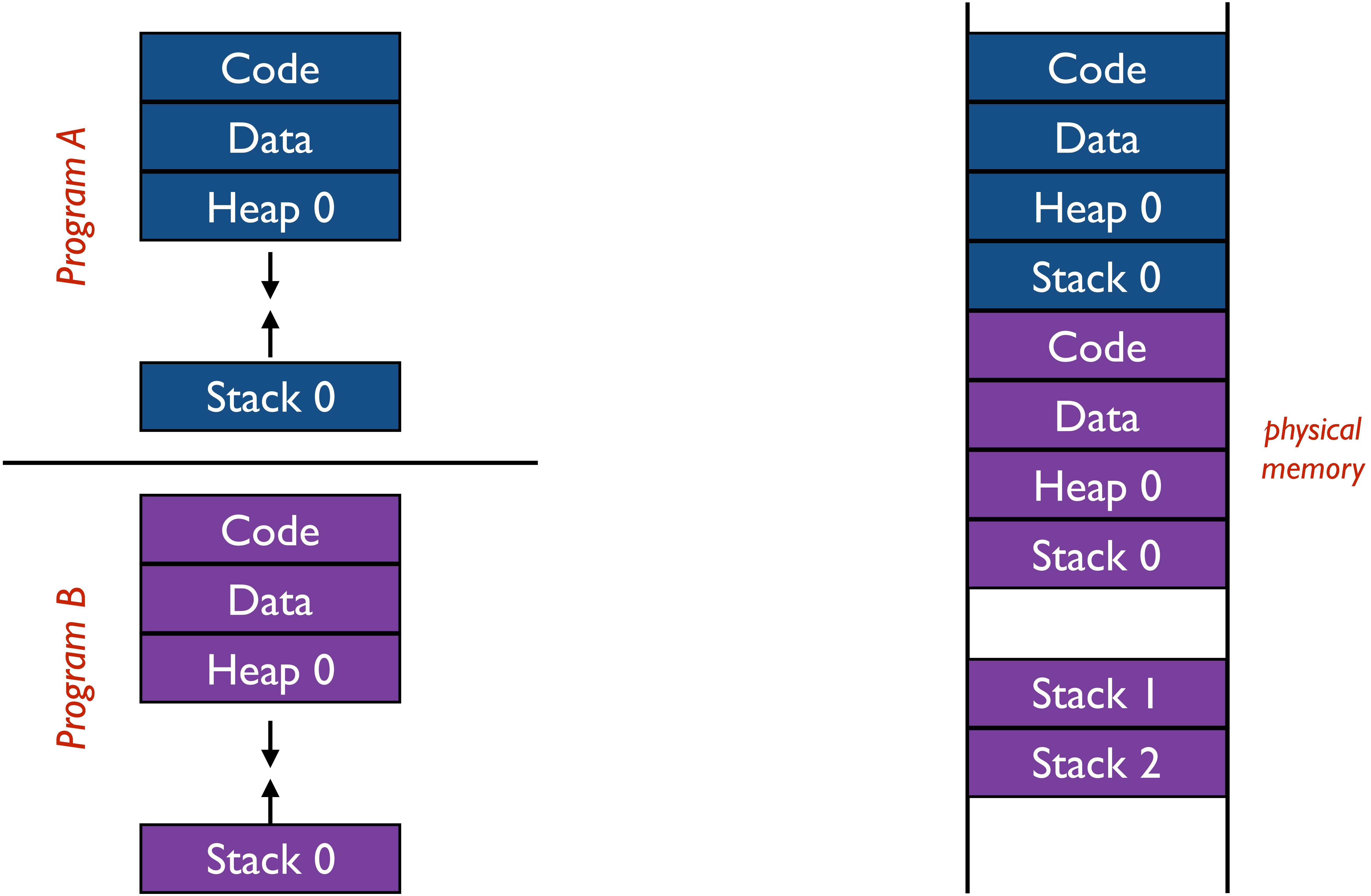
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 1
Stack 1
Stack 2
physical memory

Paging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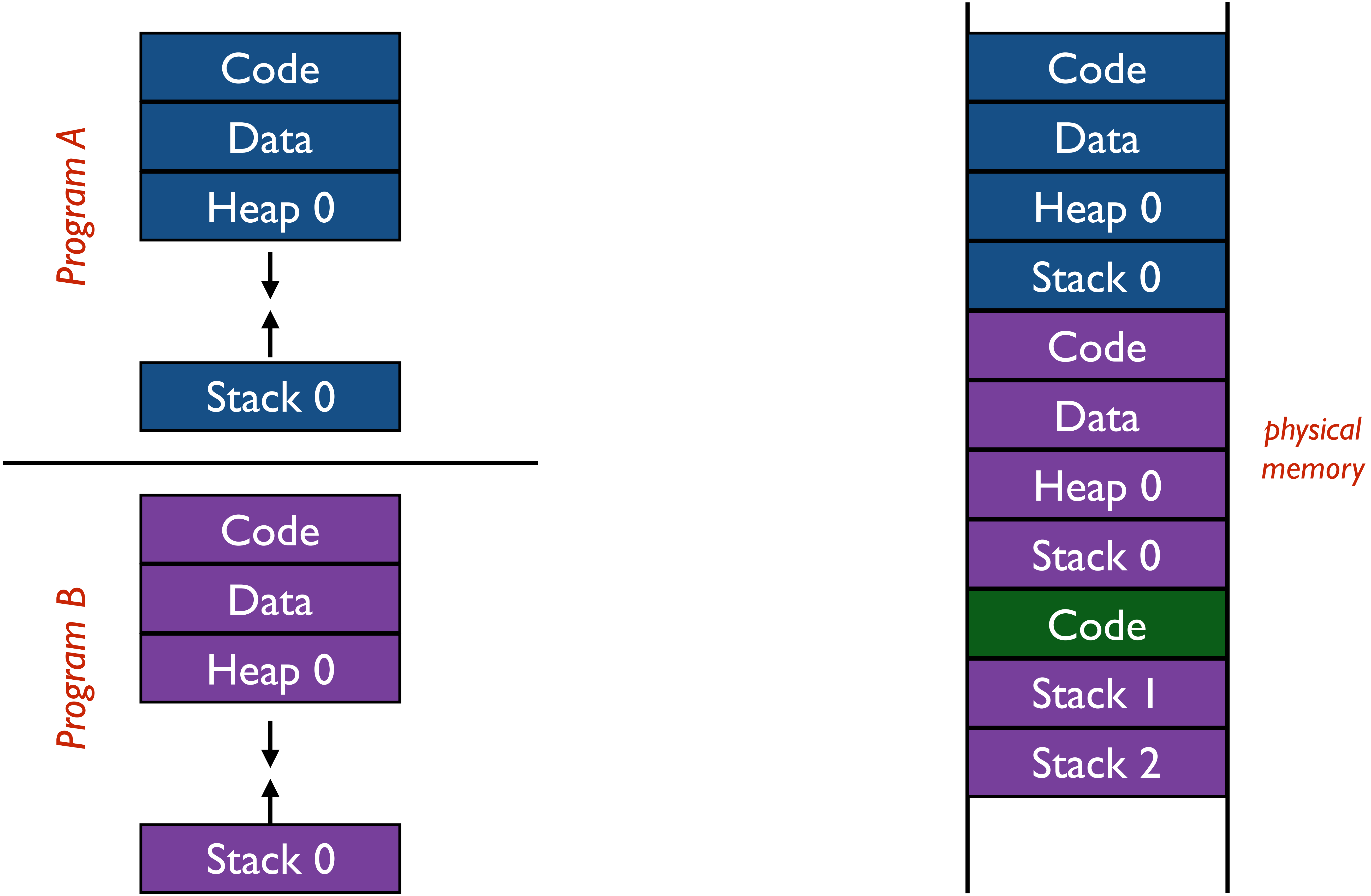
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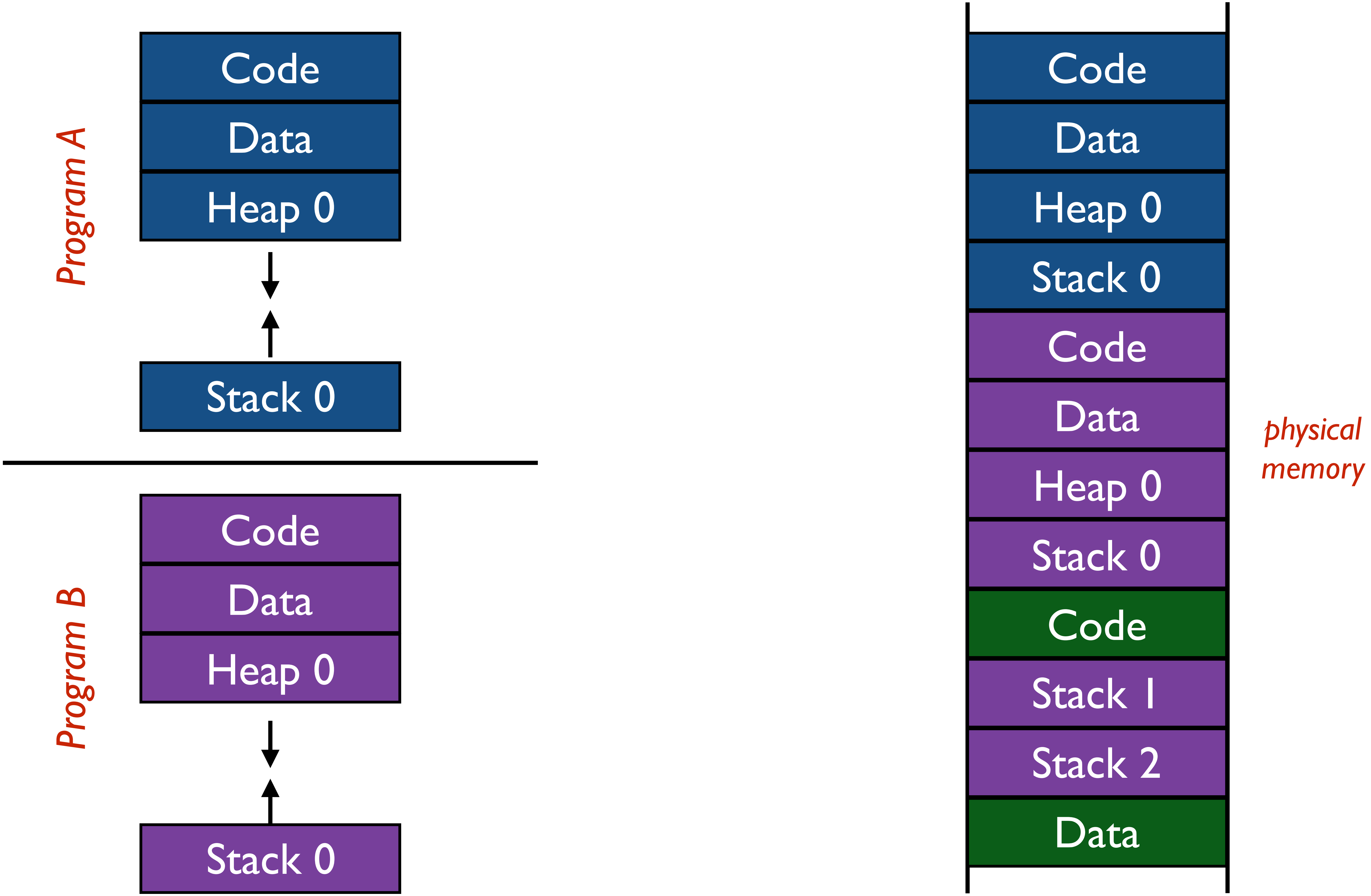
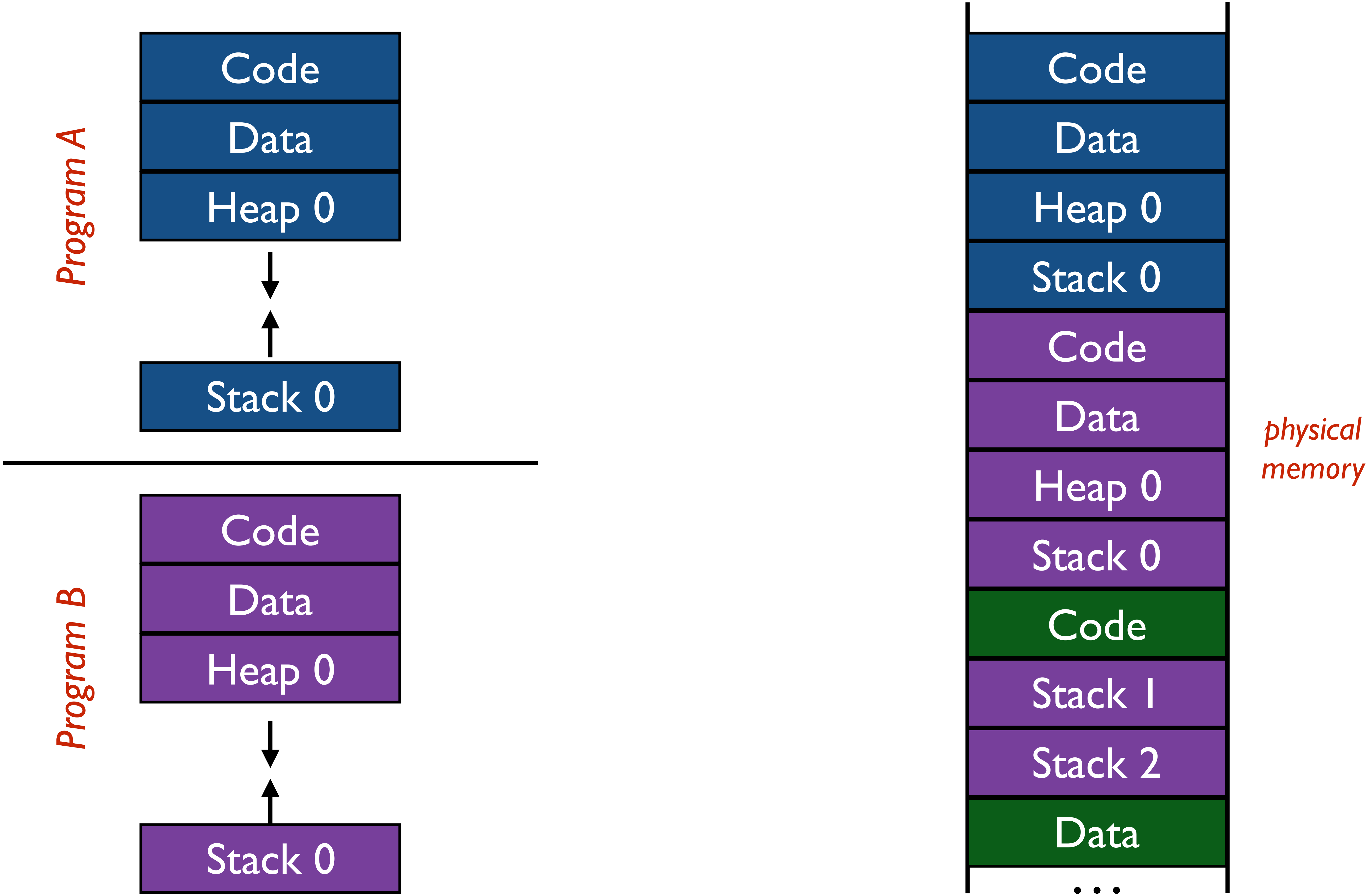
Stack 2
physical memory

Paging

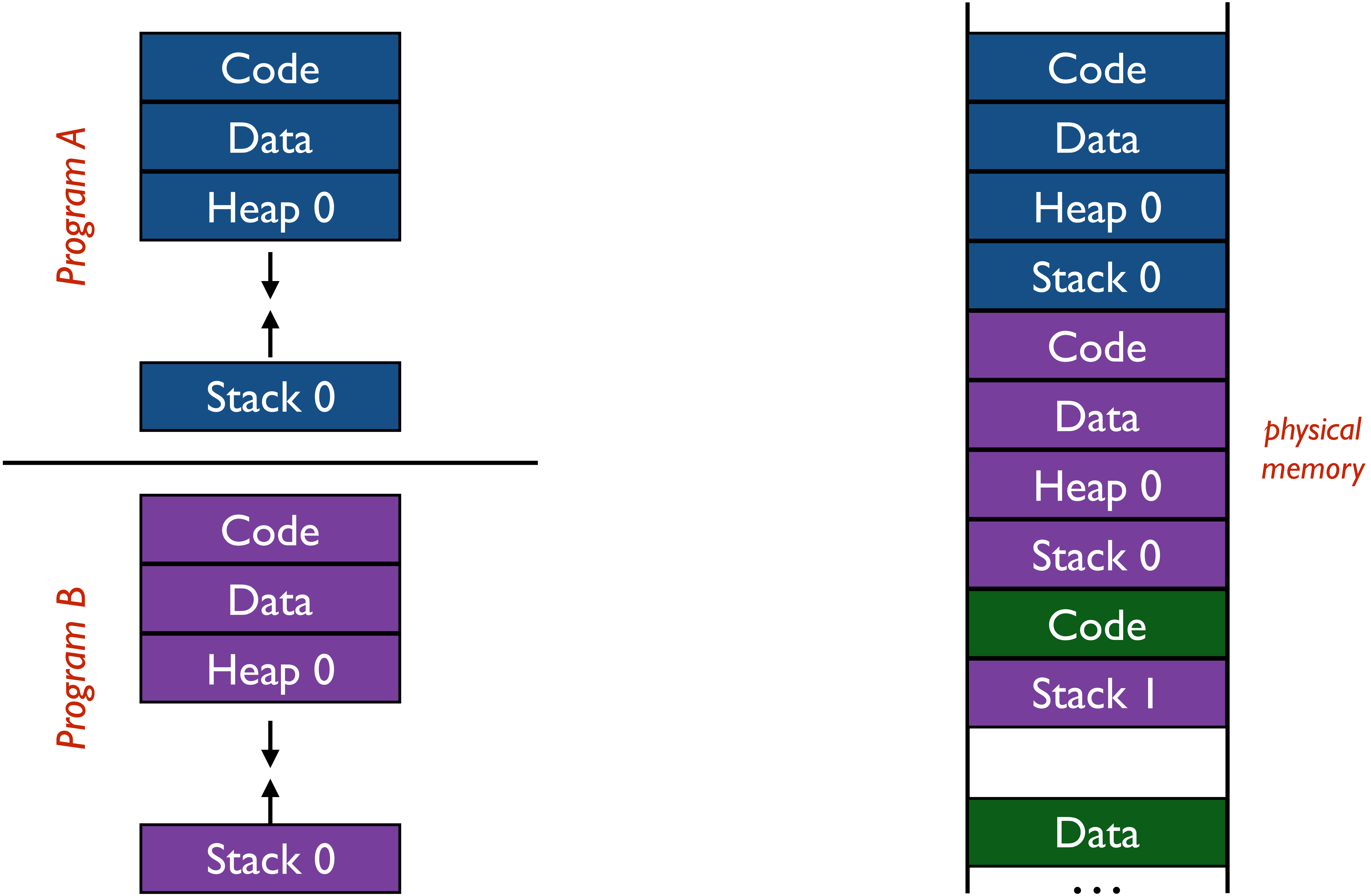


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Stack 1
Stack 2
Data
physical memory

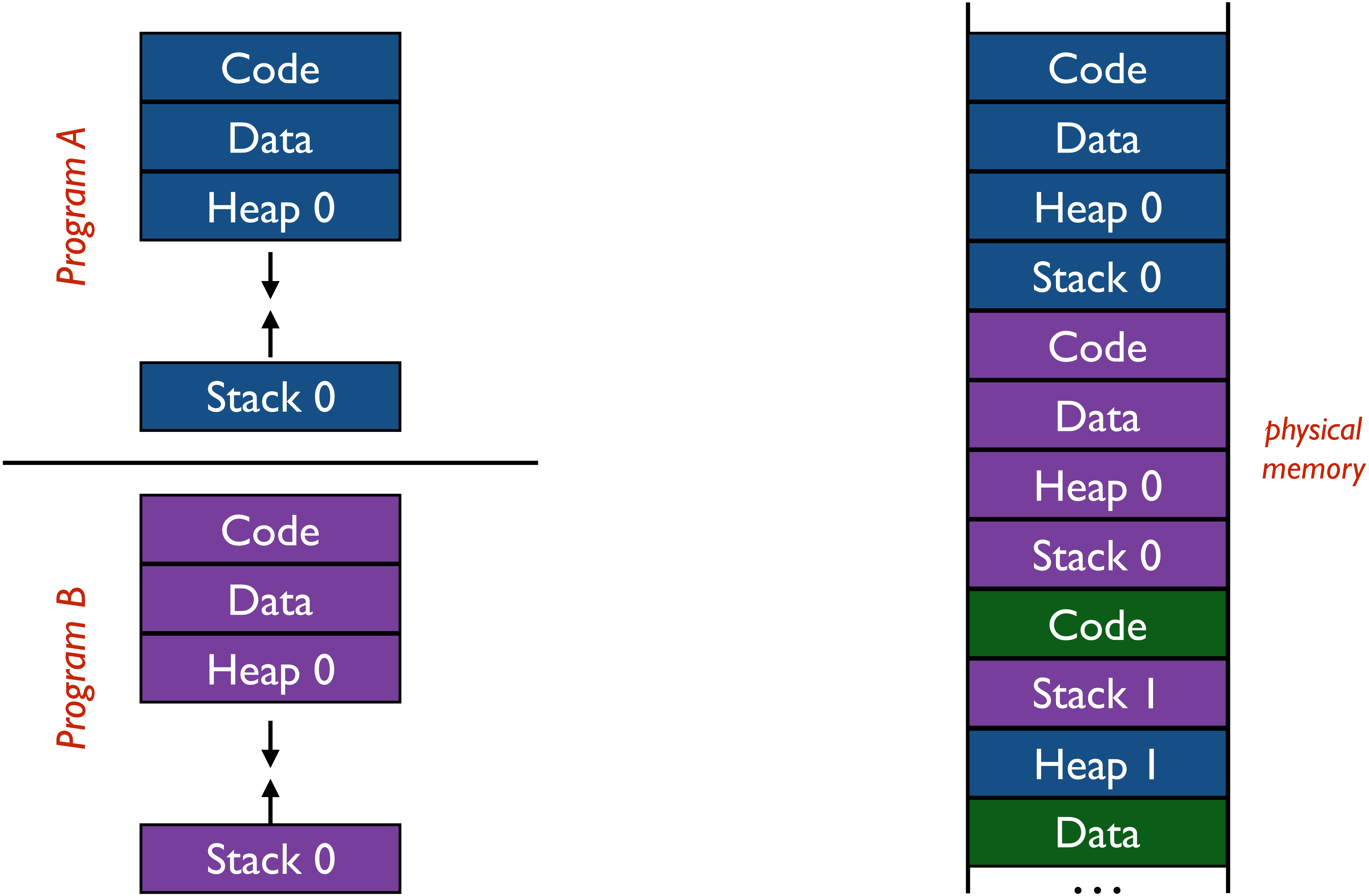
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Stack 1
Stack 2
Data
...
physical memory

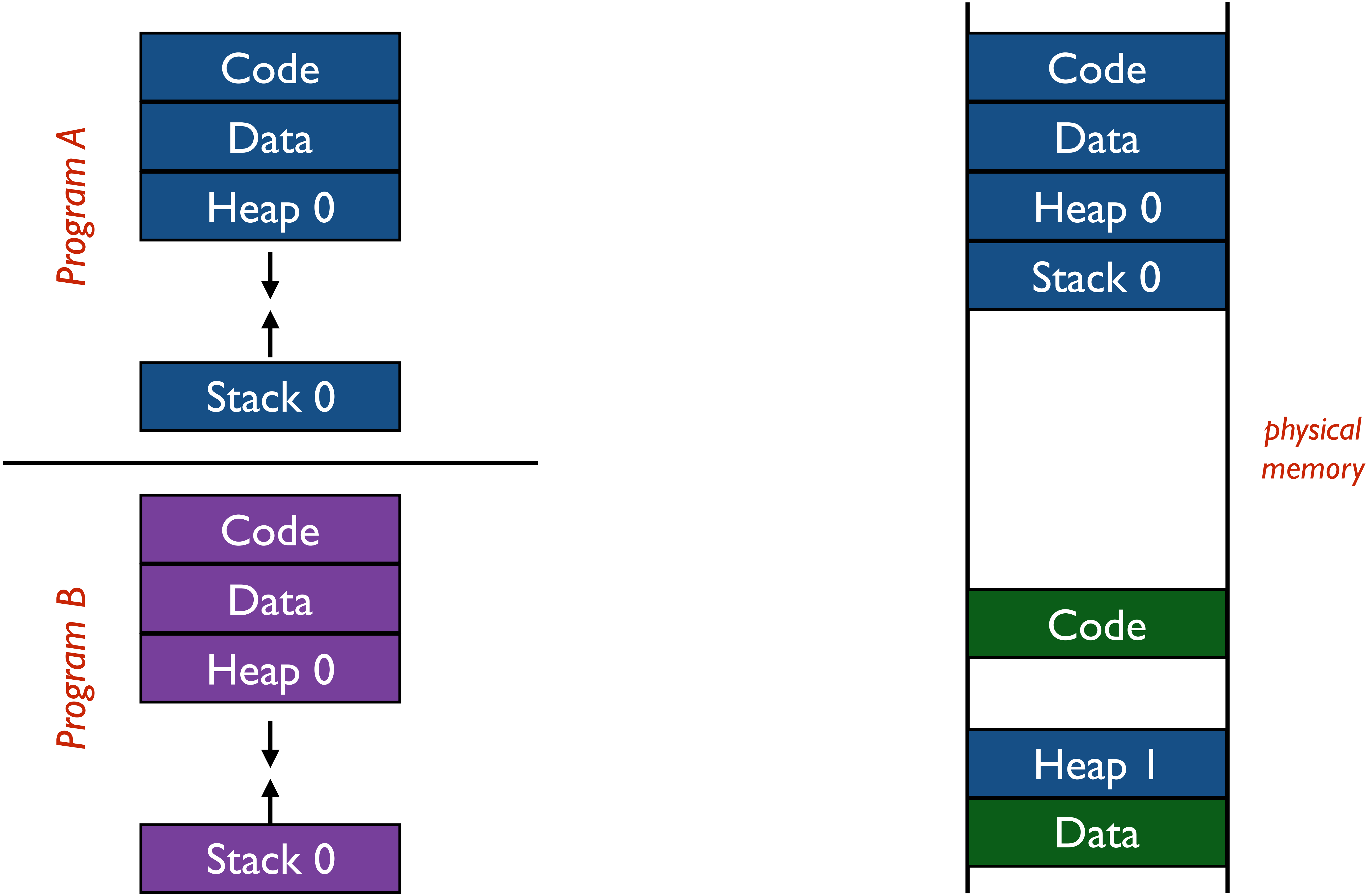
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Stack 1
Data
. . .
physical memory

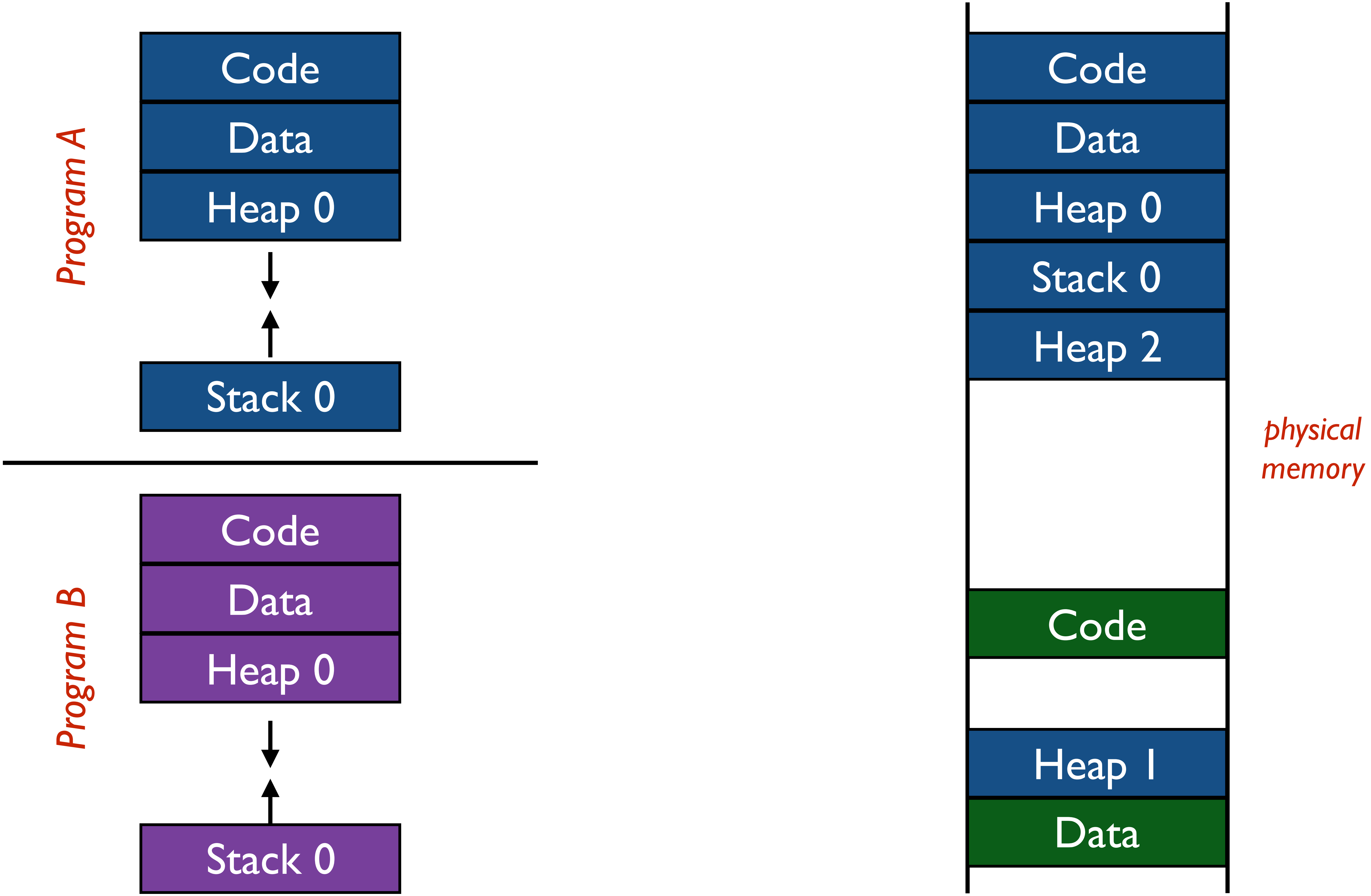
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Code
Stack 1
Heap 1
Data
. . .
physical memory

Paging

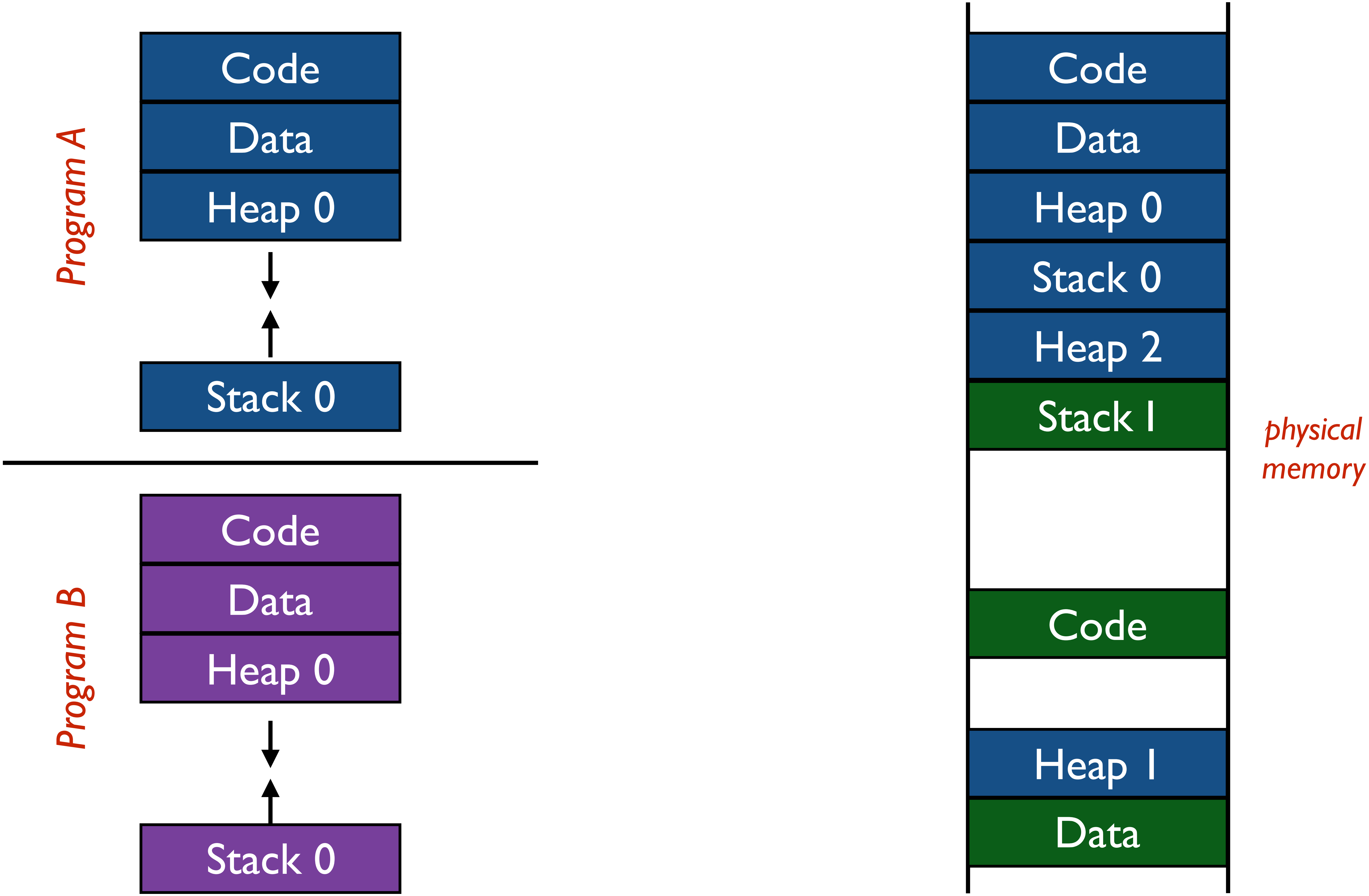

Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
physical memory
Code
Heap 1
Data

Paging

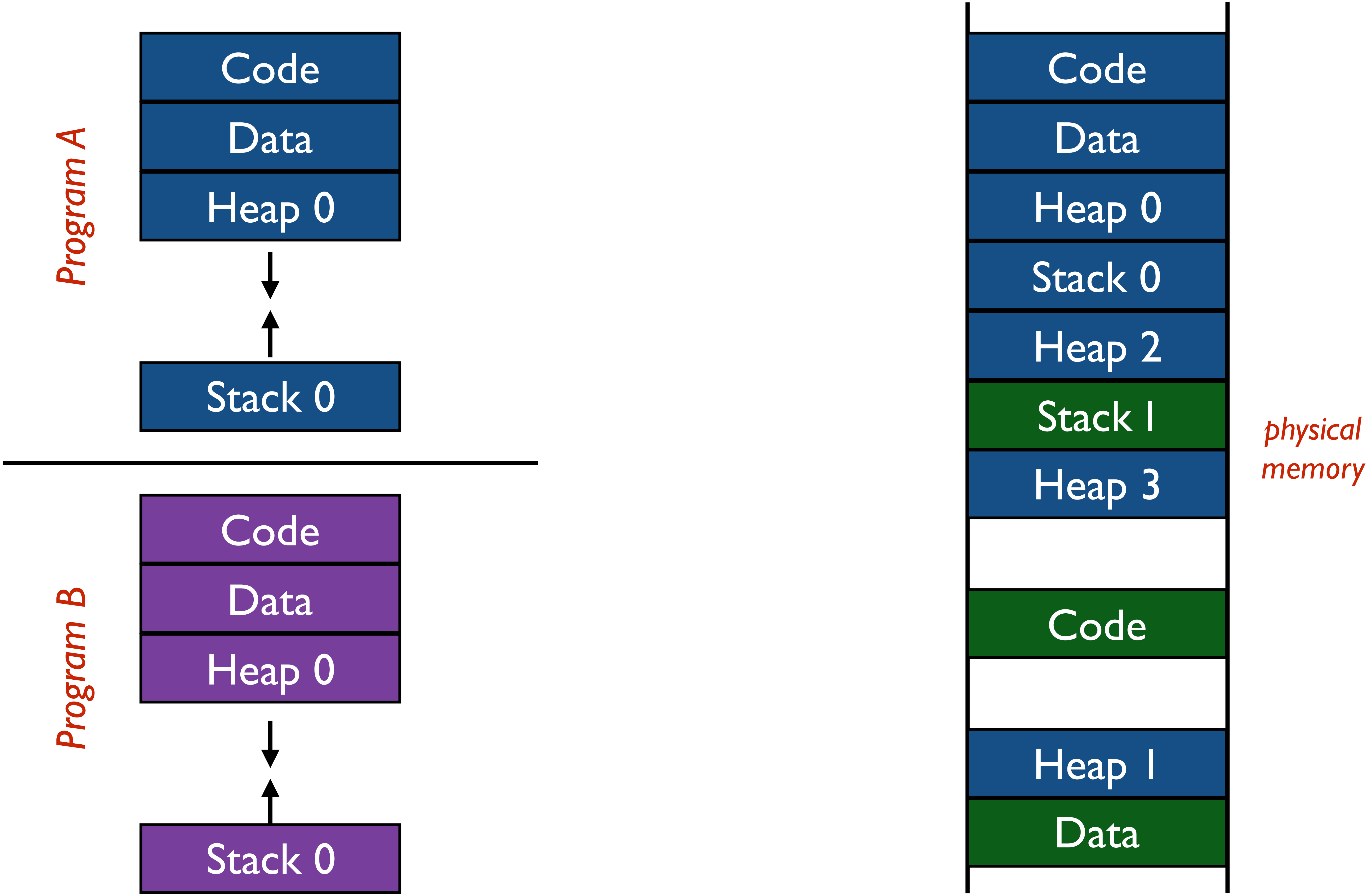


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 2
physical memory
Code
Heap 1
Data

Paging

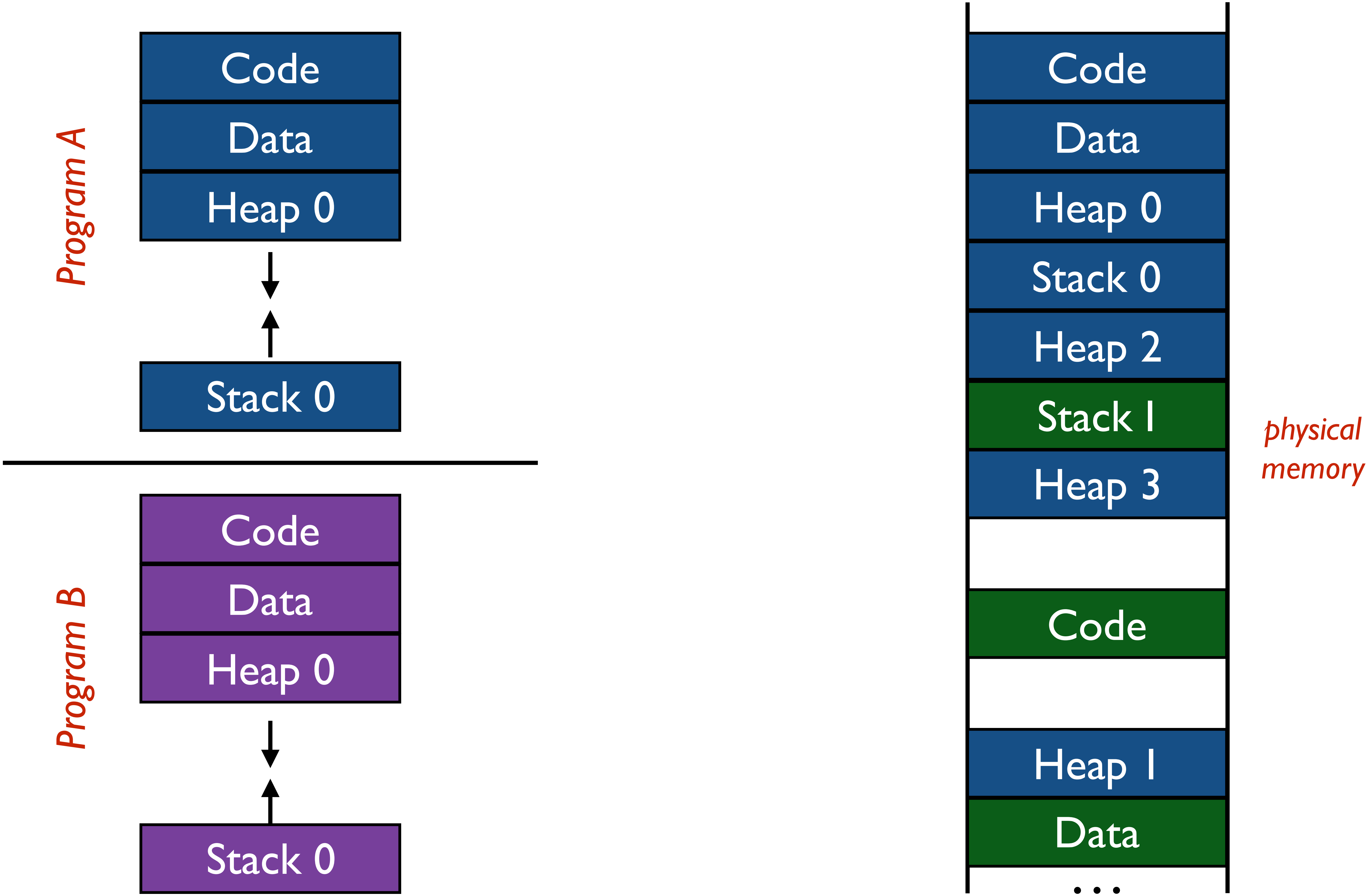

Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 2
Stack 1
Code
Heap 1
Data
physical memory

Paging

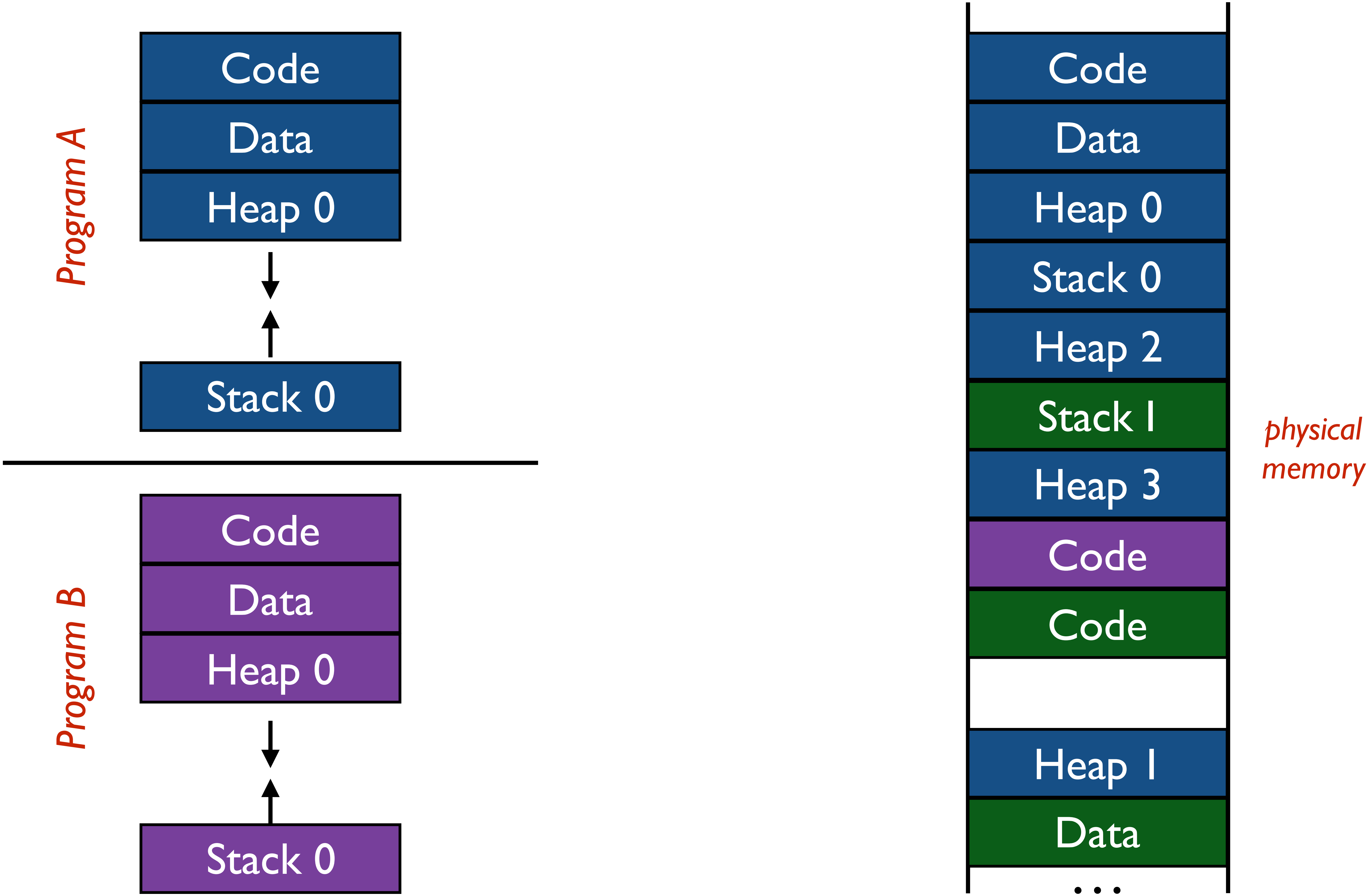


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 2
Stack 1
Heap 3
Code
Heap 1
Data
physical memory

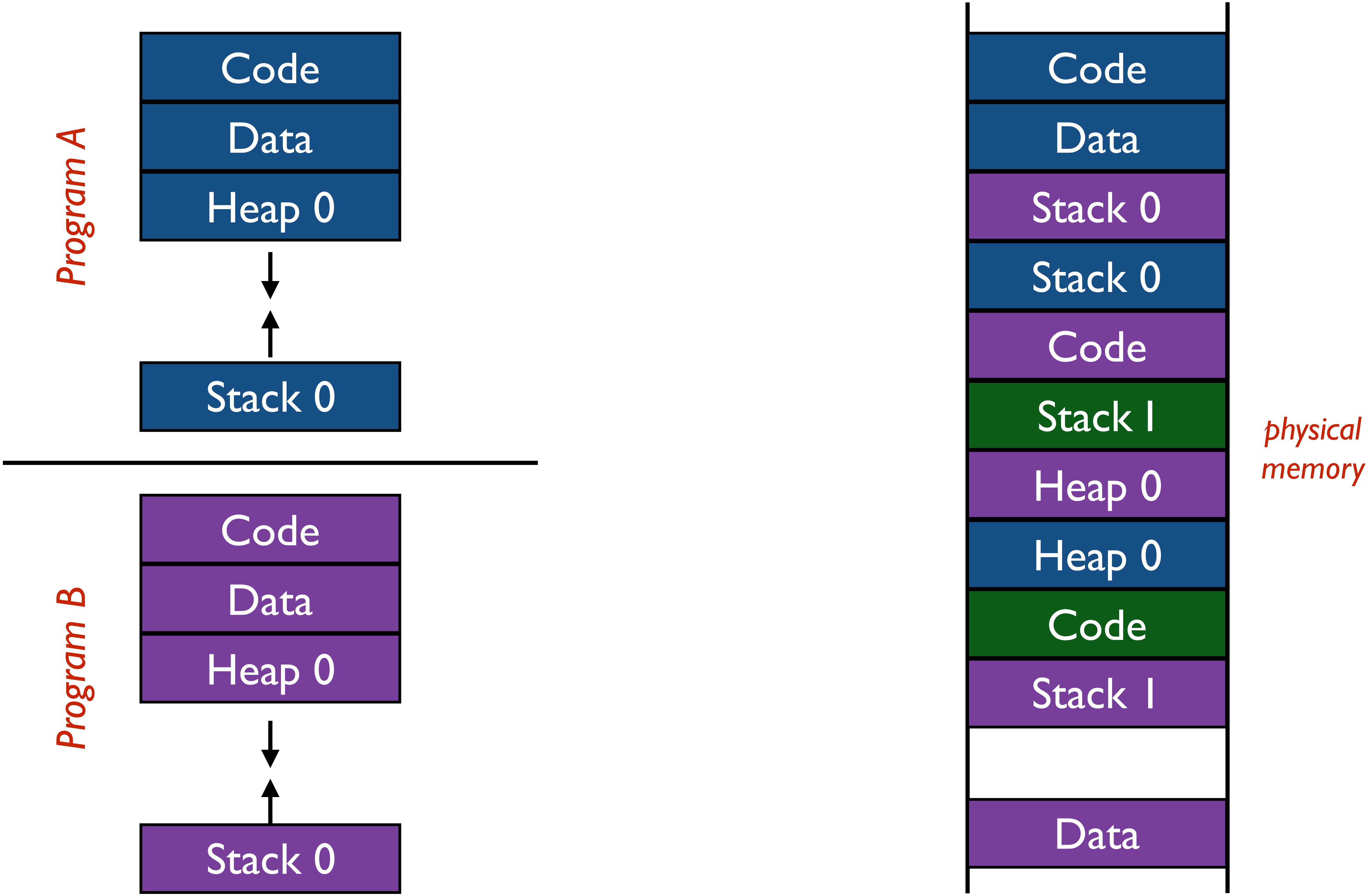
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 2
Stack 1
Heap 3
Code
Heap 1
Data
...
physical memory

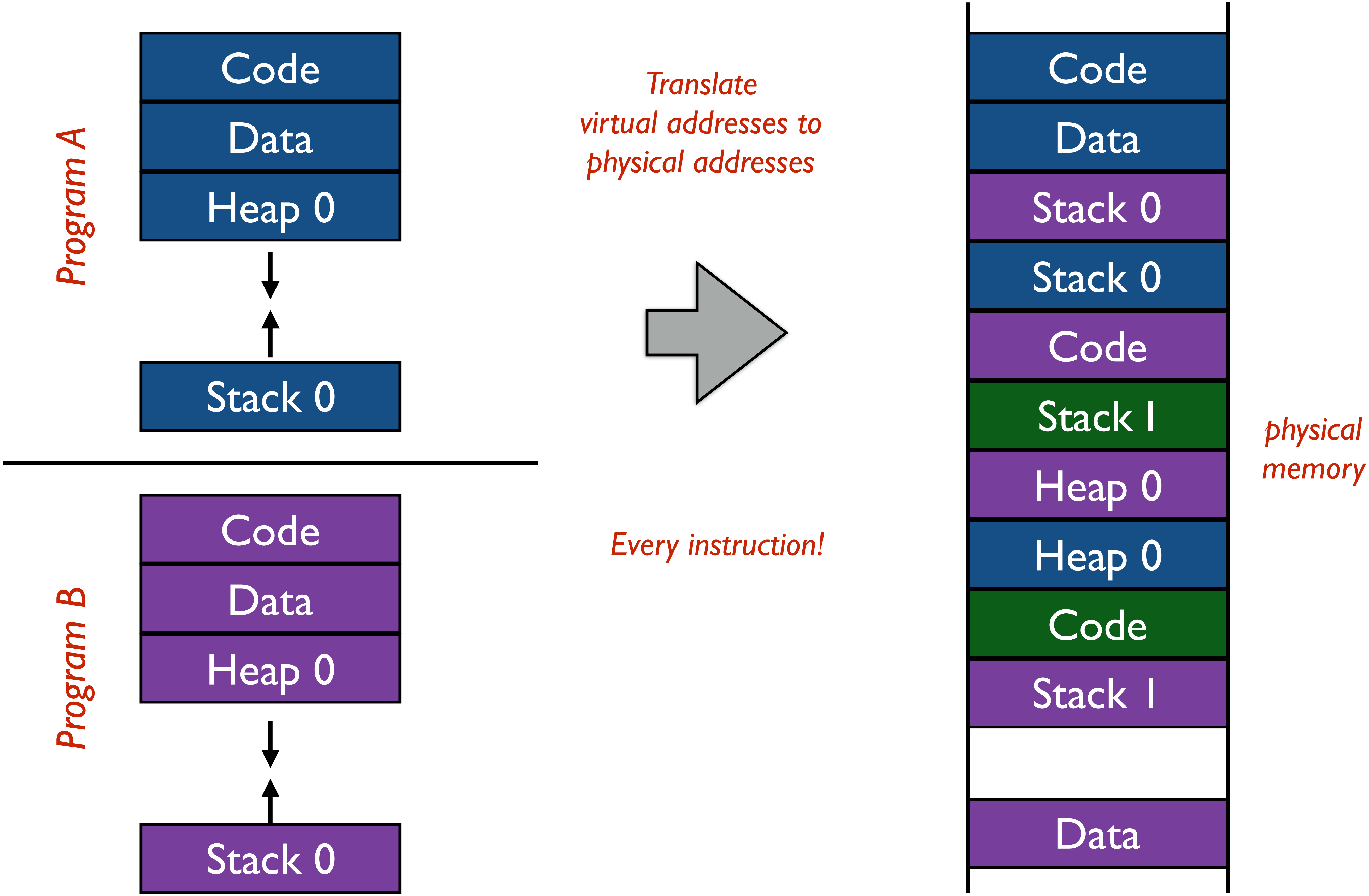
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Heap 0
Stack 0
Heap 2
Stack 1
Heap 3
Code
Code
Heap 1
Data
. . .
physical memory

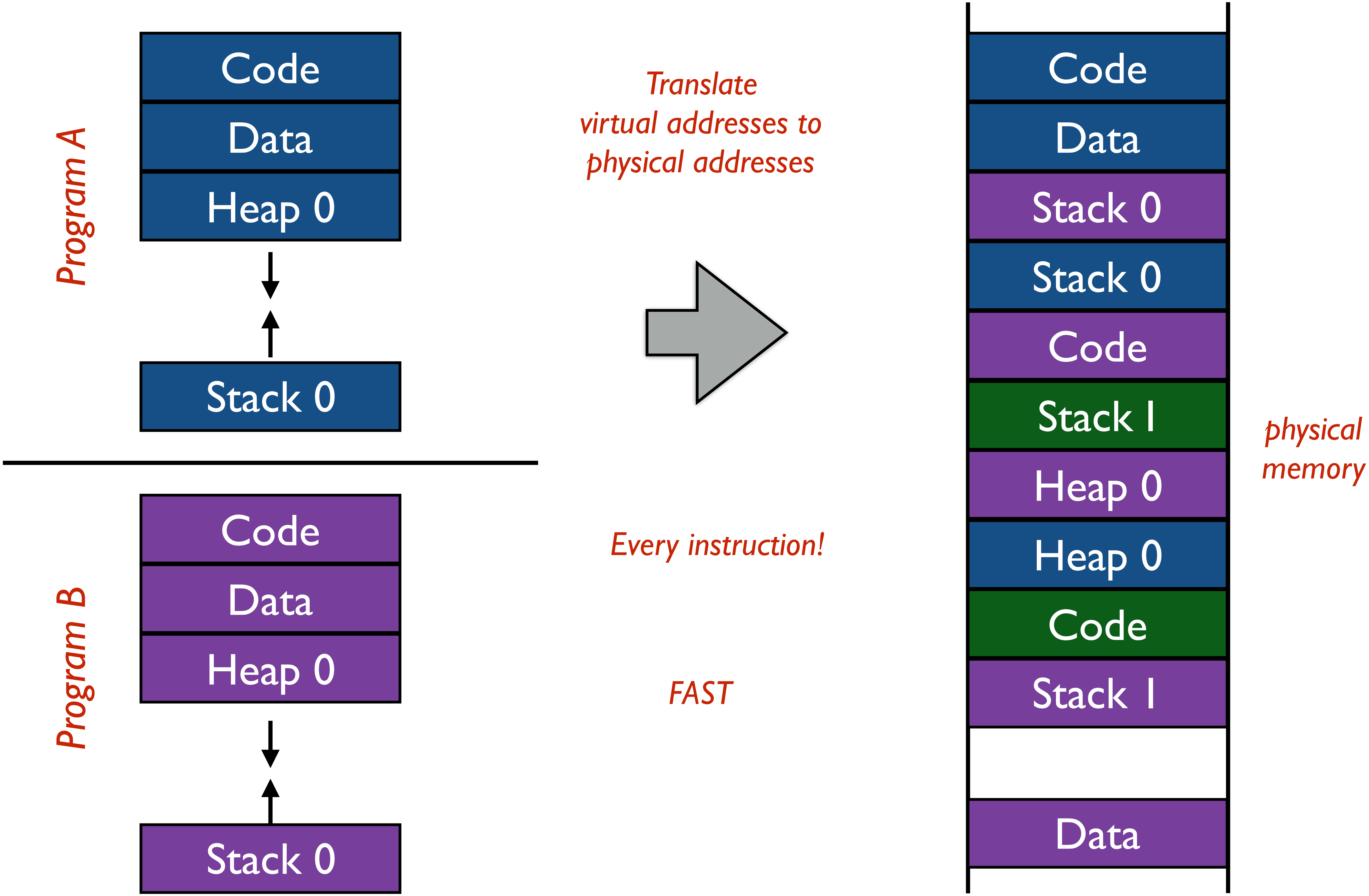
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Code
Data
Stack 0
Stack 0
Code
Stack 1
Heap 0
Heap 0
Code
Stack 1
Data
physical
memory

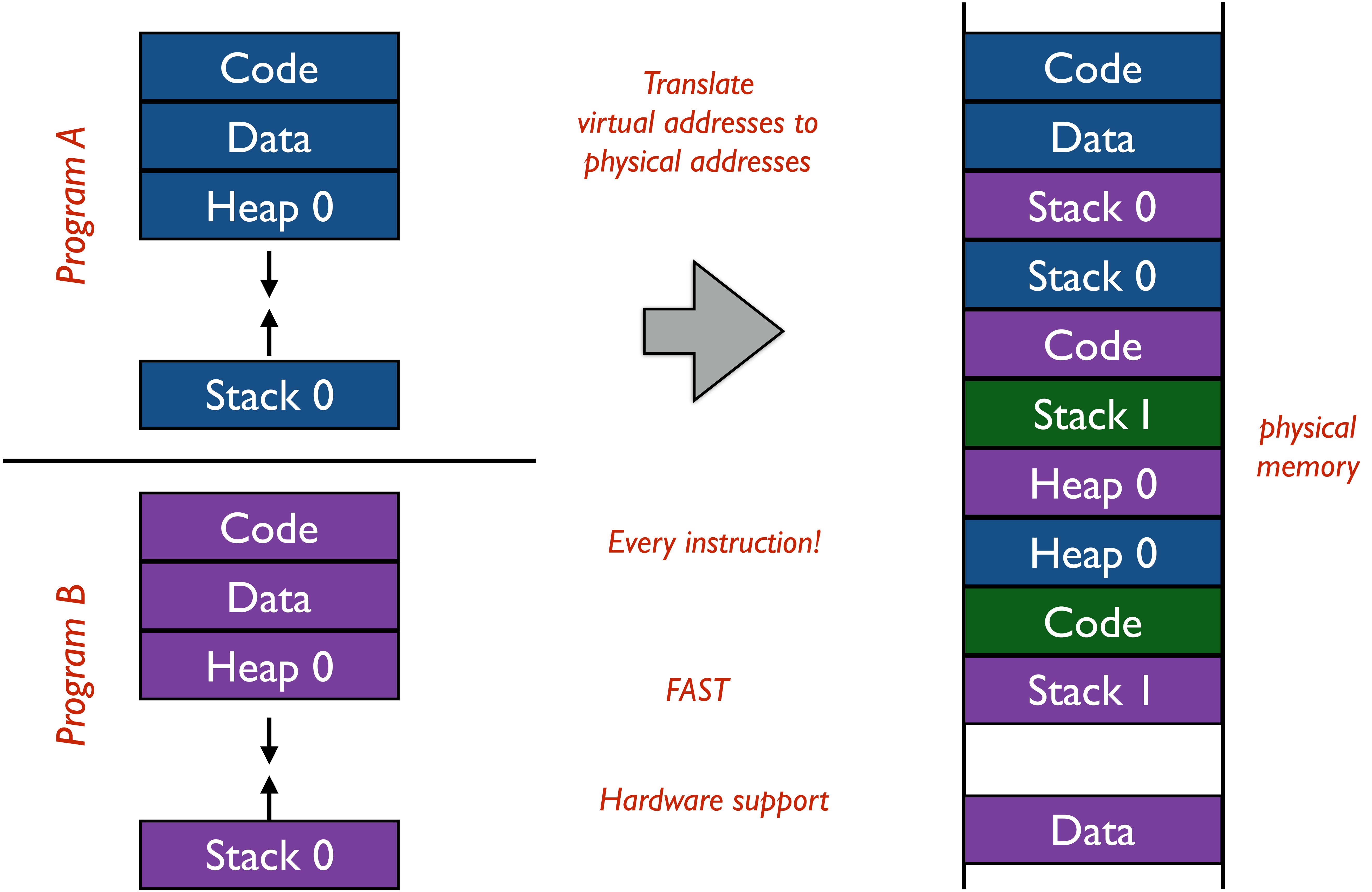
Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Translate
virtual addresses to
physical addresses
Every instruction!
Code
Data
Stack 0
Stack 0
Code
Stack 1
Heap 0
Heap 0
Code
Stack 1
Data
physical
memory

Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Translate
virtual addresses to
physical addresses
Every instruction!
FAST
Code
Data
Stack 0
Stack 0
Code
Stack 1
Heap 0
Heap 0
Code
Stack 1
Data
physical
memory

Paging


Program A
Code
Data
Heap 0
Stack 0
Program B
Code
Data
Heap 0
Stack 0
Translate
virtual addresses to
physical addresses
Every instruction!
FAST
Hardware support
Code
Data
Stack 0
Stack 0
Code
Stack 1
Heap 0
Heap 0
Code
Stack 1
Data
physical
memory

Fim