CS-428 Concurrent & Distributed Systems 2014, 2015, **Spring 2021**

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March 5, 2021

Syllabus

- Introduction
 - Brief Overview
 - Hardware Models
- Shared Memory Programming Models: pThreads, OpenMP
 - Overview
 - Posix Threads
 - First Look at OpenMP
 - Profiling
 - Work-Sharing Constructs
 - Synchronization
- 3 Vector Programming: OpenCL/CUDA
 - Overview
 - GPGPU's: OpenCL & CUDA
 - OpenCL Specification
 - First Look at OpenCL

- CUDA Programming
- Optimization
- Distributed Memory Programming
 Model: MPI
 - Overview
 - Communicators
 - First Look at OpenMPI
 - Sending/Receiving Messages
 - Point-to-Point Send/Receive
 - Collective Communication
 - Multiple Communicators
- 5 Hadoop
 - HDFS
 - HDFS API's
 - Map Reduce Framework
- 6 Spark

About the Course

Learning Outcomes

CLO1 Have a good understanding of concurrent and distributed systems

CLO2 Be able to write programs for Concurrent systems

CLO3 Be able to write programs for Distributed systems

CLO4 Be able to write programs for specialized Performance Hardwares

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Marks Breakdown

Sessional I: 15%

• Sessional II: 15%

• Final Examination: 50%

Assignments: 20% (including Takehome Lab Activities)



About the Course (cont.)

Assignment Instructions

- Will accept assignments after last date, provided said assignment for entire class is not marked.
- Parts of assignment may appear in examinations. If not, then similarity checks may be applied on submitted assignments.
- HPC Setup with support for various parallel and distributed computing frameworks will be made available to all students for duration of semester (and beyond upon request)

Generating Public Key for Assignments

- On Windows, Use https://winscp.net/eng/docs/ui_puttygen
- On Linux, use ssh-keygen command
- Share generated key with me by email.



About the Course (cont.)

Probability Distribution of Previous Grades

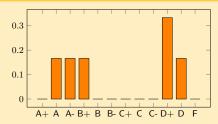


Figure 1: Spring 2014

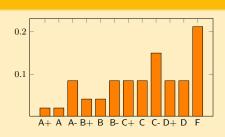


Figure 2: Spring 2015



Where are We

- Clock rates 40 MHz (MIPS R3000 1988) \rightarrow 4.0 GHz (Intel Core-i7-4790K 2015), 4.4 GHz (Intel Xeon X5698 2015)
- Transistor has reached size of 32 nm (Generation 3 Core-i7). Size limit: How much more smaller can it get?
- What is a single clock cycle worth?
 - xchg: Exchange values in two registers
 - push: Push operation using registers
 - pop: Pop operation using registers
 - add,sub: 3 additions/subtractions involving registers
 - cmp: 3 comparisons involving registers
 - mul: half a fp multiplication involving registers
- Can we get a 8 GHz clock frequency?
- What will happen if we reach a 8 GHz clock frequency?
- Support for executing multiple instructions per clock cycle, fast cache technologies, superscalar architectures . . .
- Dramatic increase in Floating Point Operations per Second (FLOPs)

Where are We (cont.)



Figure 3: AMD breaks Guinness World Record for fastest processor frequency at 8.429 gigahertz (2011)

Where are We (cont.)

A question to think about

 Akram has a 12 GHz single core processor. Akbar has a quad-core 3 GHz multiprocessor. Which one is faster?

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