Assignment #2

Due: Thursdays 5th of April, 2018 before 11:55 pm

Note:

1. Late submissions receive zero credit.
2. If you write only the correct answer without steps you get very low credit.
3. Even if you completed the first two parts of the questions, do it again for correct answer.

Q:-1. [Points 50]

A majority function has an output 1 if there are more ones than zeros on its input, the output is zero otherwise. In this question we are going to design a three input majority function. You are required to do the following,

A. Create a truth table corresponding to the problem showing the inputs, output. Name the inputs as X, Y, Z and output as M. Also show the function in terms of minterms.

B. Solve the function using karnauf map to get the simplified function. Use the map I drawn below.

X\YZ	00	01	11	10
0				
1				

C. Implement the function using 8-to-1 line multiplexer. Show the inputs that you provided to the lines and the output.
(Note: Represent the inputs to multiplexer by I(0), …, I(3)).

D. Implement the function using 4-to-1 line multiplexer. (Hint: First do some work on truth table to obtain the same function in terms of variable Z, 0 and 1. Example 3-16 and 3-17 may be helpful).
(Note: Represent the inputs to multiplexer by I(0), I(1), I(2), I(3))

E. Implement the same function using 3-to-8 line decoder. (Hint: Figure 3-22 of book may help you).

Q:-2. [Points 40]

We are trying to design a BCD-to-Excess-3 code converter that will gives us output 0000 for all invalid input combination, i.e., from m10 to m15 it will give us 0. The rest of the circuit will perform as usual (as discussed in the class).

A. Draw the truth table corresponding to this problem. The inputs should be A, B, C, D while the outputs are W, X, Y, Z. (I will detect marks if you didn't follow this).

B. Find the Boolean expressions representing the four functions. Use the following karnauf map. (Again I will may detect credit if you didn't follow the map that I provided below)

AB\CD	00	01	11	10
00				
01				
11				
10				

C. Design the circuit using Quad 4-to-1 multiplexer.
(Note: The input to the first multiplexer is I(0,0), I(1,0), I(2,0), I(3,0), The inputs for the second multiplexer are I(0,1), I(1,1), I(2,1), I(3,1). Similarly, for the third and fourth the inputs are I(0,2), I(1,2), I(2,2), I(3,2) and I(0,3), I(1,3), I(2,3), I(3,3) respectively. Also note that the output W corresponds to first multiplexer, X to second, Y to third and Z to fourth. Strictly follow these conventions or I may deduct from your credit)

D. Design the circuit using 4-to-16 line decoder.

Good luck