Digital Logic Design Lab

Spring 2018

FAST-NU Peshawar
Campus

Lab Report # 1-5: Weightage: 8
Due Date: 04 March 2018

A note of warning: Start work on assignments as soon as they are given. Do not underestimate the demanding nature of this course. Expect the system to crash the night before your program is due. Aim to have it done the day before.

Submit the assignment on **slate.** Do not email me assignments after due date. It will not be accepted in any case. Students are required to submit actual content written in MS word or Pdf. Hand written/ Scanned assignments will not be accepted.

Use Logic.ly to design circuit diagrams.

Lab: 1

- F1 = A'B'C+A'B'C+A'BC+ABC'+ABC+A'B'+BC'+AB
- F2 = A'B'C'D+AB'C'D+A'BC'D+ABC'D+A'BCD+ABCD
- F3 = AB+A'BC'D+A'BCD+AB'C'D
- F4 = C + S where C = xy + xz + yz and S = C' (x + y+ z) + xyz
- F5 = F1 + F2 (F4)

Your Task is

1. Design Truth tables for all the above Boolean Functions.
2. Design Circuit Diagrams for all the Boolean Functions using basic gates (OR, AND, NOT).
3. Design Circuit Diagrams for all the Boolean Functions using Universal Gate (NAND).
4. Design Circuit Diagrams for all the Boolean Functions using Universal Gate (NOR).

Lab: 2-3

- F1 = A'B'+AB'C+'BC+AB'+C+AB'+C'+AB

- F2 = AB’C’D+ABC’+C’D+BC’D+A’B+AD
- F3 = AB+A’B’D+A’B+AB’C’D
- F4 = C + S where C = xy + yz and S = C’ (x + y) + xyz
- F5 = F4 + F2 (F3)

Your Task is

1. Design Truth tables for all the above Boolean Functions.

2. Derive function's standard forms from the table i.e. in the form of sum of minterms and in the form of product of maxterms.

3. Design circuits for the original function, for sum of minterms form and for the product of maxterms form and verify that all the three forms are giving same results i.e. following same truth table.

4. Design circuits for functions' inverse. You need first to derive functions' inverse from truth table.

Lab: 4-5

- F1 = A’B’+AB’C+A’BC+AB’+C+AB’+C’+AB
- F2 = AB’C’D+AC’D+C’D+C’D+A’B+AD
- F3 = AB+A’C’D+A’BD+AB’C’
- F4 = C + S where C = xy + yz and S = C’ (x + y) + xyz
- F5 = F3 + F1 (F4)

Your Task is

1. Design Truth tables for all the above Boolean Functions.
2. Simplify the given functions using KMAP.
3. Design Two-level NAND implementation of the given functions
4. Compute complement of the given functions if possible. The complement will be in the form of MAX terms. Simplify these complement functions using KMAP and Implement the simplified functions using Two-level NOR implementation.

Good Luck ☺!