Group members : Hale Şahin(150116841) and
Yasemin Eder(150113032)

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Detail Information About Our İnstructions

Bgez

For this instruction we didnt add any new signals. We used only branch signal and aluop0 as 1. Other signals are 0. We add a new out signal to the ALU unit. It is like zero signal and it show the negativity of the result. It called as nout. We send this nout with zero signal tot the OR gate.and this or gate connected with the branch signal to AND gate, it replaced zero signals wire.

Example instruction for this one:

100111 00111 0000001111111111

9C E0 03 FF

Xori

We add a new signal that called as ext. It will help to select output of a mux which takes input of zero extended immediate and sign extended immediate. If it is on we use zero extended immediate this will help to make xori. Then, we add the output of this mux to the another mux as input. This mux will select if the second data of the ALU is immediate value or a register value. ALUsrc signal will select the immediate value for the instruction XORI, because of that ALUsrc has to be 1.

Example instruction for this one:

001110 00110 00010 1111111000000000

38 C2 FE 00

Brn

For this instruction we didn't add any new signals. We used only branch signal as 1. Other signals are 0. We add new mux, this mux takes two inputs as first data from instruction[25:21] and adder2 result(immediate sign extended and shifted address and pc +4). And the result of this mux goes to another mux with pc+4. It will select one of the inputs according to branch&zero .

Example instruction for this one:

000000 00110 00000 00000 00000 010101

00 C0 00 15

Balz

For this instruction, jump and regwrite signals are on and ALU op bits are 01 for the subttraction. We took Instruction[25:0] address as 26 bits and put it to shift left 2 times with adding 00 at the end it will become 28 bits. [28:0] of the jumping address comes from there and then we concatenate it with the [31:28] bits of the PC+4. Then our jump address will become 32 bit. This address goes to a new mux 1 gate. Zero gate of this new mux takes PC+4, and the selection signal is new signal we added,Jump. Output of this mux put to the 1 gate of new mux to choose jump or branch it is again controlled by the jump signal. We also add a new mux to the output of ALU unit it will go through 0 gate of this mux and 1 gate is again PC+4, jump signal is the control, this will help writing link address to the register rather then ALU result if the instruction is jump or balz. Output of this mux will be again selected if this result or memory readed data goes to write data according to MemtoReg signal. At the end, we add another mux to select between Reg[31] or output of the mux of RegDst to choose Destination register, this will controlled by again jump signal.

011010 00000011001110011111100110010

68 19 CF 32

Jspal

In this instruction, we really used help the implementation of balz. We add a new mux to the select between 32 bit jump address and M[Reg[29]] by the help of jspa signal that we added newly. Output of this mux will go to a newer mux's 1 gate as jump address with the PC+4 which controlled by zout. If the ALU result 0, then jump will be occured, if not it doesnt occur. Jspa, jump, memread,memwrite,alusrc are on. And aLU op is 00(add). We send 29 as the address immediate then it will become the write and read address in the memory.

010011 00000 00000 0000000000001101

4C 00 00 1D

Srl

For this instruction we didnt add any new signals. We used only regdst signal and regwrite as 1 because it is R-type. Other signals are 0. We add shift amount instr[10:6] as input to the ALU unit. Then ALU makes the shift right operation because we add it to ALU with function code 2. Then ALU result goes to mux 0 gate. Because MemtoReg is not on, mux will select ALU result to go to register file in order to write this result to destination register.

Example instruction for this one:

000000 00000 00101 00010 00011 000010

00 05 10 C2