Opcode #	Memonic	Instruction size
0x0	NOP	1
0x1	EDAO ####	3
0x2	EDAI ####	3
0x3	LDAI ##	2
0x4	LDXI ##	2
0x5	LDYI ##	2
0x6	LDAR (####)	3
0x7	LDARX (####)	3
0x8	LDARY (####)	3
0x9	LDARI (####)	3
0xA	STAR (####)	3
0xB	STXR (####)	3
0xC	STYR (####)	3
0xD	STARX (####)	3
0xE	STARY (####)	3
0xF	STARI (####)	3
0x10	INCA	1
0x11	INCX	1
0x12	INCY	1
0x13	DECA	1
0x14	DECX	1
0x15	DECY	1
0x16	TAX	1
0x17	TXA	1
0x18	TYA	1
0x19	TAY	1
0x1A	TXY	1
0x1B	TYX	1
0x1C	TSA	1
0x1D	TAS	1
0x1E	SEC	1
0x1F	CLC	1
0x20	ADDI ##	2
0x21	ADDR ####	3
0x22	ADDX	1
0x23	ADDY	1
0x24	SUBI ##	2
0x25	SUBR ####	3
0x26	SUBX	1
0x27	SUBY	1
0x28	NANDI ##	2
0x29	NANDR ####	3
0x2A	NANDX	1
0x2B	NANDY	1
0x2C	ASR	1
0x2D	ASR2	1
0x2E	ASR4	1
0x2F	ANDI ##	2

0x30	ORI ##	2
0x31	NOTA	1
0x32	XORI ##	2
0x33	JMP ####	3
0x34	JEQ ####	3
0x35	JCS ####	3
0x36	JMPR ####	3
0x37	RSP	1
0x38	PHA	1
0x39	PHX	1
0x3A	PHY	1
0x3B	PLA	1
0x3C	PLX	1
0x3D	PLY	1
0x3E	JSR	3
0x3F	RTS	1
0x40	LDSA ##	2
0x41	STSA ##	2
0x42	CPAI ##	2
0x43	CPAR ####	3
0x44	CPXI ##	2
0x45	CPYI ##	2
0x46	BIT ##	2
0x47	INCR ####	3
0x48	DECR ####	3
0x49	PHI	2
0x4A	ROLA XX	2
0x4B	ROLM XX ####	4
0x4C	ORR ####	3
	EDOR ####	3
	EDIR ####	3

Description
No Operation; PC+=1
ACC → External Device Port[####]
External Device Port[####] → ACC
RAM[PC] → ACC
RAM[PC] → X
RAM[PC] → Y
RAM[####] → ACC
RAM[####] + X → ACC
RAM[####] + Y → ACC
RAM[RAM[####]] → ACC
ACC → RAM[####]
X → RAM[####]
Y → RAM[####]
ACC → RAM[#### + X]
ACC → RAM[#### + Y]
ACC → RAM[RAM[####]
ACC += 1
X += 1
Y += 1
ACC -= 1
X -= 1
Y -= 1
A → X
X → A
Y → A
A → Y
X → Y
Y → X
SP → ACC
ACC → SP
1 → Carry
0 → Carry
ACC = ACC + RAM[PC + 1] + Carry
ACC = ACC + RAM[#####] + Carry
ACC = ACC + X + Carry
ACC + ACC + Y + Carry
ACC = ACC – RAM[PC+1] + Carry
ACC = ACC – RAM[#####] + Carry
ACC = ACC – X + Carry
ACC = ACC – Y + Carry
ACC = ~(ACC & RAM[PC+1]) ; Carry ignored
ACC = ~(ACC & RAM[####]) ; Carry ignored
ACC = ~(ACC & X)
ACC = ~(ACC & Y)
ACC = ACC << 1 ; Carry ignored
ACC = ACC << 2 ; Carry ignored
ACC = ACC << 4 ; Carry ignored
ACC = (ACC & RAM[PC+1])

```
ACC = (ACC | RAM[PC+1])
ACC = ~ACC
ACC = ACC ^ RAM[PC+1]
#### → PC
#### → PC IF ~ZF == 0
#### → PC IF ~CF == 0
RAM[####] → PC
0xFF → SP
ACC → RAM[SP]; SP -= 1
X → RAM[SP]; SP -= 1
Y → RAM[SP]; SP -= 1
RAM[SP += 1] → ACC
RAM[SP += 1] → X
RAM[SP += 1] → Y
PC → RAM[SP]; SP -= 2; #### → PC
RAM[SP-1, SP-2] → PC; PC += 3; SP -= 2
RAM[SP - ##] → ACC; No change to SP
ACC → RAM[SP - ##]; No change to SP
ACC – RAM[PC+1] + Carry ; Status register changed only
ACC - RAM[####] + Carry ; Status register changed only
X – RAM[PC+1] + Carry   ; Status register changed only
Y – RAM[PC+1] + Carry   ; Status register changed only
~(ACC & RAM[PC+1])      ; Status register changed only
RAM[####] += 1
RAM[####] -= 1
RAM[PC+1] → RAM[SP] ; SP -= 1   (Push immediate to stack)
ACC = (ACC < 1) | Carry   (Requires temp byte XX encoded in instruction)
RAM[####] = (RAM[####] < 1) | Carry   (Requires temp byte XX)
ACC = (ACC | RAM[####])
ACC → External Device Port[RAM[####]]
External Device Port[RAM[####]] → ACC
```

To be changed