



RESET HIGH WHEN WORKING, LOW WHEN CONNECTING POWER OR WHEN SYSTEM NEED RESET
CMUTE, REQUIRED LOW PULSE AT NMOS GATE WHEN WORKING HIGH WHEN MUTE REQUIRED
30dB gain selection, PVDD- ACTUAL VDD, other all VDD-5v
DNU: OSC PINS FOR MASTER SLAVE CONFIGURATION, FAULT AND OTW ARE OUPUT STATUS FOR MCU